INTERNAL BLOCK DIAGRAM

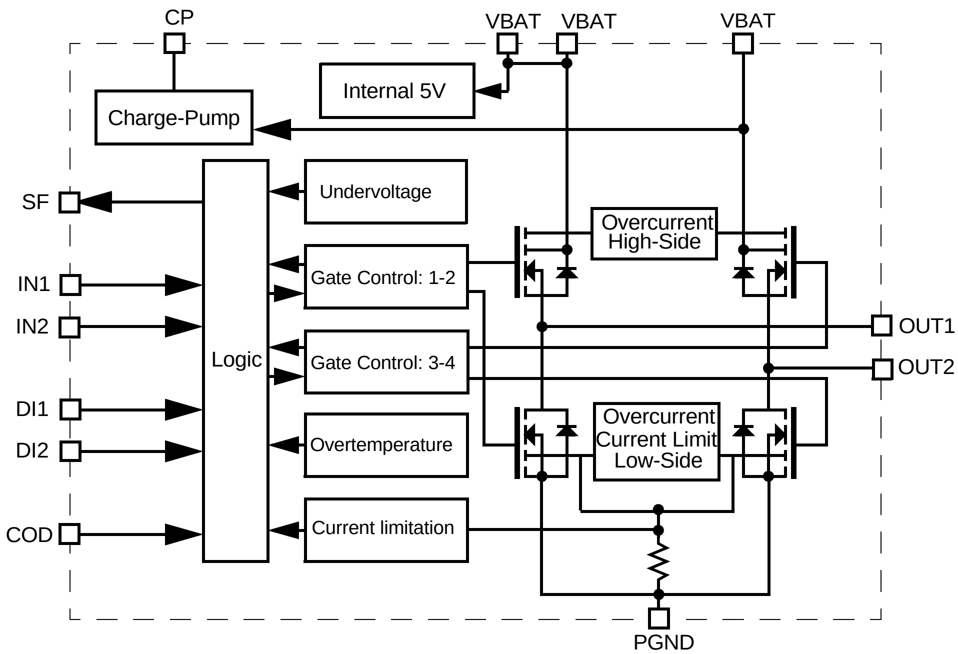


Figure 2. 33186 Simplified Internal Block Diagram

PIN CONNECTIONS

PIN CONNECTIONS

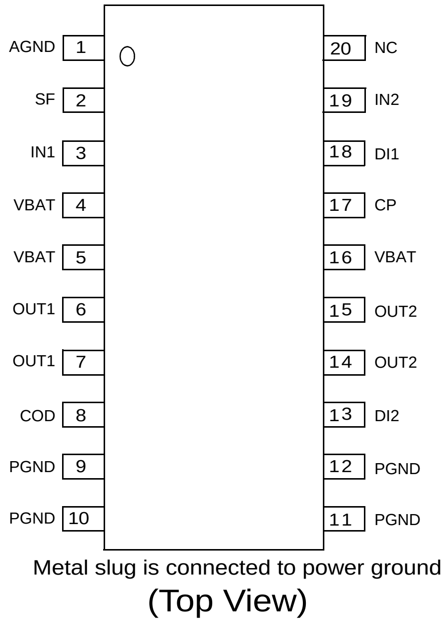


Figure 3. 33186 Pin Locations

Table 1. 33186 Pin Description

Pin	Name	Description
9, 10, 11, 12 Metal slug	PGND	Power Ground. All the ground are connected together, they should be connected as short as possible on the PCB.
1	AGND	Analog ground. All the ground are connected together, they should be connected as short as possible on the PCB.
2	Output Status flag (SF)	Open drain output, active low. Is set according to the truth table. When a fault appears, SF changes typically in less than 100 ms.
3,13 18, 19	Inputs IN1, IN2, DI1, DI2, COD	Voltage controlled inputs with hysteresis
8	COD	When not connected or connected to GND, a stored failure will be reset by change of the voltage-level on DI1 or DI2. When connected to VCC, the disable Pin DI1 and DI2 are inactive. A stored failure will be reset by change of the voltage-level on IN1 or IN2.
6, 7, 14, 15	OUT1, OUT2	H-Bridge outputs with integrated free-wheeling diodes.

Table 1. 33186 Pin Description(continued)

Pin	Name	Description
4, 5, 16	VBAT	The Pins 4 and 5 are internally connected. These Pins supply the left high side and the analog/logic part of the device. The Pin 16 supplies the right high side and the charge pump. The Pins 4, 5 and 16 should be connected together on the printed circuit board with connections as short as possible. Supervision and protection functions a) Supply voltage supervision The supply voltage is supervised. If it is below its specific threshold, the power stages are switched in tristate and the status flag is switched low. If the supply voltage is over the specific threshold again, the power stage switches independently into normal operation, according to the input Pins and the status flag is reset. b) Thermal supervision In case of overtemperature, the power stages are switched in tristate independent of the inputs signals and the status flag is switched low. If the level changes from high to low on DI1 (IN1) or low to high on DI2 (IN2), the output stage switches on again if the temperature is below the specified limit.The status-flag is reset to high level (Pin names in brackets refer to coding Pin = VCC). c) *Supervision of overcurrent on high sides and low sides* In case of over-current detection, the power stages are switched in tristate independent of the inputs signals and the status flag is set. If the level changes from high to low on DI1 (IN1) or low to high on DI2 (IN2) the output stage switches on again and the status flag is reset to high level (Pin names in brackets refer to coding Pin = VCC). The output stage switches into the mode defined by the inputs Pins provided, and/if the temperature is below the specified limits. d) Current limiting on low sides The maximum current which can flow under normal operating conditions is limited to Imax = 6,5 A +/- 20%. When the maximum current value is reached, the output stages are switched tristate for a fixed time. According to the time constant the current decreases until the next switch on occurs. See page 8 for schematics.
17	CP	Charge Pump output Pin A filtering capacitor (up to 33 nF) can be connected between Pin 17 and Gnd. Device can operate without external capacitor, although Pin 17 decoupling capacitor help in noise reduction and allows the device to perform a maximum speed, timing and PWM frequency.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Min	Typ	Max	Unit
ELECTRICAL RATINGS					
Supply Voltage Static Destruction Proof Dynamic Destruction Proof t < 0,5 s	 V_{BAT} V_{Bat}	 - 1.0 - 2.0	 – –	 28 40	V
Logic Inputs (IN1, IN2, DI1, DI2, CODE)	U	- 0.5	–	7.0	V
Output Status - Flag SF	U_{SF}	- 0.5	–	7.0	V
THERMAL RATINGS					
Junction Temperature	T_J	- 40	–	+150	°C
Storage Temperature	T_S	- 55	–	+125	°C
Ambient Temperature	T_A	- 40	–	+125	°C
Thermal Resistance (with power applied on 2 power MOS)	Rth_{JC}	–	–	+1.5	K/W
Thermal Resistance (with power applied on 2 power MOS)	Rth_{JC}	–	–	+1.5	K/W
Peak Package Reflow Temperature During Reflow [(1)], [(2)]	T_{PPRT}	Note 2.			°C

Notes

1. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
2. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. STATIC ELECTRICAL CHARACTERISTICS

Characteristic noted under conditions -40°C to +125 °C, VBAT from 5 V to 28 V, unless otherwise note. Typical values reflect approximate mean at 25°C, nominal VCC, at time of device characterization.

Characteristics	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range: Static Dynamic (t < 500 ms)	V_{BAT} V_{BAT}	5.0 –	– –	28 40	V V
Stand-by current f = 0 to 10 KHz; IOUT = 0 A	$I\ V_{BAT}$	–	–	35	mA
VBAT-undervoltage switch-off (without load) Switch-off Voltage Switch-on Voltage Hysteresis		4.15 4.5 150	4.4 4.75 –	4.65 5.0 –	V V mV
CHARGE-PUMP SUPPLY					
VBAT = 4.15 V VBAT < 40 V	$V_{CP} - V_{BAT}$ $V_{CP} - V_{BAT}$	3.35 –	– –	– 20	V V
LOGIC INPUTS					
Input High	VINH	3.4	–	–	V
Input Low	VINL	–	–	1.4	V
Input Hysteresis	U	0.7	1.0	–	V
Input Pull Up Current (IN1, IN2, DI1) UIN = 0.0 V	I	- 200	- 80	–	µA
Input Pull Down Current (DI2,COD)(3) UDI2 = 5.0 V	I_{DI2}	–	25	100	µA
POWER OUTPUTS: OUT1, OUT2					
Switch on resistance: $R_{OUT - VBAT}$; $R_{OUT - GND}$ VBAT = 5 to 28 V; CCP = 0 to 33 nF		–	–	300	mΩ
Switch-off Current during Current Limitation on Low Sides	(I_{OUT}) MAX	5.2	6.5	7.8	A
Switch-off Time during Current Limitation on Low Sides	t_A	15	20.5	26	µs
Blanking Time during Current Limitation on Low Sides	t_B	12	16.5	21	µs

Notes

3. In case of negative voltage at OUT2 (respectively OUT1) this maximum pull down current at DI2 (respectively COD) Pin can be exceeded. This happens during recirculation when the current is flowing in the low side. See curve 22.

Table 3. STATIC ELECTRICAL CHARACTERISTICS(continued)

Characteristic noted under conditions -40°C to +125 °C, VBAT from 5 V to 28 V, unless otherwise note. Typical values reflect approximate mean at 25°C, nominal VCC, at time of device characterization.

Characteristics	Symbol	Min	Typ	Max	Unit
High Side Overcurrent Detection[4] Low Side Overcurrent Detection	I_{OCHS} I_{OCLS}	11 8.0	– –	– –	A
Leakage Current Output Stage Switched off		–	–	100	µA
Free-Wheeling Diode Forward Voltage IOU = 3.0 A	U_D	–	–	2.0	V
Free-Wheeling Diode Reverse Recovery Time IFM =1.0 A, di/dt = 4.0 A/µs	t_{RR}	–	2.0	5.0	µs
Switch-off Temperature Hysteresis		160 20	– –	190 30	°C °C
OUTPUT STATUS FLAG (OPEN DRAIN OUTPUT)					
Output High (SF not set) USF = 5.0 V	I_{SF}	–	–	10	µA
Output Low (SF set) ISF = 300 µA	VSF	–	–	1.0	V
TIMING					
PWM frequency CCP = 33 nF	f	–	–	10	KHz
Maximum Switching Frequency During Current Limitation VBAT = 6....28 V.....C_{CP} = 33 nF	f	–	–	20	KHz
Output ON Delay IN1.....>OUT1 or IN2.....>OUT2	t_{DON}	–	–	15	µs
Output OFF Delay IN1.....>OUT1 or IN2.....>OUT2	t_{DOFF}	–	–	15	µs
Output Switching Time CCP = 0 to 33 nF OUTiH.....OUTiL, OUTiL.....OUTiH, IOUT = 3.0 A	t_r, t_f	2.0	–	5.0	µs
Disable Delay Time DIi.....OUTi	t_{DDIS}	–	–	8.0	µs
Turn off in Case of Overcurrent or Overtemperature		–	4.0	8.0	µs
Power On Delay Time (CCP = 33 nF)[5]		–	1.0	5.0	ms

Notes

4. In case of overcurrent, the time when the current is greater than 7.8 A is lower than 30 µs, with a maximum frequency of 1 kHz.
5. This parameter corresponds to the time for CCP to reach its nominal value when VBAT is applied.

TRUTH TABLE

Table 4. TRUTH TABLE

Device State	Input Conditions				Status		Outputs	
	DI1 [(8)]	DI2 [(8)]	IN1	IN2	SF[(9)]	SF[(10)]	OU1	OU2
1-Forward	L	H	H	L	H	H	H	L
2-Reverse	L	H	L	H	H	H	L	H
3-Free Wheeling Low	L	H	L	L	H	H	L	L
4-Free Wheeling High	L	H	H	H	H	H	H	H
5-Disable 1	H	X	X	X	L	H	Z	Z
6-Disable 2	X	L	X	X	L	H	Z	Z
7-IN1 Disconnected	L	H	Z	X	H	H	H	X
8-IN2 Disconnected	L	H	X	Z	H	H	X	H
9-DI1 Disconnected	Z	X	X	X	L	H	Z	Z
10-DI2 Disconnected	X	Z	X	X	L	H	Z	Z
11-Current Limit.active	L	H	X	X	H	H	Z	Z
12-Undervoltage[(6)]	X	X	X	X	L	L	Z	Z
13-Overtemperature[(7)]	X	X	X	X	L	L	Z	Z
14-Overcurrent[(7)]	X	X	X	X	L	L	Z	Z

Notes

6. In case of undervoltage, tristate and status-flag are reset automatically.
7. Whenever overcurrent or overtemperature is detected, the fault is stored (i.e.status-flag remains low). The tristate conditions and the status-flag are reset via DI1 (IN1) or DI2 (IN2). Pin names in brackets refer to coding Pin (COD = VCC).
8. If COD = VCC then DI1 and DI2 are not active.
9. COD = nc or GND
10. COD = VCC

L = Low
H = High
X = High or Low
Z = High impedance (all output stage transistors are switched off).

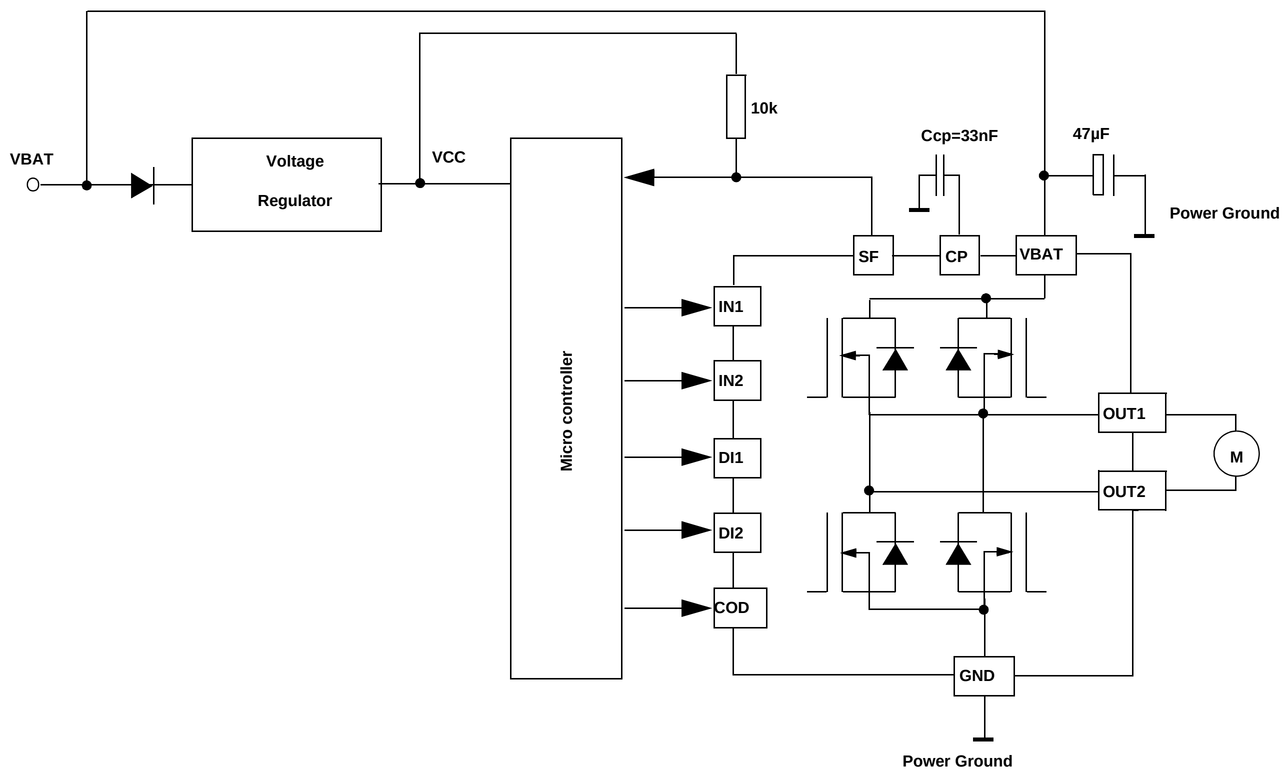


Figure 4. Typical Application

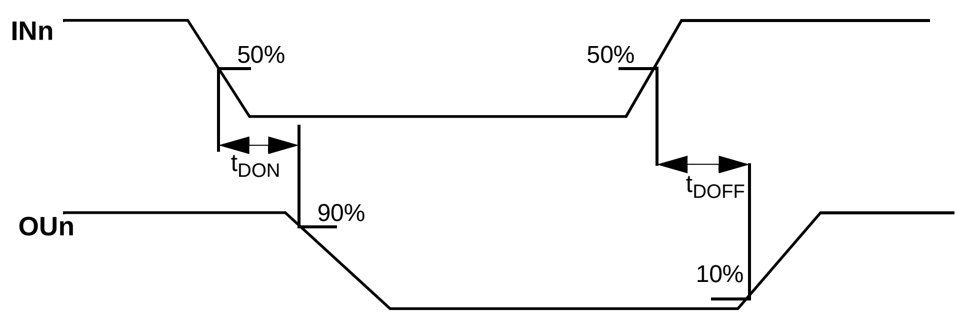


Figure 5. Output Delay Time

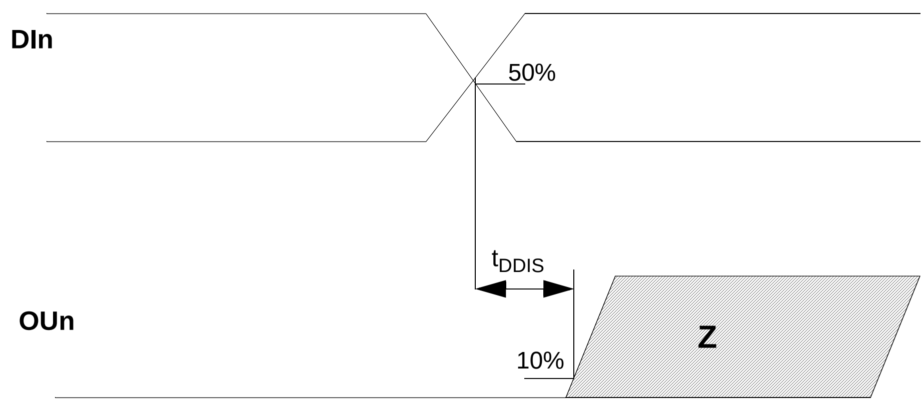


Figure 6. Disable Delay Time

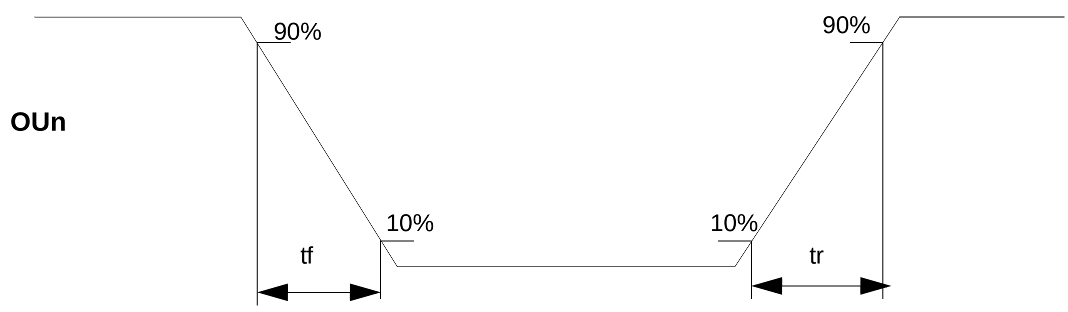


Figure 7. Output Switching Time

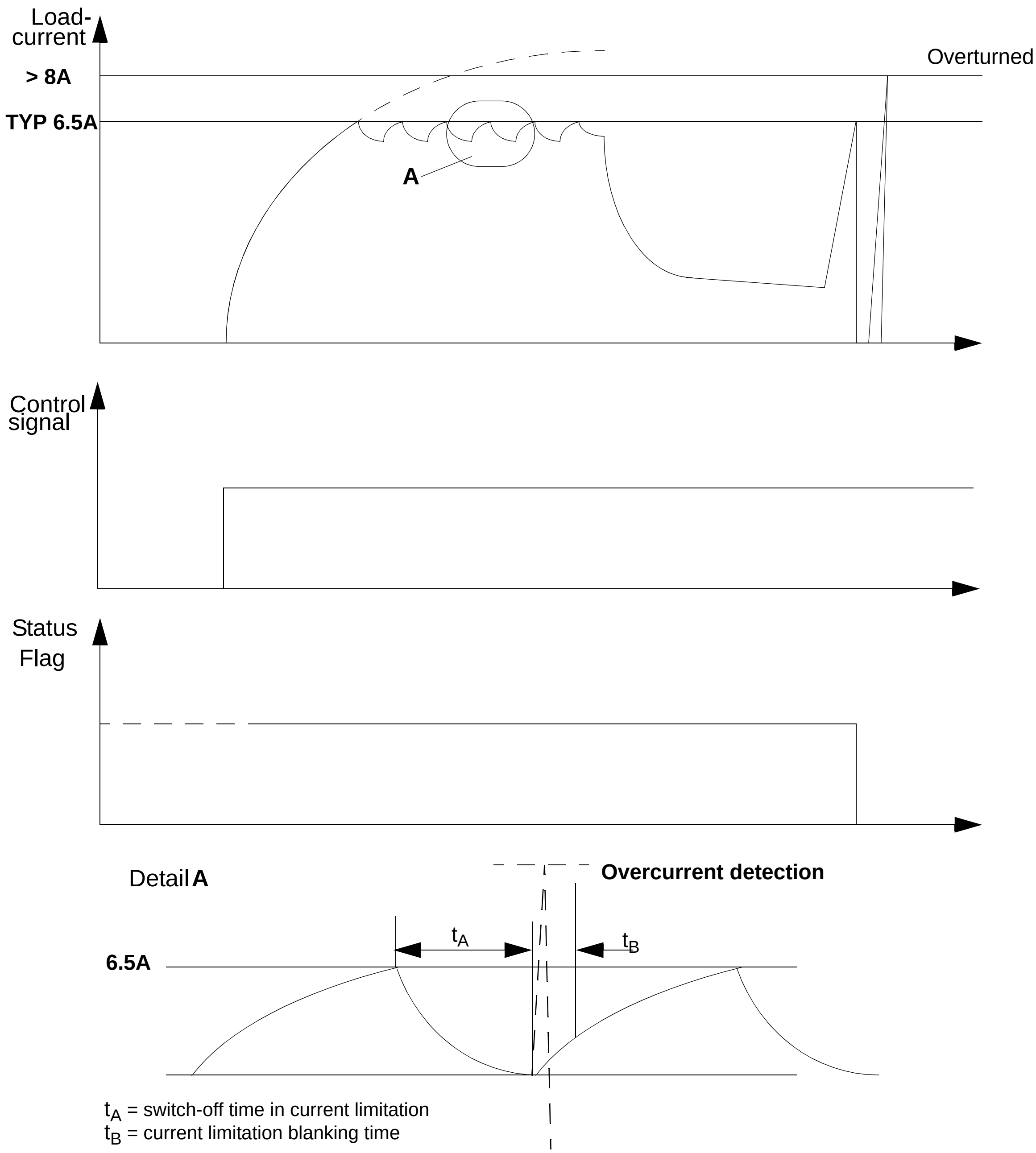


Figure 8. Current Limitation on Low Side

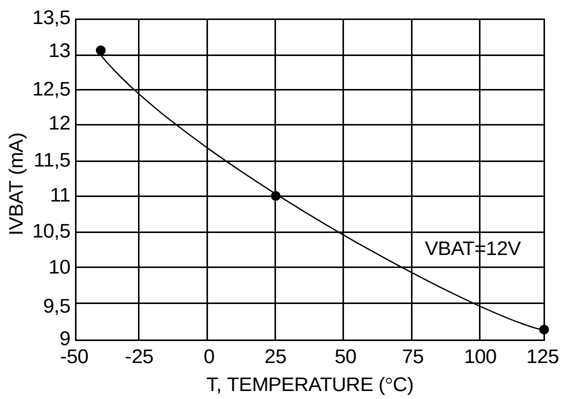


Figure 9. Stand-by Current vs. Temperature

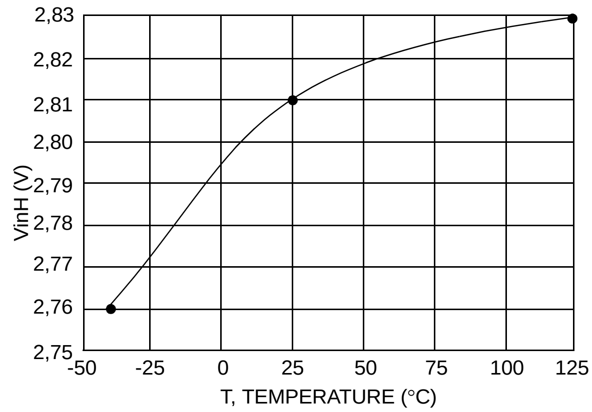


Figure 12. High Threshold Input Voltage vs. Temperature

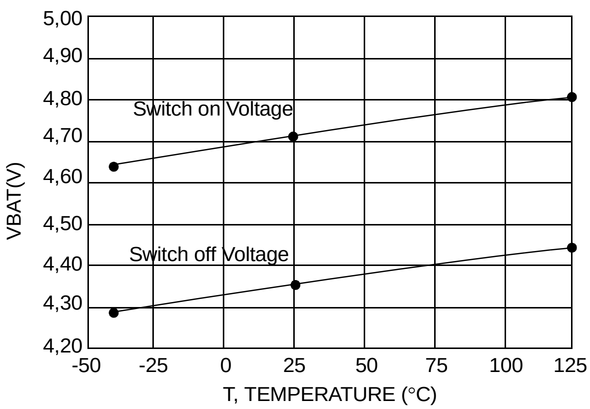


Figure 10. VBAT Undervoltage vs. Temperature

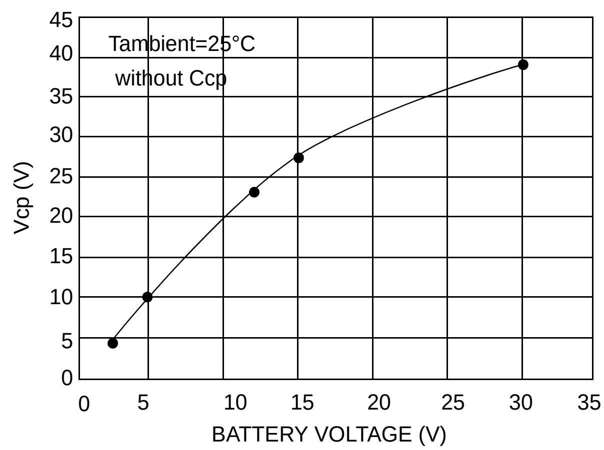


Figure 13. Vcp vs. Battery Voltage

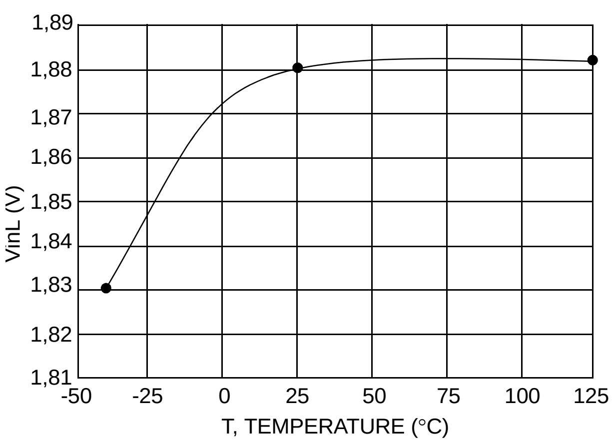


Figure 11. Low Threshold Input Voltage vs. Temperature

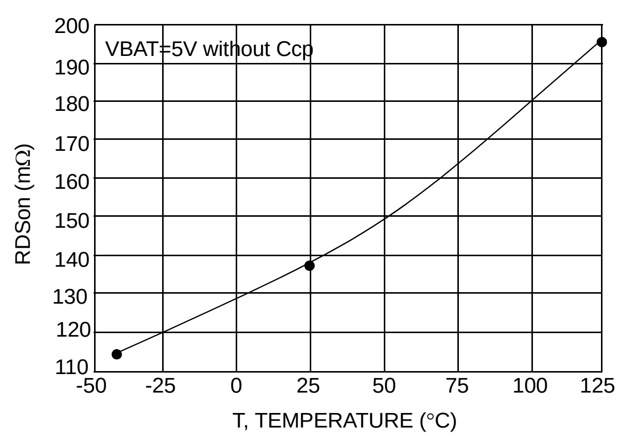


Figure 14. RDSON vs. Temperature

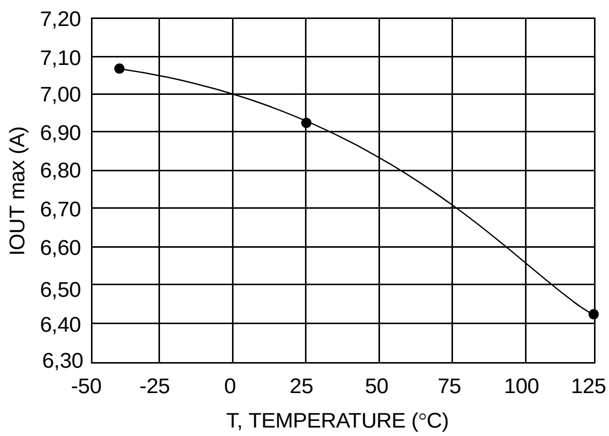


Figure 15. Switch off Current vs. Temperature

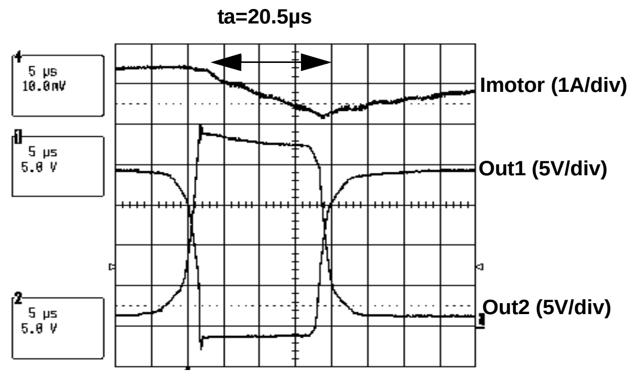


Figure 18. Switch off Time

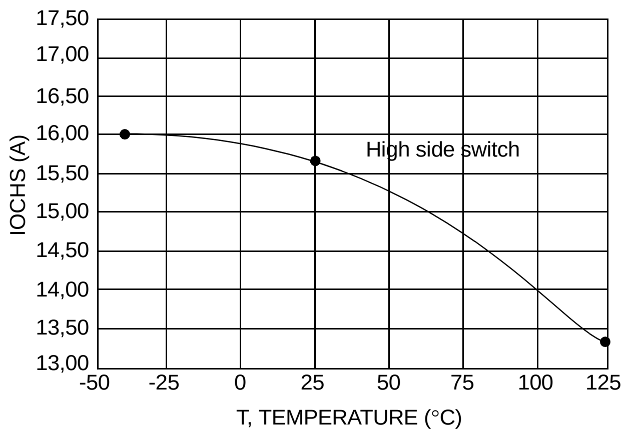


Figure 16. Overcurrent Detection vs. Temperature

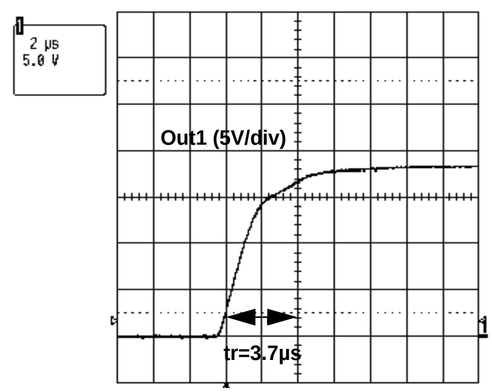


Figure 19. Output Switching Time: Tr

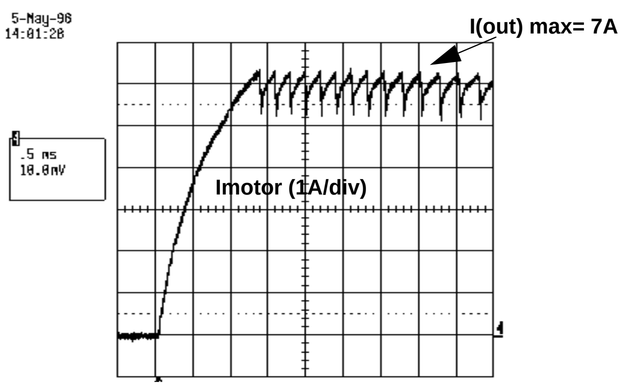


Figure 17. Current Limitation

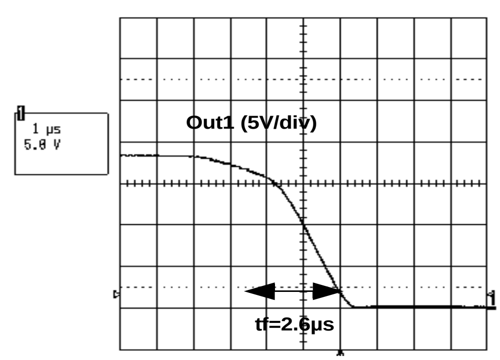


Figure 20. Output Switching Time: Tf

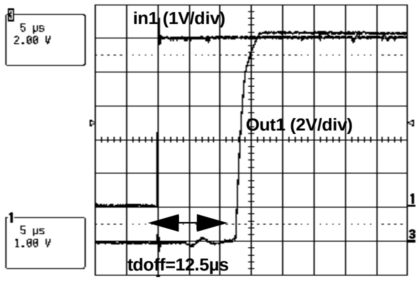


Figure 21. Output OFF Delay

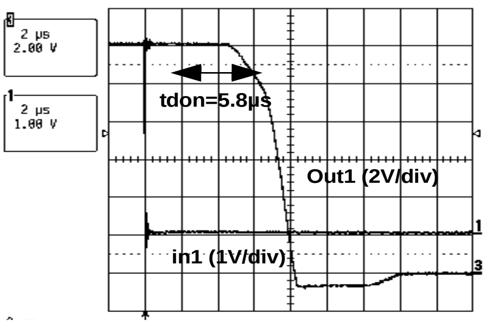


Figure 22. Output ON Delay

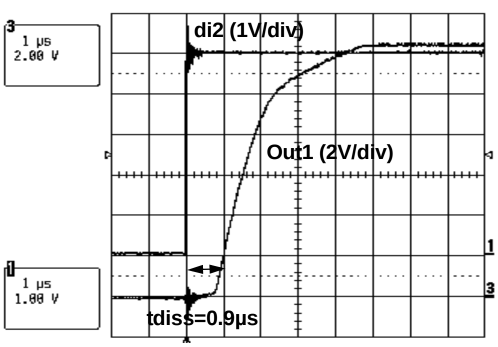


Figure 23. Disable Delay Time

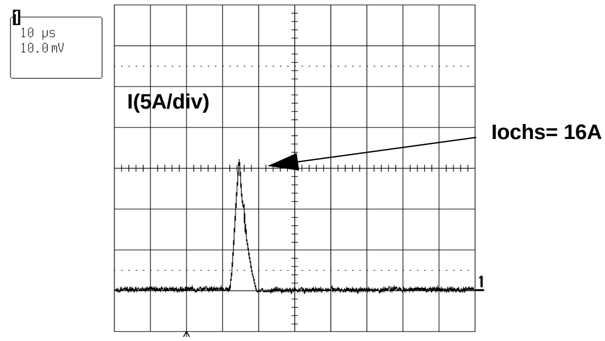
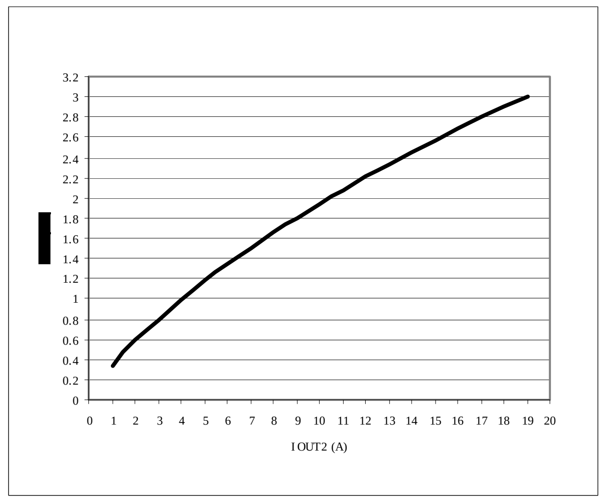


Figure 24. High Side Overcurrent High Side Detection



Note: Current through internal recirculation diode, @125°C in case of negative voltage at OUT2

Figure 25. Maximum Di2 Input Current vs. Iout2, current

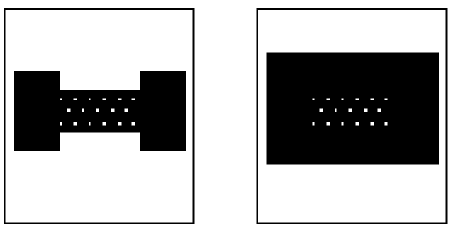
PACKAGING

SOLDERING

The 20 HSOP package is designed for enhanced thermal performance. The particularity of this package is its copper base plate on which the power die is soldered. The base plate is soldered on a PCB to provide heat flow to the ambient and also to provide a large thermal capacitance.

Of course, the more copper area on the PCB, the better the power dissipation and transient behavior.

We characterized the 20 HSOP on a double side PCB. The bottom side area of the copper is 7.8 cm^2. The top surface is 2.7 cm^2, see Figure 26.



Top Side Bottom Side

Figure 26. PCB Test Layout

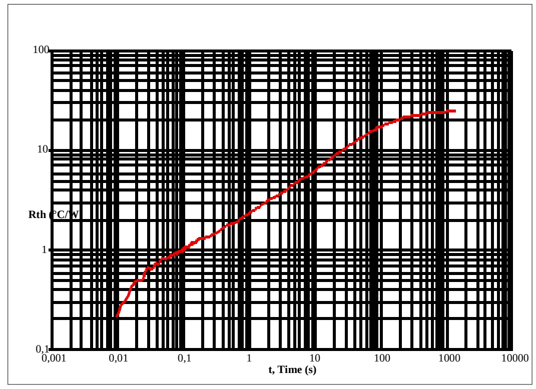
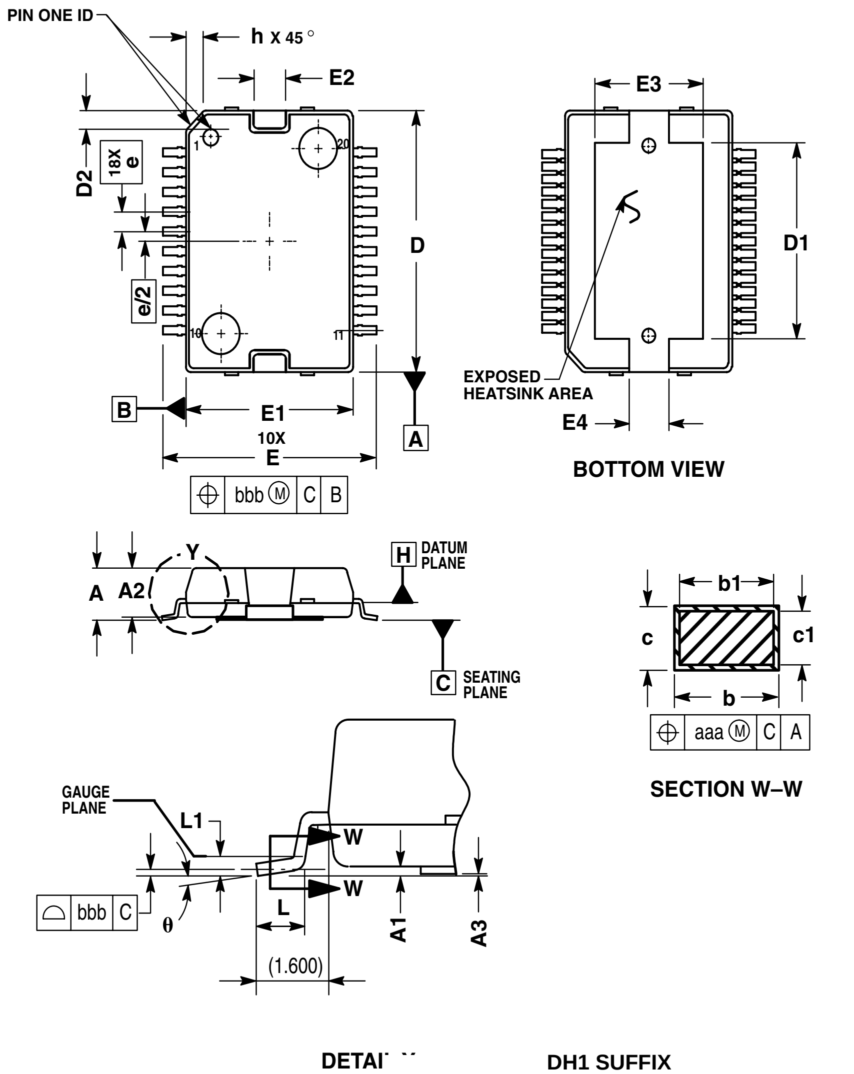


Figure 27. PHSOP20 Thermal Response

Figure 27 shows the thermal response with the device soldered on to the test PCB described on Figure 26.

PACKAGE DIMENSIONS

Important: For the most current revision of the package, visit www.freescale.com and perform a keyword search on the 98A number listed below.



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

	MILLIMETERS	
DIM	MIN	MAX
A	3.000	3.400
A1	0.100	0.300
A2	2.900	3.100
A3	0.00	0.100
D	15.800	16.000
D1	11.700	12.600
D2	0.900	1.100
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	6.400	7.200
E4	2.700	2.900
L	0.840	1.100
L1	0.350 BSC	
b	0.400	0.520
b1	0.400	0.482
c	0.230	0.320
c1	0.230	0.280
e	1.270 BSC	
h	—	1.100
θ	0°	8°
aaa	0.200	
bbb	0.100	

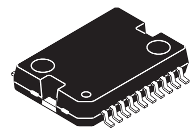
DH1 SUFFIX
VW1 SUFFIX (PB-FREE)
20-PIN HSOP
PLASTIC PACKAGE
98ASH70702A
ISSUE A

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 2.0)

33186DW
33186VW

20-PIN
HSOP-EP



DH SUFFIX
VW SUFFIX (Pb-FREE)
98ASH70273A
20-PIN HSOP-EP

Note For package dimensions, refer to the 33186 data sheet.

Introduction

This thermal addendum is provided as a supplement to the MC33186 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Package and Thermal Considerations

The MC33186 is offered in a 20 pin HSOP exposed pad, single die package. There is a single heat source (P), a single junction temperature (T_J), and thermal resistance ($R_{\theta JA}$).

$$\{T_J\} = [R_{\theta JA}] \cdot \{P\}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 5. Thermal Performance Comparison

Thermal Resistance	[°C/W]
$R_{\theta JA}$ [1], [2]	29
$R_{\theta JB}$ [2], [3]	9.0
$R_{\theta JA}$ [1], [4]	69
$R_{\theta JC}$ [5]	2.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-5 and JESD51-7.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad surface; cold plate attached to the package bottom side, remaining surfaces insulated.

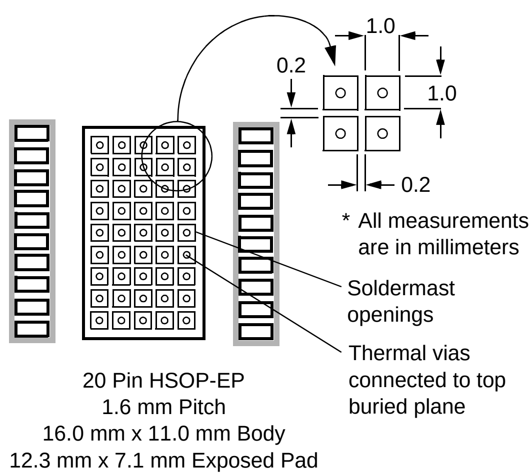


Figure 28. Thermal Land Pattern for Direct Thermal Attachment According to JESD51-5

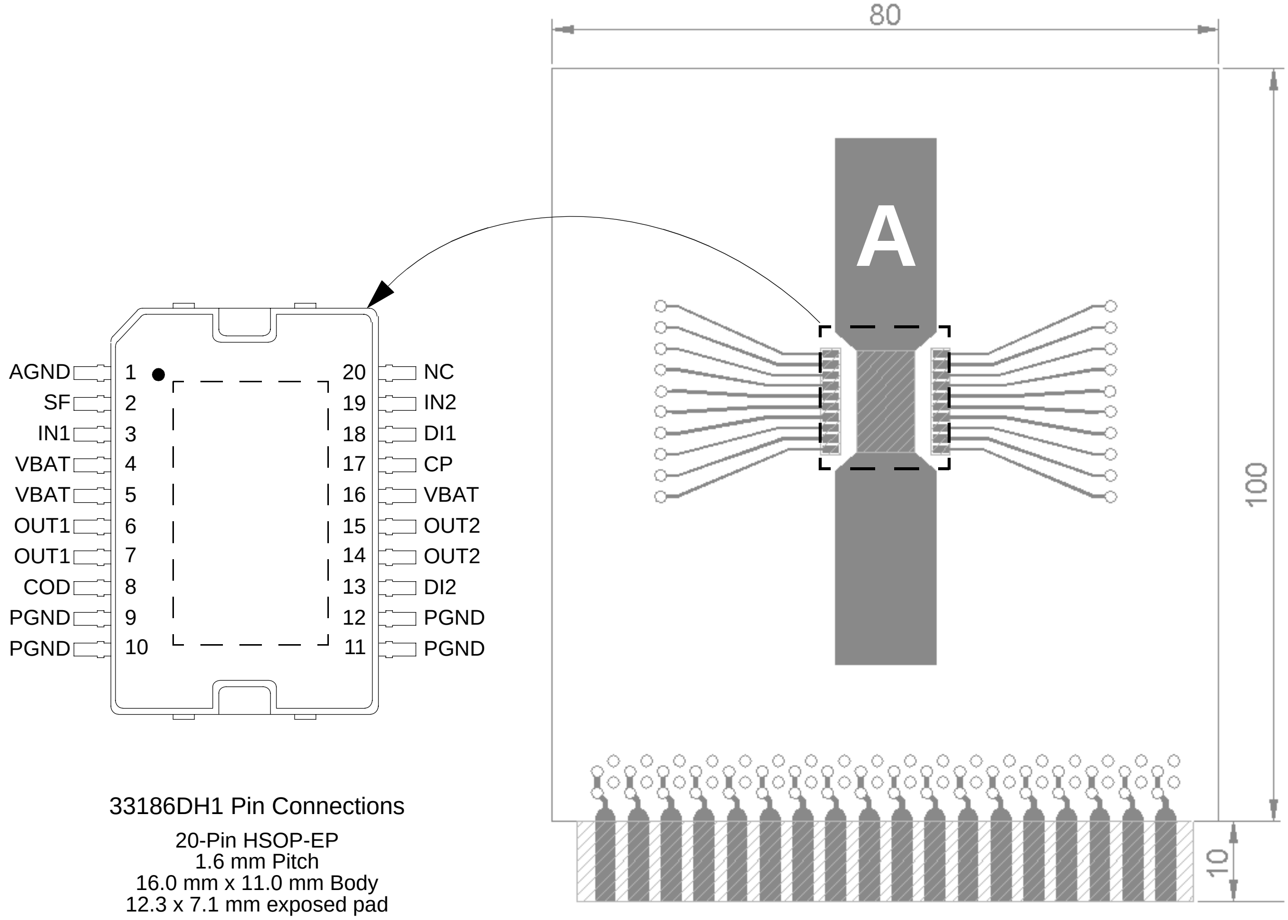


Figure 29. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area A:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 6. Thermal Resistance Performance

A [mm^2]	$R_{\theta JA}$ [°C/W]
0	70
300	49
600	47

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

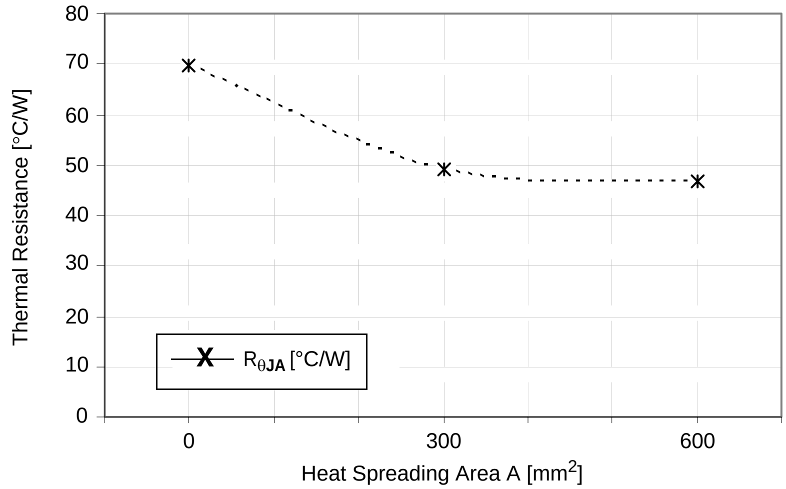


Figure 30. Device on Thermal Test Board $R_{\theta JA}$

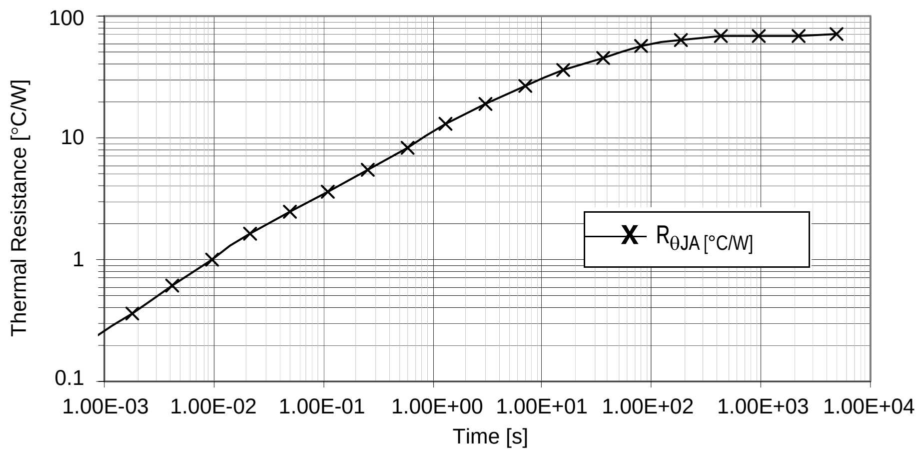


Figure 31. Transient Thermal Resistance $R_{\theta JA}$
1 W Step Response, Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
5.0	5/2006	• Implemented Revision History page • Added Lead Free (Pb-Free) Part Number MC33186VW1
6.0	10/2006	• Updated data sheet formal • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from MAXIMUM RATINGS on page 5. Added note with instructions to obtain this information from www.freescale.com.

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MC33186
Rev. 6.0
10/2006

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