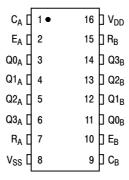
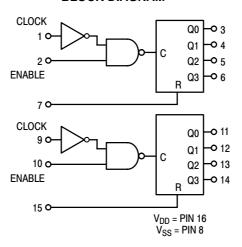
### **PIN ASSIGNMENT**



## **BLOCK DIAGRAM**



## **TRUTH TABLE**

Clock	Enable	Reset	Action	
	1	0	Increment Counter	
0	~	0	Increment Counter	
~	Х	0	No Change	
Х		0	No Change	
	0	0	No Change	
1	~	0	No Change	
Х	Х	1	Q0 thru Q3 = 0	

X = Don't Care

## **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

			V <sub>DD</sub>	- 5	5°C	25°C 125°C			5°C		
Characteristic		Symbol	Vdc	Min	Max	Min	Typ <sup>(3.)</sup>	Max	Min	Max	Unit
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level	V <sub>OL</sub>	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	"1" Level	V <sub>OH</sub>	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Input Voltage $(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$	"0" Level	V <sub>IL</sub>	5.0 10 15		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	"1" Level	V <sub>IH</sub>	5.0 10 15	3.5 7.0 11		3.5 7.0 11	2.75 5.50 8.25		3.5 7.0 11		Vdc
Output Drive Current $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$	Source	I <sub>OH</sub>	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	_ _ _ _	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	_ _ _ _	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I <sub>OL</sub>	5.0 10 15	0.64 1.6 4.2	_ _ _	0.51 1.3 3.4	0.88 2.25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Current		l <sub>in</sub>	15	_	± 0.1	_	±0.00001	± 0.1	_	± 1.0	μAdc
Input Capacitance (V <sub>in</sub> = 0)		C <sub>in</sub>	_	_	_	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)		I <sub>DD</sub>	5.0 10 15	_ _ _	5.0 10 20	_ _ _	0.005 0.010 0.015	5.0 10 20	_ _ _	150 300 600	μAdc
Total Supply Current <sup>(4.)</sup> <sup>(5</sup> (Dynamic plus Quiesce Per Package) (C <sub>L</sub> = 50 pF on all outp buffers switching)	ent,	I <sub>T</sub>	5.0 10 15			$I_T = (1$	I ).6 μΑ/kHz) f I.2 μΑ/kHz) f I.7 μΑ/kHz) f	+ I <sub>DD</sub>	1		μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency, and k = 0.002.

# SWITCHING CHARACTERISTICS (6.) $(C_L = 50 \text{ pF}, T_A = 25^{\circ}\text{C})$

		All Types					
Characteristic	Symbol	$V_{DD}$	Min	Typ <sup>(7.)</sup>	Max	Unit	
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t <sub>TLH</sub> , t <sub>THL</sub>	5.0 10 15	_ _ _	100 50 40	200 100 80	ns	
Propagation Delay Time  Clock to Q/Enable to Q $t_{PLH}$ , $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 215 ns $t_{PLH}$ , $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 97 ns $t_{PLH}$ , $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 75 ns	t <sub>PLH</sub> , t <sub>PHL</sub>	5.0 10 15	_ _ _	280 115 80	560 230 160	ns	
Reset to Q $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 117 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 95 \text{ ns}$	t <sub>PHL</sub>	5.0 10 15	_ _ _	330 130 90	650 230 170	ns	
Clock Pulse Width	t <sub>w(H)</sub> t <sub>w(L)</sub>	5.0 10 15	200 100 70	100 50 35	_ _ _	ns	
Clock Pulse Frequency	f <sub>cl</sub>	5.0 10 15	_ _ _	2.5 6.0 8.0	1.5 3.0 4.0	MHz	
Clock or Enable Rise and Fall Time	t <sub>THL</sub> , t <sub>TLH</sub>	5.0 10 15	_ _ _	 	15 5 4	μs	
Enable Pulse Width	t <sub>WH(E)</sub>	5.0 10 15	440 200 140	220 100 70	_ _ _	ns	
Reset Pulse Width	t <sub>WH(R)</sub>	5.0 10 15	280 120 90	125 55 40	_ _ _	ns	
Reset Removal Time	t <sub>rem</sub>	5.0 10 15	- 5 15 20	- 45 - 15 - 5	_ _ _	ns	

<sup>6.</sup> The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

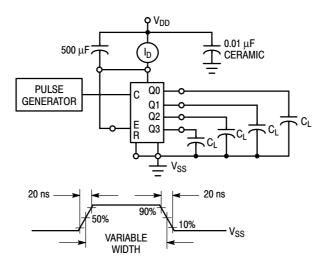


Figure 1. Power Dissipation Test Circuit and Waveform

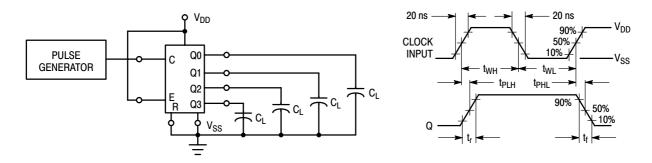


Figure 2. Switching Time Test Circuit and Waveforms

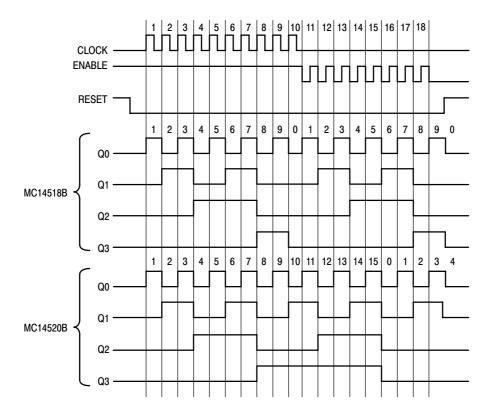


Figure 3. Timing Diagram

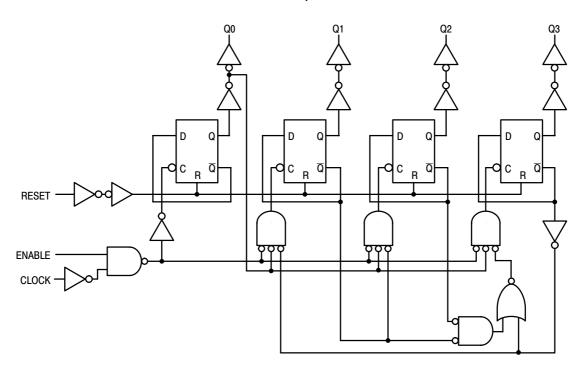


Figure 4. Decade Counter (MC14518B) Logic Diagram (1/2 of Device Shown)

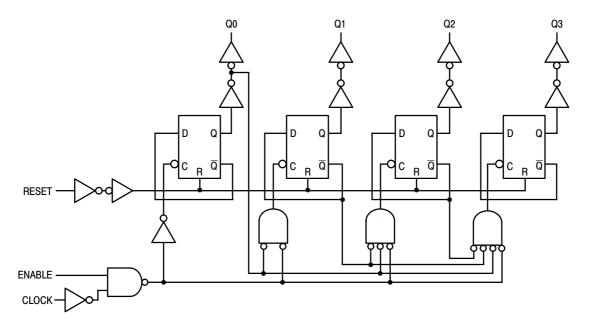


Figure 5. Binary Counter (MC14520B) Logic Diagram (1/2 of Device Shown)

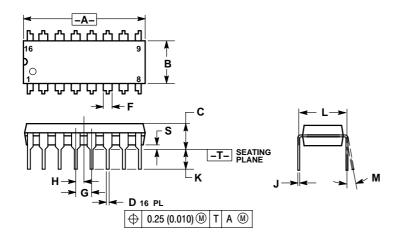
## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC14518BCP	PDIP-16	500 Units / Rail
MC14518BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14518BDW	SOIC-16	47 Units / Rail
MC14518BDWG	SOIC-16 (Pb-Free)	47 Units / Rail
MC14518BDWR2	SOIC-16	1000 Units / Tape & Reel
MC14518BDWR2G	SOIC-16 (Pb-Free)	1000 Units / Tape & Reel
MC14518BFEL	SOEIAJ-16	2000 Units / Tape & Reel
MC14518BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel
MC14520BCP	PDIP-16	500 Units / Rail
MC14520BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14520BDW	SOIC-16	47 Units / Rail
MC14520BDWG	SOIC-16 (Pb-Free)	47 Units / Rail
MC14520BDWR2	SOIC-16	1000 Units / Tape & Reel
MC14520BDWR2G	SOIC-16 (Pb-Free)	1000 Units / Tape & Reel
MC14520BFEL	SOEIAJ-16	2000 Units / Tape & Reel
MC14520BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

### PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08 **ISSUE T**

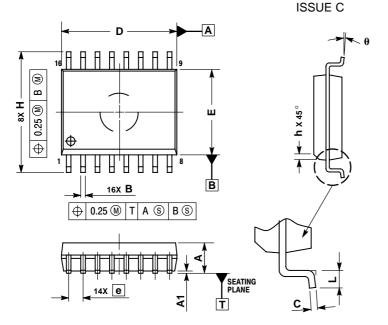


- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE

- MOLD FLASH. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100 BSC		2.54 BSC		
Н	0.050 BSC		1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
М	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

## SOIC-16 **DW SUFFIX** PLASTIC SOIC PACKAGE CASE 751G-03



- NOTES:
  1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
- PROTRUSION.

  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

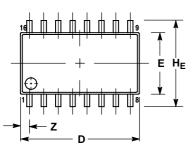
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

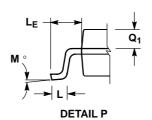
	MILLIMETERS					
DIM	MIN	MAX				
Α	2.35	2.65				
A1	0.10	0.25				
В	0.35	0.49				
С	0.23	0.32				
D	10.15	10.45				
Е	7.40	7.60				
е	1.27	1.27 BSC				
Н	10.05	10.55				
h	0.25	0.75				
L	0.50	0.90				
θ	0 °	7°				

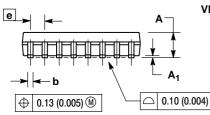
#### PACKAGE DIMENSIONS

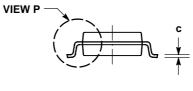
### SOEIAJ-16 **F SUFFIX**

PLASTIC EIAJ SOIC PACKAGE CASE 966-01 **ISSUE O** 









#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE
  MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

  TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
- 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

  DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD

	MILLIN	IETERS	INC	HES
DIM	MIN	MIN MAX		MAX
Α		2.05		0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10°
$Q_1$	0.70	0.90	0.028	0.035
Z		0.78		0.031

ON Semiconductor and un are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice on semiconductor and are registered readerlands of semiconductor Components industries, Ltc (SCILLC) solicit eserves the inject that changes without further holice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082-1312 USA Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Japan: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051 Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative