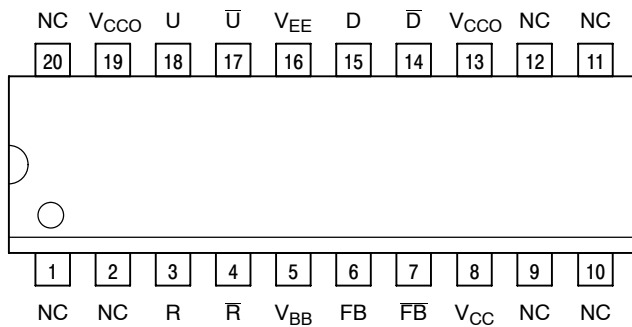


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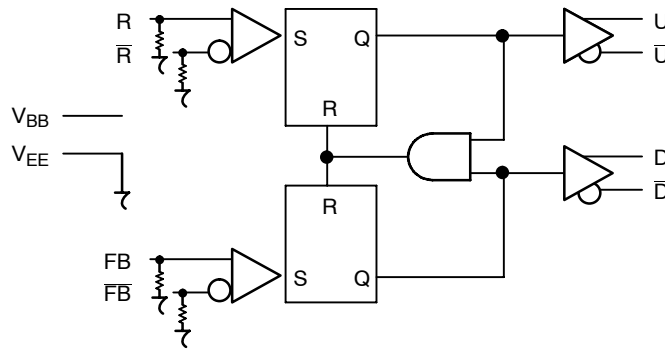


Warning: All V<sub>CC</sub>, V<sub>CCO</sub>, and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. 20-Lead Pinout (Top View)**

**Table 1. PIN DESCRIPTION**

PIN	FUNCTION
U, $\bar{U}$	ECL Up Differential Outputs
D, $\bar{D}$	ECL Down Differential Outputs
FB, $\bar{FB}$	ECL Feedback Differential Inputs
R, $\bar{R}$	ECL Reference Differential Inputs
V <sub>BB</sub>	Reference Voltage Output
V <sub>CC</sub> , V <sub>CCO</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply
NC	No Connect



**Figure 2. Logic Diagram**

**Table 2. ATTRIBUTES**

Characteristics	Value	
ESD Protection Human Body Model	> 2 kV	
Moisture Sensitivity (Note 1)	Pb Pkg	Pb-Free Pkg
SOIC-20	Level 1	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count	356 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

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**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8 to 0	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		–8 to 0	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 to 0 –6 to 0	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			–40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			–65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction–to–Ambient)	0 lfpm 500 lfpm	SOIC–20 SOIC–20	90 306	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction–to–Case)	Standard Board	SOIC–20	30 to 35	°C/W
T <sub>sol</sub>	Wave Solder Pb Pb–Free			265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 4. LVPECL DC CHARACTERISTICS** V<sub>CC</sub> = 3.3 V, V<sub>EE</sub> = 0 V (Note 2)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		38	45		38	47		38	47	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 3)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
V <sub>OL</sub>	Output LOW Voltage (Note 3)	1470	1605	1745	1490	1595	1380	1490	1595	1680	mV
V <sub>IH</sub>	Input HIGH Voltage (Single–Ended)	2135		2420	2135		2420	2135		2420	mV
V <sub>IL</sub>	Input LOW Voltage (Single–Ended)	1490		1825	1490		1825	1490		1825	mV
V <sub>BB</sub>	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Note 7) V <sub>pp</sub> < 500 mV V <sub>pp</sub> ≥ 500 mV	1.3 1.5		3.3 3.3	1.2 1.4		3.3 3.3	1.2 1.4		3.3 3.3	V V
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current Others R, FB	0.5 –300			0.5 –300			0.5 –300			μA μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary ±0.3 V.
- Outputs are terminated through a 50 Ω resistor to V<sub>CC</sub> – 2 V.
- V<sub>IHCMR</sub> min varies 1:1 with V<sub>EE</sub>, max varies 1:1 with V<sub>CC</sub>. The V<sub>IHCMR</sub> range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V<sub>ppmin</sub> and 1 V.

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**Table 5. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  (Note 5)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		38	45		38	47		38	47	mA
$V_{OH}$	Output HIGH Voltage (Note 6)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 6)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Note 7) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$	-2.0 -1.8		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	V V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current Others $\bar{R}, \bar{FB}$	0.5 -300			0.5 -300			0.5 -300			$\mu\text{A}$ $\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

6. All loading with  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .

7.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 8)

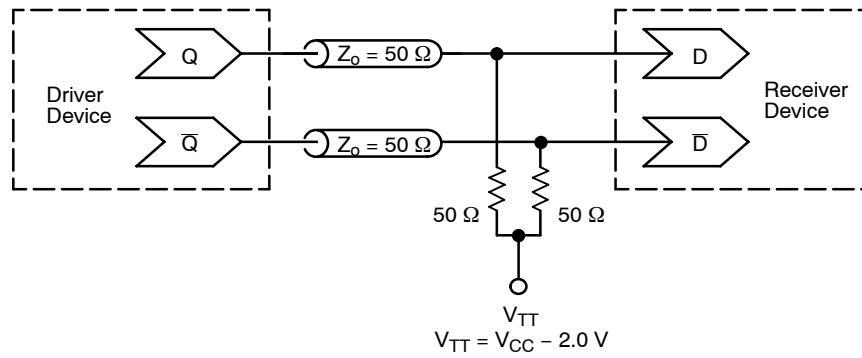
Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$F_{max}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay R to U, FB to D	430 1200		630 1400	450 1250		650 1450	480 1370		680 1590	ps
$V_{PP}$	Input Swing (Differential Configuration) (Note 9)	150		1000	150		1000	150		1000	mV
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_r, t_f$	Output Rise/Fall Times	175		475	175		475	175		475	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

9.  $V_{PP(min)}$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .

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**Figure 3. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC10LVEL40DW	SOIC-20	38 Units / Rail
MC10LVEL40DWG	SOIC-20 (Pb-Free)	38 Units / Rail
MC10LVEL40DWR2	SOIC-20	1000 / Tape & Reel
MC10LVEL40DWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

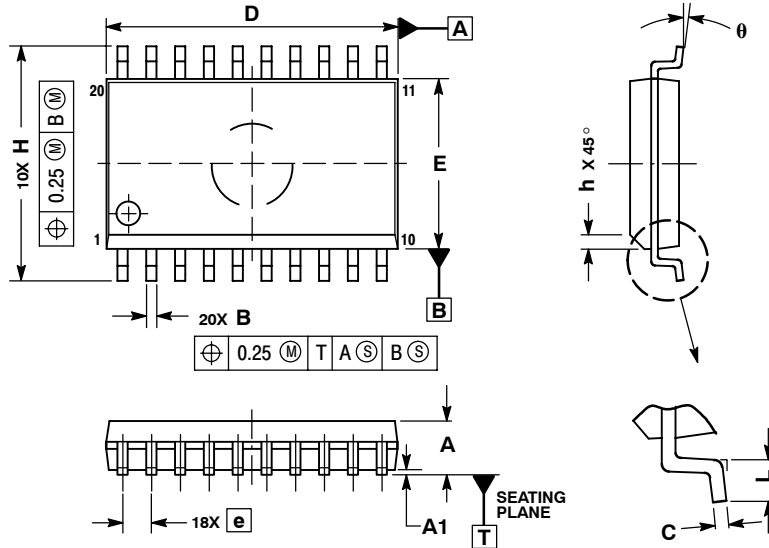
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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## PACKAGE DIMENSIONS

SO-20 WB  
CASE 751D-05  
ISSUE G




### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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