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1 Orderable parts

Table 1. Orderable part variations

Part number	Temperature (T_A)	Package
MC09XS3400AFK [1]	-40 °C to 125 °C	24 PQFN

Notes
1. To order parts in tape & reel, add the R2 suffix to the part number.

2 Internal block diagram

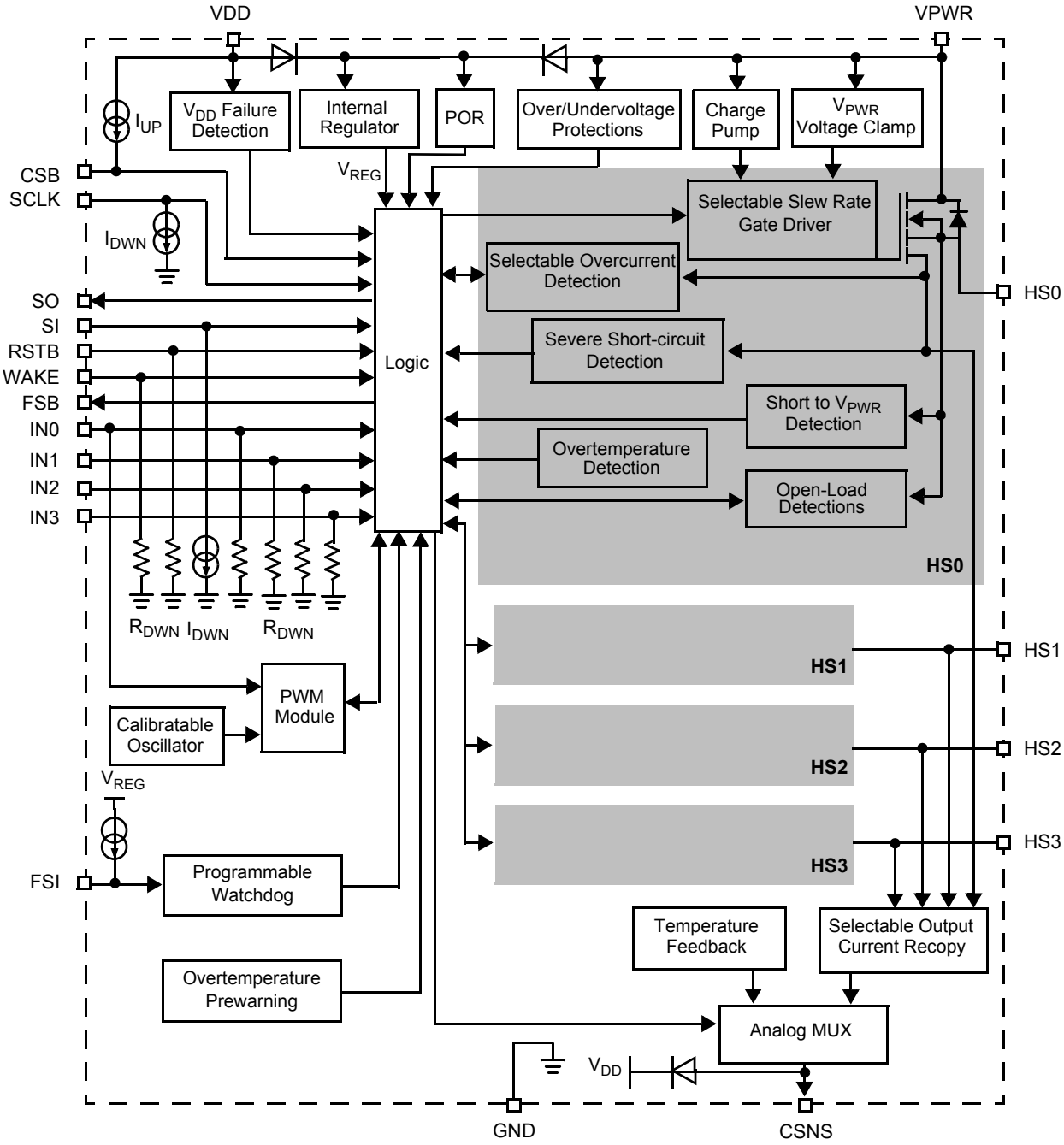


Figure 2. 09XS3400 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

Transparent top view of package

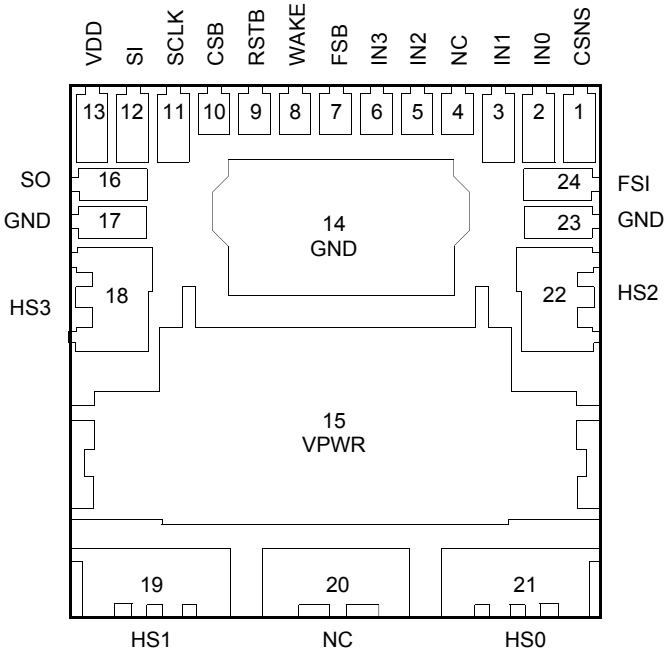


Figure 3. 09XS3400 pin connections

3.2 Pin definitions

A functional description of each pin can be found in the functional pin description section beginning on page 19.

Table 2. 09XS3400 pin definitions

Pin number	Pin name	Pin function	Formal name	Definition
1	CSNS	Output	Output Current Monitoring	This pin reports an analog value proportional to the designated HS[0:3] output current or the temperature of the GND flag (pin 14). It is used externally to generate a ground-referenced voltage for the microcontroller (MCU) . Current recopy and temperature feedback is SPI programmable.
2 3 5 6	IN0 IN1 IN2 IN3	Input	Direct Inputs	Each direct input controls the device mode. The IN[0:3] high-side input pins are used to directly control HS0:HS3 high-side output pins. If the device is SPI configured to use an external clock, the external clock is applied at the IN0 pin.
7	FSB	Output	Fault Status (Active Low)	This pin is an open drain configured output requiring an external pull-up resistor to VDD for fault reporting.
8	WAKE	Input	Wake	This input pin controls the device mode.
9	RSTB	Input	Reset	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low-current sleep mode.
10	CSB	Input	Chip Select (Active Low)	This input pin is connected to a chip select output of a master microcontroller (MCU).
11	SCLK	Input	Serial Clock	This input pin is connected to the MCU providing the required bit shift clock for SPI communication.

Table 2. 09XS3400 pin definitions (continued)

Pin number	Pin name	Pin function	Formal name	Definition
12	SI	Input	Serial Input	This pin is a command data input pin connected to the SPI Serial Data Output of the MCU or to the SO pin of the previous device of a daisy-chain of devices.
13	VDD	Power	Digital Drain Voltage	This pin is an external voltage input pin used to supply power interfaces to the SPI bus.
14, 17, 23	GND	Ground	Ground	These pins, internally shorted, are the ground for the logic and analog circuitry of the device. These ground pins must be also shorted on the board.
15	VPWR	Power	Positive Power Supply	This pin connects to the positive power supply and is the source of operational power for the device and power for the load.
16	SO	Output	Serial Output	This output pin is connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device of a daisy-chain of devices.
18 19 21 22	HS3 HS1 HS0 HS2	Output	High-side Outputs	Protected 9.0 mΩ high-side power output pins to the load.
4, 20	NC	N/A	No Connect	These pins can be left open or shorted to GND.
24	FSI	Input	Fail-safe Input	This input enables the watchdog timeout feature.

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{PWR(SS)}$	V_{PWR} Supply Voltage Range • Load Dump (400 ms) • Maximum Operating Voltage • Reverse Battery	 41 28 -18	V	
V_{DD}	VDD Supply Voltage Range	-0.3 to 5.5	V	
V_{DIG}	Input/Output Voltage	-0.3 to 5.5	V	(5)
V_{SO}	SO and CSNS Output Voltage	-0.3 to V_{DD} + 0.3	V	
I_{DIG}	Digital Input/Output Current in Clamp Mode	100	µA	(5)
$I_{CL(WAKE)}$	WAKE Input Clamp Current	2.5	mA	
$I_{CL(CSNS)}$	CSNS Input Clamp Current	2.5	mA	
$V_{HS[0:3]}$	HS [0:3] Voltage • Positive • Negative	 41 -24	V	
V_{PWR} - V_{HS}	High-side Breakdown Voltage	47	V	
$I_{HS[0:3]}$	Output Current	6.0	A	(2)
$E_{CL[0:3]}$	Output Clamp Energy Using Single Pulse Method	100	mJ	(3)
V_{ESD1} V_{ESD2} V_{ESD3} V_{ESD4}	ESD Voltage • Human Body Model (HBM) for HS[0:3], VPWR and GND • Human Body Model (HBM) for other pins • Charge Device Model (CDM) • Corner Pins (1, 13, 19, 21) • All Other Pins (2-12, 14-18, 20, 22-24)	 ±8000 ±2000 ±750 ±500	V	(4)
Thermal ratings				
T_A T_J	Operating Temperature • Ambient • Junction	 -40 to 125 -40 to 150	°C	
T_{STG}	Storage Temperature	-55 to 150	°C	

Notes

2. Continuous high-side output current rating per channel so long as maximum junction temperature is not exceeded. Calculation of maximum output current using package thermal resistance is required.
3. Active clamp energy using single-pulse method (L = 2.0 mH, R_L = 0 Ω, V_{PWR} = 14.0 V, T_J = 150 °C initial).
4. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
5. Input / Output pins are: IN[0:3], RSTB, FSI, SI, SCLK, CSB, and FSB.

Table 3. Maximum ratings *(continued)*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal resistance				
$R_{\theta JC}$ $R_{\theta JA}$	Thermal Resistance • Junction to Case • Junction to Ambient	 <1.0 30	°C/W	(6)
T_{SOLDER}	Peak Pin Reflow Temperature During Solder Mounting	Note 8	°C	(7), (8)

Notes

6. Thermal resistance for all channels active. Device mounted on a 2s2p test board per JEDEC JESD51-2 all channels active. 15 °C/W of $R_{\theta JA}$ can be reached in a real application case (4 layer board).
7. Refer to Soldering information.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values are measured at T_A = 25 °C and at nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power inputs						
V_{PWR}	Battery Supply Voltage Range • Fully Operational • Extended mode	 6.0 4.0	 – –	 20 28	V	(9)
$V_{PWR(CLAMP)}$	Battery Clamp Voltage	41	47	53	V	(10)
$I_{PWR(ON)}$	V_{PWR} Operating Supply Current • Outputs commanded ON, HS[0:3] open, IN[0:3] > V_{IH}	–	7.2	10	mA	
$I_{PWR(SBY)}$	V_{PWR} Supply Current • Outputs commanded OFF, OFF Open Load Detection Disabled, HS[0:3] shorted to the ground with VDD= 5.5 V, WAKE > V_{IH} or RSTB > V_{IH} and IN[0:3] < V_{IL}	–	6.5	7.5	mA	
$I_{PWR(SLEEP)}$	Sleep State Supply Current V_{PWR} = 12 V, RSTB = WAKE = IN[0:3] < V_{IL}, HS[0:3] shorted to the ground • T_A = 25 °C • T_A = 85 °C	 – –	 1.0 –	 5.0 30	µA	
$V_{DD(ON)}$	V_{DD} Supply Voltage	3.0	–	5.5	V	
$I_{DD(ON)}$	V_{DD} Supply Current at V_{DD} = 5.5 V • No SPI Communication • 8.0 MHz SPI Communication	 – –	 1.6 5.0	 2.2 –	mA	(11)
$I_{DD(SLEEP)}$	V_{DD} Sleep State Current at V_{DD} = 5.5 V	–	–	5.0	µA	
$V_{PWR(OV)}$	Overvoltage Shutdown Threshold	28	32	36	V	
$V_{PWR(OVHYS)}$	Overvoltage Shutdown Hysteresis	0.2	0.8	1.5	V	
$V_{PWR(UV)}$	Undervoltage Shutdown Threshold	3.3	3.9	4.3	V	(12)
$V_{SUPPLY(POR)}$	V_{PWR} and V_{DD} Power on Reset Threshold	0.5	–	0.9	$V_{PWR(UV)}$	
$V_{PWR(UV)\_UP}$	Recovery Undervoltage Threshold	3.4	4.1	4.5	V	
$V_{DD(FAIL)}$	V_{DD} Supply Failure Threshold (for V_{PWR} > $V_{PWR(UV)}$)	2.2	2.5	2.8	V	
Outputs HS0 TO HS3						
$R_{DS(on)}$	HS[0:3] Output Drain-to-Source ON Resistance (I_{HS} = 5.0 A, T_A = 25 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	 – – – –	 – – – –	 32.5 14.5 9.0 9.0	mΩ	
$R_{DS(on)}$	HS[0:3] Output Drain-to-Source ON Resistance (I_{HS} = 5.0 A, T_A = 150 °C) • V_{PWR} = 4.5 V • V_{PWR} = 6.0 V • V_{PWR} = 10 V • V_{PWR} = 13 V	 – – – –	 – – – –	 55.3 24.7 15.3 15.3	mΩ	

Notes

9. In extended mode, the functionality is guaranteed but not the electrical parameters. From 4.0 V to 6.0 V voltage range, the device is only protected with the thermal shutdown detection.
10. Measured with the outputs open.
11. Typical value guaranteed per design.
12. Output automatically recover with time limited autoretry to instructed state when V_{PWR} voltage is restored to normal, as long as the V_{PWR} degradation level does not go below the undervoltage power-ON reset threshold. This applies to all internal device logic supplied by V_{PWR} and assumes the external V_{DD} supply is within specification.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values are measured at T_A = 25 °C and at nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Outputs HS0 TO HS3 (continued)						
$R_{SD(ON)}$	HS[0:3] Output Source-to-Drain ON Resistance (I_{HS} = -5.0 A, $V_{PWR=}$ -18 V) • T_A = 25 °C • T_A = 150 °C	 – –	 – –	 13.5 18	mΩ	(13)
R_{SHORT}	HS[0:3] Maximum Severe Short-circuit Impedance Detection	21	47	75	mΩ	(14)
$I_{LEAK(OFF)}$	HS[0:3] Output Leakage Current in OFF State • Sleep mode, outputs grounded, T_A = 25 °C • Sleep mode, outputs grounded, T_A = 125 °C Normal mode (OLOFF_dis_s=1 and OS_dis_s=1), outputs grounded	 – – –	 0 0 20	 2.0 3.0 25	µA	
OCHI1 OCHI2 OC1 OC2 OC3 OC4 OCLO4 OCLO3 OCLO2 OCLO1	HS[0:3] Output Overcurrent Detection Levels (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V)	89.4 55.8 49.8 42.4 35.7 28.1 21.6 14 11 6.9	– – – – – – – – – –	131.6 83.7 73 62.7 52 41.6 31.2 20.8 16.7 11.5	A	
C_{SR0} C_{SR1}	HS[0:3] Current Sense Ratio (6.0 V ≤ $_{HS[0:3]}$ ≤ 20 V, CSNS ≤ 5.0 V) • CSNS_ratio bit = 0 • CSNS_ratio bit = 1	 – –	 1/10300 1/61000	 – –	–	(15)
C_{SR0_ACC}	HS[0:3] Current Sense Ratio (C_{SR0}) Accuracy (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) • $I_{HS[0:3]}$ = 12.5 A • $I_{HS[0:3]}$ = 5.0 A • $I_{HS[0:3]}$ = 3.0 A • $I_{HS[0:3]}$ = 1.5 A	 -12 -13 -16 -20	 – – – –	 12 13 16 20	%	
$C_{SR0\_ACC(CAL)}$	HS[0:3] Current Recopy Accuracy with one calibration point done at 5.0 A and 25 °C (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) • $I_{HS[0:3]}$ = 5.0 A	-5.0	–	5.0	%	(16)
$\Delta(C_{SR0})/\Delta(T)$	HS[0,3] C_{SR0} Current Recopy Temperature Drift (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) • $I_{HS[0:3]}$ = 5.0 A	–	–	0.04	%/°C	(17)
C_{SR1_ACC}	HS[0,3] Current Sense Ratio (C_{SR1}) Accuracy (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) • $I_{HS[0:3]}$ = 12.5 A • $I_{HS[0:3]}$ = 75 A	 -17 -12	 – –	 +17 +12	%	
$C_{SR1\_ACC(CAL)}$	HS[0,3] Current Recopy Accuracy with one calibration point done at 12.5 A and 25 °C (6.0 V ≤ $V_{HS[0:3]}$ ≤ 20 V) • $I_{HS[0:3]}$ = 12.5 A	-5.0	–	5.0	%	(16)
$V_{CL(CSNS)}$	Current Sense Clamp Voltage • CSNS Open; $I_{HS[0:3]}$ = 5.0 A with C_{SR0} ratio	V_{DD}+0.25	–	V_{DD}+1.0	V	

Notes

13. Source-Drain ON Resistance (Reverse Drain-to-Source ON Resistance) with negative polarity V_{PWR}.
14. Short-circuit impedance calculated from HS[0:3] to GND pins. Value guaranteed per design.
15. Current sense ratio = I_{CSNS} / $I_{HS[0:3]}$
16. Based on statistical analysis. It is not production tested.
17. Based on statistical data: delta(C_{SR0})/delta(T) = {(measured I_{CSNS} at T_1 - measured I_{CSNS} at T_2) / measured I_{CSNS} at room} / {T_1-T_2}. Not production tested.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values are measured at T_A = 25 °C and at nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Outputs HS0 TO HS3 (continued)						
$I_{OLD(off)}$	OFF Open Load Detection Source Current	30	–	100	µA	(18)
$V_{OLD(THRES)}$	OFF Open Load Fault Detection Voltage Threshold	2.0	3.0	4.0	V	(18)
$I_{OLD(on)}$	ON Open Load Fault Detection Current Threshold	110	330	660	mA	
$I_{OLD(ON\_LED)}$	ON Open Load Fault Detection Current Threshold with LED $V_{HS[0:3]}$ = V_{PWR} - 0.75 V	2.5	5.0	10	mA	
$V_{OSD(THRES)}$	Output Short to V_{PWR} Detection Voltage Threshold, Output programmed OFF	V_{PWR}-1.2	V_{PWR}-0.8	V_{PWR}-0.4	V	
V_{CL}	Output Negative Clamp Voltage • 0.5 A ≤ $I_{HS[0:3]}$ ≤ 5.0 A, Output programmed OFF	-22	–	-16	V	
T_{SD}	Output Overtemperature Shutdown for 4.5 V < V_{PWR} < 28 V	155	175	195	°C	
V_{IH}	Input Logic High Voltage	2.0	–	5.5	V	(19)
V_{IL}	Input Logic Low Voltage	-0.3	–	0.8	V	(19)
I_{DWN}	Input Logic Pull-down Current (SCLK, SI)	5.0	–	20	µA	(22)
I_{UP}	Input Logic Pull-up Current (CSB)	5.0	–	20	µA	(23)
C_{SO}	SO, FSB Tri-state Capacitance	–	–	20	pF	(20)
R_{DWN}	Input Logic Pull-down Resistor (RSTB, WAKE and IN[0:3])	125	250	500	kΩ	
CIN	Input Capacitance	–	4.0	12	pF	(20)
$V_{CL(WAKE)}$	Wake Input Clamp Voltage • $I_{CL(WAKE)}$ < 2.5 mA	18	25	32	V	(21)
$V_{F(WAKE)}$	Wake Input Forward Voltage • $I_{CL(WAKE)}$ = -2.5 mA	-2.0	–	-0.3	V	
V_{SOH}	SO High-state Output Voltage • I_{OH} = 1.0 mA	$V_{DD-0.4}$	–	–	V	
Control interface						
V_{SOL}	SO and FSB Low-state Output Voltage • I_{OL} = -1.0 mA	–	–	0.4	V	
$I_{SO(LEAK)}$	SO, CSNS and FSB Tri-state Leakage Current • CSB = V_{IH} and 0 V ≤ V_{SO} ≤ V_{DD}, or FSB = 5.5 V, or CSNS = 0.0 V	-2.0	0.0	2.0	µA	
RFS	FSI External Pull-down Resistance • Watchdog Disabled • Watchdog Enabled	– 10	0.0 Infinite	1.0 –	kΩ	(24)

Notes

18. Output OFF Open Load Detection current is the internal current source used during OFF state open load diagnostic. An open load fault is detected when the output voltage is greater than $V_{OLD(THRES)}$
19. Upper and lower logic threshold voltage range applies to SI, CSB, SCLK, RSTB, IN[0:3] and WAKE input signals. The WAKE and RSTB signals may be supplied by a voltage reference derived from V_{PWR}.
20. Input capacitance of SI, CSB, SCLK, RSTB, IN[0:3] and WAKE. This parameter is guaranteed by process monitoring but is not production tested.
21. The current must be limited by a series resistance when using voltages > 7.0 V.
22. Pull-down current is with V_{SI} ≥ 1.0 V and V_{SCLK} ≥ 1.0 V.
23. Pull-up current is wiTH V_{CSB} ≤ 2.0 V. CSB has an active internal pull-up to V_{DD}.
24. In fail-safe HS[0:3] output depends respectively on IN[0:3] input. FSI has an active internal pull-up to V_{REG} ~ 3.0 V.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values are measured at T_A = 25 °C and at nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output timing HS0 TO HS3						
SR_{R_00}	Output Rising Medium Slew Rate (medium speed slew rate / SR[1:0] = 00) • V_{PWR} = 14 V	0.25	0.6	1.0	V/µs	(25)
SR_{R_01}	Output Rising Slow Slew Rate (low speed slew rate / SR[1:0] = 01) • V_{PWR} = 14 V	0.125	0.3	0.5	V/µs	(25)
SR_{R_10}	Output Rising Fast Slew Rate (high speed slew rate / SR[1:0] = 10) • V_{PWR} = 14 V	0.5	1.2	1.5	V/µs	(25)
SR_{F_00}	Output Falling Medium Slew Rate (medium speed slew rate / SR[1:0] = 00) • V_{PWR} = 14 V	0.25	0.6	1.0	V/µs	(25)
SR_{F_01}	Output Falling Slow Slew Rate (low speed slew rate / SR[1:0] = 01) • V_{PWR} = 14 V	0.125	0.3	0.5	V/µs	(25)
SR_{F_10}	Output Falling Fast Slew Rate (high speed slew rate / SR[1:0] = 10) • V_{PWR} = 14 V	0.5	1.2	1.5	V/µs	(25)
$t_{DLY(on)}$	HS[0:3] Outputs Turn-ON Delay Times • V_{PWR} = 14 V for medium speed slew rate (SR[1:0] = 00)	55	–	105	µs	(26)(27)
$t_{DLY(off)}$	HS[0:3] Outputs Turn-OFF Delay Times • V_{PWR} = 14 V for medium speed slew rate (SR[1:0] = 00)	15	–	65	µs	(26)(27)
ΔSR	Driver Output Matching Slew Rate (SR_R /SR_F) V_{PWR} = 14 V at 25 °C and for medium speed slew rate (SR[1:0] = 00)	0.64	1.0	0.96		
Δt_{RF}	HS[0:3] Driver Output Matching Time ($t_{DLY(on)}$ - $t_{DLY(off)}$) V_{PWR} = 14 V, f_{PWM} = 240 Hz, PWM duty cycle = 50%, at 25 °C for medium speed slew rate (SR[1:0] = 00)	15	–	65	µs	
t_{FAULT}	Fault Detection Blanking Time	1.0	5.0	20	µs	(28)
t_{DETECT}	Output Shutdown Delay Time	–	7.0	30	µs	(29)
t_{CNSVAL}	CSNS Valid Time	–	70	100	µs	(30)
t_{WDTO}	Watchdog Timeout	217	310	400	ms	(31)
$t_{OLD(LED)}$	ON Open Load Fault Cyclic Detection Time with LED • default value (PWM_en bit = 0) • Outputs controlled with PWM module (PWM_en bit = 1)	6.3 –	8.4 PWM period	12 –	ms	

Notes

25. Rise and Fall Slew Rates measured across a 5.0 Ω resistive load at high-side output = 30% to 70% (see Figure 4, page 16).
26. Turn-ON delay time measured from rising edge of any signal (IN[0:3] and CSB) that would turn the output ON to $V_{HS[0:3]}$ = V_{PWR} / 2 with R_L = 5.0 Ω resistive load.
27. Turn-OFF delay time measured from falling edge of any signal (IN[0:3] and CSB) that would turn the output OFF to $V_{HS[0:3]}$ = V_{PWR} / 2 with R_L = 5.0 Ω resistive load.
28. Time necessary to report the fault to the FSB pin.
29. Time necessary to switch-off the output in case of OT or OC or SC or UV fault detection (from negative edge of the FSB pin to HS voltage = 50% of V_{PWR}
30. Time necessary for CSNS to be within ±5.0% of the targeted value (from HS voltage = 50% of V_{PWR} to ±5.0% of the targeted CSNS value).
31. For FSI open, the Watchdog timeout delay measured from the rising edge of RST, to commanded HS[0:3] output state depend on the corresponding input command.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values are measured at T_A = 25 °C and at nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power output timing HS0 TO HS3 (continued)						
t_{OC1_00}	HS[0:3] Output Overcurrent Time Step for OC[1:0] = 00 (slow by default)	4.40	6.30	8.02	ms	
t_{OC2_00}		1.62	2.32	3.00		
t_{OC3_00}		2.10	3.00	3.90		
t_{OC4_00}		2.88	4.12	5.36		
t_{OC5_00}		4.58	6.56	8.54		
t_{OC6_00}		10.16	14.52	18.88		
t_{OC7_00}		73.2	104.6	134.0		
t_{OC1_01}	OC[1:0] = 01 (fast)	1.10	1.57	2.00		
t_{OC2_01}		0.40	0.58	0.75		
t_{OC3_01}		0.52	0.75	0.98		
t_{OC4_01}		0.72	1.03	1.34		
t_{OC5_01}		1.14	1.64	2.13		
t_{OC6_01}		2.54	3.63	4.72		
t_{OC7_01}		18.2	26.1	34.0		
t_{OC1_10}	OC[1:0] = 10 (medium)	2.20	3.15	4.01		
t_{OC2_10}		0.81	1.16	1.50		
t_{OC3_10}		1.05	1.50	1.95		
t_{OC4_10}		1.44	2.06	2.68		
t_{OC5_10}		2.29	3.28	4.27		
t_{OC6_10}		5.08	7.26	9.44		
t_{OC7_10}		36.6	52.3	68.0		
t_{OC1_11}	OC[1:0] = 11 (very slow)	8.8	12.6	16.4		
t_{OC2_11}		3.2	4.6	21.4		
t_{OC3_11}		4.2	6.0	7.8		
t_{OC4_11}		5.7	8.2	10.7		
t_{OC5_11}		9.1	13.1	17.0		
t_{OC6_11}		20.3	29.0	37.7		
t_{OC7_11}		146.4	209.2	272.0		
t_{BC1_00}	HS[0:3] Bulb Cooling Time Step for CB[1:0] = 00 or 11 (medium)	242	347	452	ms	
t_{BC2_00}		126	181	236		
t_{BC3_00}		140	200	260		
t_{BC4_00}		158	226	294		
t_{BC5_00}		181	259	337		
t_{BC6_00}		211	302	393		
t_{BC1_01}	CB[1:0] = 01 (fast)	121	173	226		
t_{BC2_01}		63	90	118		
t_{BC3_01}		70	100	130		
t_{BC4_01}		79	113	147		
t_{BC5_01}		90	129	169		
t_{BC6_01}		105	151	197		
	CB[1:0] = 10 (slow)					
t_{BC1_10}		484	694	1904		
t_{BC2_10}		252	362	472		
t_{BC3_10}		280	400	520		
t_{BC4_10}		316	452	588		
t_{BC5_10}		362	518	674		
t_{BC6_10}		422	604	786		

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values are measured at T_A = 25 °C and at nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
PWM module timing						
f_{IN0}	Input PWM Clock Range on IN0	7.68	–	30.72	kHz	
$f_{IN0(LOW)}$	Input PWM Clock Low Frequency Detection Range on IN0	1.0	2.0	4.0	kHz	(32)
$f_{IN0(HIGH)}$	Input PWM Clock High Frequency Detection Range on IN0	100	–	400	kHz	(32)
f_{PWM}	Output PWM Frequency Range using external clock on IN0	31.25	–	781	Hz	
$A_{FPWM(CAL)}$	Output PWM Frequency Accuracy using Calibrated Oscillator	-10	–	+10	%	
$f_{PWM(0)}$	Default Output PWM Frequency using Internal Oscillator	84	120	156	Hz	
$t_{CSB(MIN)}$	CSB Calibration Low Minimum Time Detection Range	14	20	26	µs	
$t_{CSB(MAX)}$	CSB Calibration Low Maximum Time Detection Range	140	200	260	µs	
R_{PWM_1k}	Output PWM Duty Cycle Range for f_{PWM} = 1.0 kHz for high speed slew rate	10		94	%	(33)
R_{PWM_400}	Output PWM Duty Cycle Range for f_{PWM} = 400 Hz	6.0		98	%	(33)
R_{PWM_200}	Output PWM Duty Cycle Range for f_{PWM} = 200 Hz	5.0		98	%	(33)
Input timing						
t_{IN}	Direct Input Toggle Timeout	175	250	325	ms	
Autoretry timing						
t_{AUTO}	Autoretry Period	105	150	195	ms	
Temperature on the GND flag						
T_{OTWAR}	Thermal Prewarning Detection	110	125	140	°C	(34)
T_{FEED}	Analog Temperature Feedback at T_A = 25 °C with R_{CSNS} = 2.5 kΩ	1.15	1.20	1.25	V	
DT_{FEED}	Analog Temperature Feedback Derating with R_{CSNS} = 2.5 kΩ	-3.5	-3.7	-3.9	mV/°C	(34)

Notes

32. Clock Fail detector available for PWM_en bit is set to logic [1] and CLOCK_sel is set to logic [0].
33. The PWM ratio is measured at V_{HS} = 50% of V_{PWR} and for the default SR value. It is possible to put the device fully-on (PWM duty cycle 100%) and fully-off (duty cycle 0%). For values outside this range, a calibration is needed between the PWM duty cycle programming and the PWM on the output with R_L = 5.0 Ω resistive load.
34. Parameters guaranteed by design, not production tested.

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 20 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values are measured at T_A = 25 °C and at nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface characteristics (35)						
f_{SPI}	Maximum Frequency of SPI Operation	–	(41)	8.0	MHz	
t_{WRST}	Required Low State Duration for RSTB	10	–	–	µs	(36)
t_{CS}	Rising Edge of CSB to Falling Edge of CSB (Required Setup Time)	–	–	500	ns	(37)
t_{ENBL}	Rising Edge of RSTB to Falling Edge of CSB (Required Setup Time)	–	–	5.0	µs	(37)
t_{LEAD}	Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)	–	–	500	ns	(37)
t_{WSCLKh}	Required High State Duration of SCLK (Required Setup Time)	–	–	50	ns	(37)
t_{WSCLKl}	Required Low State Duration of SCLK (Required Setup Time)	–	–	50	ns	(37)
t_{LAG}	Falling Edge of SCLK to Rising Edge of CSB (Required Setup Time)	–	–	60	ns	(37)
$t_{SI(SU)}$	SI to Falling Edge of SCLK (Required Setup Time)	–	–	37	ns	(38)
$t_{SI(HOLD)}$	Falling Edge of SCLK to SI (Required Setup Time)	–	–	49	ns	(38)
t_{RSO}	SO Rise Time • C_L = 80 pF	–	–	13	ns	
t_{FSO}	SO Fall Time • C_L = 80 pF	–	–	13	ns	
t_{RSI}	SI, CSB, SCLK, Incoming Signal Rise Time	–	–	13	ns	(38)
t_{FSI}	SI, CSB, SCLK, Incoming Signal Fall Time	–	–	13	ns	(38)
$t_{SO(EN)}$	Time from Falling Edge of CSB to SO Low-impedance	–	–	60	ns	(39)
$t_{SO(DIS)}$	Time from Rising Edge of CSB to SO High-impedance	–	–	60	ns	(40)

Notes

35. Parameters guaranteed by design, not production tested.
36. RSTB low duration measured with outputs enabled and going to OFF or disabled condition.
37. Maximum setup time required for the 09XS3400 is the minimum guaranteed time needed from the microcontroller.
38. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
39. Time required for output status data to be available for use at SO. 1.0 kΩ on pull-up on CSB.
40. Time required for output status data to be terminated at SO. 1.0 kΩ on pull-up on CSB.
41. The SPI frequency is limited if t_{RSI} and t_{FSI} are higher than 13 ns due to resistor in series with SPI signal.

4.4 Timing diagrams

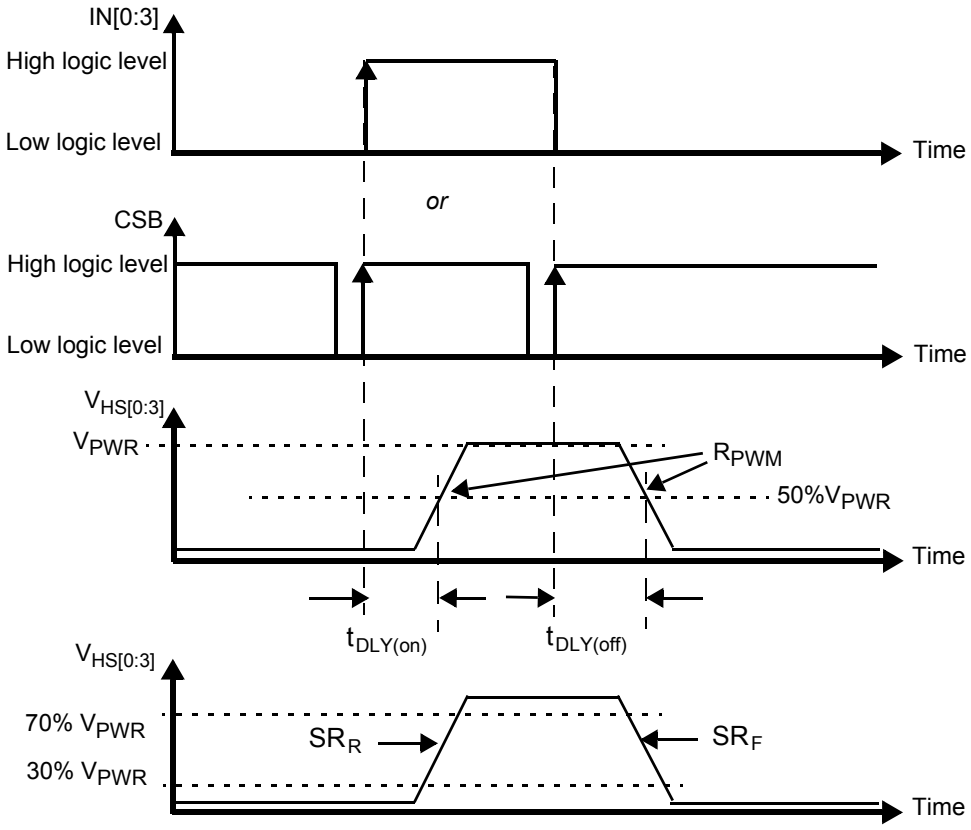


Figure 4. Output slew rate and time delays

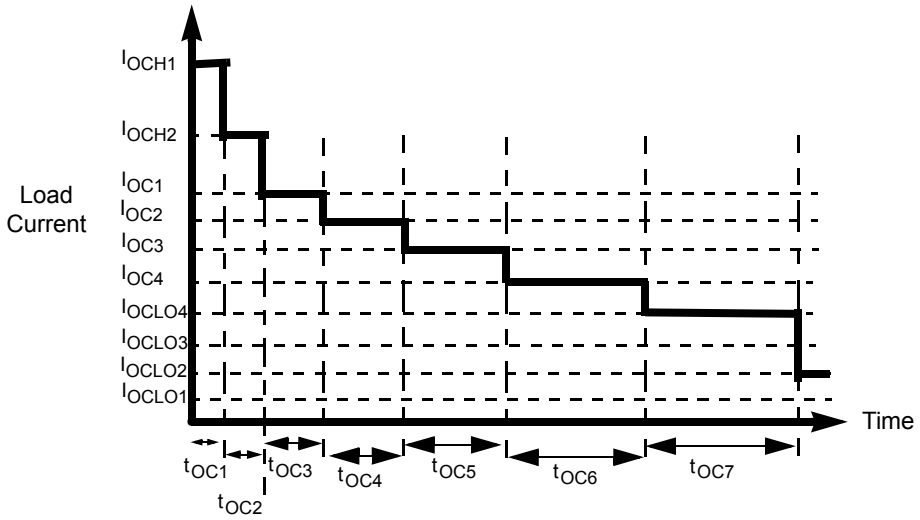


Figure 5. Overcurrent shutdown protection

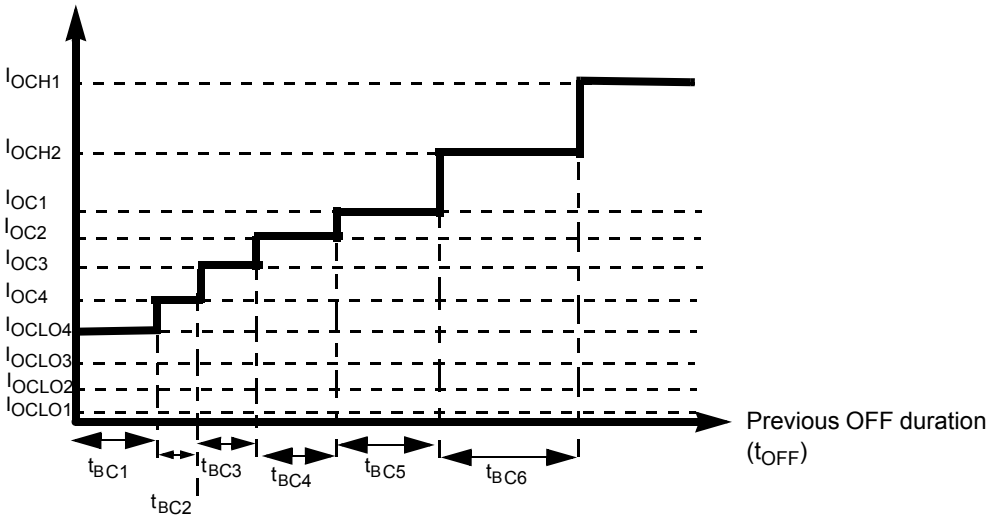


Figure 6. Bulb cooling management

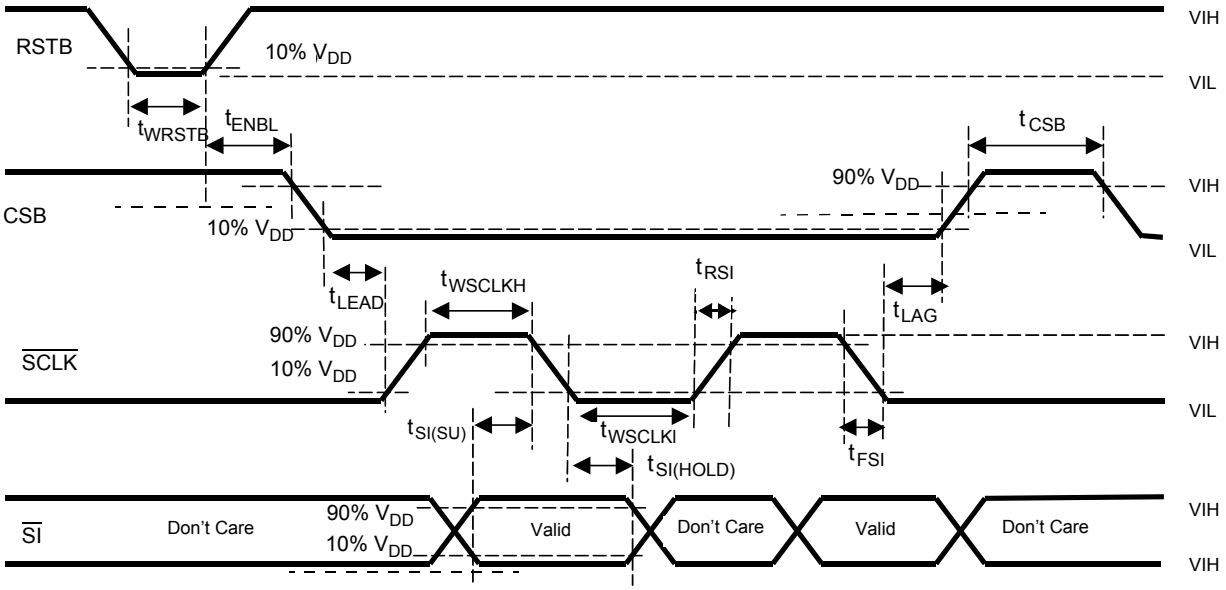


Figure 7. Input timing switching characteristics

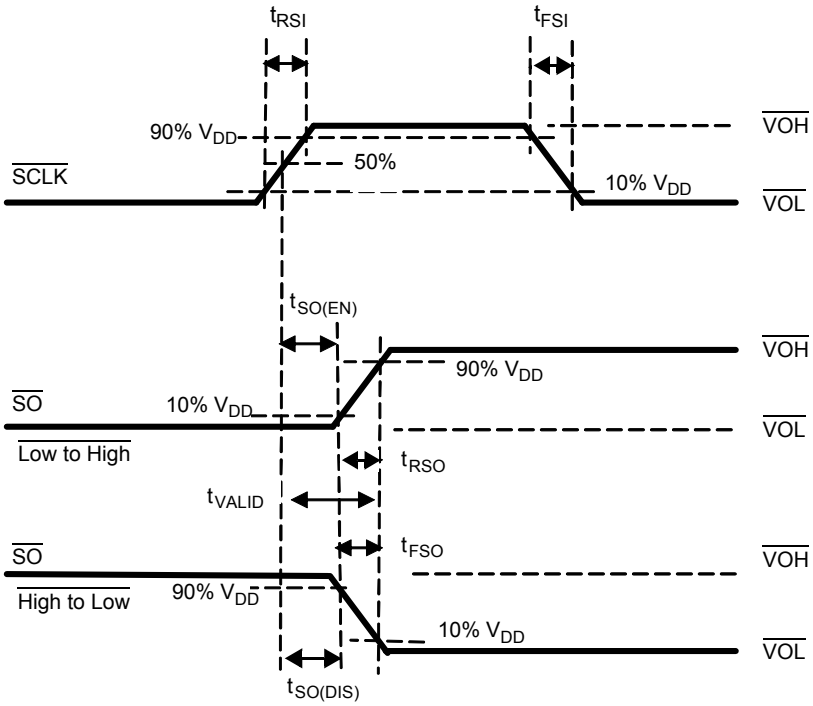


Figure 8. SCLK waveform and valid SO data delay time

5 Functional description

5.1 Introduction

The 09XS3400 is one in a family of devices designed for low-voltage automotive lighting applications. Its four low $R_{DS(on)}$ MOSFETs (quad 9.0 mΩ) can control four separate 55 W/28 W bulbs and/or Xenon modules.

Programming, control and diagnostics are accomplished using a 16-bit SPI interface. Its output with selectable slew-rate improves electromagnetic compatibility (EMC) behavior. Additionally, each output has its own parallel input or SPI control for pulse-width modulation (PWM) control if desired. The 09XS3400 allows the user to program via the SPI the fault current trip levels and duration of acceptable lamp inrush. The device has fail-safe mode to provide fail-safe functionality of the outputs in case of MCU damage.

5.2 Functional pin description

5.2.1 Output current monitoring (CSNS)

The current sense pin provides a current proportional to the designated HS0:HS3 output or a voltage proportional to the temperature on the GND flag. This current feeds into a ground-referenced resistor (2.5 kΩ typical) and its voltage is monitored by an MCU's A/D. The output type is selected via the SPI. This pin can be tri-stated through the SPI.

5.2.2 Direct inputs (IN0, IN1, IN2, IN3)

Each IN input wakes the device. The IN0:IN3 high-side input pins are also used to directly control HS0:HS3 high-side output pins. In case of the outputs are controlled by PWM module, the external PWM clock is applied to IN0 pin. These pins are to be driven with CMOS levels, and they have a passive internal pull-down, R_{DWN}.

5.2.3 Fault status (FSB)

This pin is an open drain configured output requiring an external pull-up resistor to V_{DD} for fault reporting. If a device fault condition is detected, this pin is active LOW. Detailed diagnostic and fault in formation is reported via the SPI SO pin.

5.2.4 Wake

The WAKE input wakes the device. An external resistor (10 kΩ typical) and in internal voltage clamp protect this pin from high damaging voltages. This input has a passive internal pull-down, R_{DWN}.

5.2.5 Reset (RSTB)

The reset input wakes the device. This is used to initialize the device configuration and fault registers, as well as place the device in a low current sleep mode. The pin also starts the watchdog timer when transitioning from logic [0] to logic [1]. This pin has a passive internal pull-down, R_{DWN}.

5.2.6 Chip select (CSB)

The CSB pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the device is capable of transferring information to, and receiving information from, the MCU. The 09XS3400 latches in data from the Input Shift registers to the addressed registers on the rising edge of CSB. The device transfers status information to the Shift register on the falling edge of CSB. The SO output driver is enabled when CSB is logic [0]. CSB should transition from a logic [1] to a logic [0] state only when SCLK is a logic [0]. CSB has an active internal pull-up to V_{DD}, I_{UP}.

5.2.7 Serial clock (SCLK)

The SCLK pin clocks the internal shift registers of the 09XS3400 device. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output (SO) pin shifts data information out of the SO line driver on the rising edge of the SCLK signal. The SCLK pin should be in a logic low state whenever CSB makes any transition. For this reason, it is recommended the SCLK pin be in a logic [0] whenever the device is not accessed (CSB logic [1] state). When CSB is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high-impedance) (see Figure 10). SCLK input has an active internal pull-down, I_{DWN}.

5.2.8 Serial Input (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 (MSB) to D0 (LSB). The internal registers of the 09XS3400 are configured and controlled using a 5-bit addressing scheme described in Table 10. Register addressing and configuration are described in Table 11. SI input has an active internal pull-down, I_{DWN}.

5.2.9 Digital drain voltage (VDD)

This pin is an external voltage input pin used to supply power to the SPI circuit. When V_{DD} is lost (V_{DD} Failure), the device goes to fail-safe mode.

5.2.10 Ground (GND)

These pins are the ground for the device.

5.2.11 Positive power supply (VPWR)

This pin connects to the positive power supply and is the source of operational power for the device. The VPWR contact is the backside surface mount tab of the package.

5.2.12 Serial output (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the CSB pin is put into a logic [0] state. The SO data is capable of reporting the status of the output, the device configuration, the state of the key inputs, etc. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. SO reporting descriptions are provided in Table 23.

5.2.13 High-side outputs (HS3, HS1, HS0, HS2)

These are protected 9.0 mΩ high-side power outputs to the loads.

5.2.14 Fail-safe input (FSI)

This pin incorporates an active internal pull-up current source from internal supply (V_{REG}). This enables the watchdog timeout feature. When the FSI pin is opened, the watchdog circuit is enabled. After a watchdog timeout occurs, the output states depends on IN[0:3]. In case of a V_{DD} failure and when V_{DD} failure detection is activated, the output states depend on IN{0:3].

5.3 Functional internal block description

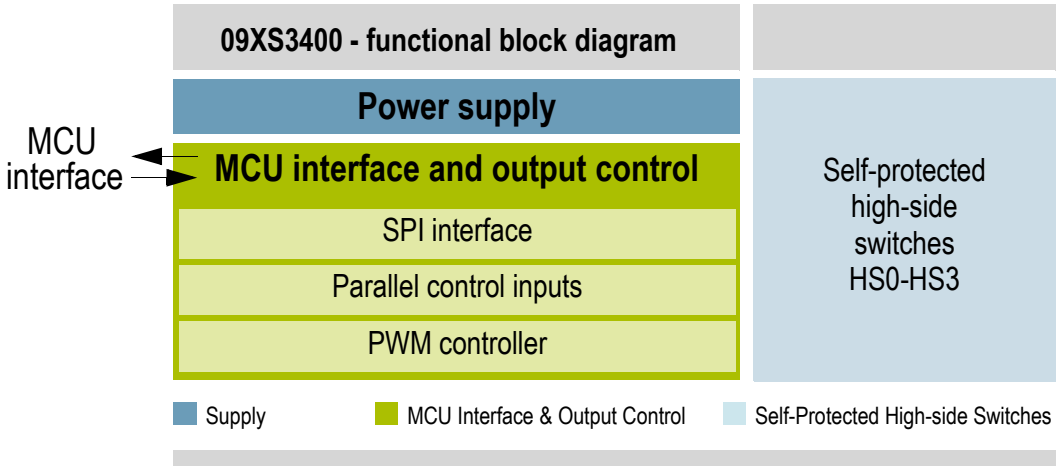


Figure 9. Functional block diagram

5.3.1 Power supply

The 09XS3400 is designed to operate from 4.0 V to 28 V on the VPWR pin. Device characterization is provided from 6.0 V to 20 V. The VPWR pin supplies power to internal regulator, analog, and logic circuit blocks. The V_{DD} supply is used for serial peripheral interface (SPI) communication to configure and diagnose the device. This IC architecture provides a low quiescent current sleep mode. Applying V_{PWR} and V_{DD} to the device places the device in the Normal mode. The device transits to fail-safe mode in case of failures on the SPI or/and on V_{DD} voltage.

5.3.2 High-side switches: HS0–HS3

These pins are the high-side outputs controlling automotive lamps, such as 65 W/55 W bulbs and Xenon-HID modules. Those N-channel MOSFETs with 9.0 mΩ $R_{DS(on)}$ are self-protected and present extended diagnostics in order to detect bulb outage and short-circuit fault condition. The HS output is actively clamped during turn off of inductive loads and inductive battery line. When driving DC motor or solenoid loads, an external recirculation device must be used to maintain the device in its safe operating area.

5.3.3 MCU interface and output control

In Normal mode, each bulb is controlled directly from the MCU through SPI. A pulse width modulation control module allows improvement of lamp lifetime with bulb power regulation (PWM frequency range from 100 Hz to 400 Hz) and addressing the dimming application (day running light). An analog feedback output provides a current proportional to the load current or the temperature of the board. The SPI is used to configure and to read the diagnostic status (faults) of high-side outputs. The reported fault conditions are: open load, short-circuit to battery, short-circuit to ground (overcurrent and severe short-circuit), thermal shutdown, and under/overvoltage. With accurate and configurable overcurrent detection circuitry and wire harness optimization, the vehicle is lighter.

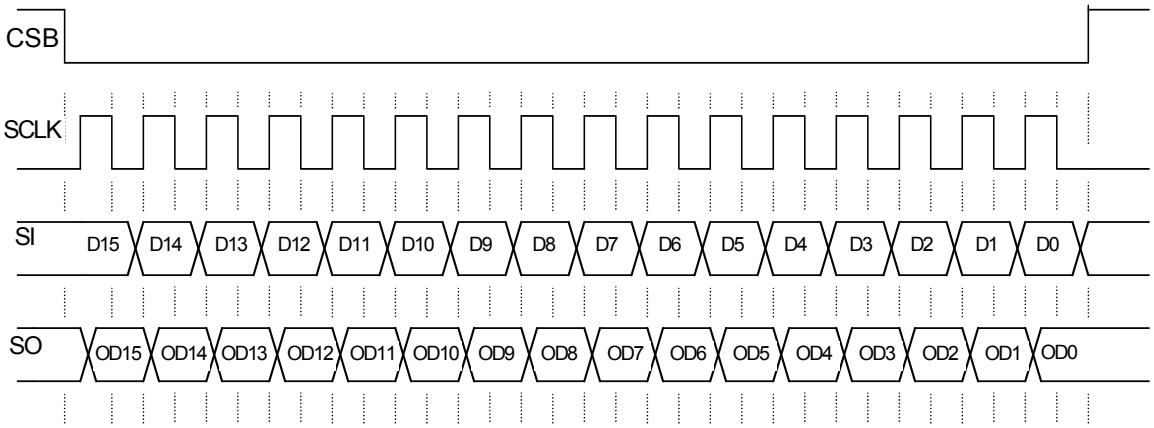
In Fail-safe mode, each lamp is controlled with dedicated parallel input pins. The device reverts to its default mode.

6 Functional device operation

6.1 SPI protocol description

The SPI interface has a full duplex, three-wire synchronous data transfer with four I/O lines associated with it: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select (CSB).

The SI/SO pins of the 09XS3400 follow a first-in first-out (D15 to D0) protocol, with both input and output words transferring the most significant bit (MSB) first. All inputs are compatible with 5.0 V or 3.3 V CMOS logic levels.



Notes 1. RSTB is a logic [1] state during the above operation.
2. D15:D0 relate to the most recent ordered entry of data into the device.
3. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the device.

Figure 10. Single 16-Bit word SPI Communication

6.2 Operational modes

The 09XS3400 has four operating modes: Sleep, Normal, Fail-safe, and Fault. Table 6 and Figure 12 summarize details contained in succeeding paragraphs. The Figure 11 describes an internal signal called IN_ON[x] which is a function of the respective IN[x] input.

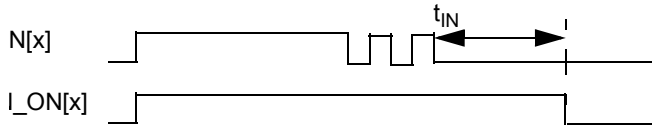


Figure 11. IN_ON[x] Internal Signal

The 09XS3400 transits to operating modes according to the following signals:

- wake-up = RSTB or WAKE or IN_ON[0] or IN_ON[1] or IN_ON[2] or IN_ON[3],
- fail = (V_{DD} Failure and VDD_FAIL_en) or (Watchdog timeout and FSI input not shorted to ground),
- fault = OC[0:3] or OT[0:3] or SC[0:3] or UV or (OV and $\overline{\text{OV\_dis}}$).

Table 6. 09XS3400 operating modes

Mode	Wake-up	Fail	Fault	Comments
Sleep	0	x	x	Device is in Sleep mode. All outputs are OFF.
Normal	1	0	0	Device is currently in Normal mode. Watchdog is active if enabled.
Fail-safe	1	1	0	Device is currently in fail-safe mode due to Watchdog timeout or V_{DD} Failure conditions.
Fault	1	X	1	Device is currently in fault mode. The faulted output(s) is (are) OFF. The safe autoretry circuitry is active to turn-on again the output(s).

x = Don't care.

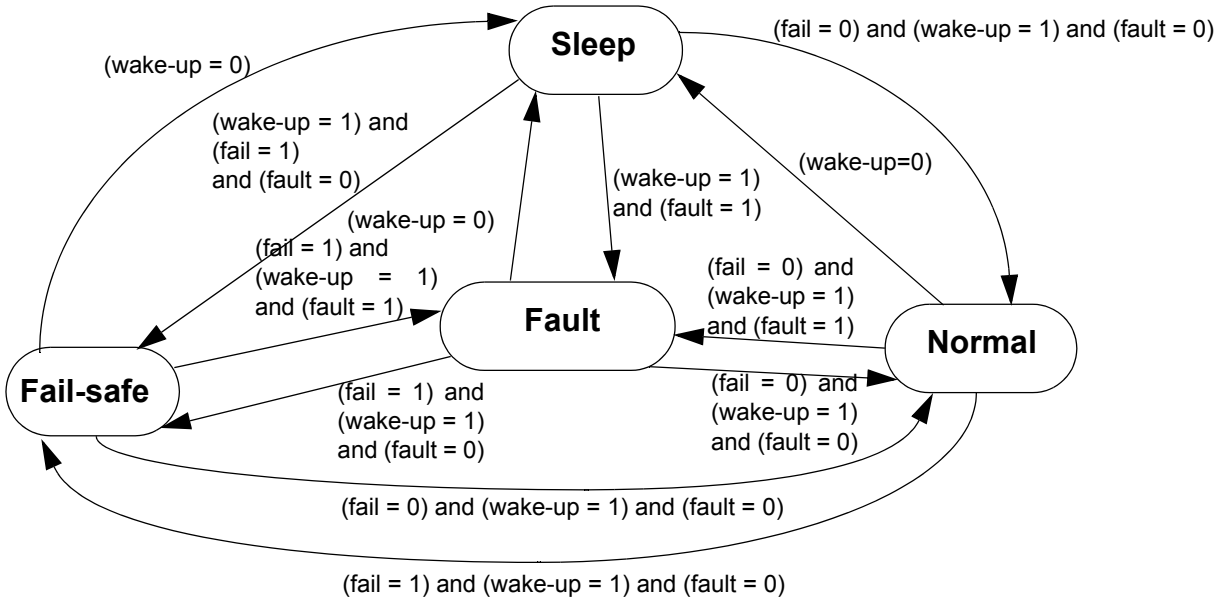


Figure 12. Operating modes

6.2.1 Sleep mode

The 09XS3400 is in Sleep mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 0,
- fail = X,
- fault = X.

This is the Default mode of the device after first applying battery voltage (V_{PWR}) prior to any I/O transitions. This is also the state of the device when the WAKE and RSTB and IN_ON[0:3] are logic [0]. In the Sleep mode, the output and all unused internal circuitry, such as the internal regulator, are off to minimize draw current. In addition, all SPI-configurable features of the device are set to logic [0].

6.2.2 Normal mode

The 09XS3400 is in Normal mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 1,
- fail = 0,
- fault = 0.

In this mode, the NM bit is set to fault_control logic [1] and the outputs HS[0:3] are under control, as defined by the hson signal:
hson[x] = (((IN[x] and $\overline{\text{DIR\_dis}}$[x]) or On bit[x]) and $\overline{\text{PWM\_en}}$) or (On bit [x] and Duty_cycle[x] and PWM_en).
In this mode and also in fail-safe, the fault condition reset depends on fault_control signal, as defined by the following:
fault_control[x] = ((IN_ON[x] and $\overline{\text{DIR\_dis}}$[x]) and $\overline{\text{PWM\_en}}$) or (On bit [x]).

6.2.2.1 Programmable PWM module

The outputs HS[0:3] are controlled by the programmable PWM module if PWM_en and On bit [x] are set to logic [1]. The clock frequency from IN0 input pin or from internal clock is the factor 2^7 (128) of the output PWM frequency (CLOCK_sel bit). The outputs HS[0:3] can be controlled in the range of 5% to 98% with a resolution of 7 bits of duty cycle (Table 7). The states of other IN pins are ignored.

Table 7. Output PWM Resolution

On bit	Duty cycle	Output state
0	**X**	**OFF**
1	0000000	PWM (1/128 duty cycle)
1	0000001	PWM (2/128 duty cycle)
1	0000010	PWM (3/128 duty cycle)
1	n	PWM ((n+1)/128 duty cycle)
1	1111111	fully ON

The timing includes seven programmable PWM switching delays (number of PWM clock rising edges) to stagger the turn on/off times of the outputs (Table 8).

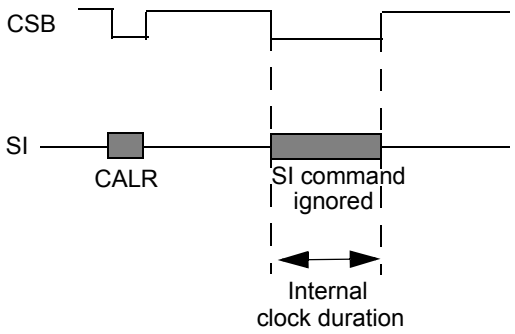
Table 8. Output PWM Switching Delay

Delay bits	Output delay
000	no delay
001	16 PWM clock periods
010	32 PWM clock periods
011	48 PWM clock periods
100	64 PWM clock periods
101	80 PWM clock periods
110	96 PWM clock periods
111	112 PWM clock periods

The clock frequency from IN0 is permanently monitored to report a clock failure in case the frequency is outside a specified frequency range (from $f_{IN0(LOW)}$ to $f_{IN0(HIGH)}$). During a clock failure, no PWM feature is provided, the On bit defines the outputs' states and the CLOCK_fail bit reports [1].

6.2.2.2 Calibratable internal clock

The internal clock can vary as much as ±30 percent relative to the to typical $f_{PWM(0)}$ output switching period. Using the existing SPI inputs and the precision timing reference already available to the MCU, the 09XS3400 allows clock calibration to ±10 percent of accuracy. Calibrating the internal clock is initiated by defined word to CALR register. The calibration pulse is provided by the MCU. The pulse is sent on the CSB pin after the SPI word is launched. The MCU keeps the CSB pin low for 1/128th of the desired PWM frequency.



If the negative CSB pulse is outside a predefined time range (from $t_{CSB(MIN)}$ to $t_{CSB(MAX)}$), the calibration event is ignored and the internal clock is unaltered or reset to its default value ($f_{PWM(0)}$), if this was not calibrated before. The calibratable clock is used, instead of the clock from IN0 input, when CLOCK_sel is set to [1].

6.2.3 Fail-safe mode

The 09XS3400 is in Fail-safe mode when:

- V_{PWR} is within the normal voltage range,
- wake-up = 1,
- fail = 1,
- fault = 0.

6.2.4 Watchdog

If the FSI input is not grounded, the watchdog timeout detection is active when either the WAKE or IN_ON[0:3] or RSTB input pin transitions from logic [0] to logic [1]. The WAKE input is capable of being pulled up to V_{PWR} with a series resistance limiting the internal clamp current according to the specification.

The Watchdog timeout interval is a multiple of the internal oscillator. As long as the WD bit (D15) of an incoming SPI message is toggled within the minimum watchdog timeout period (WDTO), the device operates normally.

6.2.4.1 Fail-safe conditions

If an internal watchdog timeout occurs before the WD bit for FSI open (Table 9) or in case of V_{DD} failure condition (V_{DD}< $V_{DD(FAIL)}$)) for VDD_FAIL_en bit is set to logic [1], the device reverts to a fail-safe mode until the WD bit is written to logic [1] (see fail-safe to normal mode transition paragraph) and V_{DD} is within the normal voltage range.

Table 9. SPI watchdog activation

Typical RFSI (Ω)	Watchdog
0 (shorted to ground)	Disabled
(open)	Enable

During the Fail-safe mode, the outputs depend on the corresponding input. The SPI register contents are reset to their default values (except POR bit) and fault protections are fully operational. The NM bit is set to (0] when the device is in Fail-safe mode.

6.2.5 Normal and fail-safe mode transitions

6.2.5.1 Transition fail-safe to normal mode

To leave the Fail-safe mode, V_{DD} must be within its valid operating voltage range and the microcontroller has to send an SPI command with WDIN bit set to logic [1]; the other bits are not considered. The previously latched faults are reset by the transition into Normal mode (autoretry included). Moreover, the device can be brought out of the Fail-safe mode due to a watchdog timeout issue by forcing the FSI pin to logic [0].

6.2.5.2 Transition normal to fail-safe mode

To enter the Fail-safe mode from normal mode, a fail-safe condition must occur (fail = 1). The previous latched faults are reset by the transition into Fail-safe mode (autoretry included).

6.2.6 Fault mode

The 09XS3400 is in Fault mode when:

- V_{PWR} and V_{DD} are within the normal voltage range,
- wake-up = 1,
- fail = X,
- fault = 1.

This device indicates the faults below as they occur by driving the FSB pin to logic [0], provided the RSTB input is pulled up:

- Overtemperature fault,
- Overcurrent fault,
- Severe short-circuit fault,
- Output(s) shorted to VPWR fault in OFF state,
- Open load fault in OFF state,
- Overvoltage fault (enabled by default),
- Undervoltage fault.

The FS pin automatically returns to logic [1] when the fault condition is removed, except for overcurrent, severe short-circuit, overtemperature, and undervoltage which resets by a new turn-on command (each fault_control signal to be toggled). Fault information is retained in the SPI fault register and is available (and reset) via the SO pin during the first valid SPI communication. The open load fault in ON state is only reported through the SPI register without effect on the corresponding output state (HS[x]) and the FSB pin.

6.2.7 Typical start-up sequence

The 09XS3400 enters in Normal mode after start-up if following sequence is provided:

- V_{PWR} and V_{DD} power supplies must be above their undervoltage thresholds,
- generate wake-up event (wake-up = 1) from 0 to 1 on RSTB. The device switches to Normal mode with SPI register content is reset (as defined in Table 11 and Table 23). All features of the 09XS3400 are available after 50 µs typical, and all SPI registers are set to default values (set to logic [0]).
- toggle WD bit from 0 to 1.

And, if the PWM module is used (PWM_en bit is set to logic [1]) with an external reference clock:

- apply PWM clock on IN0 input pin between 26 µs and 140 µs.

If the correct start-up sequence is not provided, the PWM function is not guaranteed.

6.3 Protection and diagnostic features

6.3.1 Protections

6.3.1.1 Overtemperature fault

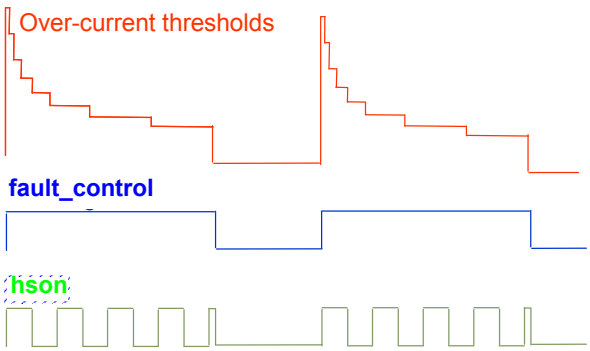
The 09XS3400 incorporates overtemperature detection and shutdown circuitry for each output channel. Two cases need to be considered when the output temperature is higher than T_{SD}:

- If the output command is ON: the corresponding output is latched OFF. FSB also latches to logic [0]. To delatch the fault and be able to turn ON again the outputs, the failure condition must disappear and the autoretry circuitry must be active or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output) or $V_{SUPPLY(POR)}$ condition if V_{DD} = 0.
- If the output command is OFF: FSB goes to logic [0] until the corresponding output temperature is below T_{SD}.

For both cases, the fault register OT[0:3] bit into the status register is set to [1]. The fault bits are cleared in the status register after a SPI read command.

6.3.1.2 Overcurrent fault

The 09XS3400 incorporates output shutdown to protect each output structure against resistive short-circuit condition. This protection is composed of four predefined current levels (time dependent) to fit Xenon-HID current profiles by default or 55 W bulb profiles, selectable by Xenon bit (as illustrated Figure 14). Initial turn-on of a cold lamp filament usually creates a large inrush current, as shown in Figure 5. This overcurrent protection is programmable: OC[1:0] bits select overcurrent slope speed and OCHI1 current step can be removed in case of OCHI bit is set to [1].

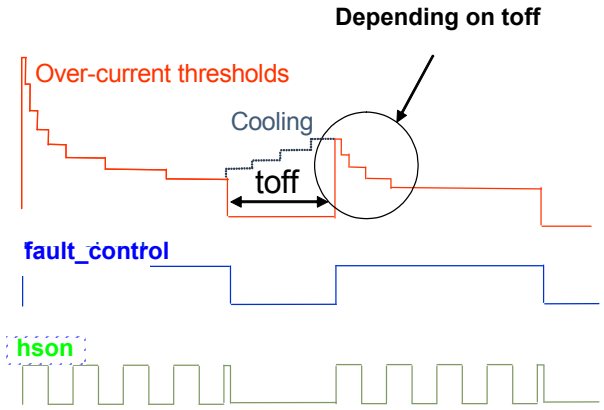


In steady state, the wire harness is protected by OCLO2 current level by default. Three other DC overcurrent levels are available: OCLO1 or OCLO3 or OCLO4 based on the state of the OCLO[1,0] bits.

If the load current level ever reaches the overcurrent detection level, the corresponding output latches the output OFF and FSB is also latched to logic [0]. To delatch the fault and be able to turn ON again the corresponding output, the failure condition must disappear and the autoretry circuitry must be active or the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output) or the $V_{SUPPLY(POR)}$ condition if V_{DD} = 0.

The SPI fault bits (OC[0:3] bits) are cleared after a read operation.

In Normal mode using internal PWM module, the 09XS3400 also incorporates a cooling bulb filament management if OC_mode and Xenon are set to logic [1]. In this case, the 1st step of multi-step overcurrent protection depends on the previous OFF duration, as illustrated in Figure 6. The following figure illustrates how the current level depends on the duration of previous OFF state (toff). The slope of cooling bulb emulator is configurable with OCOFFCB[1:0] bits.



6.3.1.3 Severe short-circuit fault

The 09XS3400 immediately turns-off an output channel if it detects a severe short circuit at turn-on. If the short-circuit impedance is below R_{SHORT}, the device latches the output OFF, FSB goes to logic [0] and the fault register SC[0:3] bit is set to [1]. To delatch the fault and be able to turn ON again the outputs, the failure condition must disappear and the corresponding output must be commanded OFF and then ON (toggling fault_control signal of corresponding output) or $V_{SUPPLY(POR)}$ condition if V_{DD} = 0. The SPI fault bits (SC[0:3] bits) are cleared after a read operation.

6.3.1.4 Overvoltage fault (enabled by default)

By default, the overvoltage protection is enabled. The 09XS3400 shuts down all outputs and FSB goes to logic [0] during an overvoltage fault condition on the VPWR pin ($V_{PWR} \geq V_{PWR(OV)}$). The outputs remain in the OFF state until the overvoltage condition is removed ($V_{PWR} \leq V_{PWR(OV)} - V_{PWR(OVHYS)}$). When experiencing this fault, the OVF fault bit is set to logic [1] and cleared after a valid SPI read.

The overvoltage protection can be disabled through SPI (OV_dis bit is disabled when set to logic [1]). The fault register reflects any overvoltage condition ($V_{PWR} \geq V_{PWR(OV)}$). This overvoltage diagnosis, as a warning, is removed after a read operation, if the fault condition disappears. The HS[0:3] outputs cannot be commanded on during an over voltage condition.

6.3.1.5 Undervoltage fault

The output(s) latch off at some battery voltage below $VPWR_{(UV)}$. As long as the V_{DD} level stays within the normal specified range, the internal logic states within the device will remain (configuration and reporting). If the battery voltage drops below the undervoltage threshold ($V_{PWR} \leq V_{PWR(UV)}$), the outputs turn off, FSB goes to logic [0], and the fault register UV bit is set to [1].

The FSB pin follows the battery voltage. This pin goes to a logic [0] when $V_{PWR} < V_{PWR(UV)}$ and returns to a logic [1] when $V_{PWR} > V_{PWR(UV)\_UP}$.

In **extended mode**, the output is protected by overtemperature shutdown circuitry. All previous latched faults, which occurred when V_{PWR} was within the normal voltage range, are guaranteed if V_{DD} is within the operational voltage range or until $V_{SUPPLY(POR)}$ if V_{DD} = 0. Any new OT fault is detected (VDD failure included) and reported through SPI above $V_{PWR(UV)}$. The output state is not changed as long as the V_{PWR} voltage does not drop any lower than 3.5 V typical.

Below 3.5 V (typ) of V_{PWR}, the output shutdown delay time is not guaranteed. The N-channel MOSFSET could drain current during the next 10 µs to 30 µs.

All latched faults (overtemperature, overcurrent, severe short-circuit, over and undervoltage) are reset if:

- $V_{DD} \leq V_{DD(FAIL)}$ with V_{PWR} in nominal voltage range,
- V_{DD} and V_{PWR} supplies are below $V_{SUPPLY(POR)}$ voltage value.

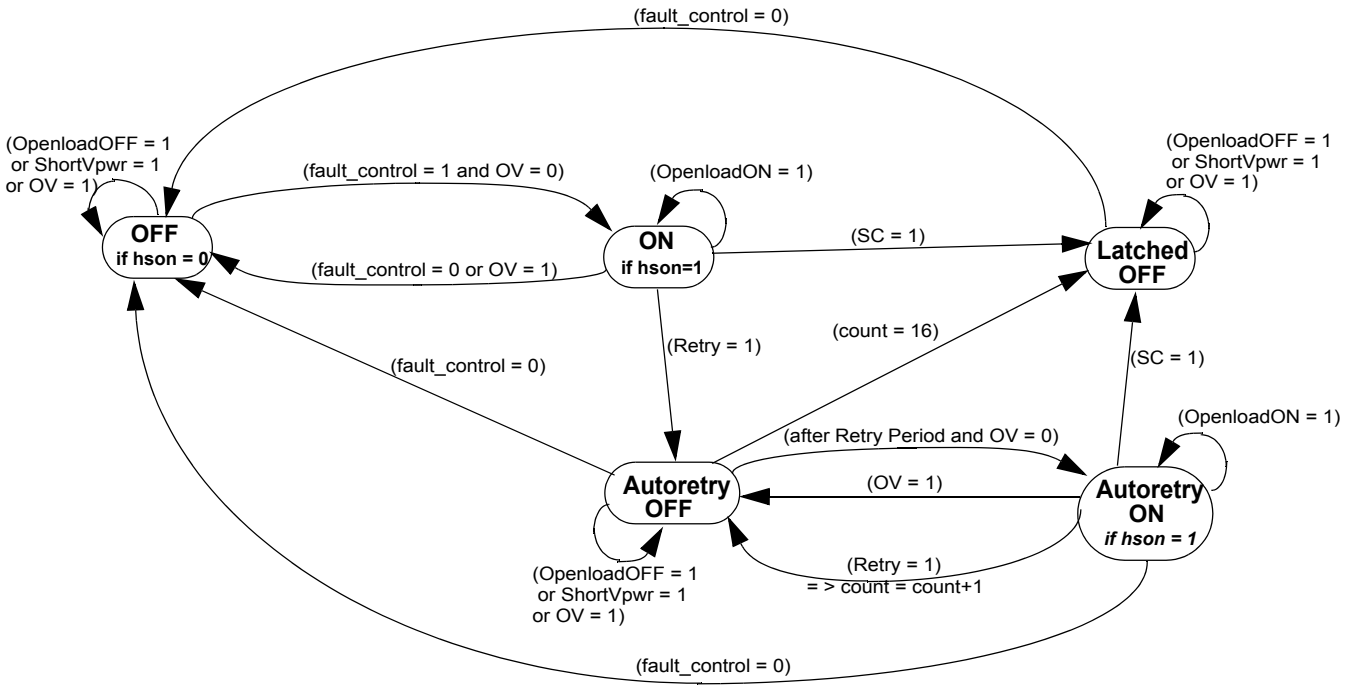


Figure 13. Auto-retry state machine

6.3.2 Auto-retry

The auto-retry circuitry is used to reactivate the output(s) automatically in case of overcurrent or overtemperature or undervoltage failure conditions, to provide a high availability of the load.

Auto-retry feature is available in Fault mode. It is activated when the internal retry signal is set to logic [1]:

retry[x] = OC[x] or OT[x] or UV.

The feature attempts to reactivate the output(s) after one auto-retry period (t_{AUTO}), limited to 16 retries per channel. The counter of retry occurrences is reset in case of Fail-safe to Normal or Normal to Fail-safe mode transitions. At each auto-retry, the overcurrent detection is set to default values to sustain the inrush current. The Figure 13 describes the auto-retry state machine.

6.3.3 Diagnostic

6.3.3.1 Output shorted to VPWR fault

The 09XS3400 incorporates output shorted to V_{PWR} detection circuitry in OFF state. Output shorted to V_{PWR} fault is detected if output voltage is higher than $V_{OSD(THRES)}$ and reported as a fault condition when the output is disabled (OFF). The output shorted to V_{PWR} fault is latched into the status register after the internal gate voltage is pulled low enough to turn OFF the output. The OS[0:3] and OL_OFF[0:3] fault bits are set in the status register and the FSB pin reports the fault in real time. If the output shorted to VPWR fault is removed, the status register clears after reading the register. The output shorted to V_{PWR} protection can be disabled through the SPI (OS_DIS[0:3] bit).

6.3.3.2 Open load faults

The 09XS3400 incorporates three dedicated open load detection circuitries on the output to detect in OFF and in ON state.

6.3.3.3 Open-load detection in off state

The OFF output open load fault is detected when the output voltage is higher than $V_{OLD(THRES)}$ pulled up with internal current source ($I_{OLD(off)}$) and reported as a fault condition when the output is disabled (OFF). The OFF Output open load fault is latched into the status register when the internal gate voltage is pulled low enough to turn OFF the output. The OL_OFF[0:3] fault bit is set in the status register. If the open load fault is removed (FSB output pin goes to high), the status register clears after reading the register. The OFF output open load protection can be disabled through the SPI (OLOFF_DIS[0:3] bit).

6.3.3.4 Open load detection in on state

The ON output open load current thresholds can be chosen by the SPI to monitor standard bulbs or LEDs (OLLED[0:3] bit set to logic [1]). In the case where load current drops below the defined current threshold, the OLON bit is set to logic [1], the output stays ON and FSB is not disturbed.

6.3.3.5 Open load detection in on state for LED

Open load for LEDs only (OLLED[0:3] set to logic [1]) is detected periodically each t_{OLLED} (fully-on, D[6:0] = 7F). To detect OLLED in fully-on state, the output must be ON at least t_{OLLED}. To delatch the diagnosis, the condition should be removed and an SPI read operation is needed (OL_ON[0:3] bit). The ON output open-load protection can be disabled through SPI (OLON_DIS[0:3] bit).

6.3.4 Analog current recopy and temperature feedbacks

The CSNS pin is an analog output reporting a current proportional to the designed output current or a voltage proportional to the temperature of the GND flag (pin #14). The designed signal is SPI programmable (TEMP_en, CSNS_en, CSNS_s[1,0] and CSNS_ratio_s bits).

In case the current recopy is active, the CSNS output delivers current only during ON time of the output switch. The CSNS control circuitry creates the signal without overshoot. The maximum current is.0 mA typical. The typical value of external CSNS resistor connected to the ground is 2.5 kΩ. The current recopy is not active in Fail-safe mode.

6.3.4.1 Temperature prewarning detection

In Normal mode, the 09XS3400 provides a temperature prewarning reported via SPI if the temperature of the GND flag is higher than T_{OTWAR}. This diagnosis (OTW bit set to [1]) is latched in the SPI DIAGR0 register. To delatch this diagnostic, a read SPI command is needed and the temperature must be below T_{OTWAR}.

6.3.5 Active clamp on VPWR

The device provides an active gate clamp circuit to limit the maximum transient V_{PWR} voltage at $VPWR_{(CLAMP)}$. In case of an overload on an output, the corresponding output is turned off, which leads to high voltage at V_{PWR} with an inductive V_{PWR} line. When V_{PWR} voltage exceeds $V_{PWR(CLAMP)}$ threshold, the turn-off on the corresponding output is deactivated and all HS[0:3] outputs are switched ON automatically to demagnetize the inductive Battery line.

6.3.6 Reverse battery on VPWR

The output survives the application of reverse voltage as low as -18 V. Under these conditions, the ON resistance of the output is two times higher than typical ohmic values in forward mode. No additional passive components are required except a diode in the V_{DD} regulator circuitry.

6.3.7 Ground disconnect protection

In the event the 09XS3400 ground is disconnected from load ground, the device protects itself and safely turns OFF the outputs regardless of the state of the outputs at the time of disconnection (maximum V_{PWR} = 16 V). A 10 kΩ resistor needs to be added between the MCU and each digital input pin in order to ensure the device turns off during a ground disconnect and to prevent this pin from exceeding maximum ratings.

6.3.8 Loss of supply lines

6.3.8.1 Loss of V_{DD}

If the external V_{DD} supply is disconnected (or not within specification: $V_{DD} < V_{DD(FAIL))}$ with VDD_FAIL_en bit is set to logic [1]), all SPI register content is reset.

The outputs can still be driven by the direct inputs IN[0:3] if V_{PWR} is within its specified voltage range. The 09XS3400 uses the battery input to power the output MOSFET-related current sense circuitry and any other internal logic providing fail-safe device operation with no V_{DD} supplied. In this state, the overtemperature, overcurrent, severe short-circuit, short to V_{PWR}, and OFF open load protection circuitry are fully operational with default values corresponding to all SPI bits are set to logic [0]. SPI fault register remain reset.

During a loss of V_{DD}, no current is conducted from V_{PWR} to V_{DD}.

6.3.8.2 Loss of V_{PWR}

If the external V_{PWR} supply is disconnected (or not within specification), the SPI configuration, reporting, and daisy chain features are maintained provided $\overline{RST}$ to set to logic [1] and V_{DD} is within nominal operating range. This fault condition can be diagnosed with UV fault in SPI STATR_s registers. The SPI pull-up and pull-down current sources are not operational. The previous device configuration is maintained. No current is conducted from V_{DD} to V_{PWR}.

6.3.8.3 Loss of V_{PWR} and V_{DD}

If the external V_{PWR} and V_{DD} supplies are disconnected (or not within specification: (V_{DD} and V_{PWR}) < $V_{SUPPLY(POR)}$), all SPI register contents are reset with default values corresponding to all SPI bits are set to logic [0] and all latched faults are also reset.

6.3.9 EMC performances

All following tests are performed on Freescale evaluation board in accordance with the typical application schematic. The device is protected during positive and negative transients on the V_{PWR} line (per ISO 7637-2). The 09XS3400 successfully meets the Class 5 of the CISPR25 emission standard and 200 V/m or BCI 200 mA injection level for immunity tests.

6.4 Logic commands and registers

6.4.1 Serial input communication

SPI communication is accomplished using 16-bit messages. A message is transmitted by the MCU starting with the MSB D15 and ending with the LSB, D0 (Table 10). Each incoming command message on the SI pin can be interpreted using the following bit assignments: the MSB, D15, is the watchdog bit (WDIN). In some cases, output selection is done with bits D14:D13. The next three bits, D12:D10, are used to select the command register. The remaining nine bits, D8:D0, are used to configure and control the outputs and their protection features.

Multiple messages can be transmitted in succession to accommodate those applications where daisy-chaining is desirable, or to confirm transmitted data, as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message not 16 bits is ignored. The 09XS3400 has defined registers, which are used to configure the device and to control the state of the outputs. Table 11 summarizes the SI registers.

Table 10. SI message bit assignment

Bit sig	SI Msg bit	Message bit description
MSB	D15	Watchdog in: toggled to satisfy watchdog requirements.
	D14:D13	Register address bits used in some cases for output selection (Table 12).
	D12:D10	Register address bits.
	D9	Not used (set to logic [0]).
LSB	D8:D0	Used to configure the inputs, outputs, and the device protection features and SO status content.

Table 11. Serial input address and configuration bit map

SI Register	SI data															
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
STATR_s	WDIN	X	X	0	0	0	0	0	0	0	0	SOA4	SOA3	SOA2	SOA1	SOA0
PWMR_s	WDIN	A_1	A_0	0	$\overline{0}$	1	$\overline{0}$	0 [42]	ON_s	PWM6_s	PWM5_s	PWM4_s	PWM3_s	PWM2_s	PWM1_s	PWM0_s
CONFR0_s	WDIN	A_1	A_0	0	$\overline{1}$	0	$\overline{0}$	0	0	0	DIR_dis_s	SR1_s	SR0_s	DELAY2_s	DELAY1_s	DELAY0_s
CONFR1_s	WDIN	A_1	A_0	0	1	1	0	0	0	Retry_ unlimited_s	Retry_dis_ s	OS_dis_s	OLON_dis _s	OLOFF_dis _s	OLLED_en _s	CSNS_rati o_s
OCR_s	WDIN	A_1	A_0	1	0	0	0	Xenon_s	BC1_s	BC0_s	OC1_s	OC0_s	OCHI_s	OLCO1_s	OLCO0_s	OC_mode_ s
GCR	WDIN	0	0	1	0	1	0	VDD_FAIL _en	PWM_en	CLOCK_se l	TEMP_en	CSNS_en	CSNS1	CSNS0	X	OV_dis
CALR	WDIN	0	0	1	1	1	0	1	0	1	0	1	1	0	1	1
Register state after $\overline{RST}$ = 0 or $V_{DD(FAIL)}$ or $V_{SUPPLY(POR)}$ condition	0	0	0	X	X	X	0	0	0	0	0	0	0	0	0	0

x = Don't care.
s = Output selection with the bits A_1A_0 as defined in Table 12.

Notes
42. The PWMR_s D8 bit must always be a logic low and never placed in a logic high.

6.4.2 Device register addressing

The following section describes the possible register addresses (D[14:10]) and their impact on device operation.

6.4.2.1 Address XX000—status register (STATR_s)

The STATR register is used to read the device status and the various configuration register contents without disrupting the device operation or the register contents. The five least significant register bits, F[4:0], are called SOA[4:0]. Bits SOA[4:3] are used to select the output channel of interest and bit SOA[2:0] are used to request status information for that channel. The status is returned as part of the first sixteen bits of the SO data. In addition to the device status, this feature provides the ability to read the content of the PWMR_s, CONFR0_s, CONFR1_s, OCR_s, GCR and CALR registers (Refer to the section 6.4.3 Serial output communication (device status return data), page 36.

6.4.2.2 Address $A_1A_0$001—output PWM control register (PWMR_s)

The PWMR_s register allows the MCU to control the state of corresponding output through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Tables 12).

Table 12. Output selection

A_1 (D14)	A_0 (D13)	HS selection
0	0	HS0 (default)
0	1	HS1
1	0	HS2
1	1	HS3

Bit D7 sets the output’s on/off state. A logic [1] enables the corresponding output switch and a logic [0] turns it OFF (if IN input is also pulled down). Bits D6:D0 set the output PWM duty-cycle to one of 128 levels provided PWM_en is set to logic [1], as shown Table 7.

6.4.2.3 Address $A_1A_0$010—output configuration register (CONFR0_S)

The CONFR0_s register allows the MCU to configure corresponding output switching through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Table 12).

For the selected output, a logic [0] on bit D5 (DIR_DIS_s) will enable the output for direct control by its respective IN[3:0] pin. A logic [1] on bit D5 will disable the output from direct control (in this case, the output is only controlled by On bit).

D4:D3 bits (SR1_s and SR0_s) are used to select the high or medium or low speed slew rate for the selected output, the default value [00] corresponds to the medium speed slew rate (Table 13).

Table 13. Slew rate speed selection

SR1_s (D4)	SR0_s (D3)	Slew rate speed
0	0	medium (default)
0	1	low
1	0	high
1	1	Not guaranteed

Incoming message bits D[2:0] specify the desired PWM switching delay. This delay is relative to the PWM clock rising edge as illustrated in Table 8. The adjustable phase delay is available only when the PWM_en bit is set to logic [1].

6.4.2.4 Address $A_1A_0$011—output configuration register (CONFR1_s)

The CONFR1_s register allows the MCU to configure corresponding output fault management through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Table 12).

A logic [1] on bit D6 (RETRY_unlimited_s) disables the autoretry counter for the selected output, the default value [1] corresponds to enable auto-retry feature without time limitation.

A logic [1] on bit D5 (RETRY_dis_s) disables the auto-retry for the selected output, the default value [0] enables this feature.

A logic [1] on bit D4 (OS_dis_s) disables the output hard shorted to V_{PWR} protection for the selected output, the default value [0] enables this feature.

A logic [1] on bit D3 (OLON_dis_s) disables the ON output open load detection for the selected output, the default value [0] enables this feature (Table 14).

A logic [1] on bit D2 (OLOFF_dis_s) disables the OFF output open load detection for the selected output, the default value [0] enables this feature.

A logic [1] on bit D1 (OLLED_en_s) enables the ON output open load detection for LEDs for the selected output, the default value [0] enables the On output openload detection for bulbs (Table 14).

Table 14. On open load selection

OLON_dis_s (D3)	OLLED_en_s (D1)	ON Open Load Detection
0	0	enable with bulb threshold (default)
0	1	enable with LED threshold
1	X	disable

A logic [1] on bit D0 (CSNS_ratio_s) selects the high ratio on the CSNS pin for the corresponding output. The default value [0] is the low ratio (Table 15).

Table 15. Current sense ratio selection

CSNS_high_s (D0)	Current sense ratio
0	CRS0 (default)
1	CRS1

6.4.2.5 Address A_1A_0100—output overcurrent register (OCR)

The OCR_s register allows the MCU to configure corresponding output overcurrent protection through the SPI. Each output “s” is independently selected for configuration based on the state of the D14:D13 bits (Table 12). A logic [1] on bit D8 ($\overline{\text{Xenon}}$_s) disables the Xenon overcurrent profile, as described Table 14.

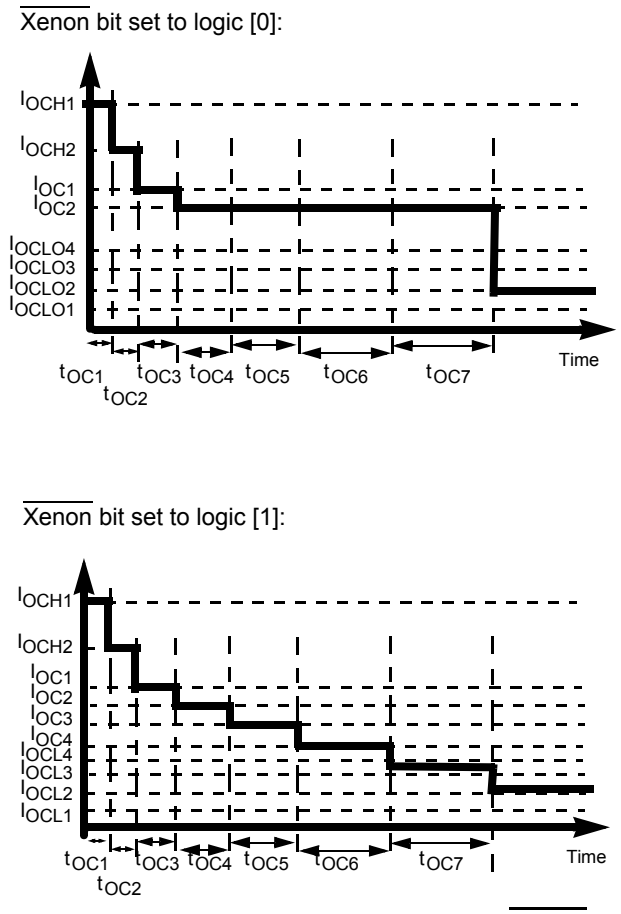


Figure 14. Overcurrent profile depending on $\overline{\text{xenon}}$ bit

D[7:6] bits are used to select the bulb cooling curves and D[5:4] bits modify the decay speed of the overcurrent profile, as shown Table 16 and Table 17.

Table 16. Cooling curve selection

BC1_s (D7)	BC0_s (D6)	Profile Curves Speed
0	0	medium (default)
0	1	slow
1	0	fast
1	1	medium

Table 17. Inrush curve selection

OC1_s (D5)	OC0_s (D4)	Profile Curves Speed
0	0	slow (default)
0	1	fast
1	0	medium
1	1	very slow

A logic [1] on bit D3 (OCHI_s bit reduces the current threshold from I_{OCHI1} to I_{OCHI2} during t_{OC1}, as shown Table 15.

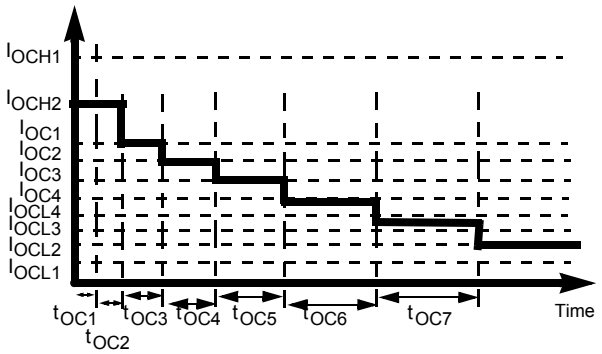


Figure 15. Overcurrent profile with OCHI bit set to '1'

The wire harness is protected by one of four possible current levels in steady state, as defined in Table 18.

Table 18. Output steady state selection

OCLO1 (D2)	OCLO0 (D1)	Steady state current
0	0	OCLO2 (default)
0	1	OCLO3
1	0	OCLO4
1	1	OCLO1

Bit D0 (OC_mode_sel) determines which of two overcurrent modes the output uses. In one mode the overcurrent profile is used every time the output turns on. In the other mode, Which can be used during PWM operation, the overcurrent profile is adjusted to account for bulb cooling effects, as described Table 19.

Table 19. Overcurrent mode selection

OC_mode_s (D0)	Overcurrent Mode
0	only inrush current management (default)
1	inrush current and bulb cooling management

6.4.2.6 Address 00101—global configuration register (GCR)

The GCR register allows the MCU to configure the device through the SPI. The D8 bit controls how the device responds to a VDD_FAIL condition, which is, $V_{DD} < V_{DD(FAIL)}$. If the VDD_FAIL_en bit is logic [1], then the loss of VDD, the device enters immediately in Fail-safe mode. In the VDD_FAIL_en bit is logic [0], the Fail-safe mode transition is done after the SPI watchdog timeout.

Bit D8 allows the MCU to enable or disable the V_{DD} failure detector. A logic [1] on VDD_FAIL_en bit allows switch-off the outputs HS[0:3] in fail-safe mode. Bit D7 allows the MCU to enable or disable the PWM module. A logic [1] on PWM_en bit allows control of the outputs HS[0:3] with PWMR register (the direct input states are ignored). Bit D6 (CLOCK_sel) is used to select the clock used as reference by PWM module, as described in the following Table 20.

Table 20. PWM module selection

PWM_en (D7)	CLOCK_sel (D6)	PWM module
0	X	PWM module disabled (default)
1	0	PWM module enabled with external clock from IN0
1	1	PWM module enabled with internal calibrated clock

Bits D5:D4 allow the MCU to select one of two analog signals on CSNS output pin, as shown in Table 21.

Table 21. CSNS reporting selection

TEMP_en (D5)	CSNS_en (D4)	CSNS reporting
0	0	CSNS tri-stated (default)
X	1	current recopy of selected output (D3:2] bits)
1	0	temperature on GND flag

The Table 22 describes how bits D[3:2] specifies the output channel whose current is being mirrored at the CSNS pin.

Table 22. Output current recopy selection

CSNS1 (D3)	CSNS0 (D2)	CSNS reporting
0	0	HS0 (default)
0	1	HS1
1	0	HS2
1	1	HS3

The GCR register disables the overvoltage protection (D0). When this bits is [0], the overvoltage is enabled (default value).

6.4.2.7 Address 00111—calibration register (CALR)

The CALR register allows the MCU to calibrate internal clock.

6.4.3 Serial output communication (device status return data)

When the CSB pin is pulled low, the output register is loaded. Meanwhile, the data is clocked out MSB- (OD15-) first as the new message data is clocked into the SI pin after a CSB transition. The first sixteen bits of data clocking out of the SO are dependent upon the previously written SPI word.

Any bits clocked out of the Serial Output (SO) pin after the first 16 bits are representative of the initial message bits clocked into the SI pin since the CSB pin first transitioned to a logic [0]. This feature is useful for daisy-chaining devices as well as for message verification.

A valid message length is determined following a CSB transition of [0] to [1]. If there is a valid message length, the data is latched into the appropriate registers. A valid message length is a multiple of 16 bits. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

SO data includes information ranging from fault status to register contents, user selected by writing to the STATR bits OD4, OD3, OD2, OD1, and OD0. The value of the previous bits SOA4 and SOA3 determine which output the SO information applies to for the registers which are output specific; viz., Fault, PWMR, CONFR0, CONFR1, and OCR registers.

Note that the SO data continues to reflect the information for each output (depending on the previous SOA4, SOA3 state) selected during the most recent STATR write until changed with an updated STATR write.

The output status register correctly reflects the status of the STATR-selected register data at the time that CSB is pulled to a logic [0] during SPI communication, and/or for the period of time since the last valid SPI communication, with the following exception:

- The previous SPI communication was determined to be invalid. In this case, the status is reported as though the invalid SPI communication never occurred.
- The V_{PWR} voltage is below 4.0 V. In this case the status must be ignored by the MCU.

6.4.4 Serial output bit assignment

The 16 bits of serial output data depend on the previous serial input message, as explained in the following paragraphs. Table 23, summarizes SO returned data for bits OD15:OD0.

- Bit OD15 is the MSB; it reflects the state of the Watchdog bit from the previously clocked-in message.
- Bits OD14:OD10 reflect the state of the bits SOA4:SOA0 from the previously clocked in message.
- Bit OD9 is set to logic [1] in Normal mode (NM).
- The contents of bits OD8:OD0 depend on bits D4:D0 from the most recent STATR command SOA4:SOA0 as explained in the paragraphs following Table 23.

Table 23. Serial output bit map description

	Previous STATR					SO returned data														
	SOA 4	**SOA 3**	**SOA 2**	**SOA 1**	**SOA 0**	**OD 15**	**OD 14**	**OD 13**	**OD 12**	**OD 11**	**OD 10**	**OD9**	**OD8**	**OD7**	**OD6**	**OD5**	**OD4**	**OD3**	**OD2**	**OD1**	**OD0**
STATR_s	A_1	A_0	0	0	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	POR	UV	OV	OLON_s	OLOFF_s	OS_s	OT_s	SC_s	OC_s
PWMR_s	A_1	A_0	0	0	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	0	ON_s	PWM6_s	PWM5_s	PWM4_s	PWM3_s	PWM2_s	PWM1_s	PWM0_s
CONFR0_s	A_1	A_0	0	1	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	DIR_dis_s	SR1_s	SR0_s	DELAY2_s	DELAY1_s	DELAY0_s
CONFR1_s	A_1	A_0	0	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	Retry_unlimited_s	Retry_dis_s	OS_dis_s	OLON_dis_s	OLOFF_dis_s	OLLED_en_s	CSNS_ratio_s
OCR_s	A_1	A_0	1	0	0	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	Xenon_s	BC1_s	BC0_s	OC1_s	OC0_s	OCHl_s	OCLO1_s	OCLO0_s	OC_mode_s
GCR	0	0	1	0	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	VDD_FAIL_en	PWM_en	CLOCK_sel	TEMP_en	CSNS_en	CSNS1	CSNS0	X	OV_dis
DIAGR0	0	0	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	X	X	CLOCK_fail	CAL_fail	OTW
DIAGR1	0	1	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	IN3	IN2	IN1	IN0	WD_en
DIAGR2	1	0	1	1	1	WDIN	SOA4	SOA3	SOA2	SOA1	SOA0	NM	X	X	X	X	X	X	0	0	0

Table 23. Serial output bit map description (continued)

	Previous STATR					SO returned data														
	SOA 4	**SOA 3**	**SOA 2**	**SOA 1**	**SOA 0**	**OD 15**	**OD 14**	**OD 13**	**OD 12**	**OD 11**	**OD 10**	**OD9**	**OD8**	**OD7**	**OD6**	**OD5**	**OD4**	**OD3**	**OD2**	**OD1**	**OD0**
Register state after $\overline{RST}$ = 0 or $V_{DD(FAIL)}$ or $V_{SUPPLY(POR)}$ condition	N/A	N/A	N/A	N/A	N/A	0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	0

s = Output selection with the bits A_1A_0 as defined in Table 12

6.4.4.1 Previous address SOA4:SOA0 = $A_1A_0$000 (STATR_s)

The returned data OD8 reports logic [1] in case of previous Power ON Reset condition ($V_{SUPPLY(POR)}$). This bit is only reset by a read operation.

Bits OD7:OD0 reflect the current state of the Fault register (FLTR) corresponding to the output previously selected with the bits SOA4:SOA3 = A_1A_0 (Table 23).

- OC_s: overcurrent fault detection for a selected output,
- SC_s: severe short-circuit fault detection for a selected output,
- OS_s: output shorted to V_{PWR} fault detection for a selected output,
- OLOFF_s: open load in OFF state fault detection for a selected output,
- OLON_s: open load in ON state fault detection (depending on current level threshold: bulb or LED) for a selected output,
- OV: overvoltage fault detection,
- UV: undervoltage fault detection
- POR: power on reset detection.

The FSB pin reports all faults. For latched faults, this pin is reset by a new Switch OFF command (toggling fault_control signal).

6.4.4.2 Previous address SOA4:SOA0 = $A_1A_0$001 (Pwmr_s)

The returned data contains the programmed values in the PWMR register for the output selected with A_1A_0.

6.4.4.3 Previous address SOA4:SOA0 = $A_1A_0$010 (confr0_s)

The returned data contains the programmed values in the CONFR0 register for the output selected with A_1A_0.

6.4.4.4 Previous address SOA4:SOA0 = $A_1A_0$011 (confr1_s)

The returned data contains the programmed values in the CONFR1 register for the output selected with A_1A_0.

6.4.4.5 Previous address SOA4:SOA0 = $A_1A_0$100 (ocr_s)

The returned data contains the programmed values in the OCR register for the output selected with A_1A_0.

6.4.4.6 Previous address SOA4:SOA0 = 00101 (gcr)

The returned data contains the programmed values in the GCR register.

6.4.4.7 Previous address SOA4:SOA0 = 00111 (diagr0)

The returned data OD2 reports logic [1] in case of PWM clock on IN0 pin is out of specified frequency range.

The returned data OD1 reports logic [1] in case of clock calibration failure.

The returned data OD0 reports logic [1] in case of overtemperature prewarning (temperature of GND flag is above T_{OTWAR}).

6.4.4.8 Previous address SOA4:SOA0 = 01111 (diagr1)

The returned data OD[4:1] report in real time the state of the direct input IN[3:0]. The OD0 indicates if the watchdog is enabled (set to logic [1]) or not (set to logic [0]). OD4:OD1 report the output state in case of fail-safe state due to watchdog time-out as explained in the following Table 24.

Table 24. Watchdog activation report

WD_en (OD0)	SPI Watchdog
0	disabled
1	enabled

6.4.4.9 Previous address SOA4:SOA0 = 10111 (diagr2)

The returned data is the product ID. Bits OD2:OD0 are set to 000 for Protected Quad 9.0 mΩ high-side Switches.

Default Device configuration

The default device configuration is explained by the following:

- HS output is commanded by corresponding IN input or On bit through the SPI. The medium slew-rate is used,
- HS output is fully protected by the Xenon overcurrent profile by default, the severe short-circuit protection, the undervoltage, and the overtemperature protection. The auto-retry feature is enabled,
- Open load in ON and OFF state and HS shorted to V_{PWR} detections are available,
- No current recopy and no analog temperature feedback active,
- Overvoltage protection is enabled,
- SO reporting fault status from HS0,
- V_{DD} failure detection is disabled.

7 Typical applications

7.1 Introduction

Figure 16 shows a typical automotive lighting application using an external PWM clock from the main MCU. In this instance, an auxiliary circuit (watchdog) provides IN[3:0] control inputs if the system detects a serious fault such as a watchdog timeout. A 22 nF decoupling capacitor, placed at the module connector, is recommended for each output. 100 nF decoupling capacitors, placed at the device power supply pins are also recommended to pass conducted emission and susceptibility tests.

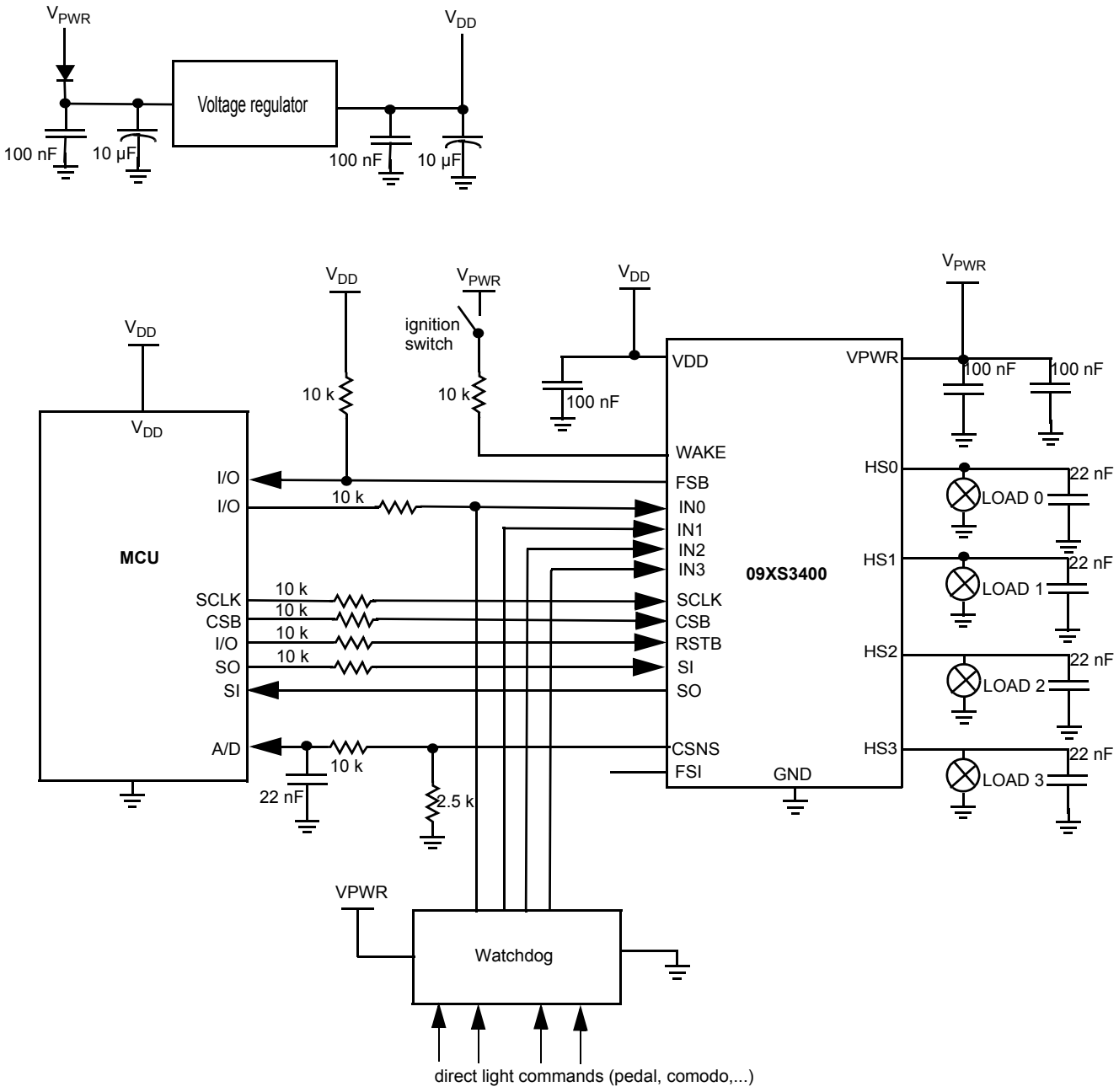


Figure 16. 09XS3400 typical application

8 Packaging

8.1 Soldering information

The 09XS3400 is packaged in a surface mount power package intended to be soldered directly to the printed circuit board. The 09XS3400 was qualified in accordance with JEDEC standards J-STD-020D for moisture sensitivity level (MSL) 3, Pb-free assembly.

The Peak Package Body Temperature (T_P) must not exceed the classification temperature T_C = 260 °C during the soldering process. The time (t_P) within the specified classification temperature T_C - 5.0 °C must not exceed 40 seconds maximum. The application note AN2467 provides guidelines for printed circuit board design and assembly.

8.2 Marking information

The device is identified by the part number: 09XS3400.

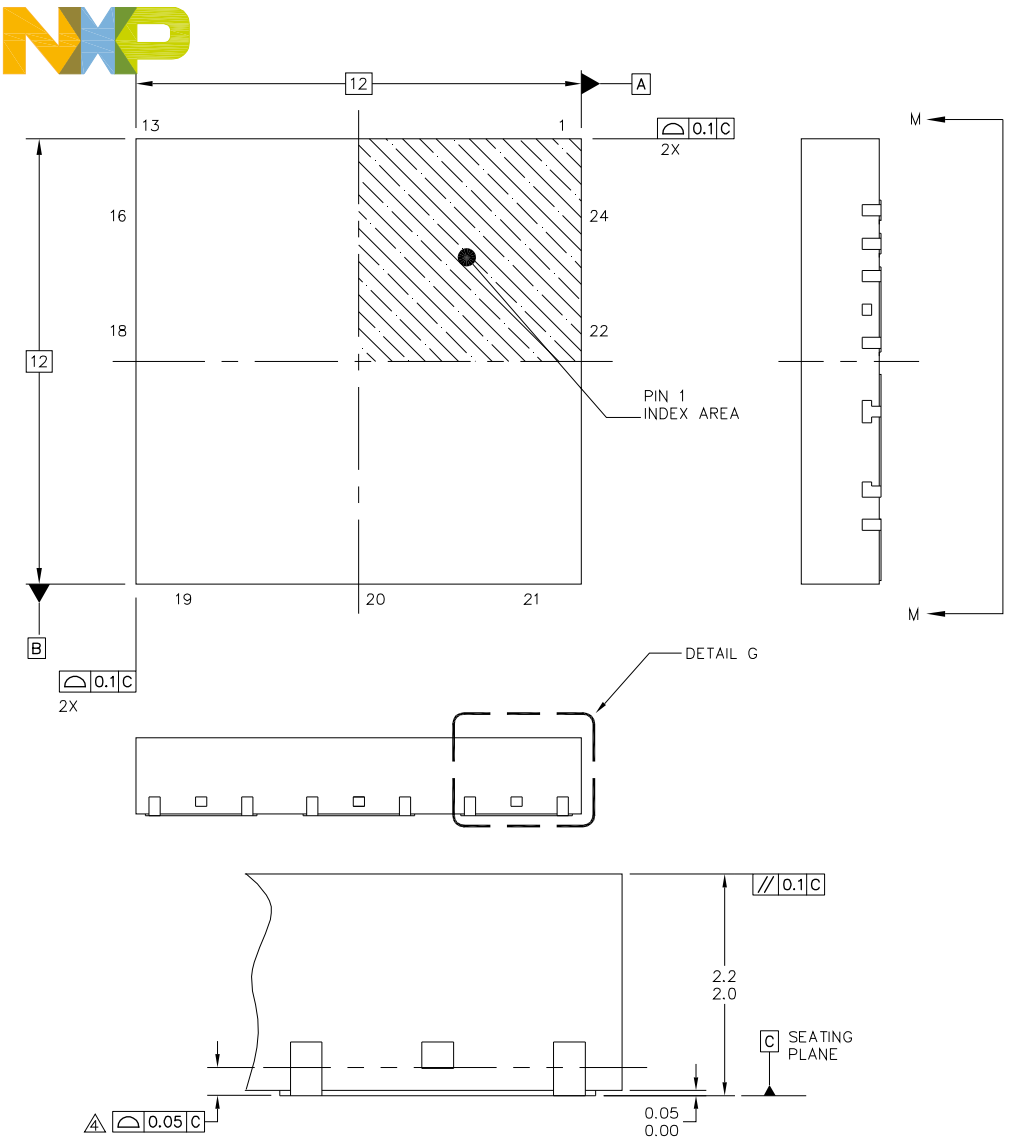
Device markings indicate build information containing the week and year of manufacture. The date is coded with the last four characters of the nine character build information code (e.g. “CTKAH0929”). The date is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the week. For instance, the date code “0929” indicates the 29th week of the year 2009.

8.3 Package dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing’s document number.

Table 25. Package outline

Package	Suffix	Package outline drawing number
24-Pin QFN	FK	98ARL10596D



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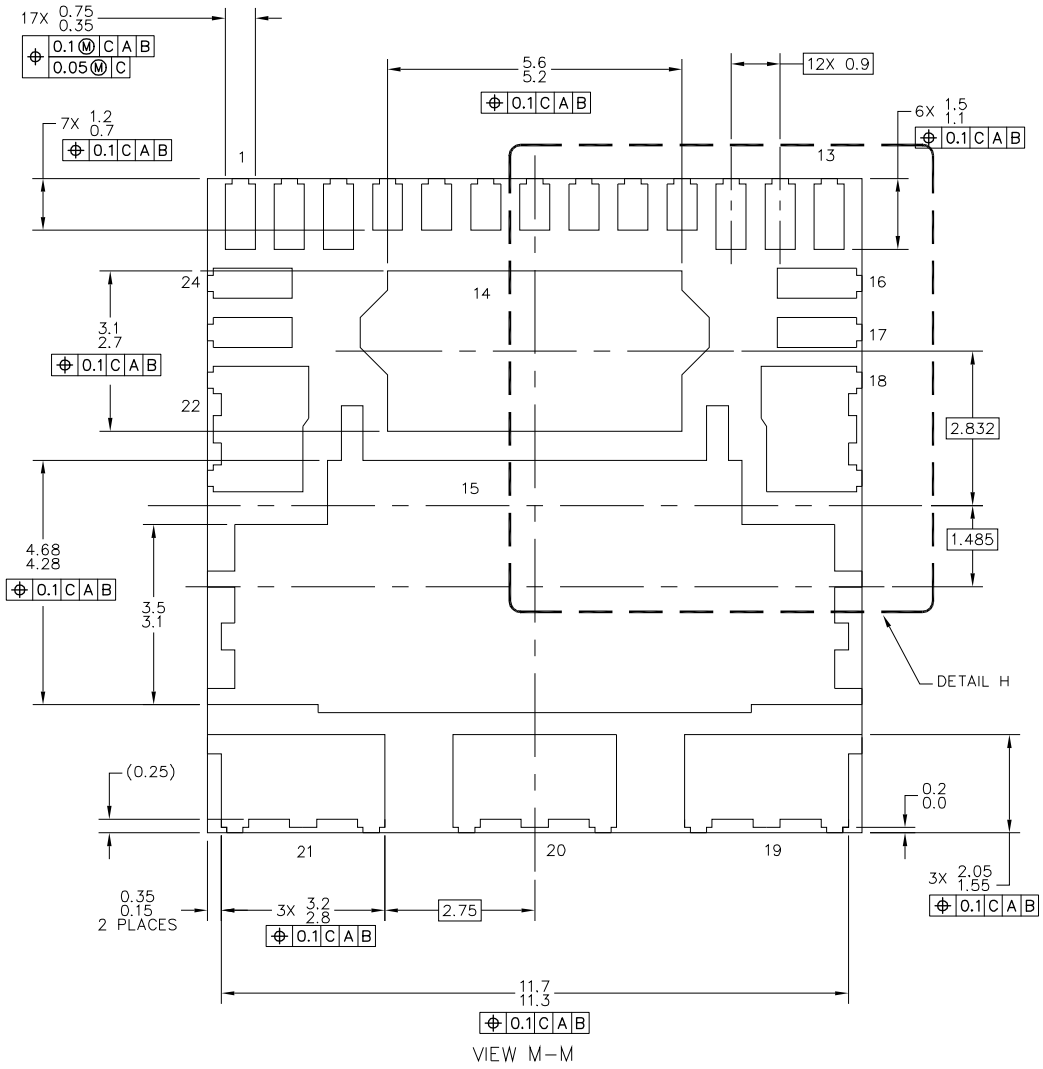
TITLE: POWER QUAD FLAT NON-LEADED (PWR QFN) PACKAGE, 24 TERMINAL, 12X12X2.1, 0.9 PITCH	DOCUMENT NO: 98ARL10596D	REV: F
	STANDARD: NON-JEDEC	
	SOT1631-2	30 DEC 2015



VIEW M–M

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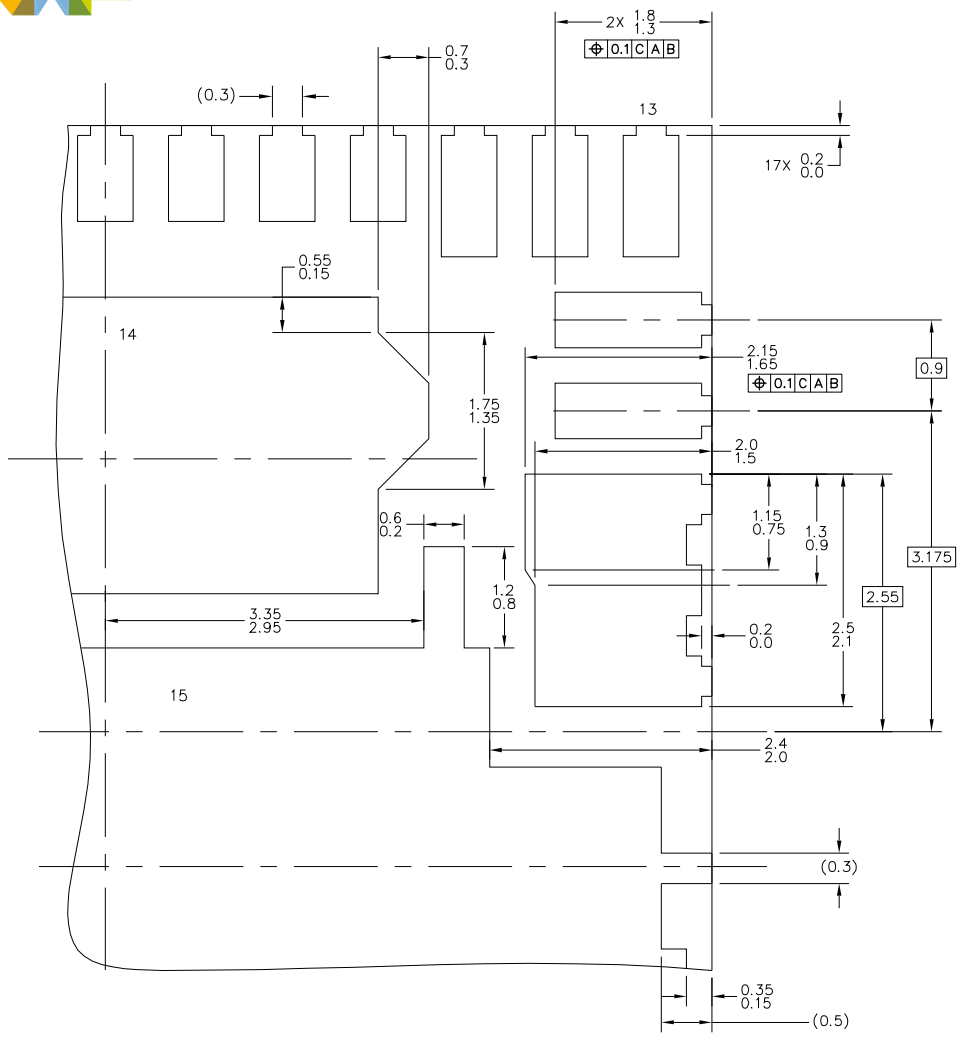
	STANDARD: NON–JEDEC	
	SOT1631–2	30 DEC 2015



DETAIL H

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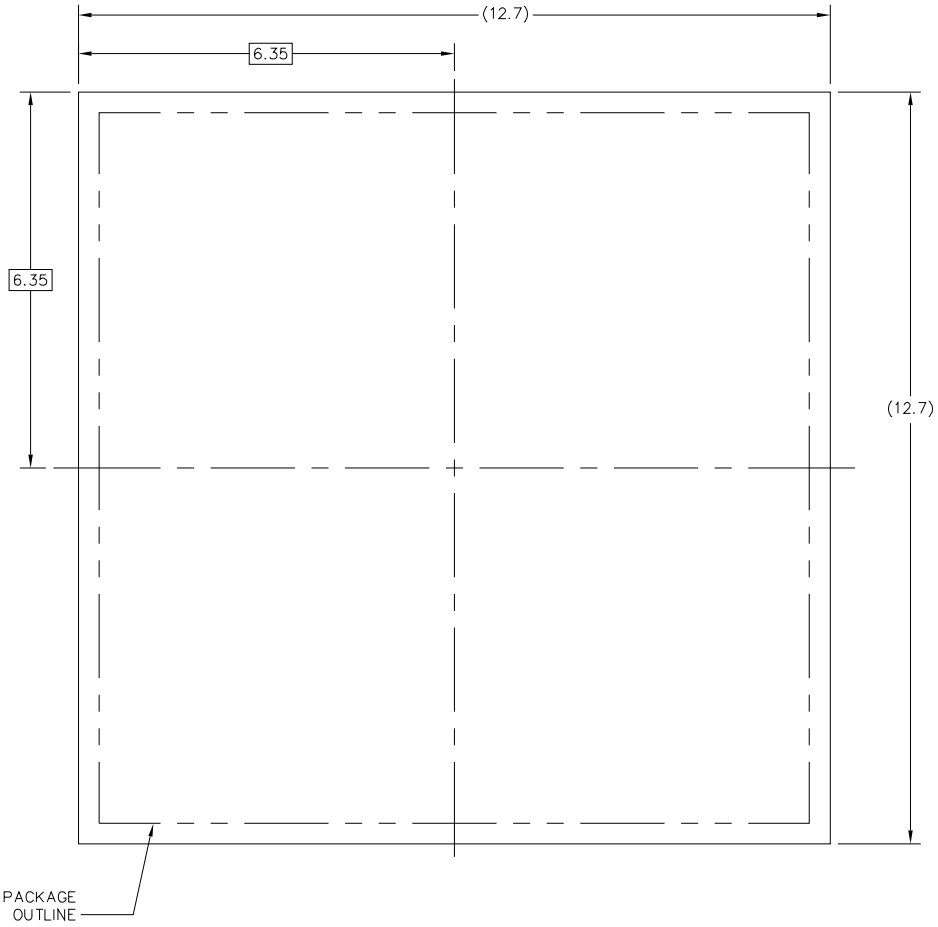
	STANDARD: NON-JEDEC	
	SOT1631-2	30 DEC 2015



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN 1

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	STANDARD: NON–JEDEC	
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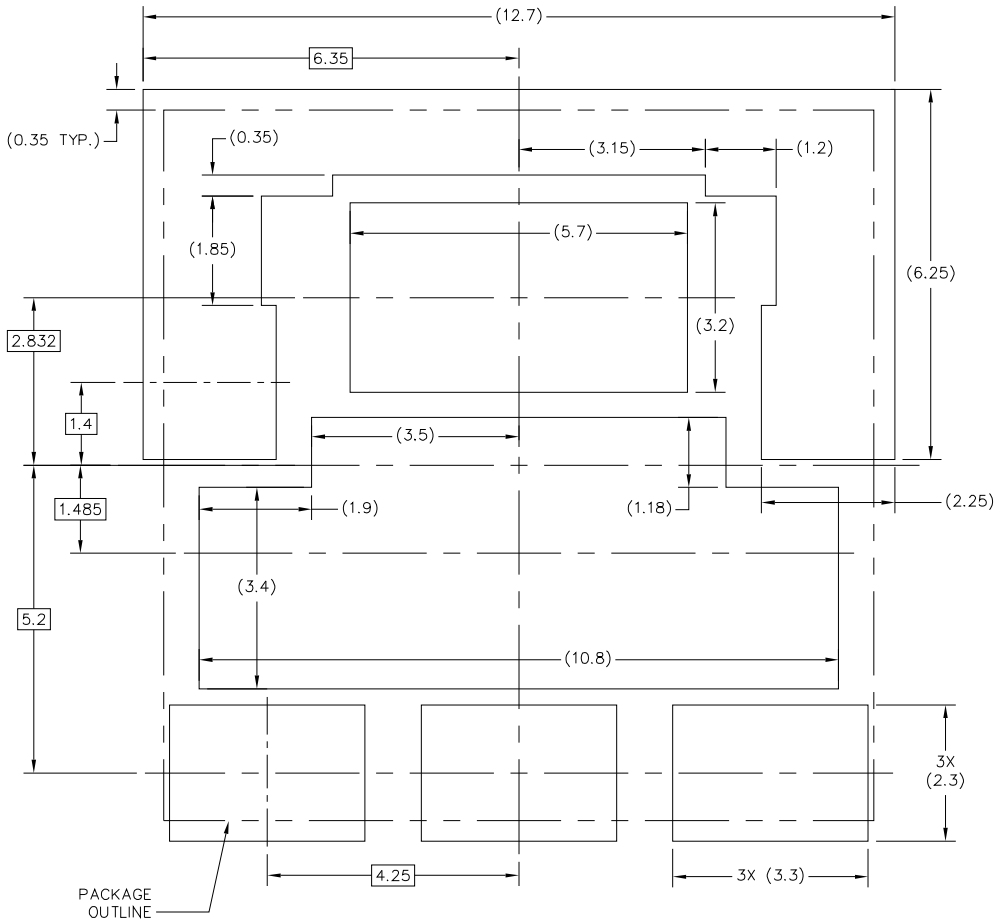

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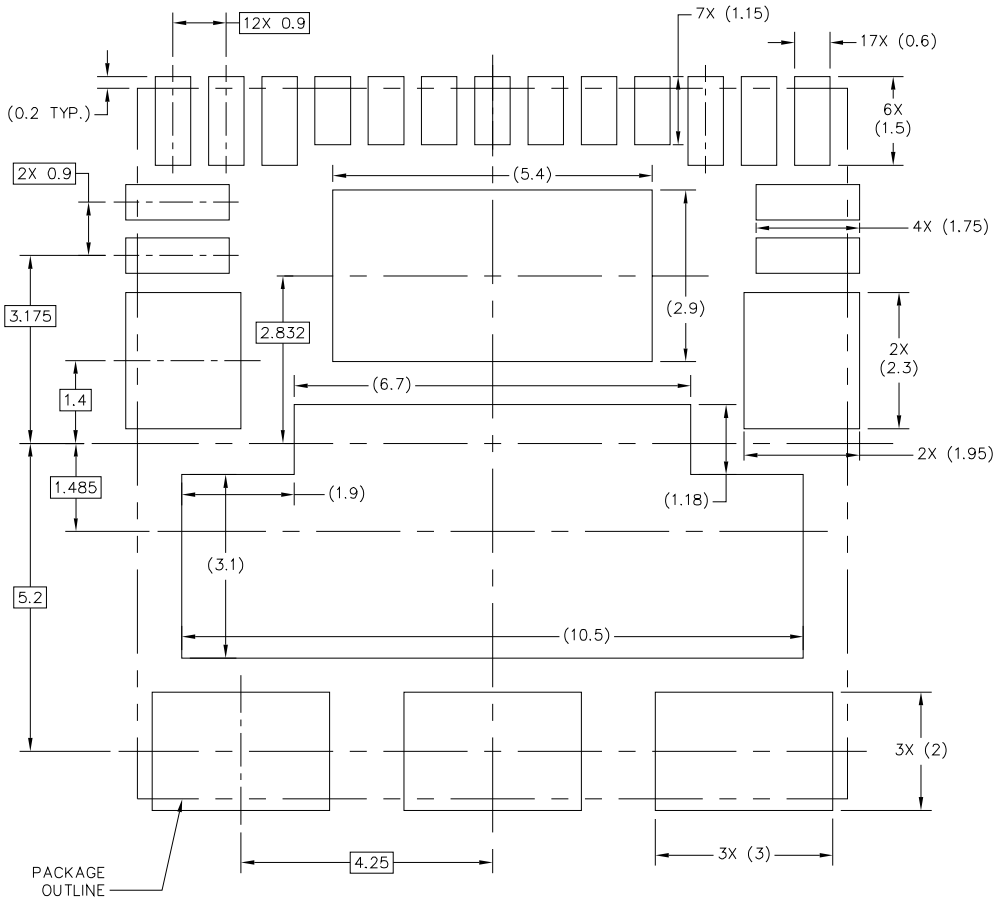

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	STANDARD: NON–JEDEC	
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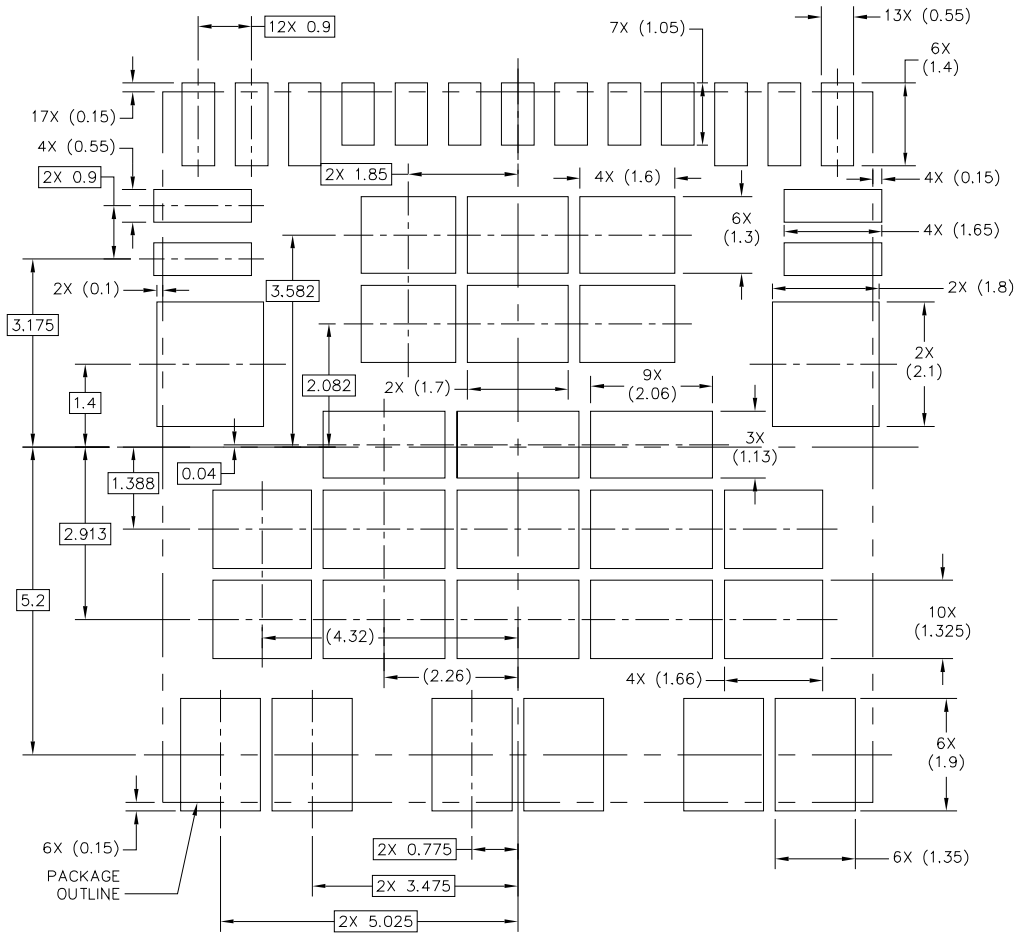

SOLDER PASTE STENCIL GUIDELINES

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	STANDARD: NON-JEDEC
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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFP–N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. MINIMUM METAL GAP IS GUARANTEED TO BE 0.25MM.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

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	STANDARD: NON–JEDEC
	SOT1631–2 30 DEC 2015

9 Revision history

Revision	Date	Description of changes
1.0	2/2012	• Initial release
2.0	4/2014	• No technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to last paragraph on page one.
3.0	8/2014	• Modified t_{DLY} and slew rates per Product Bulletin 16375 • Fixed typo in Table 5 • Updated to current data sheet template style

4.0	1/2016	• Deleted the 28W mode references as per PB 17070
		  • Table 4 - relabeled parameter descriptions, conditions, and symbols
		  • Table 5 - relabeled parameter descriptions, conditions, and symbols
		  • Table 11 - changed the PWMR_s D8 bit
		  • Table 23 - changed the PWMR_s D8 bit
		• Added note (42) for Table 11
		• Updated document form and style

	1/2016	• Corrected PB number
	1/2016	• Detailed a description for the 28W mode change.
	7/2016	• Updated to NXP document form and style.

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7/2016