

MB95560H/570H/580H Series

(Continued)

- External interrupt
 - Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
 - Can be used to wake up the device from different low power consumption (standby) modes
- 8/10-bit A/D converter
 - 8-bit or 10-bit resolution can be selected.
- Low power consumption (standby) modes
 - Stop mode
 - Sleep mode
 - Watch mode
 - Time-base timer mode
- I/O port
 - MB95F562H/F563H/F564H (maximum no. of I/O ports: 16)
 - General-purpose I/O ports (N-ch open drain) : 1
 - General-purpose I/O ports (CMOS I/O) : 15
 - MB95F562K/F563K/F564K (maximum no. of I/O ports: 17)
 - General-purpose I/O ports (N-ch open drain) : 2
 - General-purpose I/O ports (CMOS I/O) : 15
 - MB95F572H/F573H/F574H (maximum no. of I/O ports: 4)
 - General-purpose I/O ports (N-ch open drain) : 1
 - General-purpose I/O ports (CMOS I/O) : 3
 - MB95F572K/F573K/F574K (maximum no. of I/O ports: 5)
 - General-purpose I/O ports (N-ch open drain) : 2
 - General-purpose I/O ports (CMOS I/O) : 3
 - MB95F582H/F583H/F584H (maximum no. of I/O ports: 12)
 - General-purpose I/O ports (N-ch open drain) : 1
 - General-purpose I/O ports (CMOS I/O) : 11
 - MB95F582K/F583K/F584K (maximum no. of I/O ports: 13)
 - General-purpose I/O ports (N-ch open drain) : 2
 - General-purpose I/O ports (CMOS I/O) : 11
- On-chip debug
 - 1-wire serial control
 - Serial writing supported (asynchronous mode)
- Hardware/software watchdog timer
 - Built-in hardware watchdog timer
 - Built-in software watchdog timer
- Power-on reset
 - A power-on reset is generated when the power is switched on.
- Low-voltage detection reset circuit (available only on MB95F562K/F563K/F564K/F572K/F573K/F574K/F582K/F583K/F584K)
 - Built-in low-voltage detector
- Clock supervisor counter
 - Built-in clock supervisor counter function
- Dual operation Flash memory
 - The program/erase operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.
- Flash memory security function
 - Protects the content of the Flash memory

MB95560H/570H/580H Series

■ PRODUCT LINE-UP

• MB95560H Series

Part number	MB95F562H	MB95F563H	MB95F564H	MB95F562K	MB95F563K	MB95F564K
Parameter						
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	<ul style="list-style-type: none">• Number of basic instructions : 136• Instruction bit length : 8 bits• Instruction length : 1 to 3 bytes• Data bit length : 1, 8 and 16 bits• Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)• Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	<ul style="list-style-type: none">• I/O ports (Max) : 16• CMOS I/O : 15• N-ch open drain: 1			<ul style="list-style-type: none">• I/O ports (Max) : 17• CMOS I/O : 15• N-ch open drain: 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	<ul style="list-style-type: none">• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min)• The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
LIN-UART	<ul style="list-style-type: none">• A wide range of communication speed can be selected by a dedicated reload timer.• It has a full duplex double buffer.• Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled.• The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	6 channels 8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels <ul style="list-style-type: none">• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".• It has built-in timer function, PWC function, PWM function and input capture function.• Count clock: it can be selected from internal clocks (seven types) and external clocks.• It can output square wave.					
External interrupt	6 channels <ul style="list-style-type: none">• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)• It can be used to wake up the device from the standby mode.					
On-chip debug	<ul style="list-style-type: none">• 1-wire serial control• It supports serial writing (asynchronous mode).					

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MB95560H/570H/580H Series

(Continued)

<div>Part number</div>	MB95F562H	MB95F563H	MB95F564H	MB95F562K	MB95F563K	MB95F564K
Parameter						
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	<div><div><div>• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.</div><div>• It has a flag indicating the completion of the operation of Embedded Algorithm.</div><div>• Flash security feature for protecting the content of the Flash memory</div></div></div>					
	Number of program/erase cycles		1000	10000	100000	
	Data retention time		20 years	10 years	5 years	
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	LCC-32P-M19 FPT-20P-M09 FPT-20P-M10					

MB95560H/570H/580H Series

• MB95570H Series

Part number	MB95F572H	MB95F573H	MB95F574H	MB95F572K	MB95F573K	MB95F574K								
Parameter														
Type	Flash memory product													
Clock supervisor counter	It supervises the main clock oscillation.													
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte								
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes								
Power-on reset	Yes													
Low-voltage detection reset	No			Yes										
Reset input	Dedicated			Selected through software										
CPU functions	<ul style="list-style-type: none">• Number of basic instructions : 136• Instruction bit length : 8 bits• Instruction length : 1 to 3 bytes• Data bit length : 1, 8 and 16 bits• Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)• Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz)													
General-purpose I/O	<ul style="list-style-type: none">• I/O ports (Max) : 4• CMOS I/O : 3• N-ch open drain: 1			<ul style="list-style-type: none">• I/O ports (Max) : 5• CMOS I/O : 3• N-ch open drain: 2										
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)													
Hardware/software watchdog timer	<ul style="list-style-type: none">• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min)• The sub-CR clock can be used as the source clock of the hardware watchdog timer.													
Wild register	It can be used to replace 3 bytes of data.													
LIN-UART	No LIN-UART													
8/10-bit A/D converter	2 channels 8-bit or 10-bit resolution can be selected.													
8/16-bit composite timer	1 channel <ul style="list-style-type: none">• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".• It has built-in timer function, PWC function, PWM function and input capture function.• Count clock: it can be selected from internal clocks (seven types) and external clocks.• It can output square wave.													
External interrupt	2 channels <ul style="list-style-type: none">• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)• It can be used to wake up the device from standby modes.													
On-chip debug	<ul style="list-style-type: none">• 1-wire serial control• It supports serial writing (asynchronous mode).													
Watch prescaler	Eight different time intervals can be selected.													
Flash memory	<ul style="list-style-type: none">• It supports automatic programming (Embedded Algorithm) and program/erase/erase-suspend/erase-resume commands.• It has a flag indicating the completion of the operation of Embedded Algorithm.• Flash security feature for protecting the content of the Flash memory <table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table>						Number of program/erase cycles	1000	10000	100000	Data retention time	20 years	10 years	5 years
Number of program/erase cycles	1000	10000	100000											
Data retention time	20 years	10 years	5 years											
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode													
Package	FPT-8P-M08													

MB95560H/570H/580H Series

• MB95580H Series

Part number	MB95F582H	MB95F583H	MB95F584H	MB95F582K	MB95F583K	MB95F584K
Parameter						
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	<ul style="list-style-type: none">• Number of basic instructions : 136• Instruction bit length : 8 bits• Instruction length : 1 to 3 bytes• Data bit length : 1, 8 and 16 bits• Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz)• Interrupt processing time : 0.6 μs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	<ul style="list-style-type: none">• I/O ports (Max) : 12• CMOS I/O : 11• N-ch open drain: 1			<ul style="list-style-type: none">• I/O ports (Max) : 13• CMOS I/O : 11• N-ch open drain: 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/software watchdog timer	<ul style="list-style-type: none">• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min)• The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
LIN-UART	<ul style="list-style-type: none">• A wide range of communication speed can be selected by a dedicated reload timer.• It has a full duplex double buffer.• Clock-synchronized serial data transfer and clock-asynchronous serial data transfer is enabled.• The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	5 channels 8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	1 channel <ul style="list-style-type: none">• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".• It has built-in timer function, PWC function, PWM function and input capture function.• Count clock: it can be selected from internal clocks (seven types) and external clocks.• It can output square wave.					
External interrupt	6 channels <ul style="list-style-type: none">• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)• It can be used to wake up the device from standby modes.					
On-chip debug	<ul style="list-style-type: none">• 1-wire serial control• It supports serial writing (asynchronous mode).					

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MB95560H/570H/580H Series

(Continued)

Part number	MB95F582H	MB95F583H	MB95F584H	MB95F582K	MB95F583K	MB95F584K
Parameter						
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	<ul style="list-style-type: none">• It supports automatic programming (Embedded Algorithm) and program/erase/erase-suspend/erase-resume commands.• It has a flag indicating the completion of the operation of Embedded Algorithm.• Flash security feature for protecting the content of the Flash memory					
	Number of program/erase cycles		1000	10000	100000	
	Data retention time		20 years	10 years	5 years	
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	LCC-32P-M19 FPT-16P-M08 FPT-16P-M23					

MB95560H/570H/580H Series

■ PACKAGES AND CORRESPONDING PRODUCTS

• MB95560H Series

Part number Package	MB95F562H	MB95F562K	MB95F563H	MB95F563K	MB95F564H	MB95F564K
LCC-32P-M19	O	O	O	O	O	O
FPT-20P-M09	O	O	O	O	O	O
FPT-20P-M10	O	O	O	O	O	O
FPT-16P-M08	X	X	X	X	X	X
FPT-16P-M23	X	X	X	X	X	X
FPT-8P-M08	X	X	X	X	X	X

• MB95570H Series

Part number Package	MB95F572H	MB95F572K	MB95F573H	MB95F573K	MB95F574H	MB95F574K
LCC-32P-M19	X	X	X	X	X	X
FPT-20P-M09	X	X	X	X	X	X
FPT-20P-M10	X	X	X	X	X	X
FPT-16P-M08	X	X	X	X	X	X
FPT-16P-M23	X	X	X	X	X	X
FPT-8P-M08	O	O	O	O	O	O

• MB95580H Series

Part number Package	MB95F582H	MB95F582K	MB95F583H	MB95F583K	MB95F584H	MB95F584K
LCC-32P-M19	O	O	O	O	O	O
FPT-20P-M09	X	X	X	X	X	X
FPT-20P-M10	X	X	X	X	X	X
FPT-16P-M08	O	O	O	O	O	O
FPT-16P-M23	O	O	O	O	O	O
FPT-8P-M08	X	X	X	X	X	X

O: Available

X: Unavailable

■ DIFFERENCES AMONG PRODUCTS AND NOTES ON PRODUCT SELECTION

- Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “■ ELECTRICAL CHARACTERISTICS”.

- Package

For details of information on each package, see “■ PACKAGES AND CORRESPONDING PRODUCTS” and “■ PACKAGE DIMENSION”.

- Operating voltage

The operating voltage varies, depending on whether the on-chip debug function is used or not.

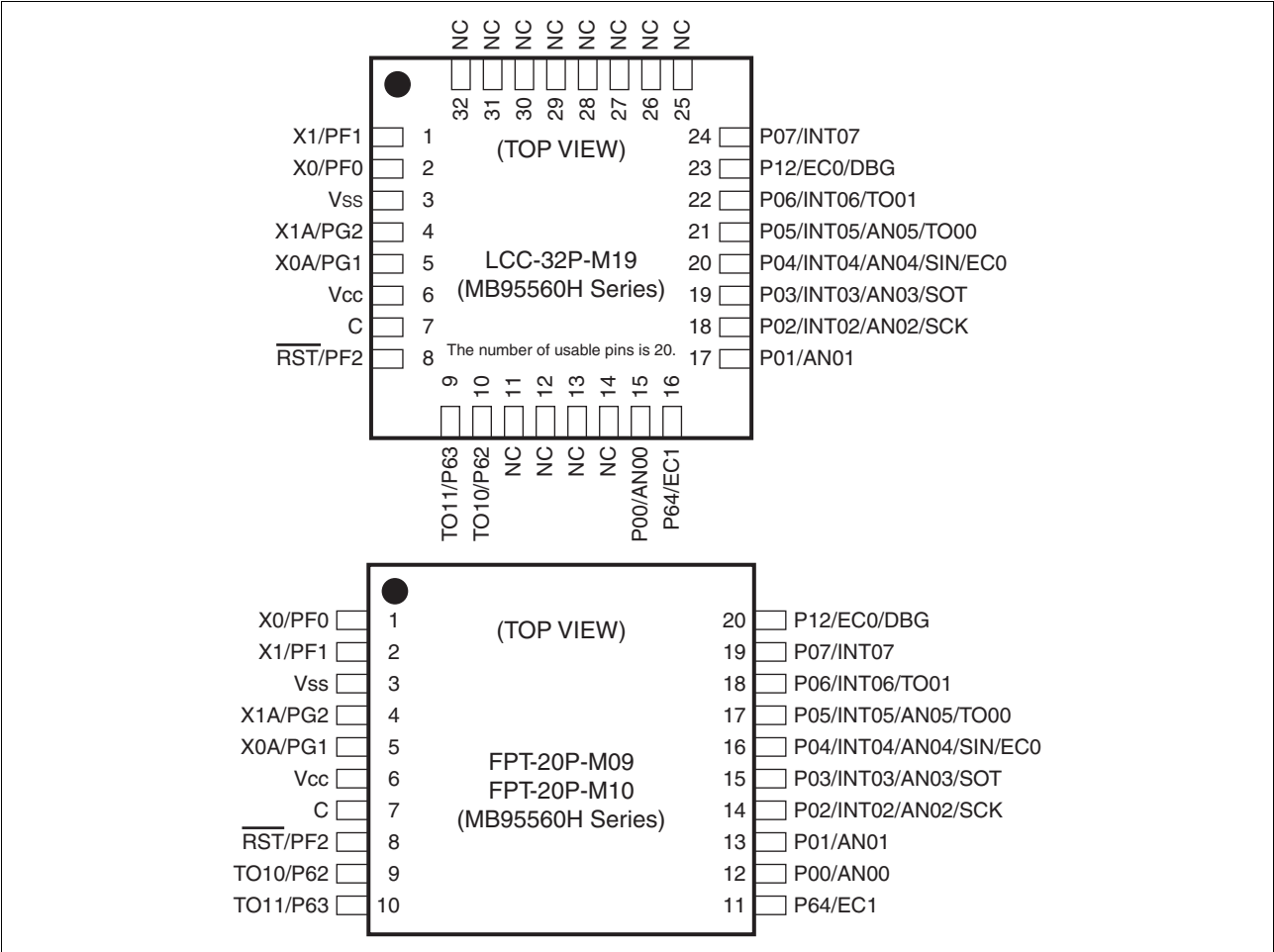
For details of the operating voltage, see “■ ELECTRICAL CHARACTERISTICS”.

- On-chip debug function

The on-chip debug function requires that V_{CC} , V_{SS} and 1 serial-wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 21 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in the hardware manual of the MB95560H/570H/580H Series.

MB95560H/570H/580H Series

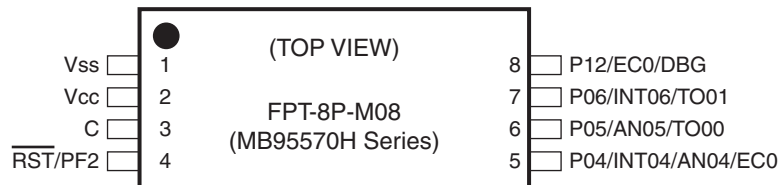
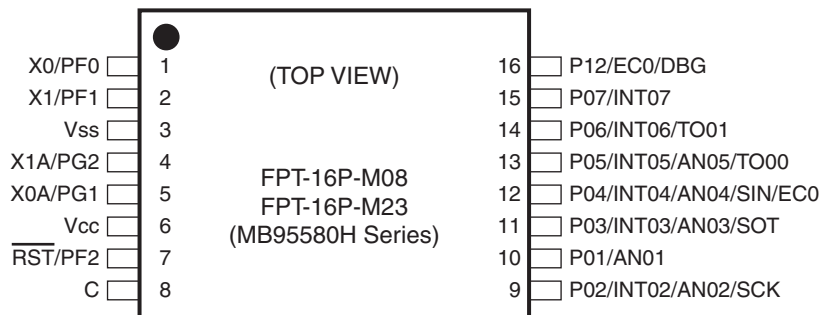
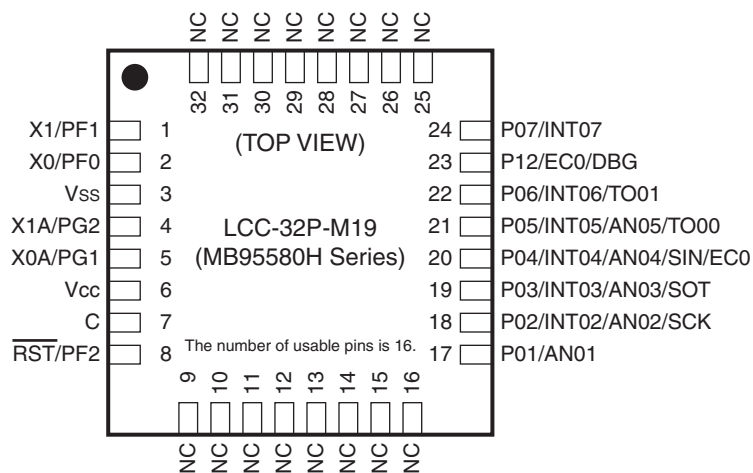
■ PIN ASSIGNMENT



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MB95560H/570H/580H Series

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MB95560H/570H/580H Series

■ PIN FUNCTIONS (MB95560H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	V _{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V _{CC}	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{\text{RST}}$		Reset pin Dedicated reset pin on MB95F562H/F563H/F564H
9	P63	E	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
10	P62	E	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
11	NC	—	It is an internally connected pin. Always leave it unconnected.
12			
13			
14			
15	P00	D	General-purpose I/O port High-current pin
	AN00		A/D converter analog input pin
16	P64	E	General-purpose I/O port High-current pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
17	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
18	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin

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MB95560H/570H/580H Series

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Pin no.	Pin name	I/O circuit type*	Function
19	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
20	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
21	P05	D	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
24	P07	E	General-purpose I/O port High-current pin
	INT07		External interrupt input pin
25	NC	—	It is an internally connected pin. Always leave it unconnected.
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28			
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31			
32			

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

MB95560H/570H/580H Series

■ PIN FUNCTIONS (MB95560H Series, 20 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V _{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V _{CC}	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{\text{RST}}$		Reset pin Dedicated reset pin on MB95F562H/F563H/F564H
9	P62	E	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
10	P63	E	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
11	P64	E	General-purpose I/O port High-current pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
12	P00	D	General-purpose I/O port High-current pin
	AN00		A/D converter analog input pin
13	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
14	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
15	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

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MB95560H/570H/580H Series

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Pin no.	Pin name	I/O circuit type*	Function
16	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
17	P05	D	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
18	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
19	P07	E	General-purpose I/O port High-current pin
	INT07		External interrupt input pin
20	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

MB95560H/570H/580H Series

■ PIN FUNCTIONS (MB95570H Series, 8 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	V _{SS}	—	Power supply pin (GND)
2	V _{CC}	—	Power supply pin
3	C	—	Capacitor connection pin
4	PF2	A	General-purpose I/O port
	$\overline{\text{RST}}$		Reset pin Dedicated reset pin on MB95F572H/F573H/F574H
5	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
6	P05	D	General-purpose I/O port High-current pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
7	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
8	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

MB95560H/570H/580H Series

■ PIN FUNCTIONS (MB95580H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	V _{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V _{CC}	—	Power supply pin
7	C	—	Capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{\text{RST}}$		Reset pin Dedicated reset pin on MB95F582H/F583H/F584H
9	NC	—	It is an internally connected pin. Always leave it unconnected.
10			
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16			
17	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
18	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

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MB95560H/570H/580H Series

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
20	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
21	P05	D	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
24	P07	E	General-purpose I/O port High-current pin
	INT07		External interrupt input pin
25	NC	—	It is an internally connected pin. Always leave it unconnected.
26			
27			
28			
29			
30			
31			
32			

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

MB95560H/570H/580H Series

■ PIN FUNCTIONS (MB95580H Series, 16 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V _{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V _{CC}	—	Power supply pin
7	PF2	A	General-purpose I/O port
	$\overline{\text{RST}}$		Reset pin Dedicated reset pin on MB95F582H/F583H/F584H
8	C	—	Capacitor connection pin
9	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
10	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
11	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
12	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

(Continued)

MB95560H/570H/580H Series

(Continued)

Pin no.	Pin name	I/O circuit type*	Function
13	P05	D	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
14	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
15	P07	E	General-purpose I/O port High-current pin
	INT07		External interrupt input pin
16	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “■ I/O CIRCUIT TYPE”.

MB95560H/570H/580H Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> • N-ch open drain output • Hysteresis input • Reset output
B		<ul style="list-style-type: none"> • Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		<ul style="list-style-type: none"> • Oscillation circuit • Low-speed side Feedback resistance: approx. 10 MΩ • CMOS output • Hysteresis input • Pull-up control available

(Continued)

MB95560H/570H/580H Series

(Continued)

Type	Circuit	Remarks
D	<p>Pull-up control</p> <p>Digital output</p> <p>Digital output</p> <p>Analog input</p> <p>A/D control</p> <p>Standby control</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up control available • Analog input
E	<p>Pull-up control</p> <p>Digital output</p> <p>Digital output</p> <p>Standby control</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> • CMOS output • Hysteresis input • Pull-up control available
F	<p>Standby control</p> <p>Hysteresis input</p> <p>Digital output</p> <p>N-ch</p>	<ul style="list-style-type: none"> • N-ch open drain output • Hysteresis input

■ NOTES ON DEVICE HANDLING

- Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "1. Absolute Maximum Ratings" of "■ ELECTRICAL CHARACTERISTICS" is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

- Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

- Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

■ PIN CONNECTION

- Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 k Ω . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

- Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1 μ F as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

- DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

The DBG pin should not stay at "L" level after power-on until the reset output is released.

- \overline{RST} pin

Connect the \overline{RST} pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the \overline{RST} pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.

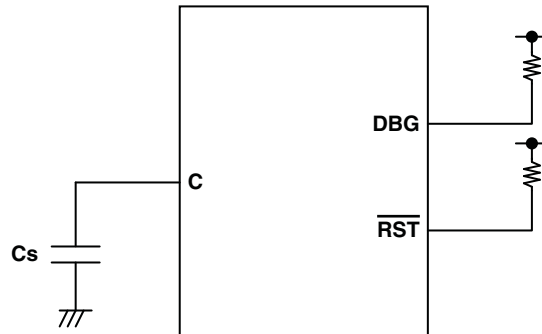
The PF2/ \overline{RST} pin functions as the reset input/output pin after power-on. In addition, the reset output of the PF2/ \overline{RST} pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

MB95560H/570H/580H Series

- C pin

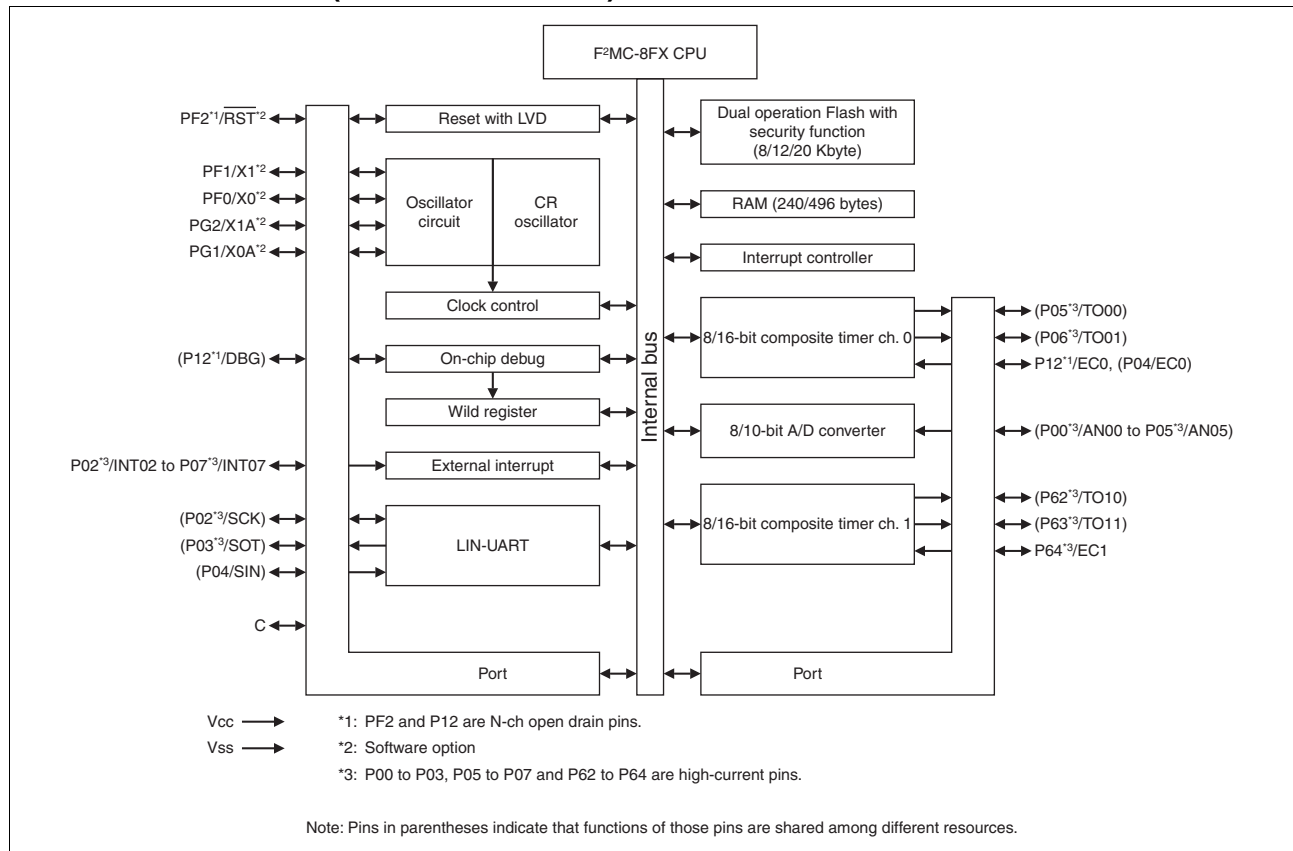
Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_s . For the connection to a smoothing capacitor C_s , see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and C_s and the distance between C_s and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG/ \overline{RST} /C pins connection diagram



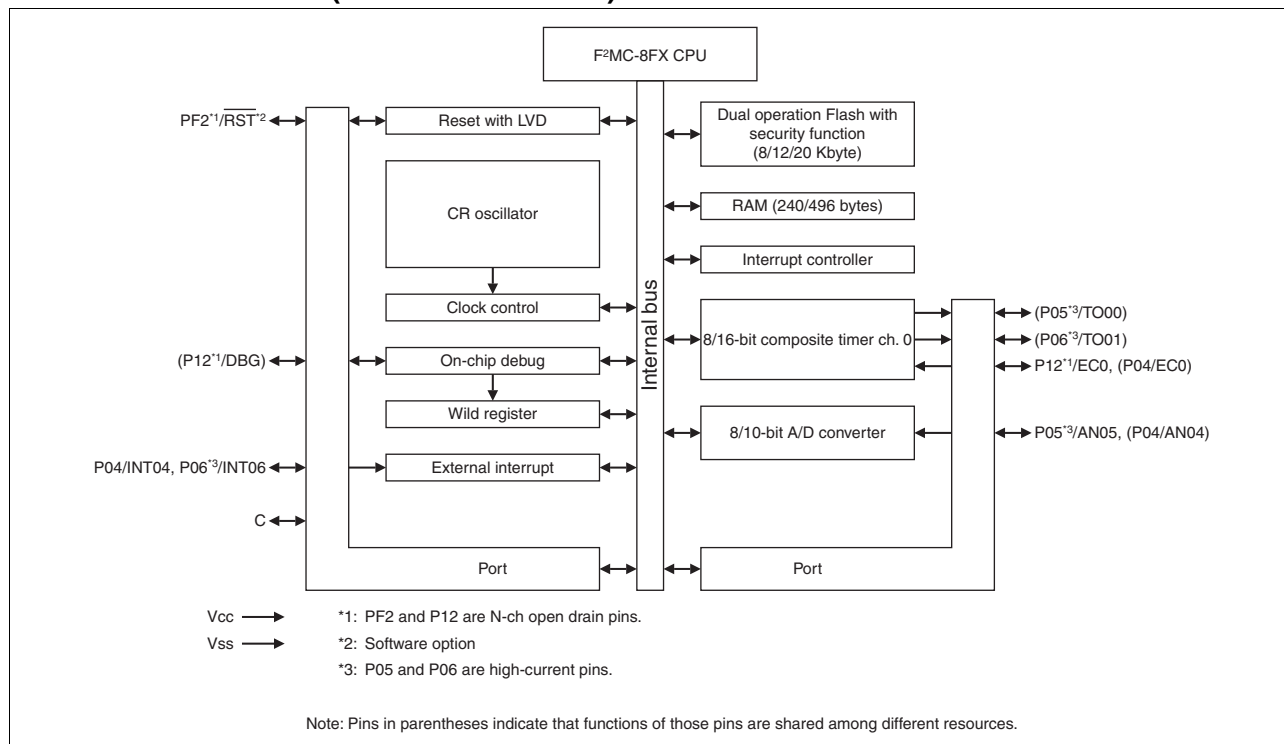
MB95560H/570H/580H Series

■ BLOCK DIAGRAM (MB95560H Series)



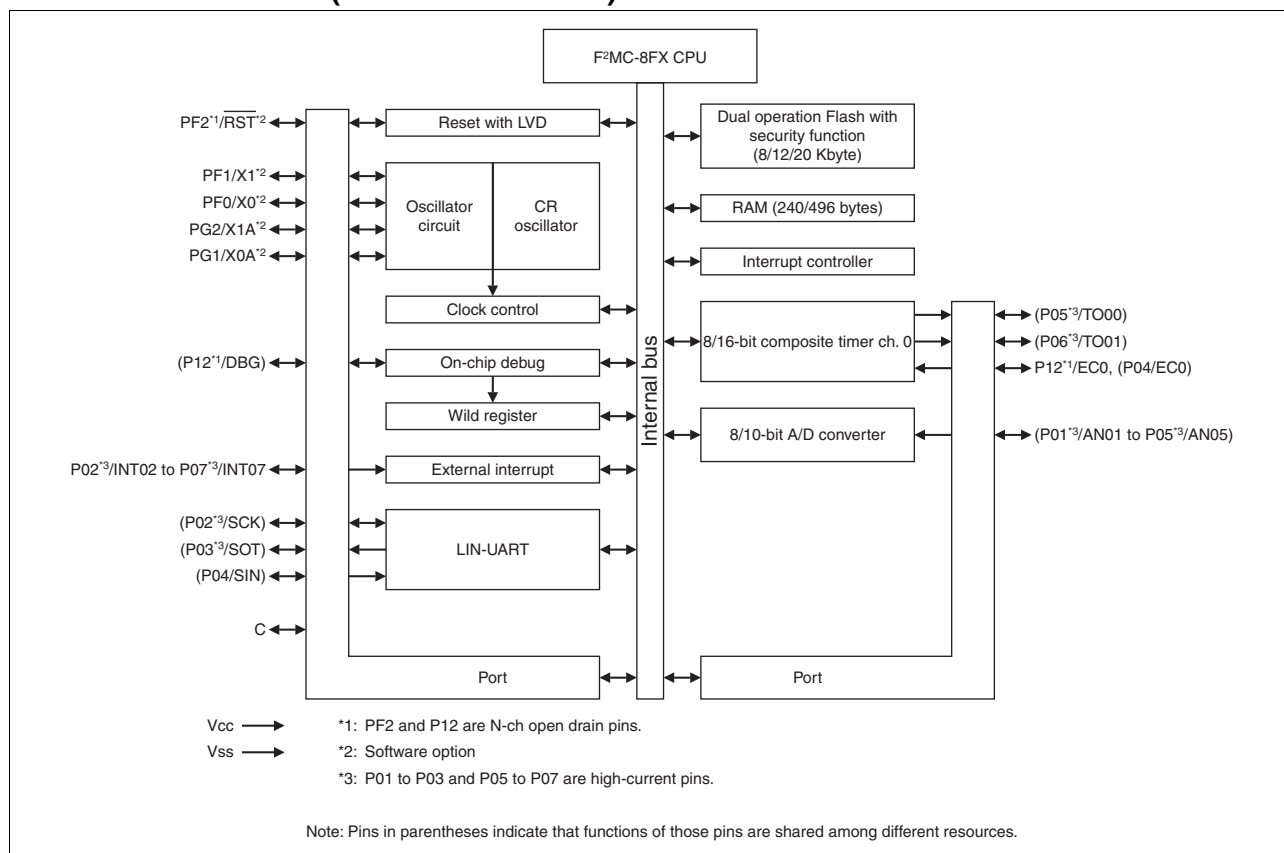
MB95560H/570H/580H Series

■ BLOCK DIAGRAM (MB95570H Series)



MB95560H/570H/580H Series

■ BLOCK DIAGRAM (MB95580H Series)



MB95560H/570H/580H Series

■ CPU CORE

• Memory Space

The memory space of the MB95560H/570H/580H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95560H/570H/580H Series are shown below.

• Memory Maps

MB95F562H/F562K/F572H/ F572K/F582H/F582K	MB95F563H/F563K/F573H/ F573K/F583H/F583K	MB95F564H/F564K/F574H/ F574K/F584H/F584K
0000 _H 0080 _H 0090 _H 0100 _H 0180 _H 0F80 _H 1000 _H B000 _H C000 _H F000 _H FFFF _H	0000 _H 0080 _H 0090 _H 0100 _H 0200 _H 0280 _H 0F80 _H 1000 _H B000 _H C000 _H E000 _H FFFF _H	0000 _H 0080 _H 0090 _H 0100 _H 0200 _H 0280 _H 0F80 _H 1000 _H B000 _H FFFF _H
I/O area Access prohibited RAM 240 bytes Register Access prohibited Extension I/O area Access prohibited Flash 4 Kbyte Access prohibited Flash 4 Kbyte	I/O area Access prohibited RAM 496 bytes Register Access prohibited Extension I/O area Access prohibited Flash 4 Kbyte Access prohibited Flash 8 Kbyte	I/O area Access prohibited RAM 496 bytes Register Access prohibited Extension I/O area Access prohibited Flash 20 Kbyte

MB95560H/570H/580H Series

■ I/O MAP (MB95560H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000 _H	PDR0	Port 0 data register	R/W	00000000 _B
0001 _H	DDR0	Port 0 direction register	R/W	00000000 _B
0002 _H	PDR1	Port 1 data register	R/W	00000000 _B
0003 _H	DDR1	Port 1 direction register	R/W	00000000 _B
0004 _H	—	(Disabled)	—	—
0005 _H	WATR	Oscillation stabilization wait time setting register	R/W	11111111 _B
0006 _H	PLLC	PLL control register	R/W	00000000 _B
0007 _H	SYCC	System clock control register	R/W	XXX11011 _B
0008 _H	STBC	Standby control register	R/W	00000000 _B
0009 _H	RSRR	Reset source register	R/W	000XXXXX _B
000A _H	TBTC	Time-base timer control register	R/W	00000000 _B
000B _H	WPCR	Watch prescaler control register	R/W	00000000 _B
000C _H	WDTC	Watchdog timer control register	R/W	00XX0000 _B
000D _H	SYCC2	System clock control register 2	R/W	XXXX0011 _B
000E _H	STBC2	Standby control register 2	R/W	00000000 _B
000F _H to 0015 _H	—	(Disabled)	—	—
0016 _H	PDR6	Port 6 data register	R/W	00000000 _B
0017 _H	DDR6	Port 6 direction register	R/W	00000000 _B
0018 _H to 0027 _H	—	(Disabled)	—	—
0028 _H	PDRF	Port F data register	R/W	00000000 _B
0029 _H	DDRF	Port F direction register	R/W	00000000 _B
002A _H	PDRG	Port G data register	R/W	00000000 _B
002B _H	DDRG	Port G direction register	R/W	00000000 _B
002C _H	PUL0	Port 0 pull-up register	R/W	00000000 _B
002D _H to 0032 _H	—	(Disabled)	—	—
0033 _H	PUL6	Port 6 pull-up register	R/W	00000000 _B
0034 _H	—	(Disabled)	—	—
0035 _H	PULG	Port G pull-up register	R/W	00000000 _B
0036 _H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000 _B
0037 _H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000 _B
0038 _H	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	00000000 _B
0039 _H	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000 _B
003A _H to 0048 _H	—	(Disabled)	—	—

(Continued)

MB95560H/570H/580H Series

Address	Register abbreviation	Register name	R/W	Initial value
0049 _H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000 _B
004A _H	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000 _B
004B _H	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000 _B
004C _H , 004D _H	—	(Disabled)	—	—
004E _H	LVDR	LVDR reset voltage selection ID register	R/W	00000000 _B
004F _H	—	(Disabled)	—	—
0050 _H	SCR	LIN-UART serial control register	R/W	00000000 _B
0051 _H	SMR	LIN-UART serial mode register	R/W	00000000 _B
0052 _H	SSR	LIN-UART serial status register	R/W	00001000 _B
0053 _H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000 _B
0054 _H	ESCR	LIN-UART extended status control register	R/W	00000100 _B
0055 _H	ECCR	LIN-UART extended communication control register	R/W	000000XX _B
0056 _H to 006B _H	—	(Disabled)	—	—
006C _H	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 _B
006D _H	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 _B
006E _H	ADDH	8/10-bit A/D converter data register upper	R/W	00000000 _B
006F _H	ADDL	8/10-bit A/D converter data register lower	R/W	00000000 _B
0070 _H	—	(Disabled)	—	—
0071 _H	FSR2	Flash memory status register 2	R/W	00000000 _B
0072 _H	FSR	Flash memory status register	R/W	000X0000 _B
0073 _H	SWRE0	Flash memory sector write control register 0	R/W	00000000 _B
0074 _H	FSR3	Flash memory status register 3	R	000XXXXX _B
0075 _H	FSR4	Flash memory status register 4	R/W	00000000 _B
0076 _H	WREN	Wild register address compare enable register	R/W	00000000 _B
0077 _H	WROR	Wild register data test setting register	R/W	00000000 _B
0078 _H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079 _H	ILR0	Interrupt level setting register 0	R/W	11111111 _B
007A _H	ILR1	Interrupt level setting register 1	R/W	11111111 _B
007B _H	ILR2	Interrupt level setting register 2	R/W	11111111 _B
007C _H	ILR3	Interrupt level setting register 3	R/W	11111111 _B
007D _H	ILR4	Interrupt level setting register 4	R/W	11111111 _B
007E _H	ILR5	Interrupt level setting register 5	R/W	11111111 _B
007F _H	—	(Disabled)	—	—
0F80 _H	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000 _B
0F81 _H	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000 _B
0F82 _H	WRDR0	Wild register data setting register ch. 0	R/W	00000000 _B

(Continued)

MB95560H/570H/580H Series

Address	Register abbreviation	Register name	R/W	Initial value
0F83 _H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000 _B
0F84 _H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000 _B
0F85 _H	WRDR1	Wild register data setting register ch. 1	R/W	00000000 _B
0F86 _H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000 _B
0F87 _H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000 _B
0F88 _H	WRDR2	Wild register data setting register ch. 2	R/W	00000000 _B
0F89 _H to 0F91 _H	—	(Disabled)	—	—
0F92 _H	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000 _B
0F93 _H	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000 _B
0F94 _H	T01DR	8/16-bit composite timer 01 data register	R/W	00000000 _B
0F95 _H	T00DR	8/16-bit composite timer 00 data register	R/W	00000000 _B
0F96 _H	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000 _B
0F97 _H	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	00000000 _B
0F98 _H	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	00000000 _B
0F99 _H	T11DR	8/16-bit composite timer 11 data register	R/W	00000000 _B
0F9A _H	T10DR	8/16-bit composite timer 10 data register	R/W	00000000 _B
0F9B _H	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	00000000 _B
0F9C _H to 0FBB _H	—	(Disabled)	—	—
0FBC _H	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 _B
0FBD _H	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 _B
0FBE _H to 0FC2 _H	—	(Disabled)	—	—
0FC3 _H	AIDRL	A/D input disable register (Lower)	R/W	00000000 _B
0FC4 _H to 0FE3 _H	—	(Disabled)	—	—
0FE4 _H	CRTH	Main CR clock trimming register (upper)	R/W	000XXXXX _B
0FE5 _H	CRTL	Main CR clock trimming register (lower)	R/W	000XXXXX _B
0FE6 _H	—	(Disabled)	—	—
0FE7 _H	CRTDA	Main CR clock temperature dependent adjustment register	R/W	00011111 _B
0FE8 _H	SYSC	System configuration register	R/W	11000011 _B
0FE9 _H	CMCR	Clock monitoring control register	R/W	00000000 _B
0FEA _H	CMDR	Clock monitoring data register	R/W	00000000 _B

(Continued)

MB95560H/570H/580H Series

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FEB _H	WDTH	Watchdog timer selection ID register (upper)	R/W	XXXXXXXX _B
0FEC _H	WDTL	Watchdog timer selection ID register (lower)	R/W	XXXXXXXX _B
0FED _H to 0FFF _H	—	(Disabled)	—	—

- R/W access symbols

R/W : Readable / Writable

R : Read only

- Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

MB95560H/570H/580H Series

■ I/O MAP (MB95570H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000 _H	PDR0	Port 0 data register	R/W	00000000 _B
0001 _H	DDR0	Port 0 direction register	R/W	00000000 _B
0002 _H	PDR1	Port 1 data register	R/W	00000000 _B
0003 _H	DDR1	Port 1 direction register	R/W	00000000 _B
0004 _H	—	(Disabled)	—	—
0005 _H	WATR	Oscillation stabilization wait time setting register	R/W	11111111 _B
0006 _H	PLLC	PLL control register	R/W	00000000 _B
0007 _H	SYCC	System clock control register	R/W	XXX11011 _B
0008 _H	STBC	Standby control register	R/W	00000000 _B
0009 _H	RSRR	Reset source register	R/W	000XXXXX _B
000A _H	TBTC	Time-base timer control register	R/W	00000000 _B
000B _H	WPCR	Watch prescaler control register	R/W	00000000 _B
000C _H	WDTC	Watchdog timer control register	R/W	00XX0000 _B
000D _H	SYCC2	System clock control register 2	R/W	XXXX0011 _B
000E _H	STBC2	Standby control register 2	R/W	00000000 _B
000F _H to 0027 _H	—	(Disabled)	—	—
0028 _H	PDRF	Port F data register	R/W	00000000 _B
0029 _H	DDRF	Port F direction register	R/W	00000000 _B
002A _H , 002B _H	—	(Disabled)	—	—
002C _H	PUL0	Port 0 pull-up register	R/W	00000000 _B
002D _H to 0032 _H	—	(Disabled)	—	—
0033 _H	PUL6	Port 6 pull-up register	R/W	00000000 _B
0034 _H , 0035 _H	—	(Disabled)	—	—
0036 _H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000 _B
0037 _H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000 _B
0038 _H to 0049 _H	—	(Disabled)	—	—
004A _H	EIC20	External interrupt circuit control register ch. 4	R/W	00000000 _B
004B _H	EIC30	External interrupt circuit control register ch. 6	R/W	00000000 _B
004C _H , 004D _H	—	(Disabled)	—	—
004E _H	LVDR	LVDR reset voltage selection ID register	R/W	00000000 _B
004F _H to 006B _H	—	(Disabled)	—	—

(Continued)

MB95560H/570H/580H Series

Address	Register abbreviation	Register name	R/W	Initial value
006C _H	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 _B
006D _H	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 _B
006E _H	ADDH	8/10-bit A/D converter data register upper	R/W	00000000 _B
006F _H	ADDL	8/10-bit A/D converter data register lower	R/W	00000000 _B
0070 _H	—	(Disabled)	—	—
0071 _H	FSR2	Flash memory status register 2	R/W	00000000 _B
0072 _H	FSR	Flash memory status register	R/W	000X0000 _B
0073 _H	SWRE0	Flash memory sector write control register 0	R/W	00000000 _B
0074 _H	FSR3	Flash memory status register 3	R	000XXXXX _B
0075 _H	FSR4	Flash memory status register 4	R/W	00000000 _B
0076 _H	WREN	Wild register address compare enable register	R/W	00000000 _B
0077 _H	WROR	Wild register data test setting register	R/W	00000000 _B
0078 _H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079 _H	ILR0	Interrupt level setting register 0	R/W	11111111 _B
007A _H	ILR1	Interrupt level setting register 1	R/W	11111111 _B
007B _H , 007C _H	—	(Disabled)	—	—
007D _H	ILR4	Interrupt level setting register 4	R/W	11111111 _B
007E _H	ILR5	Interrupt level setting register 5	R/W	11111111 _B
007F _H	—	(Disabled)	—	—
0F80 _H	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000 _B
0F81 _H	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000 _B
0F82 _H	WRDR0	Wild register data setting register ch. 0	R/W	00000000 _B
0F83 _H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000 _B
0F84 _H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000 _B
0F85 _H	WRDR1	Wild register data setting register ch. 1	R/W	00000000 _B
0F86 _H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000 _B
0F87 _H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000 _B
0F88 _H	WRDR2	Wild register data setting register ch. 2	R/W	00000000 _B
0F89 _H to 0F91 _H	—	(Disabled)	—	—
0F92 _H	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000 _B
0F93 _H	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000 _B
0F94 _H	T01DR	8/16-bit composite timer 01 data register	R/W	00000000 _B
0F95 _H	T00DR	8/16-bit composite timer 00 data register	R/W	00000000 _B
0F96 _H	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000 _B
0F97 _H to 0FC2 _H	—	(Disabled)	—	—

(Continued)

MB95560H/570H/580H Series

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FC3 _H	AIDRL	A/D input disable register (lower)	R/W	00000000 _B
0FC4 _H to 0FE3 _H	—	(Disabled)	—	—
0FE4 _H	CRT _H	Main CR clock trimming register (upper)	R/W	000XXXXX _B
0FE5 _H	CRT _L	Main CR clock trimming register (lower)	R/W	000XXXXX _B
0FE6 _H	—	(Disabled)	—	—
0FE7 _H	CRT _{DA}	Main CR clock temperature dependent adjustment register	R/W	00011111 _B
0FE8 _H	SYSC	System configuration register	R/W	11000011 _B
0FE9 _H	CMCR	Clock monitoring control register	R/W	00000000 _B
0FEA _H	CMDR	Clock monitoring data register	R/W	00000000 _B
0FEB _H	WDTH	Watchdog timer selection ID register (upper)	R/W	XXXXXXXX _B
0FEC _H	WDTL	Watchdog timer selection ID register (lower)	R/W	XXXXXXXX _B
0FED _H to 0FFF _H	—	(Disabled)	—	—

- R/W access symbols

R/W : Readable / Writable

R : Read only

- Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

MB95560H/570H/580H Series

■ I/O MAP (MB95580H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000 _H	PDR0	Port 0 data register	R/W	00000000 _B
0001 _H	DDR0	Port 0 direction register	R/W	00000000 _B
0002 _H	PDR1	Port 1 data register	R/W	00000000 _B
0003 _H	DDR1	Port 1 direction register	R/W	00000000 _B
0004 _H	—	(Disabled)	—	—
0005 _H	WATR	Oscillation stabilization wait time setting register	R/W	11111111 _B
0006 _H	PLLC	PLL control register	R/W	00000000 _B
0007 _H	SYCC	System clock control register	R/W	XXX11011 _B
0008 _H	STBC	Standby control register	R/W	00000000 _B
0009 _H	RSRR	Reset source register	R/W	000XXXXX _B
000A _H	TBTC	Time-base timer control register	R/W	00000000 _B
000B _H	WPCR	Watch prescaler control register	R/W	00000000 _B
000C _H	WDTC	Watchdog timer control register	R/W	00XX0000 _B
000D _H	SYCC2	System clock control register 2	R/W	XXXX0011 _B
000E _H	STBC2	Standby control register 2	R/W	00000000 _B
000F _H to 0027 _H	—	(Disabled)	—	—
0028 _H	PDRF	Port F data register	R/W	00000000 _B
0029 _H	DDRF	Port F direction register	R/W	00000000 _B
002A _H	PDRG	Port G data register	R/W	00000000 _B
002B _H	DDRG	Port G direction register	R/W	00000000 _B
002C _H	PUL0	Port 0 pull-up register	R/W	00000000 _B
002D _H to 0032 _H	—	(Disabled)	—	—
0033 _H	PUL6	Port 6 pull-up register	R/W	00000000 _B
0034 _H	—	(Disabled)	—	—
0035 _H	PULG	Port G pull-up register	R/W	00000000 _B
0036 _H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000 _B
0037 _H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000 _B
0038 _H to 0048 _H	—	(Disabled)	—	—
0049 _H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000 _B
004A _H	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000 _B
004B _H	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000 _B
004C _H , 004D _H	—	(Disabled)	—	—
004E _H	LVDR	LVDR reset voltage selection ID register	R/W	00000000 _B
004F _H	—	(Disabled)	—	—

(Continued)

MB95560H/570H/580H Series

Address	Register abbreviation	Register name	R/W	Initial value
0050 _H	SCR	LIN-UART serial control register	R/W	00000000 _B
0051 _H	SMR	LIN-UART serial mode register	R/W	00000000 _B
0052 _H	SSR	LIN-UART serial status register	R/W	00001000 _B
0053 _H	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000 _B
0054 _H	ESCR	LIN-UART extended status control register	R/W	00000100 _B
0055 _H	ECCR	LIN-UART extended communication control register	R/W	000000XX _B
0056 _H to 006B _H	—	(Disabled)	—	—
006C _H	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 _B
006D _H	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 _B
006E _H	ADDH	8/10-bit A/D converter data register upper	R/W	00000000 _B
006F _H	ADDL	8/10-bit A/D converter data register lower	R/W	00000000 _B
0070 _H	—	(Disabled)	—	—
0071 _H	FSR2	Flash memory status register 2	R/W	00000000 _B
0072 _H	FSR	Flash memory status register	R/W	000X0000 _B
0073 _H	SWRE0	Flash memory sector write control register 0	R/W	00000000 _B
0074 _H	FSR3	Flash memory status register 3	R	000XXXXX _B
0075 _H	FSR4	Flash memory status register 4	R/W	00000000 _B
0076 _H	WREN	Wild register address compare enable register	R/W	00000000 _B
0077 _H	WROR	Wild register data test setting register	R/W	00000000 _B
0078 _H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079 _H	ILR0	Interrupt level setting register 0	R/W	11111111 _B
007A _H	ILR1	Interrupt level setting register 1	R/W	11111111 _B
007B _H	ILR2	Interrupt level setting register 2	R/W	11111111 _B
007C _H	—	(Disabled)	—	—
007D _H	ILR4	Interrupt level setting register 4	R/W	11111111 _B
007E _H	ILR5	Interrupt level setting register 5	R/W	11111111 _B
007F _H	—	(Disabled)	—	—
0F80 _H	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000 _B
0F81 _H	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000 _B
0F82 _H	WRDR0	Wild register data setting register ch. 0	R/W	00000000 _B
0F83 _H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000 _B
0F84 _H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000 _B
0F85 _H	WRDR1	Wild register data setting register ch. 1	R/W	00000000 _B
0F86 _H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000 _B
0F87 _H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000 _B
0F88 _H	WRDR2	Wild register data setting register ch. 2	R/W	00000000 _B

(Continued)

MB95560H/570H/580H Series

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0F89 _H to 0F91 _H	—	(Disabled)	—	—
0F92 _H	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000 _B
0F93 _H	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000 _B
0F94 _H	T01DR	8/16-bit composite timer 01 data register	R/W	00000000 _B
0F95 _H	T00DR	8/16-bit composite timer 00 data register	R/W	00000000 _B
0F96 _H	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000 _B
0F97 _H to 0FBB _H	—	(Disabled)	—	—
0FBC _H	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 _B
0FBD _H	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 _B
0FBE _H to 0FC2 _H	—	(Disabled)	—	—
0FC3 _H	AIDRL	A/D input disable register (Lower)	R/W	00000000 _B
0FC4 _H to 0FE3 _H	—	(Disabled)	—	—
0FE4 _H	CRTH	Main CR clock trimming register (upper)	R/W	000XXXXX _B
0FE5 _H	CRTL	Main CR clock trimming register (lower)	R/W	000XXXXX _B
0FE6 _H	—	(Disabled)	—	—
0FE7 _H	CRTDA	Main CR clock temperature dependent adjustment	R/W	00011111 _B
0FE8 _H	SYSC	System configuration register	R/W	11000011 _B
0FE9 _H	CMCR	Clock monitoring control register	R/W	00000000 _B
0FEA _H	CMDR	Clock monitoring data register	R/W	00000000 _B
0FEB _H	WDTH	Watchdog timer selection ID register (upper)	R/W	XXXXXXXX _B
0FEC _H	WDTL	Watchdog timer selection ID register (lower)	R/W	XXXXXXXX _B
0FED _H to 0FFF _H	—	(Disabled)	—	—

- R/W access symbols

R/W : Readable / Writable

R : Read only

- Initial value symbols

0 : The initial value of this bit is “0”.

1 : The initial value of this bit is “1”.

X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

MB95560H/570H/580H Series

■ INTERRUPT SOURCE TABLE (MB95560H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA _H	FFFB _H	L00 [1:0]	<div>High</div> <div>↑</div> <div>↓</div> <div>Low</div>
External interrupt ch. 5	IRQ01	FFF8 _H	FFF9 _H	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6 _H	FFF7 _H	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4 _H	FFF5 _H	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	FFF2 _H	FFF3 _H	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 _H	FFF1 _H	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE _H	FFEF _H	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC _H	FFED _H	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA _H	FFEB _H	L08 [1:0]	
—	IRQ09	FFE8 _H	FFE9 _H	L09 [1:0]	
—	IRQ10	FFE6 _H	FFE7 _H	L10 [1:0]	
—	IRQ11	FFE4 _H	FFE5 _H	L11 [1:0]	
—	IRQ12	FFE2 _H	FFE3 _H	L12 [1:0]	
—	IRQ13	FFE0 _H	FFE1 _H	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	FFDE _H	FFDF _H	L14 [1:0]	
—	IRQ15	FFDC _H	FFDD _H	L15 [1:0]	
—	IRQ16	FFDA _H	FFDB _H	L16 [1:0]	
—	IRQ17	FFD8 _H	FFD9 _H	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6 _H	FFD7 _H	L18 [1:0]	
Time-base timer	IRQ19	FFD4 _H	FFD5 _H	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 _H	FFD3 _H	L20 [1:0]	
—	IRQ21	FFD0 _H	FFD1 _H	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	FFCE _H	FFCF _H	L22 [1:0]	
Flash memory	IRQ23	FFCC _H	FFCD _H	L23 [1:0]	

MB95560H/570H/580H Series

■ INTERRUPT SOURCE TABLE (MB95570H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA _H	FFFB _H	L00 [1:0]	<div>High</div> <div>↑</div> <div>↓</div> <div>Low</div>
—	IRQ01	FFF8 _H	FFF9 _H	L01 [1:0]	
—	IRQ02	FFF6 _H	FFF7 _H	L02 [1:0]	
External interrupt ch. 6					
—	IRQ03	FFF4 _H	FFF5 _H	L03 [1:0]	
—					
—					
—	IRQ04	FFF2 _H	FFF3 _H	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 _H	FFF1 _H	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE _H	FFEF _H	L06 [1:0]	
—	IRQ07	FFEC _H	FFED _H	L07 [1:0]	
—	IRQ08	FFEA _H	FFEB _H	L08 [1:0]	
—	IRQ09	FFE8 _H	FFE9 _H	L09 [1:0]	
—	IRQ10	FFE6 _H	FFE7 _H	L10 [1:0]	
—	IRQ11	FFE4 _H	FFE5 _H	L11 [1:0]	
—	IRQ12	FFE2 _H	FFE3 _H	L12 [1:0]	
—	IRQ13	FFE0 _H	FFE1 _H	L13 [1:0]	
—	IRQ14	FFDE _H	FFDF _H	L14 [1:0]	
—	IRQ15	FFDC _H	FFDD _H	L15 [1:0]	
—	IRQ16	FFDA _H	FFDB _H	L16 [1:0]	
—	IRQ17	FFD8 _H	FFD9 _H	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6 _H	FFD7 _H	L18 [1:0]	
Time-base timer	IRQ19	FFD4 _H	FFD5 _H	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 _H	FFD3 _H	L20 [1:0]	
—	IRQ21	FFD0 _H	FFD1 _H	L21 [1:0]	
—	IRQ22	FFCE _H	FFCF _H	L22 [1:0]	
Flash memory	IRQ23	FFCC _H	FFCD _H	L23 [1:0]	

MB95560H/570H/580H Series

■ INTERRUPT SOURCE TABLE (MB95580H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA _H	FFFB _H	L00 [1:0]	<div>High</div> <div>↑</div> <div>↓</div> <div>Low</div>
External interrupt ch. 5	IRQ01	FFF8 _H	FFF9 _H	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6 _H	FFF7 _H	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4 _H	FFF5 _H	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	FFF2 _H	FFF3 _H	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 _H	FFF1 _H	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE _H	FFEF _H	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC _H	FFED _H	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA _H	FFEB _H	L08 [1:0]	
—	IRQ09	FFE8 _H	FFE9 _H	L09 [1:0]	
—	IRQ10	FFE6 _H	FFE7 _H	L10 [1:0]	
—	IRQ11	FFE4 _H	FFE5 _H	L11 [1:0]	
—	IRQ12	FFE2 _H	FFE3 _H	L12 [1:0]	
—	IRQ13	FFE0 _H	FFE1 _H	L13 [1:0]	
—	IRQ14	FFDE _H	FFDF _H	L14 [1:0]	
—	IRQ15	FFDC _H	FFDD _H	L15 [1:0]	
—	IRQ16	FFDA _H	FFDB _H	L16 [1:0]	
—	IRQ17	FFD8 _H	FFD9 _H	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6 _H	FFD7 _H	L18 [1:0]	
Time-base timer	IRQ19	FFD4 _H	FFD5 _H	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 _H	FFD3 _H	L20 [1:0]	
—	IRQ21	FFD0 _H	FFD1 _H	L21 [1:0]	
—	IRQ22	FFCE _H	FFCF _H	L22 [1:0]	
Flash memory	IRQ23	FFCC _H	FFCD _H	L23 [1:0]	

MB95560H/570H/580H Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6$	V	
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6$	V	*2
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6$	V	*2
Maximum clamp current	I_{CLAMP}	- 2	+ 2	mA	Applicable to specific pins*3
Total maximum clamp current	$\Sigma I_{CLAMP} $	—	20	mA	Applicable to specific pins*3
“L” level maximum output current	I_{OL1}	—	15	mA	Other than P05, P06, P62 and P63*4
	I_{OL2}		15		P05, P06, P62 and P63*4
“L” level average current	I_{OLAV1}	—	4	mA	Other than P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
	I_{OLAV2}		12		P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI_{OL}	—	48	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	I_{OH1}	—	- 15	mA	Other than P05, P06, P62 and P63*4
	I_{OH2}		- 15		P05, P06, P62 and P63*4
“H” level average current	I_{OHAV1}	—	- 4	mA	Other than P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
	I_{OHAV2}		- 8		P05, P06, P62 and P63*4 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI_{OH}	—	48	mA	
“H” level total average output current	ΣI_{OHAV}	—	- 50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	P_d	—	320	mW	
Operating temperature	T_A	- 40	+ 85	°C	
Storage temperature	T_{stg}	- 55	+ 150	°C	

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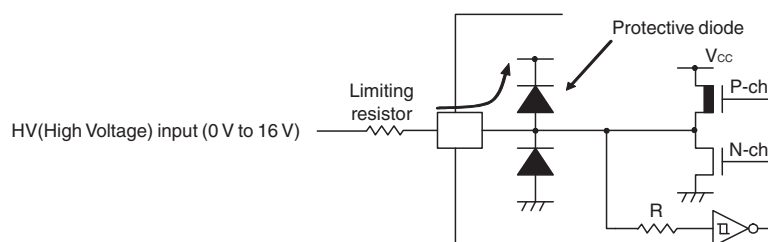
*1: The parameter is based on the condition that V_{SS} is 0.0 V.

*2: V_I and V_O must not exceed $V_{CC} + 0.3$ V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P00 to P07, P62 to P64, PF0, PF1, PG1, PG2 (P00, and P62 to P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K. P01, P02, P03, P07, PF0, PF1, PG1 and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

- Input/Output equivalent circuit



*4: P62 and P63 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB95560H/570H/580H Series

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

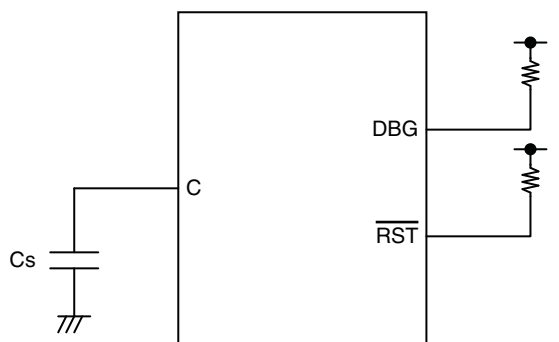
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V _{CC}	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C _S	0.022	1	μF	*3	
Operating temperature	T _A	− 40	+ 85	°C	Other than on-chip debug mode	
		+ 5	+ 35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The value is 2.88 V when the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V_{CC} pin must have a capacitance larger than C_S. For the connection to a smoothing capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG / $\overline{\text{RST}}$ / C pins connection diagram



*: Since the DBG pin becomes a communication pin in on-chip debug mode, set a pull-up resistor value suiting the input/output specifications of P12/EC0/DBG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

MB95560H/570H/580H Series

3. DC Characteristics

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P04	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	V_{IHS}	P00* ³ to P03* ⁴ , P05 to P07* ⁴ , P12, P62 to P64* ³ , PF0* ⁴ , PF1* ⁴ , PG1* ⁴ , PG2* ⁴	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	V_{IHM}	PF2	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
"L" level input voltage	V_{IL}	P04	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	Hysteresis input
	V_{ILS}	P00* ³ to P03* ⁴ , P05 to P07* ⁴ , P12, P62 to P64* ³ , PF0* ⁴ , PF1* ⁴ , PG1* ⁴ , PG2* ⁴	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
	V_{ILM}	PF2	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
Open-drain output application voltage	V_D	P12, PF2	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
"H" level output voltage	V_{OH1}	P04, PF0* ⁴ , PF1* ⁴ , PG1* ⁴ , PG2* ⁴	$I_{OH} = -4 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	V_{OH2}	P00* ³ to P03* ⁴ , P05 to P07* ⁴ , P62 to P64* ³	$I_{OH} = -8 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	V_{OL1}	P04, P12, PF0 to PF2* ⁴ , PG1* ⁴ , PG2* ⁴	$I_{OL} = 4 \text{ mA}$	—	—	0.4	V	
	V_{OL2}	P00* ³ to P03* ⁴ , P05 to P07* ⁴ , P12, P62 to P64* ³	$I_{OL} = 12 \text{ mA}$	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	$0.0 \text{ V} < V_I < V_{CC}$	-5	—	+5	μA	When pull-up resistance is disabled
Pull-up resistance	R_{PULL}	P00* ³ to P07* ⁴ , P62 to P64* ³ , PG1* ⁴ , PG2* ⁴ * ⁵	$V_I = 0 \text{ V}$	25	50	100	k Ω	When pull-up resistance is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	$f = 1 \text{ MHz}$	—	5	15	pF	

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MB95560H/570H/580H Series

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ ^{*1}	Max ^{*2}		
Power supply current ^{*5}	I _{CC}	V _{CC} (External clock operation)	F _{CH} = 32 MHz F _{MP} = 16 MHz Main clock mode (divided by 2)	—	3.6	5.8	mA	Except during Flash memory programming and erasing
				—	7.5	13.8	mA	During Flash memory programming and erasing
				—	4.1	9.1	mA	At A/D conversion
	I _{CCS}		F _{CH} = 32 MHz F _{MP} = 16 MHz Main sleep mode (divided by 2)	—	1.3	3	mA	
	I _{CCL}		F _{CL} = 32 kHz F _{MPL} = 16 kHz Subclock mode (divided by 2) T _A = +25°C	—	49	145	μA	
	I _{CCLS} ^{*6}		F _{CL} = 32 kHz F _{MPL} = 16 kHz Subsleep mode (divided by 2) T _A = +25°C	—	6	10	μA	
	I _{CCT} ^{*6}		F _{CL} = 32 kHz Watch mode Main stop mode T _A = +25°C	—	5	9	μA	
	I _{CCMCR}	V _{CC}	F _{CRH} = 4 MHz F _{MP} = 4 MHz Main CR clock mode	—	1.1	4.6	mA	
	I _{CCSCR}		Sub-CR clock mode (divided by 2) T _A = +25°C	—	58.1	230	μA	
	I _{CCTS}	V _{CC} (External clock operation)	F _{CH} = 32 MHz Time-base timer mode T _A = +25°C	—	330	370	μA	
	I _{CCH}		Substop mode T _A = +25°C	—	4	15	μA	Main stop mode for a single external clock product

(Continued)

MB95560H/570H/580H Series

(Continued)

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ ^{*1}	Max ^{*2}		
Power supply current ^{*5}	I_{LVD}	V_{CC}	Current consumption for low-voltage detection circuit only	—	4	7	μA	
	I_{CRH}		Current consumption for the main CR oscillator	—	240	320	μA	
	I_{CRL}		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	7	20	μA	

*1: $V_{CC} = 5.0 \text{ V}$, $T_A = +25^\circ\text{C}$

*2: $V_{CC} = 5.5 \text{ V}$, $T_A = +85^\circ\text{C}$ (unless otherwise specified)

*3: P00, P62, P63 and P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

*4: P01, P02, P03, P07, PF0, PF1, PG1 and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

*5: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit (I_{LVD}) to one of the value from I_{CC} to I_{CCH} . In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators (I_{CRH} , I_{CRL}) and a specified value. In on-chip debug mode, the CR oscillator (I_{CRH}) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

• See "4. AC Characteristics: (1) Clock Timing" for F_{CH} and F_{CL} .

• See "4. AC Characteristics: (2) Source Clock / Machine Clock" for F_{MP} and F_{MPL} .

*6: In sub-CR clock mode, the power supply current value will become the sum of adding I_{CRL} to I_{CCLS} or I_{CCT} . In addition, when the sub-CR clock mode is selected with F_{MPL} being 50 kHz, the current consumption will increase accordingly.

MB95560H/570H/580H Series

4. AC Characteristics

(1) Clock Timing

($V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used
		X0	X1 : open	1	—	12	MHz	When the main external clock is used
		X0, X1	*	1	—	32.5	MHz	
	F_{CRH}	—	—	3.92	4	4.08	MHz	Operating conditions • The main CR clock is used. • $0^\circ\text{C} < T_A < +70^\circ\text{C}$
				3.8	4	4.2	MHz	Operating conditions • The main CR clock is used. • $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$, + $70^\circ\text{C} < T_A \leq +85^\circ\text{C}$
				7.84	8	8.16	MHz	Operating conditions • PLL multiplier: 2 • $0^\circ\text{C} < T_A < +70^\circ\text{C}$
				7.6	8	8.4	MHz	Operating conditions • PLL multiplier: 2 • $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$, + $70^\circ\text{C} < T_A \leq +85^\circ\text{C}$
				9.8	10	10.2	MHz	Operating conditions • PLL multiplier: 2.5 • $0^\circ\text{C} < T_A < +70^\circ\text{C}$
				9.5	10	10.5	MHz	Operating conditions • PLL multiplier: 2.5 • $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$, + $70^\circ\text{C} < T_A \leq +85^\circ\text{C}$
				11.76	12	12.24	MHz	Operating conditions • PLL multiplier: 3 • $0^\circ\text{C} < T_A < +70^\circ\text{C}$
				11.4	12	12.6	MHz	Operating conditions • PLL multiplier: 3 • $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$, + $70^\circ\text{C} < T_A \leq +85^\circ\text{C}$
				15.68	16	16.32	MHz	Operating conditions • PLL multiplier: 4 • $0^\circ\text{C} < T_A < +70^\circ\text{C}$
				15.2	16	16.8	MHz	Operating conditions • PLL multiplier: 4 • $-40^\circ\text{C} \leq T_A < 0^\circ\text{C}$, + $70^\circ\text{C} < T_A \leq +85^\circ\text{C}$
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	When the sub-oscillation circuit is used
				—	32.768	—	kHz	When the sub-external clock is used
	F_{CRL}	—	—	50	100	150	kHz	When the sub-CR clock is used

(Continued)

MB95560H/570H/580H Series

(Continued)

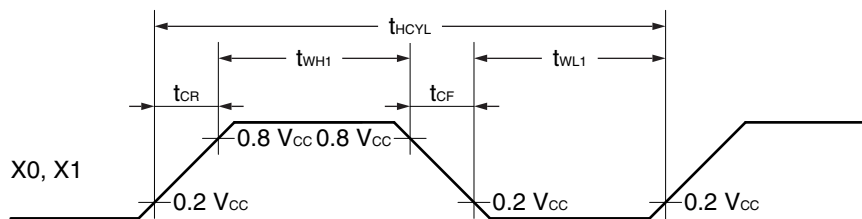
($V_{CC} = 2.4 \text{ V}$ to 5.5 V , $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock cycle time	t_{HCYL}	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used
		X0	X1 : open	83.4	—	1000	ns	When an external clock is used
		X0, X1	*	30.8	—	1000	ns	
	t_{LCYL}	X0A, X1A	—	—	30.5	—	μs	When the subclock is used
Input clock pulse width	t_{WH1}	X0	X1 : open	33.4	—	—	ns	When an external clock is used, the duty ratio should range between 40% and 60%.
	t_{WL1}	X0, X1	*	14.4	—	—	ns	
	t_{WH2} t_{WL2}	X0A	—	—	15.2	—	μs	
Input clock rise time and fall time	t_{CR}	X0	X1 : open	—	—	5	ns	When an external clock is used
	t_{CF}	X0, X1	*	—	—	5	ns	
CR oscillation start time	t_{CRHWK}	—	—	—	—	50	μs	When the main CR clock is used
	t_{CRLWK}	—	—	—	—	30	μs	When the sub-CR clock is used

*: The external clock signal is input to X0 and the inverted external clock signal to X1.

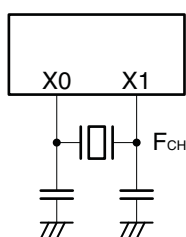
MB95560H/570H/580H Series

- Input waveform generated when an external clock (main clock) is used

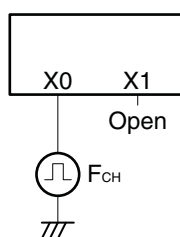


- Figure of main clock input port external connection

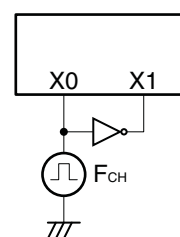
When a crystal oscillator or a ceramic oscillator is used



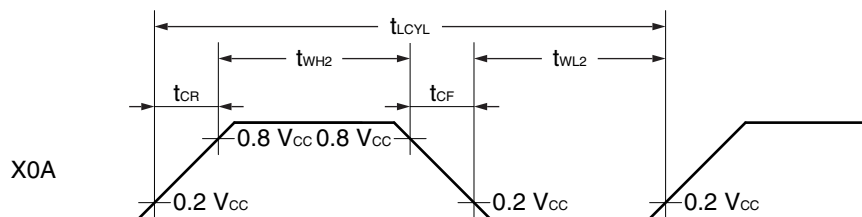
When an external clock is used (X1 is open)



When an external clock is used

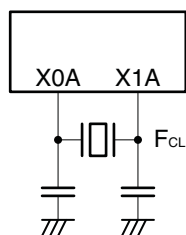


- Input waveform generated when an external clock (subclock) is used

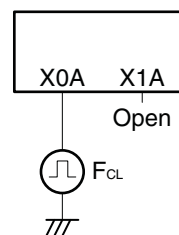


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When an external clock is used



MB95560H/570H/580H Series

(2) Source Clock / Machine Clock

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t _{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F _{CH} = 32.5 MHz, divided by 2 Max: F _{CH} = 1 MHz, divided by 2
			62.5	—	1000	ns	When the main CR clock is used Min: F _{CRH} = 4 MHz, multiplied by 4 Max: F _{CRH} = 4 MHz, divided by 4
			—	61	—	μs	When the sub-oscillation clock is used F _{CL} = 32.768 kHz, divided by 2
			—	20	—	μs	When the sub-CR clock is used F _{CRL} = 100 kHz, divided by 2
Source clock frequency	F _{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			—	4	—	MHz	When the main CR clock is used
	F _{SPL}		—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F _{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t _{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F _{SP} = 16.25 MHz, no division Max: F _{SP} = 0.5 MHz, divided by 16
			250	—	1000	ns	When the main CR clock is used Min: F _{SP} = 4 MHz, no division Max: F _{SP} = 4 MHz, divided by 4
			61	—	976.5	μs	When the sub-oscillation clock is used Min: F _{SPL} = 16.384 kHz, no division Max: F _{SPL} = 16.384 kHz, divided by 16
			20	—	320	μs	When the sub-CR clock is used Min: F _{SPL} = 50 kHz, no division Max: F _{SPL} = 50 kHz, divided by 16
Machine clock frequency	F _{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	16	MHz	When the main CR clock is used
	F _{MPL}		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F _{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV1, DIV0). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV1, DIV0). In addition, a source clock can be selected from the following.

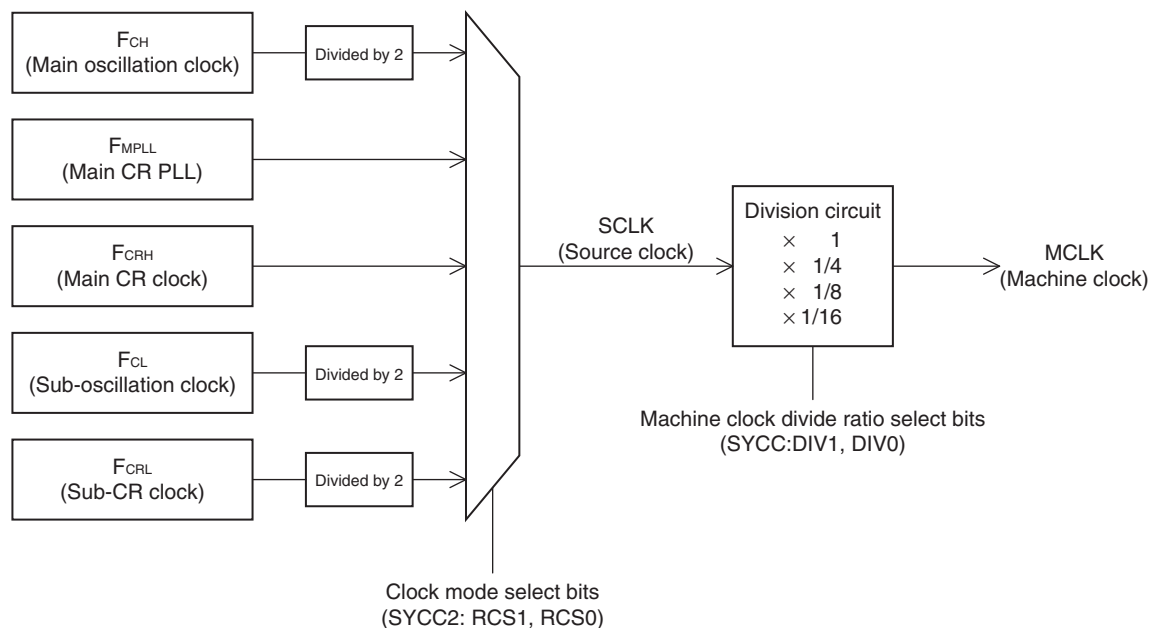
- Main clock divided by 2
- PLL multiplication of main clock (Select a multiplier from 2, 2.5, 3 and 4.)
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

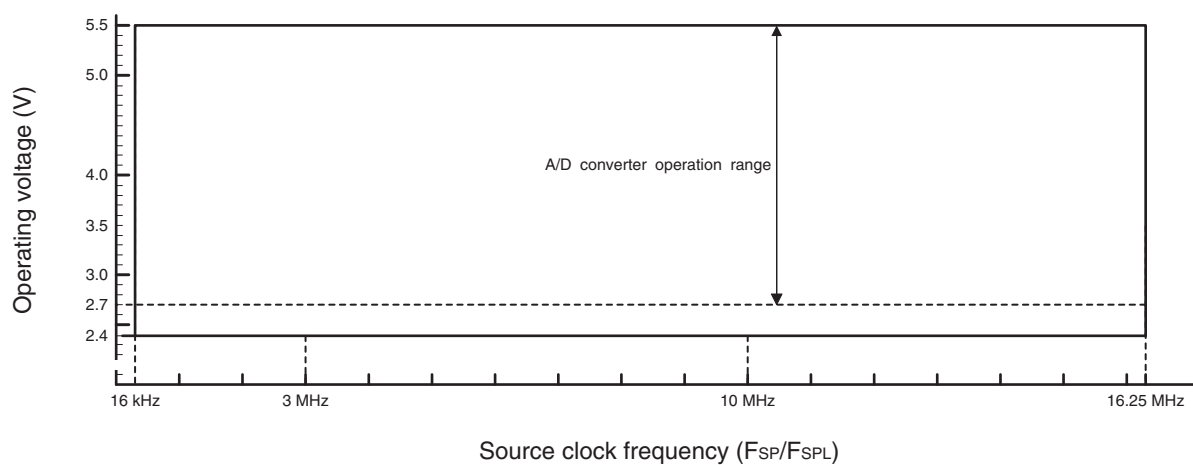
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

MB95560H/570H/580H Series

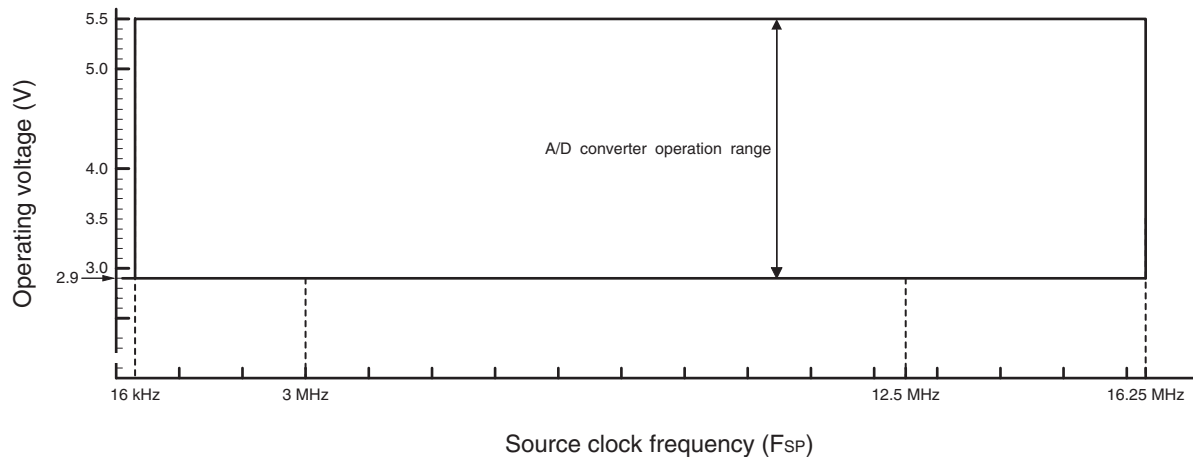
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (When $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
MB95560H/570H/580H (without the on-chip debug function)



- Operating voltage - Operating frequency (When $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)
MB95560H/570H/580H (with the on-chip debug function)



(3) External Reset

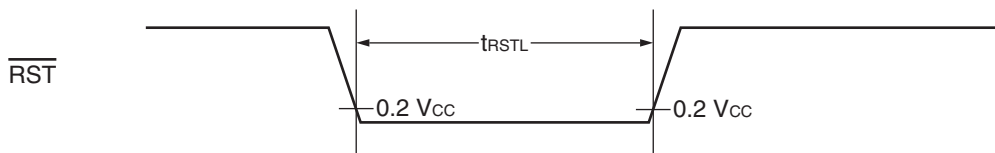
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{\text{RST}}$ "L" level pulse width	t_{RSTL}	$2 t_{\text{MCLK}}^{*1}$	—	ns	In normal operation
		Oscillation time of the oscillator ^{*2} + 200	—	μs	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		200	—	μs	In time-base timer mode

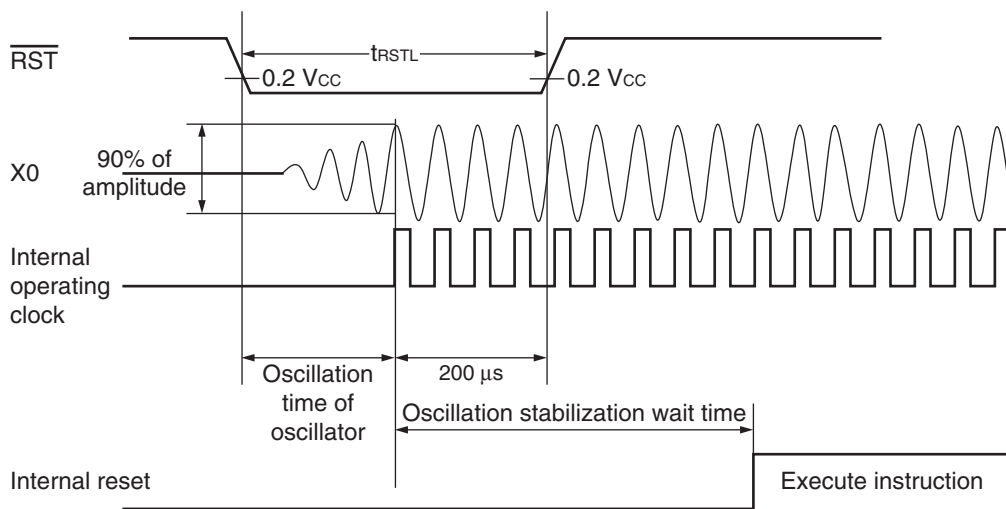
*1: See "(2) Source Clock / Machine Clock" for t_{MCLK} .

*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of μs and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several μs and several ms.

- In normal operation



- In stop mode, subclock mode, subsleep mode, watch mode and power-on

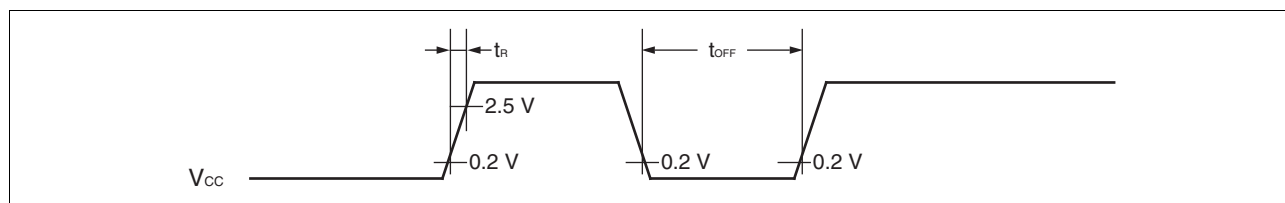


MB95560H/570H/580H Series

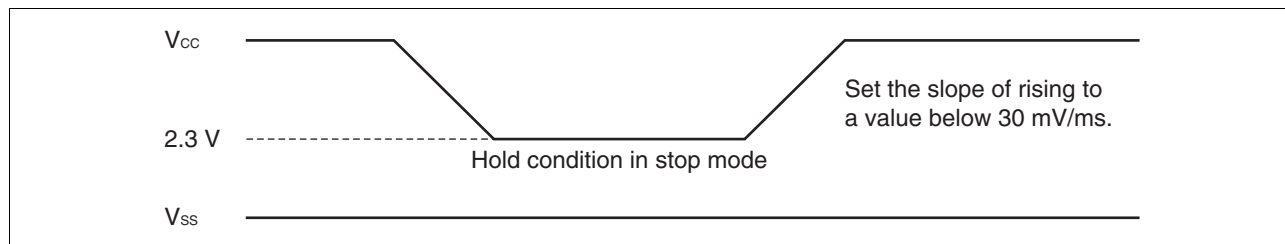
(4) Power-on Reset

($V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

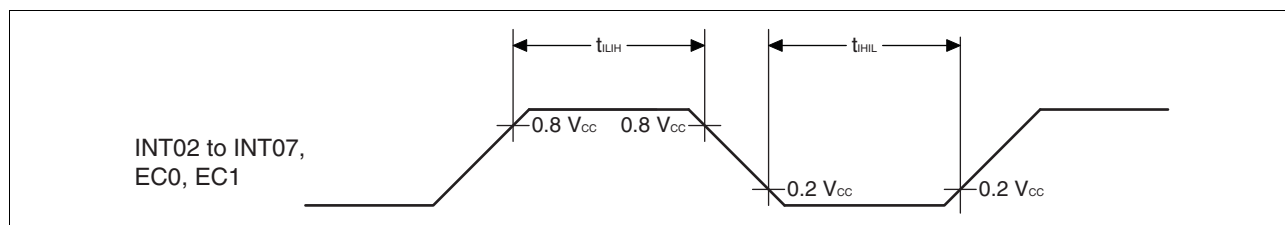


MB95560H/570H/580H Series

(5) Peripheral Input Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input "H" pulse width	t_{LH}	INT02 to INT07*1,*2, EC0*1, EC1*3	$2\ t_{MCLK}^{*4}$	—	ns
Peripheral input "L" pulse width	t_{HL}		$2\ t_{MCLK}^{*4}$	—	ns



*1: INT04, INT06 and EC0 are available on all products.

*2: INT02, INT03, INT05 and INT07 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.

*3: EC1 is only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

*4: See "(2) Source Clock / Machine Clock" for t_{MCLK} .

MB95560H/570H/580H Series

(6) LIN-UART Timing (only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K)

Sampling is executed at the rising edge of the sampling clock^{*1}, and serial clock delay is disabled^{*2}.

(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK	Internal clock operation output pin: C _L = 80 pF + 1 TTL	5 t _{MCLK} ^{*3}	—	ns
SCK ↓ → SOT delay time	t _{SLOVI}	SCK, SOT		- 50	+ 50	ns
Valid SIN → SCK ↑	t _{IVSHI}	SCK, SIN		t _{MCLK} ^{*3} + 80	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXI}	SCK, SIN		0	—	ns
Serial clock "L" pulse width	t _{SLSH}	SCK	External clock operation output pin: C _L = 80 pF + 1 TTL	3 t _{MCLK} ^{*3} - t _R	—	ns
Serial clock "H" pulse width	t _{SHSL}	SCK		t _{MCLK} ^{*3} + 10	—	ns
SCK ↓ → SOT delay time	t _{SLOVE}	SCK, SOT		—	2 t _{MCLK} ^{*3} + 60	ns
Valid SIN → SCK ↑	t _{IVSHE}	SCK, SIN		30	—	ns
SCK ↑ → valid SIN hold time	t _{SHIXE}	SCK, SIN		t _{MCLK} ^{*3} + 30	—	ns
SCK fall time	t _F	SCK		—	10	ns
SCK rise time	t _R	SCK		—	10	ns

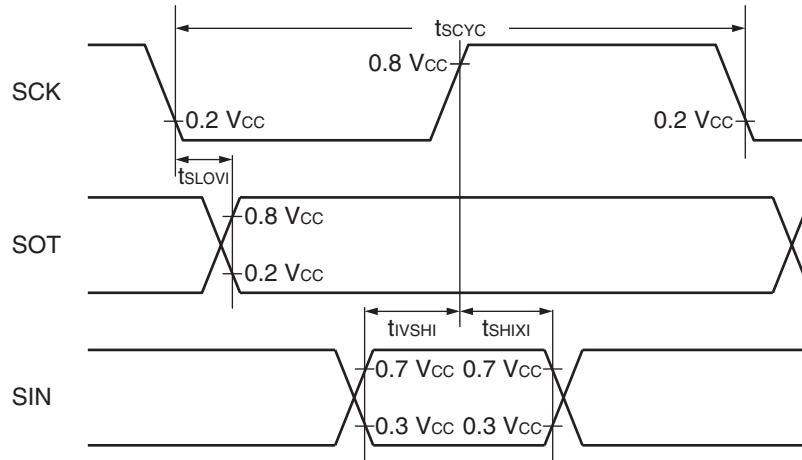
*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

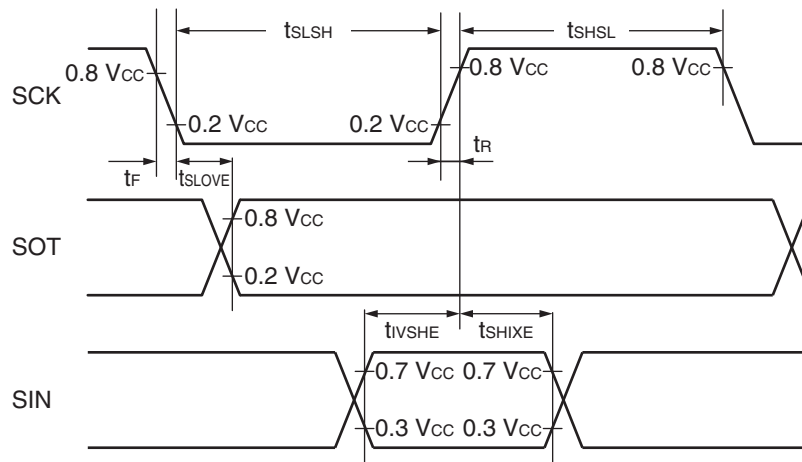
*3: See "(2) Source Clock / Machine Clock" for t_{MCLK}.

MB95560H/570H/580H Series

- Internal shift clock mode



- External shift clock mode



MB95560H/570H/580H Series

Sampling is executed at the falling edge of the sampling clock*¹, and serial clock delay is disabled*².
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t _{SCYC}	SCK	Internal clock operation output pin: C _L = 80 pF + 1 TTL	5 t _{MCLK} * ³	—	ns
SCK ↑ → SOT delay time	t _{SHOVI}	SCK, SOT		- 50	+ 50	ns
Valid SIN → SCK ↓	t _{IVSLI}	SCK, SIN		t _{MCLK} * ³ + 80	—	ns
SCK ↓ → valid SIN hold time	t _{SLIXI}	SCK, SIN		0	—	ns
Serial clock "H" pulse width	t _{SHSL}	SCK	External clock operation output pin: C _L = 80 pF + 1 TTL	3 t _{MCLK} * ³ - t _R	—	ns
Serial clock "L" pulse width	t _{SLSH}	SCK		t _{MCLK} * ³ + 10	—	ns
SCK ↑ → SOT delay time	t _{SHOVE}	SCK, SOT		—	2 t _{MCLK} * ³ + 60	ns
Valid SIN → SCK ↓	t _{IVSLE}	SCK, SIN		30	—	ns
SCK ↓ → valid SIN hold time	t _{SLIXE}	SCK, SIN		t _{MCLK} * ³ + 30	—	ns
SCK fall time	t _F	SCK		—	10	ns
SCK rise time	t _R	SCK		—	10	ns

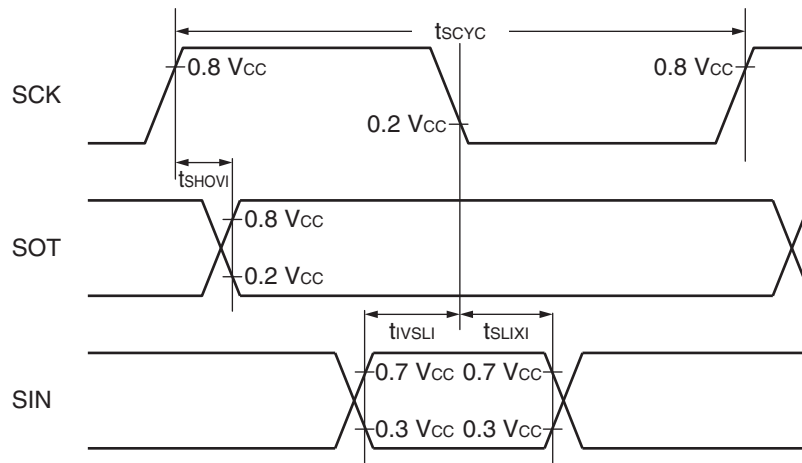
*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

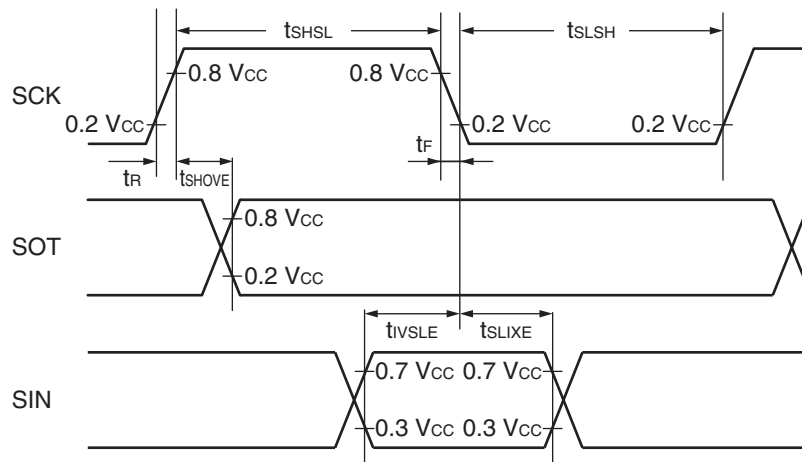
*3: See "(2) Source Clock / Machine Clock" for t_{MCLK}.

MB95560H/570H/580H Series

- Internal shift clock mode



- External shift clock mode



MB95560H/570H/580H Series

Sampling is executed at the rising edge of the sampling clock*¹, and serial clock delay is enabled*².
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

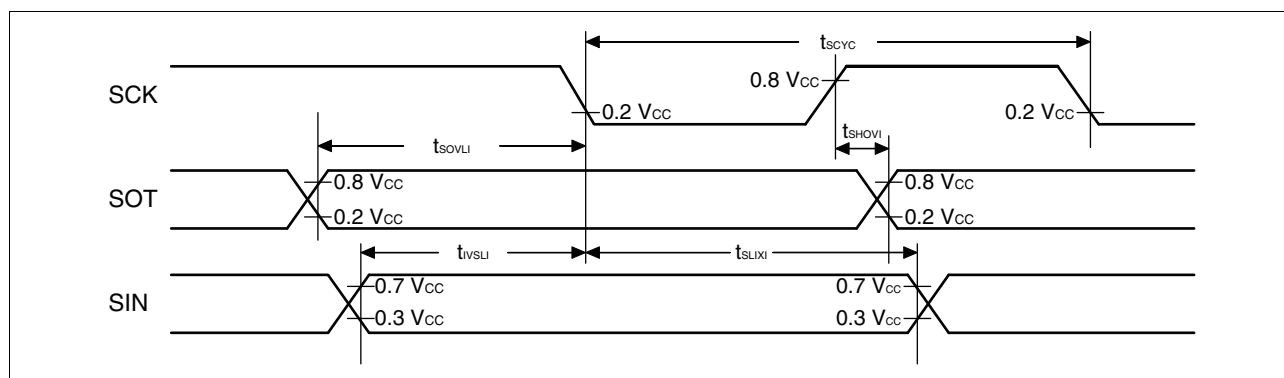
($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	t_{SHOVI}	SCK, SOT		- 50	+ 50	ns
Valid SIN \rightarrow SCK \downarrow	t_{IVSLI}	SCK, SIN		$t_{MCLK}^{*3} + 80$	—	ns
SCK $\downarrow \rightarrow$ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT \rightarrow SCK \downarrow delay time	t_{SOVLI}	SCK, SOT		$3 t_{MCLK}^{*3} - 70$	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “(2) Source Clock / Machine Clock” for t_{MCLK} .



MB95560H/570H/580H Series

Sampling is executed at the falling edge of the sampling clock*¹, and serial clock delay is enabled*².
(ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

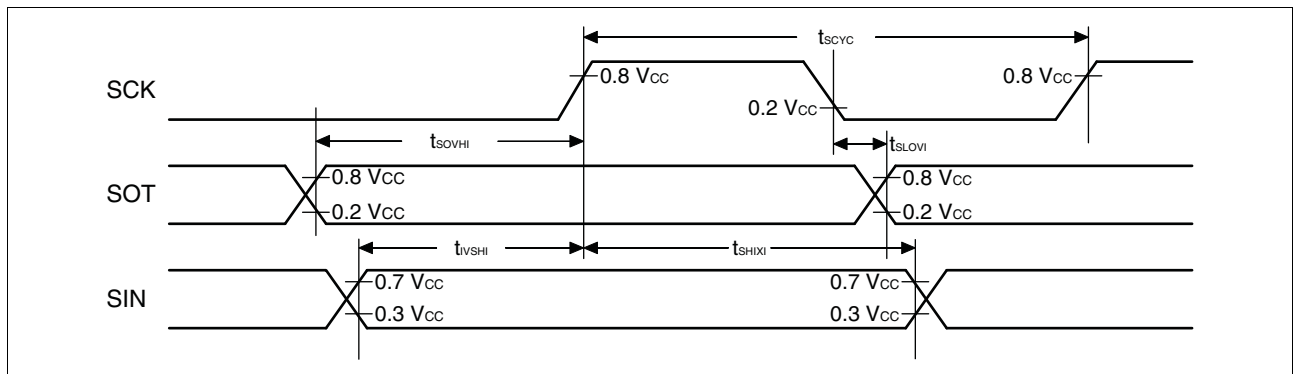
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin: $C_L = 80\text{ pF} + 1\text{ TTL}$	$5\ t_{MCLK}^{*3}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCK, SOT		- 50	+ 50	ns
Valid SIN \rightarrow SCK \uparrow	t_{IVSHI}	SCK, SIN		$t_{MCLK}^{*3} + 80$	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT \rightarrow SCK \uparrow delay time	t_{SOVHI}	SCK, SOT		$3\ t_{MCLK}^{*3} - 70$	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “(2) Source Clock / Machine Clock” for t_{MCLK} .



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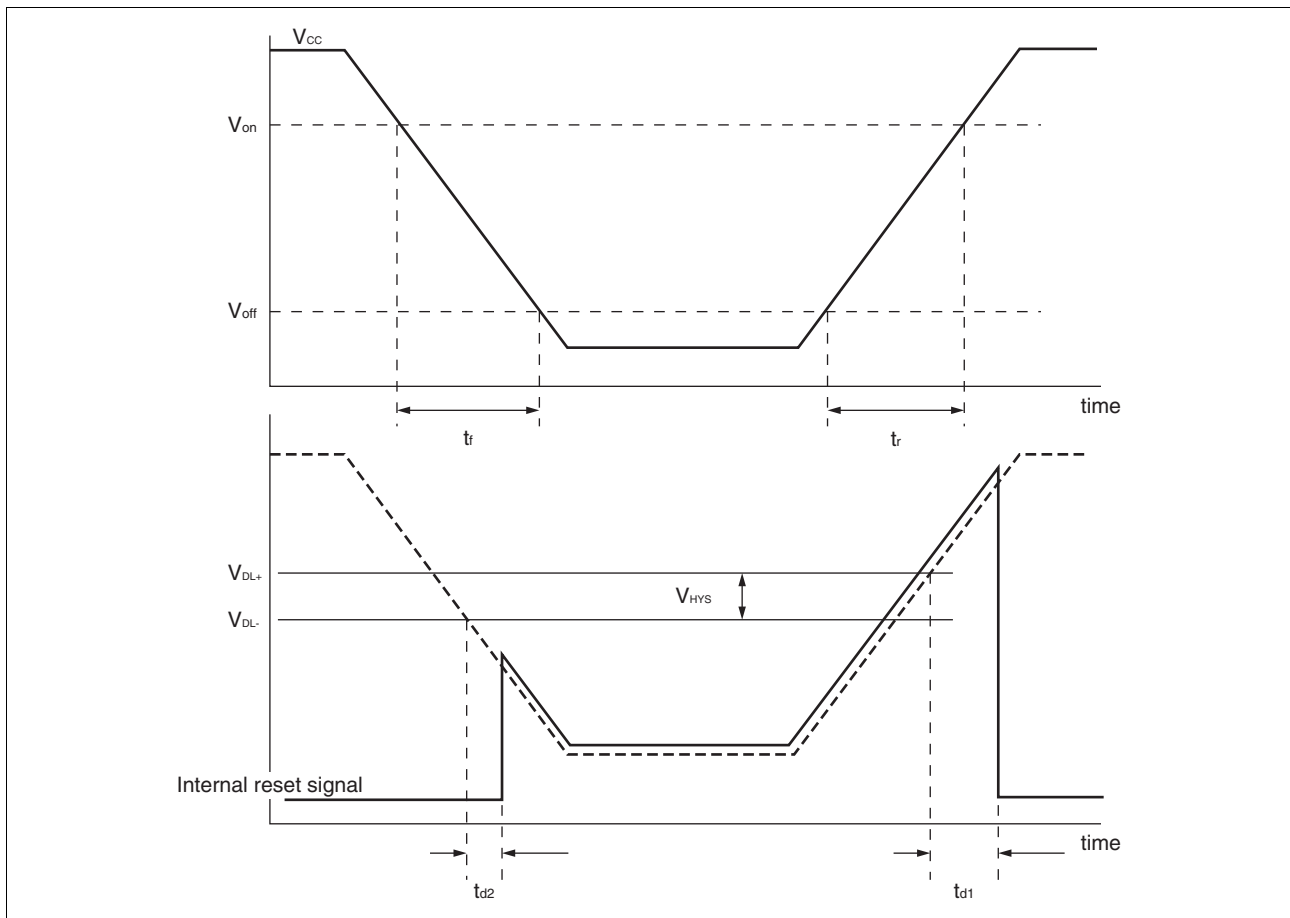
(7) Low-voltage Detection

($V_{SS} = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage*	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
		2.61	2.8	2.99		
		2.89	3.1	3.31		
		3.08	3.3	3.52		
Detection voltage*	V_{DL-}	2.43	2.6	2.77	V	At power supply fall
		2.52	2.7	2.88		
		2.80	3	3.20		
		2.99	3.2	3.41		
Hysteresis width	V_{HYS}	—	—	100	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	650	—	—	μs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	650	—	—	μs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	30	μs	
Reset detection delay time	t_{d2}	—	—	30	μs	
LVD threshold voltage transition stabilization time	t_{stb}	10	—	—	μs	

*: The release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDR register, refer to "CHAPTER 18 LOW-VOLTAGE DETECTION RESET CIRCUIT" in the hardware manual of the MB95560H/570H/580H Series.

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5. A/D Converter

(1) A/D Converter Electrical Characteristics

($V_{CC} = 2.7 \text{ V to } 5.5 \text{ V}$, $V_{SS} = 0.0 \text{ V}$, $T_A = -40^\circ\text{C to } +85^\circ\text{C}$)

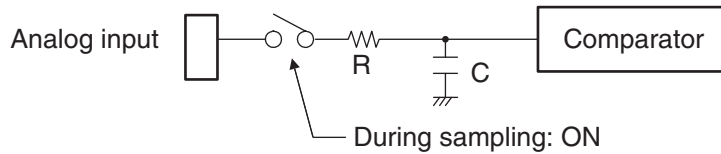
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		− 3	—	+ 3	LSB	
Linearity error		− 2.5	—	+ 2.5	LSB	
Differential linear error		− 1.9	—	+ 1.9	LSB	
Zero transition voltage	V_{OT}	$V_{SS} - 7.2 \text{ LSB}$	$V_{SS} + 0.5 \text{ LSB}$	$V_{SS} + 8.2 \text{ LSB}$	V	
Full-scale transition voltage	V_{FST}	$V_{CC} - 6.2 \text{ LSB}$	$V_{CC} - 1.5 \text{ LSB}$	$V_{CC} + 9.2 \text{ LSB}$	V	
Compare time	—	3	—	10	μs	$2.7 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$
Sampling time	—	0.517	—	∞	μs	$2.7 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$, with external impedance < 3.3 k Ω
Analog input current	I_{AIN}	− 0.3	—	+ 0.3	μA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

(2) Notes on Using the A/D Converter

• External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 μF to the analog input pin.

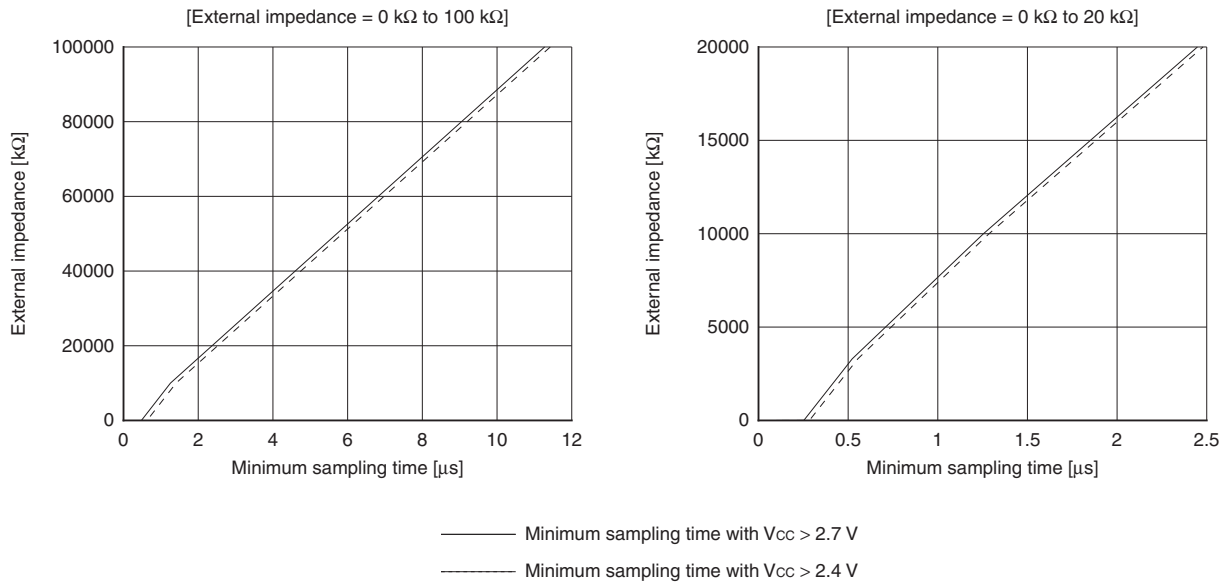
• Analog input equivalent circuit



V_{CC}	R	C
$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	3.3 k Ω (Max)	14.89 pF (Max)
$2.7\text{ V} \leq V_{CC} < 5.5\text{ V}$	15.7 k Ω (Max)	14.89 pF (Max)

Note: The values are reference values.

• Relationship between external impedance and minimum sampling time



• A/D conversion error

As $|V_{CC} - V_{SS}|$ decreases, the A/D conversion error increases proportionately.

(3) Definitions of A/D Converter Terms

- Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.

- Linearity error (unit: LSB)

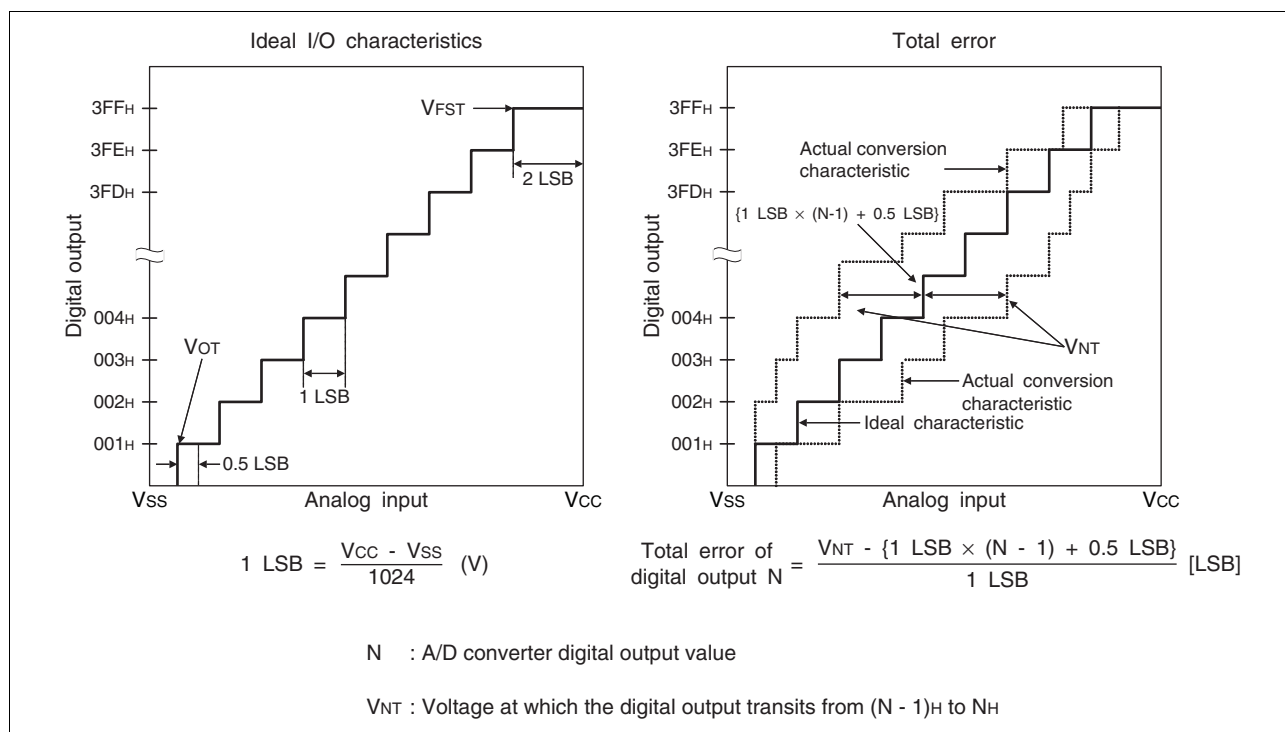
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" $\leftarrow \rightarrow$ "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" $\leftarrow \rightarrow$ "11 1111 1110") of the same device.

- Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

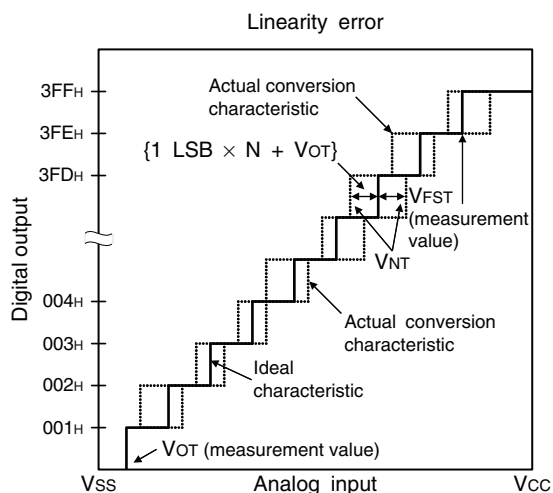
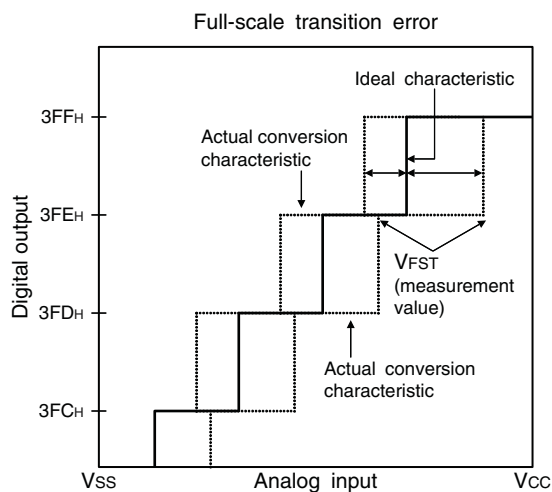
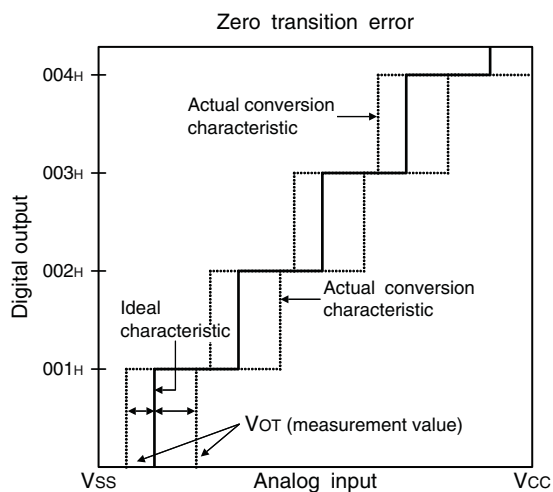
- Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.

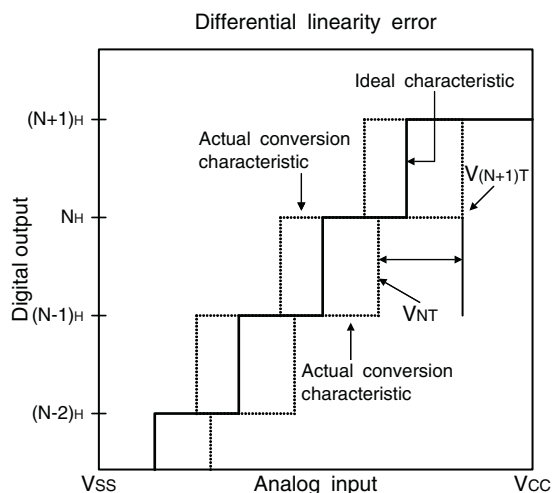


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$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + VOT\}}{1 \text{ LSB}}$$



$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D converter digital output value

VNT : Voltage at which the digital output transits from (N - 1)H to NH

VOT (ideal value) = Vss + 0.5 LSB [V]

VFST (ideal value) = Vcc - 2 LSB [V]

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6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.3 ^{*1}	1.6	s	The time of writing 00 _H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.6 ^{*1}	3.1	s	The time of writing 00 _H prior to erasure is excluded.
Byte writing time	—	17	272	μs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	2.4	—	5.5	V	
Flash memory data retention time	5 ^{*2}	—	—	year	Average T _A = + 85°C

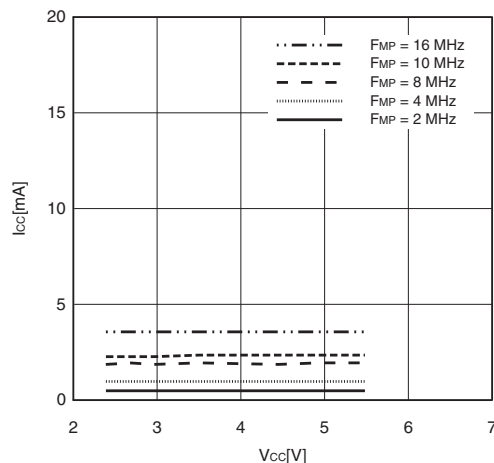
*1: V_{CC} = 5.5 V, T_A = + 25°C, 0 cycle

*2: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being + 85°C).

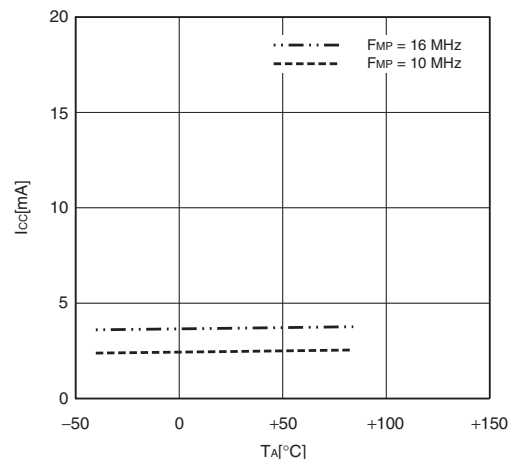
■ SAMPLE CHARACTERISTICS

- Power supply current temperature characteristics

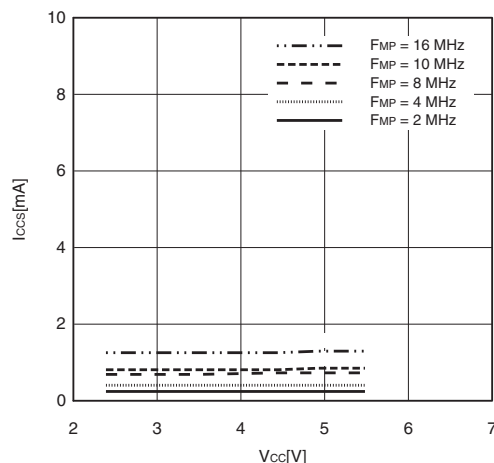
$I_{CC} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MP} = 2, 4, 8, 10, 16$ MHz (divided by 2)
 Main clock mode with the external clock operating



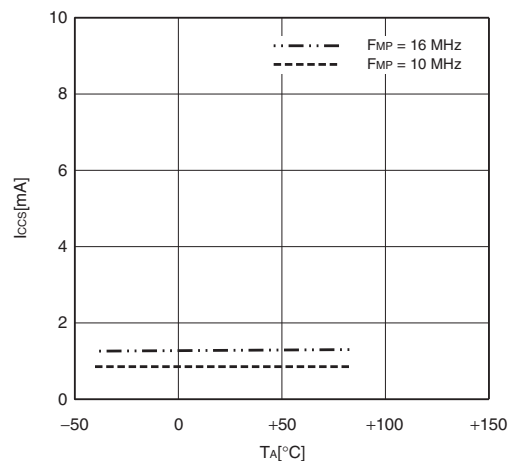
$I_{CC} - T_A$
 $V_{CC} = 5.5$ V, $F_{MP} = 10, 16$ MHz (divided by 2)
 Main clock mode with the external clock operating



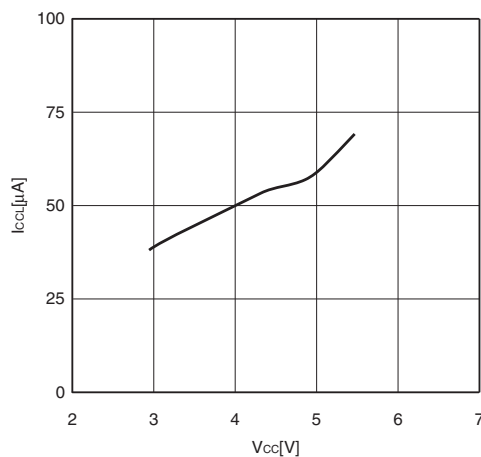
$I_{CCS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MP} = 2, 4, 8, 10, 16$ MHz (divided by 2)
 Main sleep mode with the external clock operating



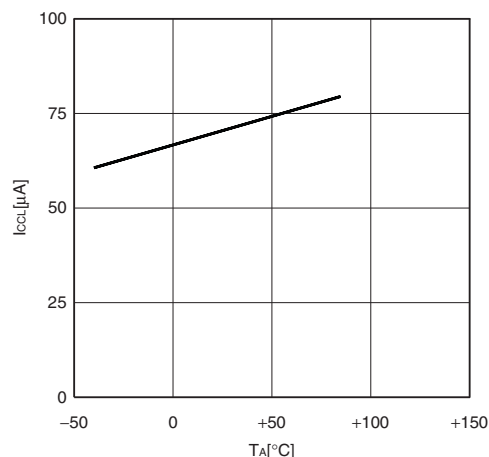
$I_{CCS} - T_A$
 $V_{CC} = 5.5$ V, $F_{MP} = 10, 16$ MHz (divided by 2)
 Main sleep mode with the external clock operating



$I_{CCL} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MPL} = 16$ kHz (divided by 2)
 Subclock mode with the external clock operating



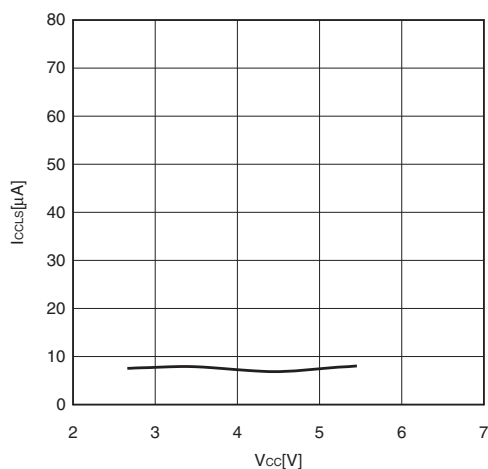
$I_{CCL} - T_A$
 $V_{CC} = 5.5$ V, $F_{MPL} = 16$ kHz (divided by 2)
 Subclock mode with the external clock operating



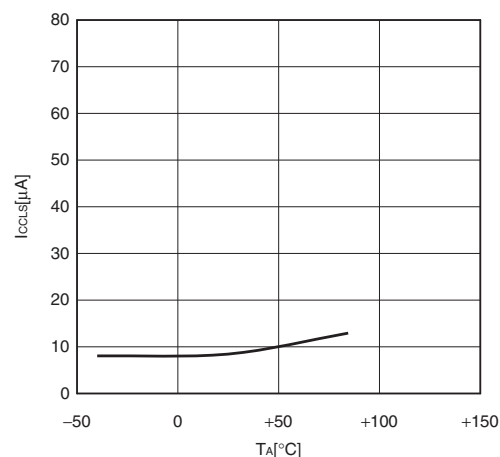
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MB95560H/570H/580H Series

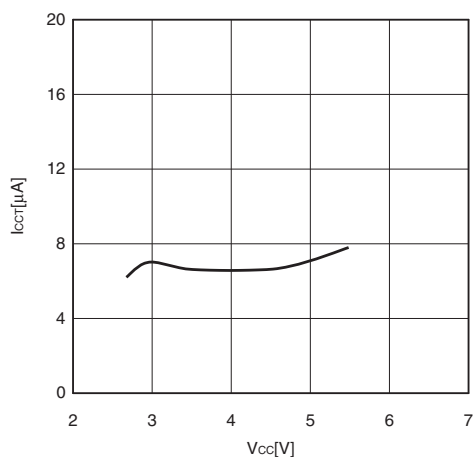
$I_{CCLS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MPL} = 16 \text{ kHz}$ (divided by 2)
 Subsleep mode with the external clock operating



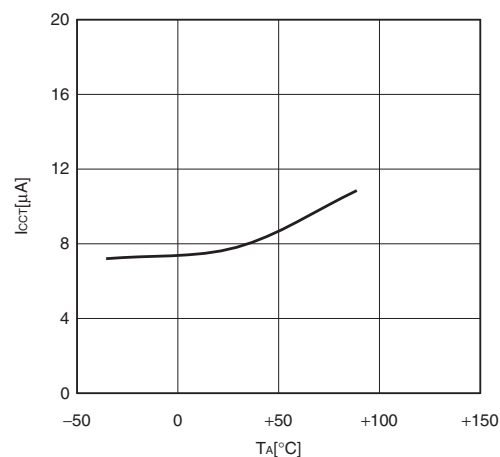
$I_{CCLS} - T_A$
 $V_{CC} = 5.5 \text{ V}$, $F_{MPL} = 16 \text{ kHz}$ (divided by 2)
 Subsleep mode with the external clock operating



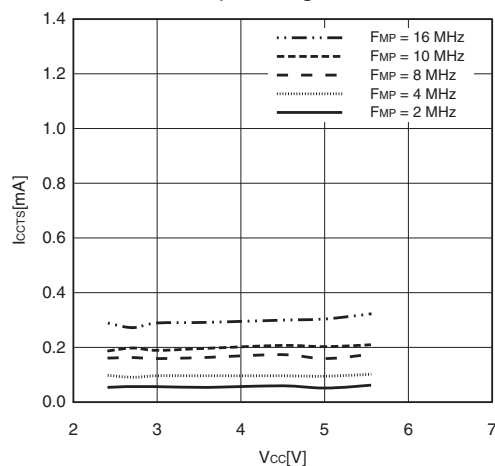
$I_{CCT} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MPL} = 16 \text{ kHz}$ (divided by 2)
 Watch mode with the external clock operating



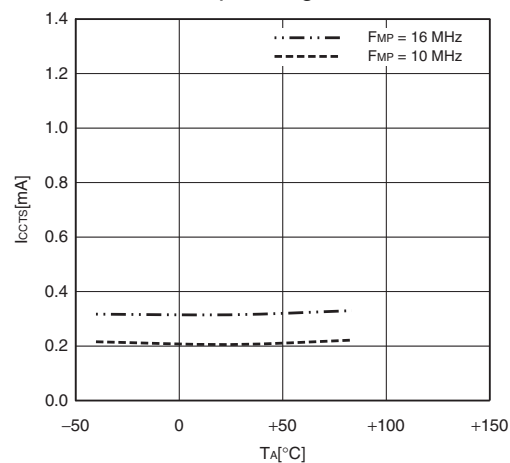
$I_{CCT} - T_A$
 $V_{CC} = 5.5 \text{ V}$, $F_{MPL} = 16 \text{ kHz}$ (divided by 2)
 Watch mode with the external clock operating



$I_{CCTS} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MP} = 2, 4, 8, 10, 16 \text{ MHz}$ (divided by 2)
 Time-base timer mode with the external clock operating



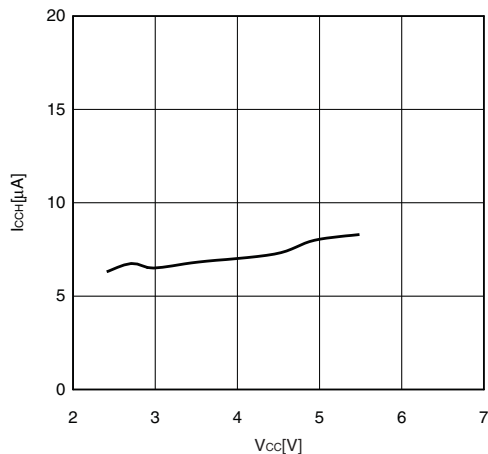
$I_{CCTS} - T_A$
 $V_{CC} = 5.5 \text{ V}$, $F_{MP} = 10, 16 \text{ MHz}$ (divided by 2)
 Time-base timer mode with the external clock operating



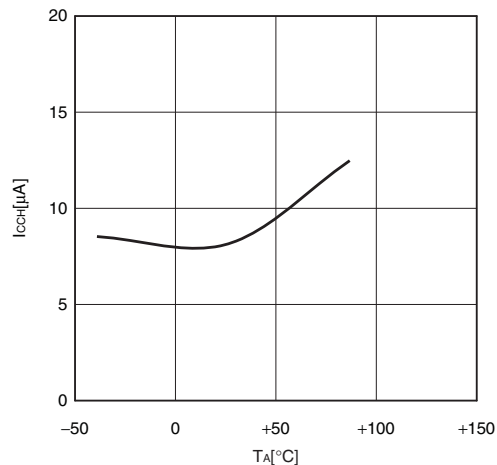
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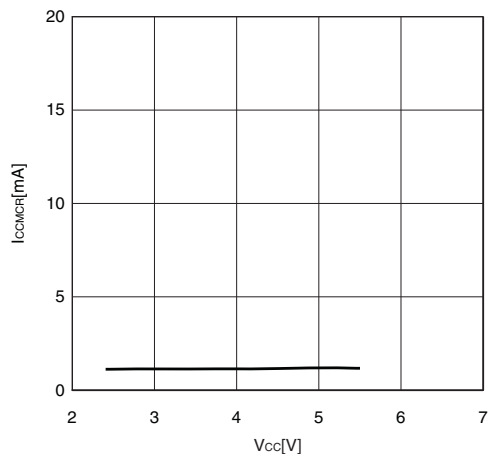
$I_{CCH} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MPL} = (\text{stop})$
 Substop mode with the external clock stopping



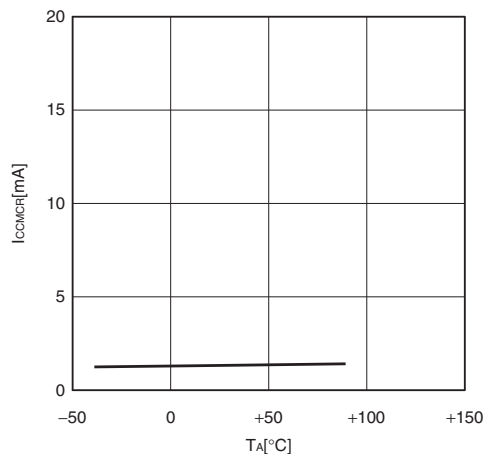
$I_{CCH} - T_A$
 $V_{CC} = 5.5 \text{ V}$, $F_{MPL} = (\text{stop})$
 Substop mode with the external clock stopping



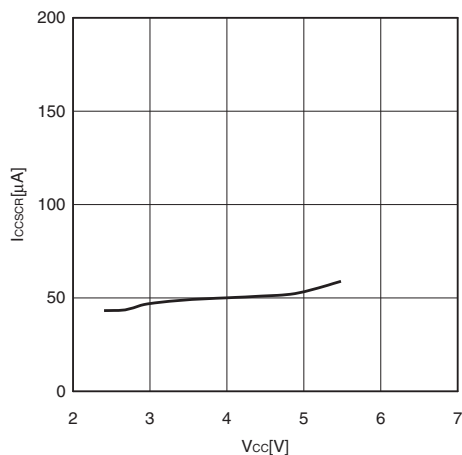
$I_{CCMCR} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MP} = 4 \text{ MHz}$ (no division)
 Main clock mode with the main CR clock operating



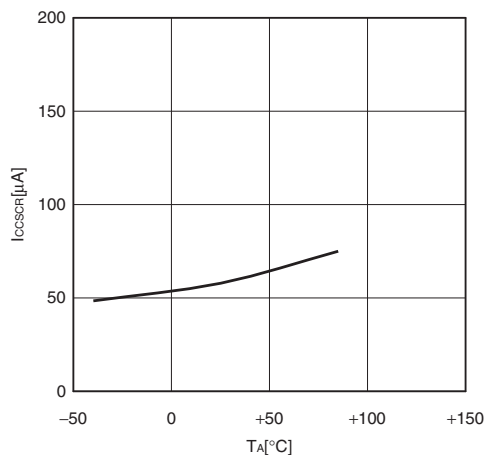
$I_{CCMCR} - T_A$
 $V_{CC} = 5.5 \text{ V}$, $F_{MP} = 4 \text{ MHz}$ (no division)
 Main clock mode with the main CR clock operating



$I_{CCSCR} - V_{CC}$
 $T_A = +25^\circ\text{C}$, $F_{MPL} = 50 \text{ kHz}$ (divided by 2)
 Subclock mode with the sub-CR clock operating

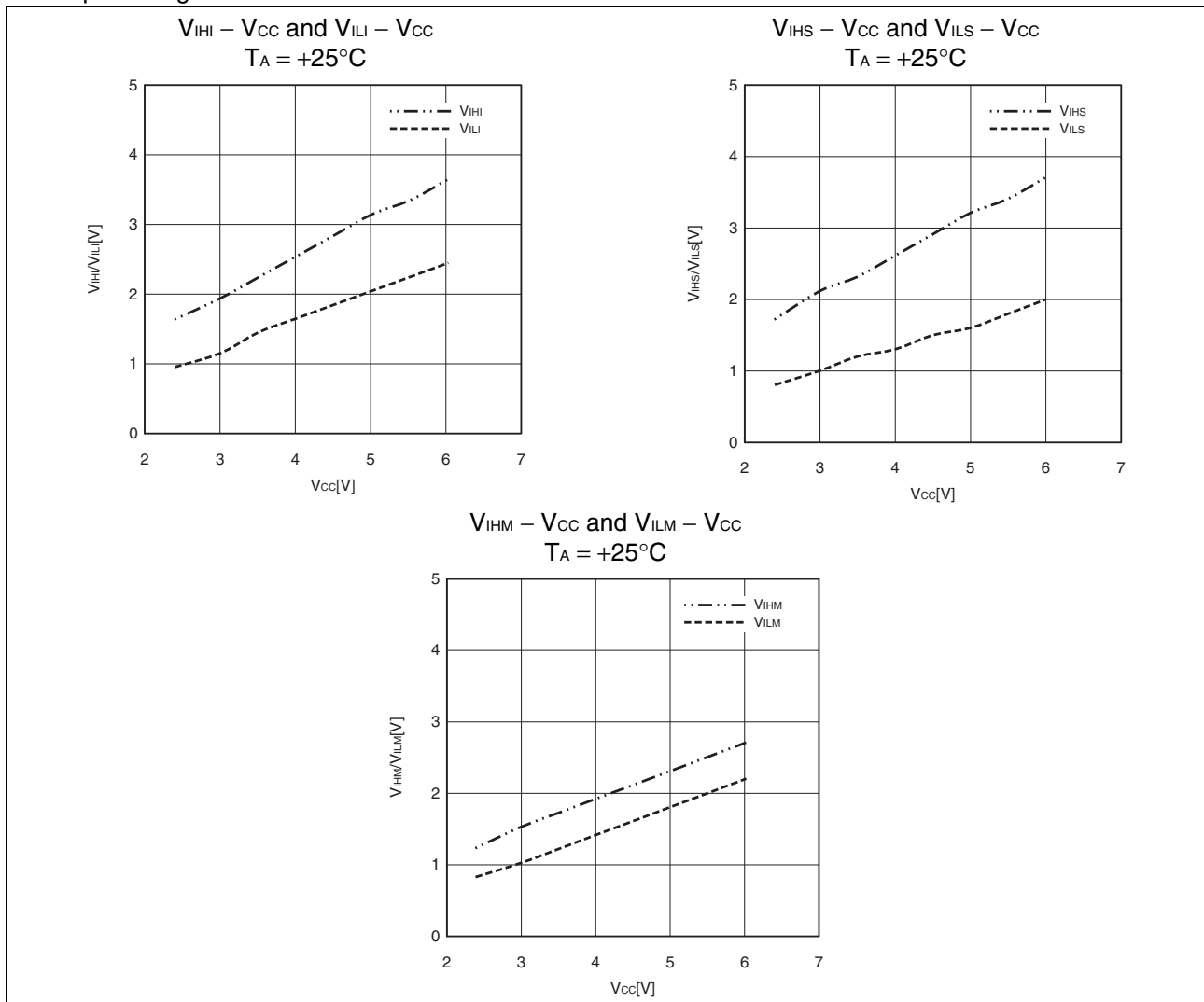


$I_{CCSCR} - T_A$
 $V_{CC} = 5.5 \text{ V}$, $F_{MPL} = 50 \text{ kHz}$ (divided by 2)
 Subclock mode with the sub-CR clock operating

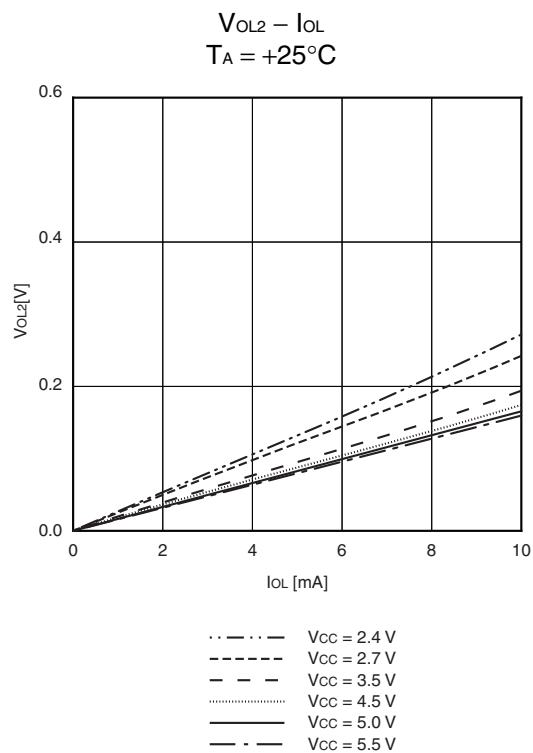
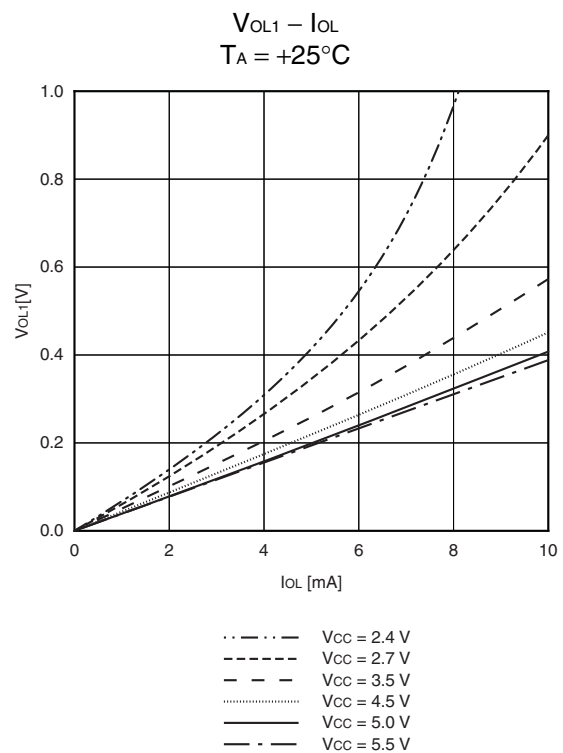
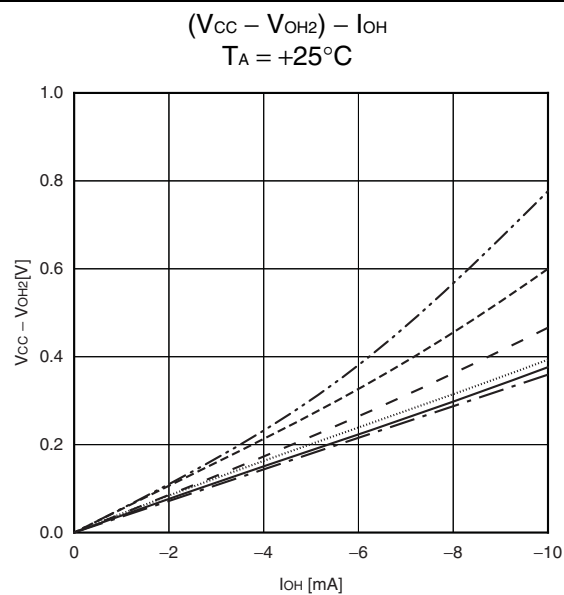
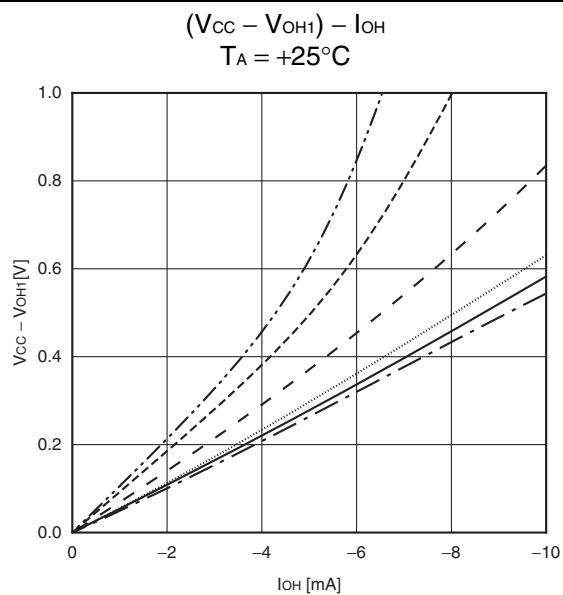


MB95560H/570H/580H Series

- Input voltage characteristics

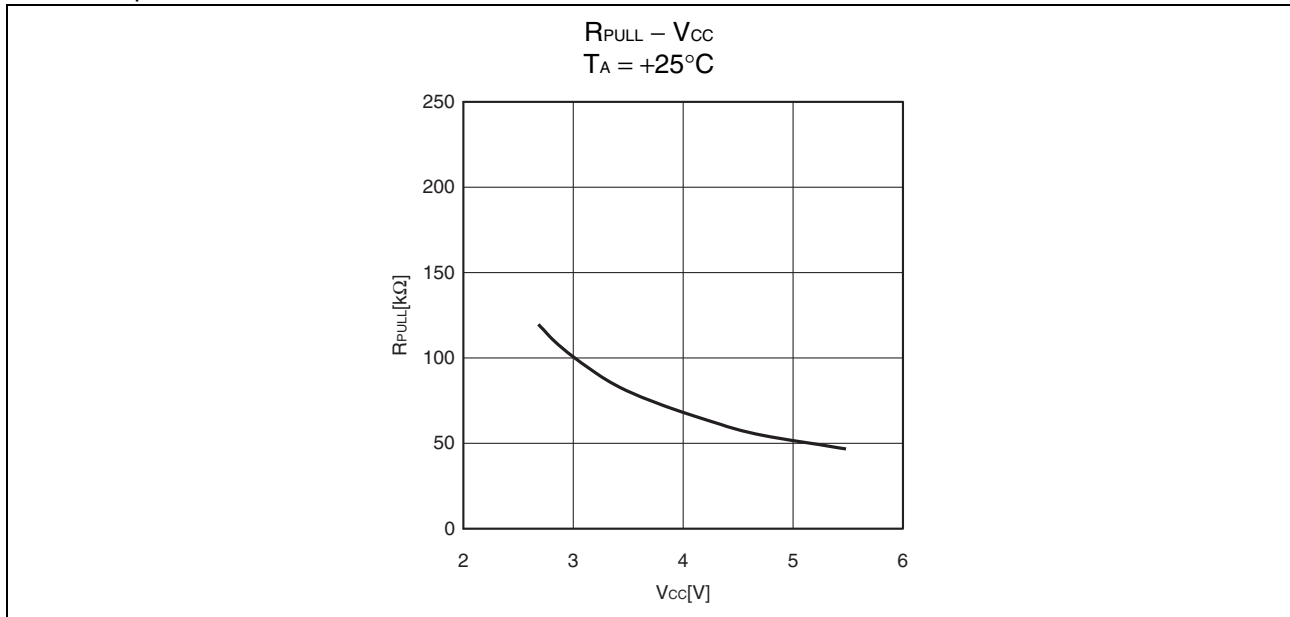


• Output voltage characteristics



MB95560H/570H/580H Series

- Pull-up characteristics



MB95560H/570H/580H Series

■ MASK OPTIONS

No.	Part Number	MB95F562H MB95F563H MB95F564H MB95F572H MB95F573H MB95F574H MB95F582H MB95F583H MB95F584H	MB95F562K MB95F563K MB95F564K MB95F572K MB95F573K MB95F574K MB95F582K MB95F583K MB95F584K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

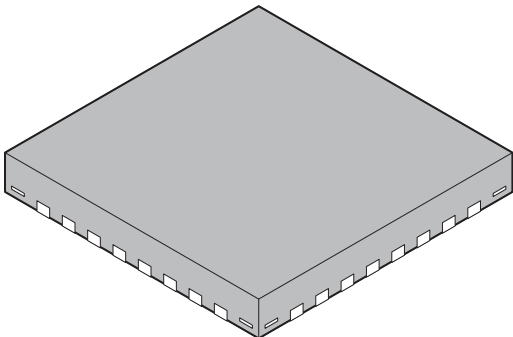
MB95560H/570H/580H Series

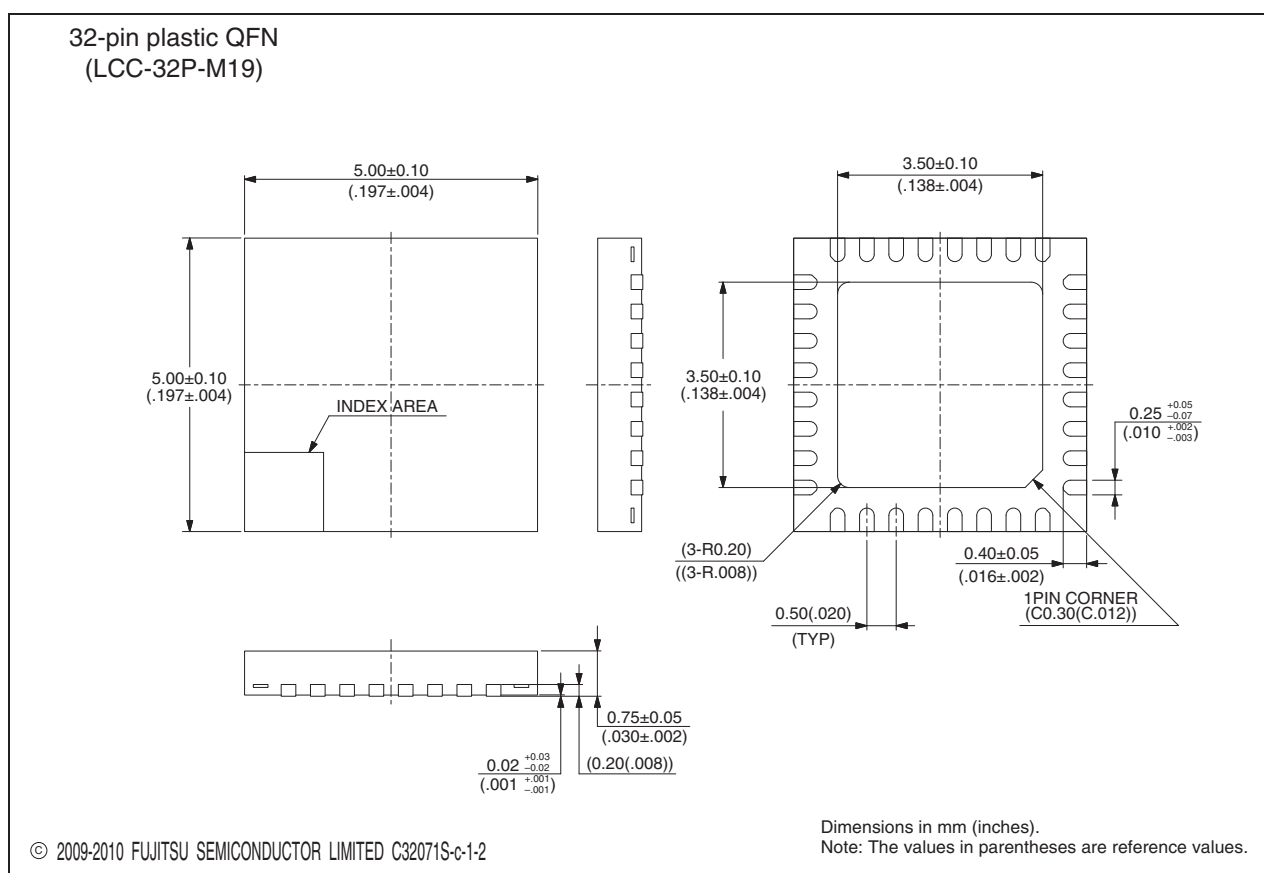
■ ORDERING INFORMATION

Part Number	Package
MB95F562HWQN-G-JNE1 MB95F562HWQN-G-JNERE1 MB95F562KWQN-G-JNE1 MB95F562KWQN-G-JNERE1 MB95F563HWQN-G-JNE1 MB95F563HWQN-G-JNERE1 MB95F563KWQN-G-JNE1 MB95F563KWQN-G-JNERE1 MB95F564HWQN-G-JNE1 MB95F564HWQN-G-JNERE1 MB95F564KWQN-G-JNE1 MB95F564KWQN-G-JNERE1	32-pin plastic QFN (LCC-32P-M19)
MB95F562HPF-G-JNE2 MB95F562KPF-G-JNE2 MB95F563HPF-G-JNE2 MB95F563KPF-G-JNE2 MB95F564HPF-G-JNE2 MB95F564KPF-G-JNE2	20-pin plastic SOP (FPT-20P-M09)
MB95F562HPFT-G-JNE2 MB95F562KPFT-G-JNE2 MB95F563HPFT-G-JNE2 MB95F563KPFT-G-JNE2 MB95F564HPFT-G-JNE2 MB95F564KPFT-G-JNE2	20-pin plastic TSSOP (FPT-20P-M10)
MB95F582HWQN-G-JNE1 MB95F582HWQN-G-JNERE1 MB95F582KWQN-G-JNE1 MB95F582KWQN-G-JNERE1 MB95F583HWQN-G-JNE1 MB95F583HWQN-G-JNERE1 MB95F583KWQN-G-JNE1 MB95F583KWQN-G-JNERE1 MB95F584HWQN-G-JNE1 MB95F584HWQN-G-JNERE1 MB95F584KWQN-G-JNE1 MB95F584KWQN-G-JNERE1	32-pin plastic QFN (LCC-32P-M19)
MB95F582HPFT-G-JNE2 MB95F582KPFT-G-JNE2 MB95F583HPFT-G-JNE2 MB95F583KPFT-G-JNE2 MB95F584HPFT-G-JNE2 MB95F584KPFT-G-JNE2	16-pin plastic TSSOP (FPT-16P-M08)
MB95F582HPF-G-JNE2 MB95F582KPF-G-JNE2 MB95F583HPF-G-JNE2 MB95F583KPF-G-JNE2 MB95F584HPF-G-JNE2 MB95F584KPF-G-JNE2	16-pin plastic SOP (FPT-16P-M23)
MB95F572HPF-G-JNE2 MB95F572KPF-G-JNE2 MB95F573HPF-G-JNE2 MB95F573KPF-G-JNE2 MB95F574HPF-G-JNE2 MB95F574KPF-G-JNE2	8-pin plastic SOP (FPT-8P-M08)

MB95560H/570H/580H Series

■ PACKAGE DIMENSION

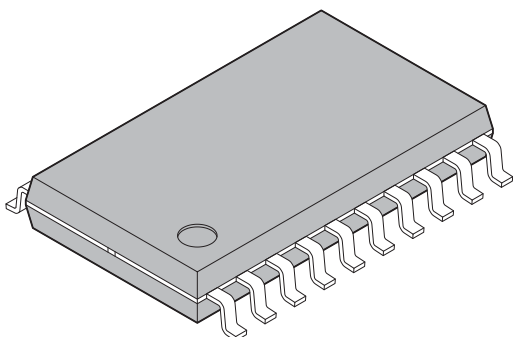
<p>32-pin plastic QFN</p>  <p>(LCC-32P-M19)</p>	Lead pitch	0.50 mm
	Package width × package length	5.00 mm × 5.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.06 g

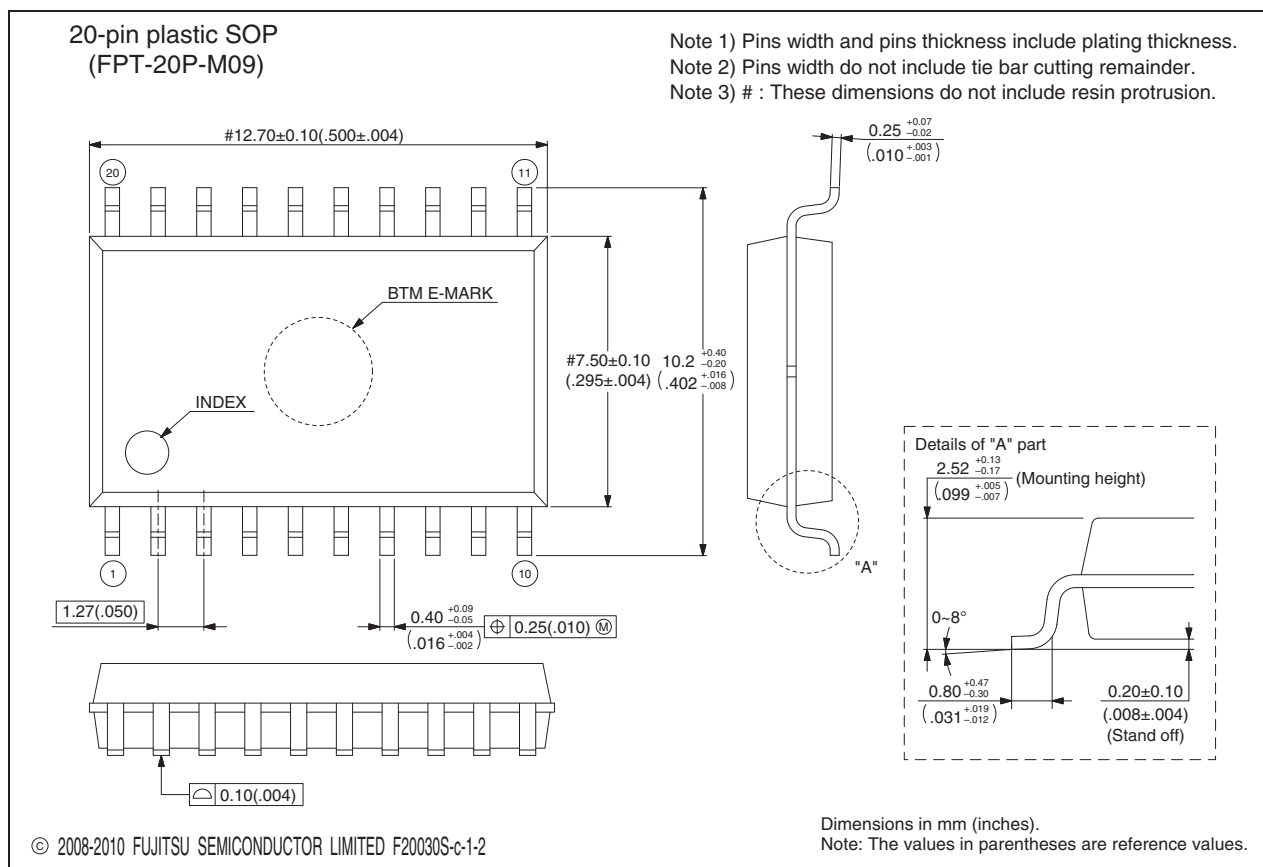


Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

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MB95560H/570H/580H Series

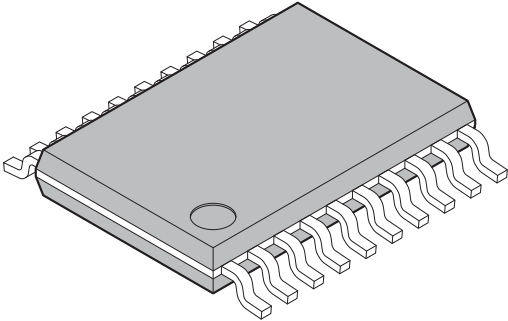
<p>20-pin plastic SOP</p>  <p>(FPT-20P-M09)</p>	Lead pitch	1.27 mm
	Package width × package length	7.50 mm × 12.70 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.65 mm Max

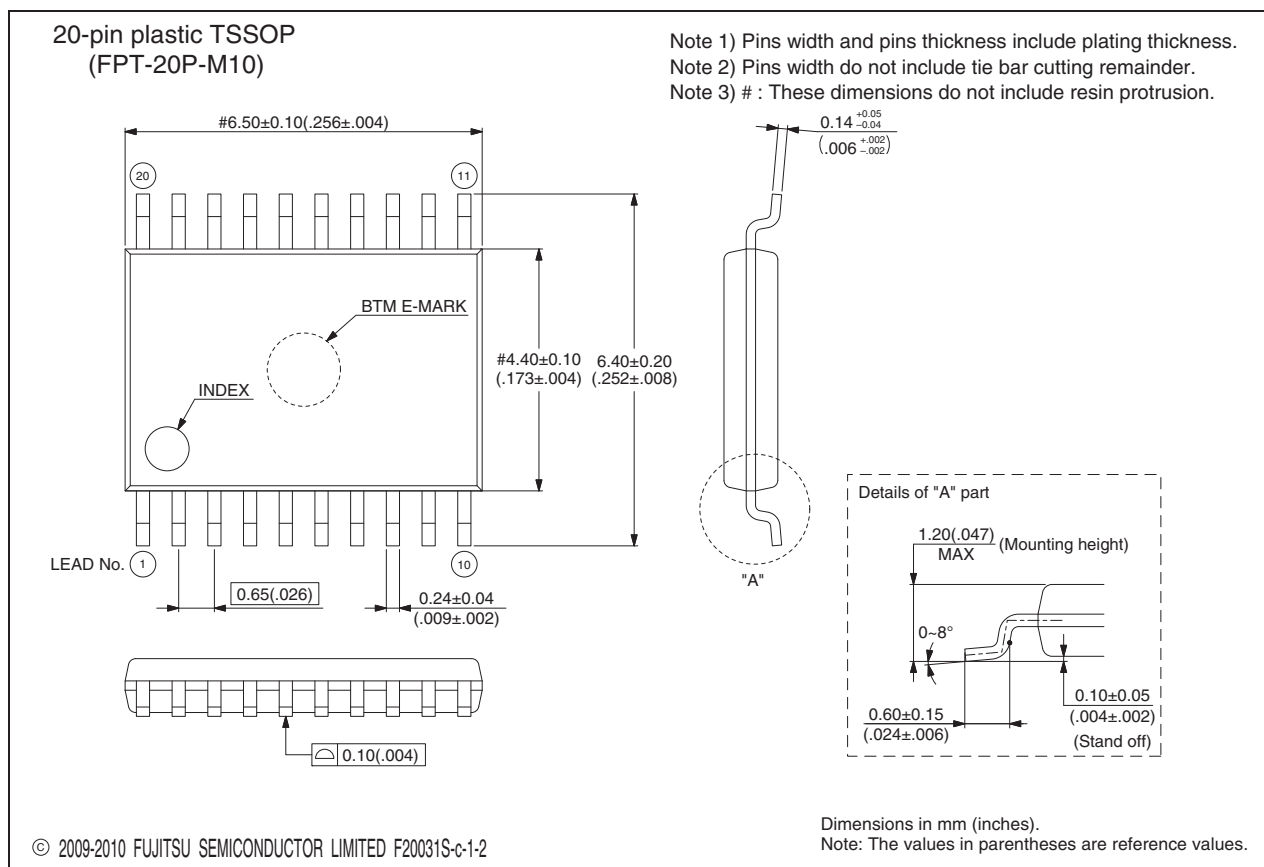


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<http://edevic.fujitsu.com/package/en-search/>

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MB95560H/570H/580H Series

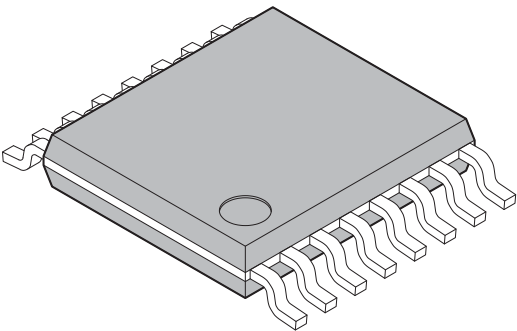
<p>20-pin plastic TSSOP</p>  <p>(FPT-20P-M10)</p>	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 6.50 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.08 g

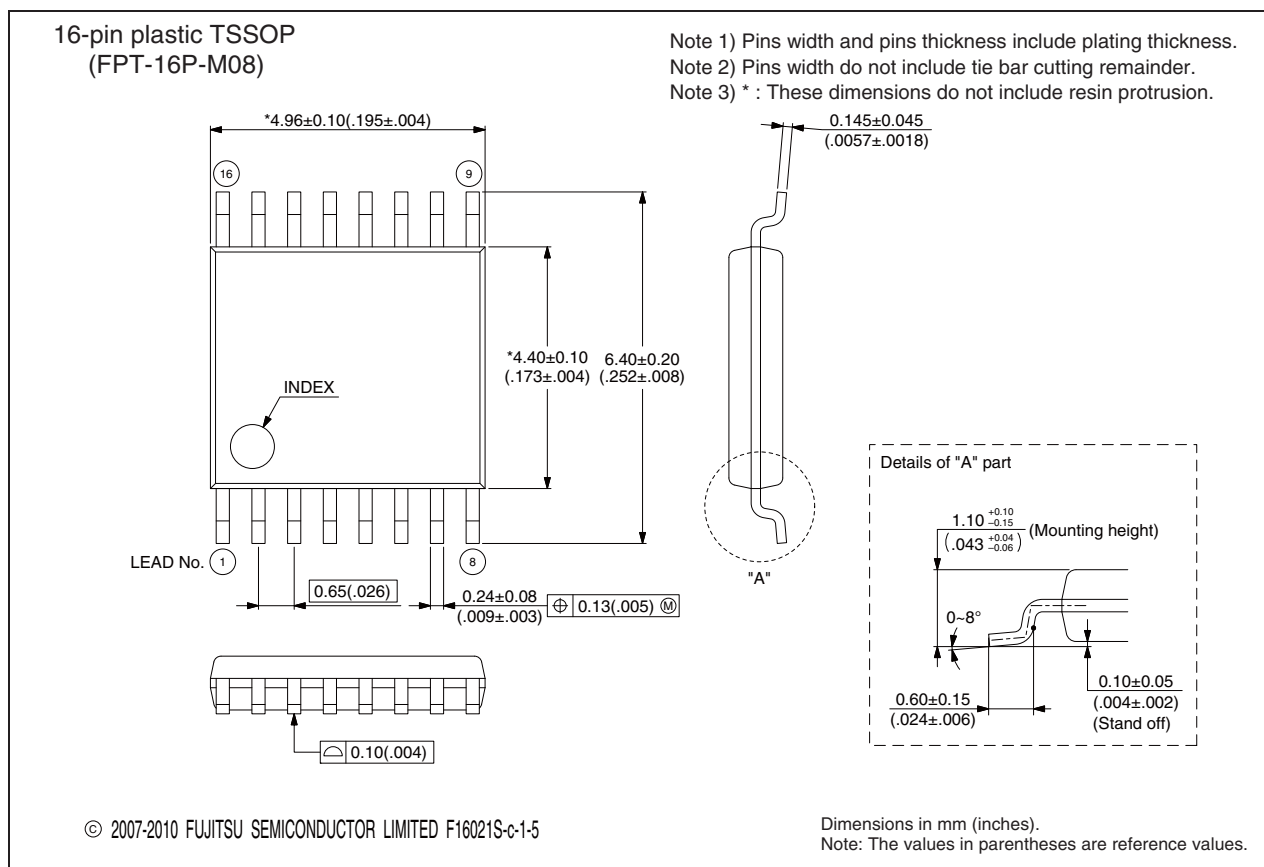


Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

MB95560H/570H/580H Series

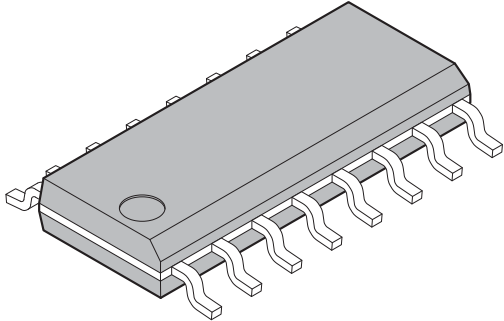
 <p>16-pin plastic TSSOP</p> <p>(FPT-16P-M08)</p>	Lead pitch	0.65 mm
	Package width × package length	4.40 mm × 4.96 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm Max
	Weight	0.06 g

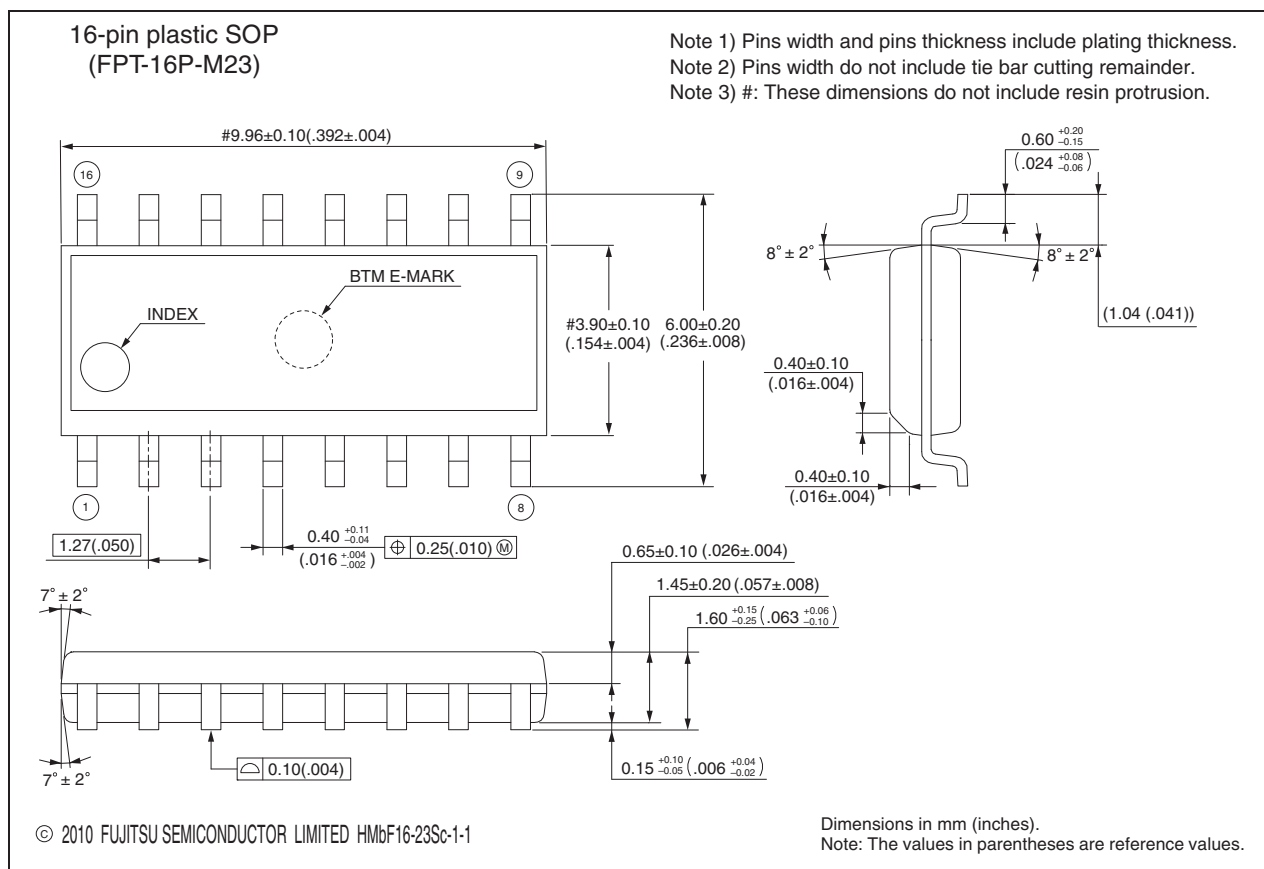


Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

MB95560H/570H/580H Series

 <p>16-pin plastic SOP</p> <p>(FPT-16P-M23)</p>	Lead pitch	1.27 mm
	Package width × package length	3.90 mm × 9.96 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.12 g

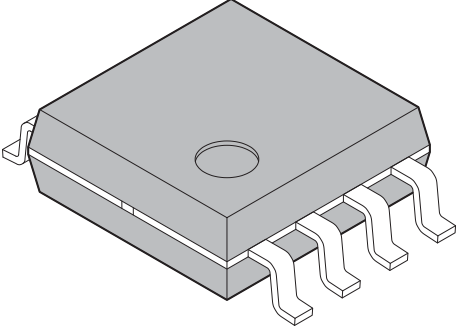


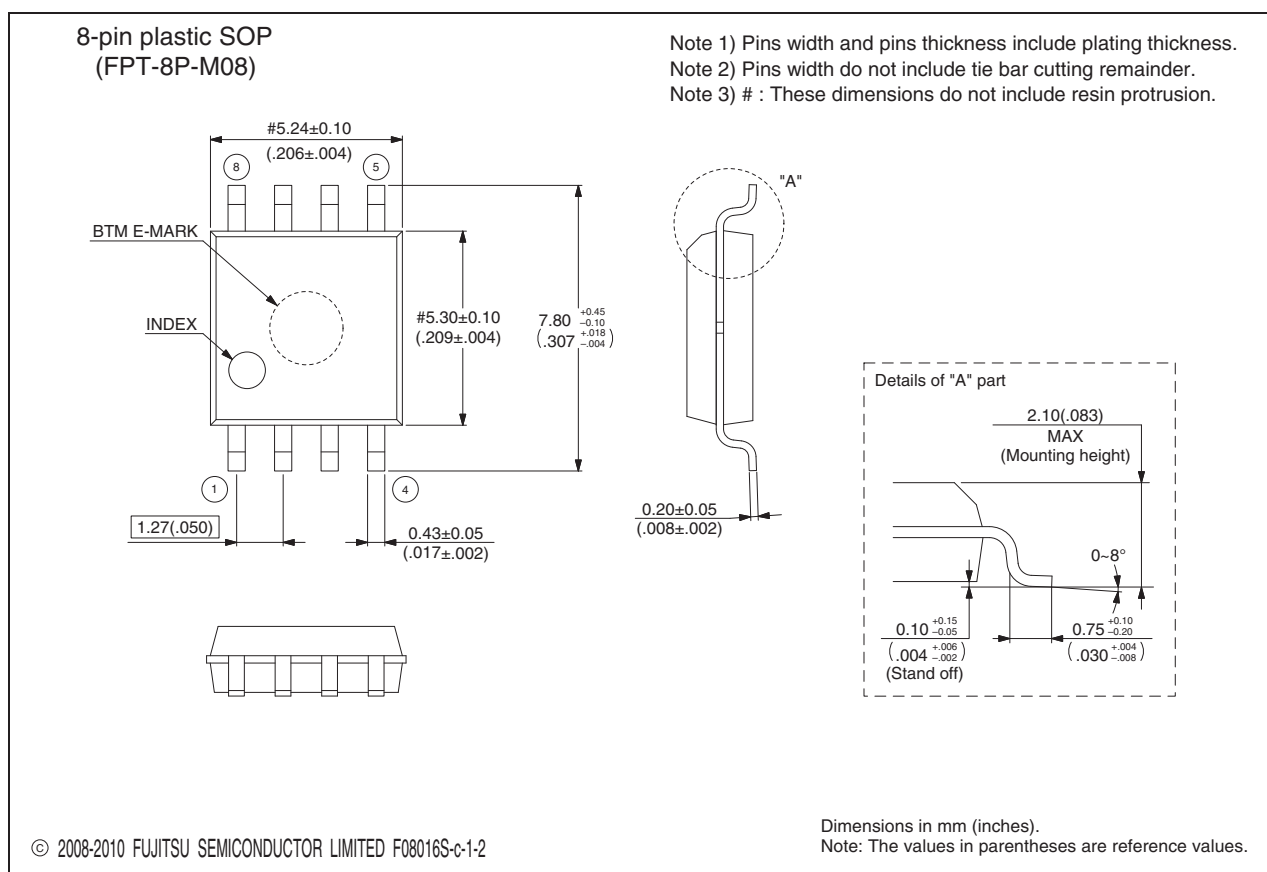
Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

(Continued)

MB95560H/570H/580H Series

(Continued)

<p>8-pin plastic SOP</p>  <p>(FPT-8P-M08)</p>	Lead pitch	1.27 mm
	Package width × package length	5.30 mm × 5.24 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	2.10 mm Max



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MB95560H/570H/580H Series

■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Details
2	■ FEATURES	Added “• Power-on reset”.
3	■ PRODUCT LINE-UP • MB95560H Series	Added the parameter “Power-on reset”.
5	■ PRODUCT LINE-UP • MB95570H Series	Added the parameter “Power-on reset”.
6	■ PRODUCT LINE-UP • MB95580H Series	Added the parameter “Power-on reset”.

MB95560H/570H/580H Series

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan

Tel: +81-45-415-5858

<http://jp.fujitsu.com/fsl/en/>

For further information please contact:

North and South America

FUJITSU SEMICONDUCTOR AMERICA, INC.

1250 E. Arques Avenue, M/S 333

Sunnyvale, CA 94085-5401, U.S.A.

Tel: +1-408-737-5600 Fax: +1-408-737-5999

<http://us.fujitsu.com/micro/>

Europe

FUJITSU SEMICONDUCTOR EUROPE GmbH

Pittlerstrasse 47, 63225 Langen, Germany

Tel: +49-6103-690-0 Fax: +49-6103-690-122

<http://emea.fujitsu.com/semiconductor/>

Korea

FUJITSU SEMICONDUCTOR KOREA LTD.

902 Kosmo Tower Building, 1002 Daechi-Dong,

Gangnam-Gu, Seoul 135-280, Republic of Korea

Tel: +82-2-3484-7100 Fax: +82-2-3484-7111

<http://kr.fujitsu.com/fsk/>

Asia Pacific

FUJITSU SEMICONDUCTOR ASIA PTE. LTD.

151 Lorong Chuan,

#05-08 New Tech Park 556741 Singapore

Tel: +65-6281-0770 Fax: +65-6281-0220

<http://sg.fujitsu.com/semiconductor/>

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),

Shanghai 200002, China

Tel: +86-21-6146-3688 Fax: +86-21-6335-1605

<http://cn.fujitsu.com/fss/>

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,

Tsimshatsui, Kowloon, Hong Kong

Tel: +852-2377-0226 Fax: +852-2376-3269

<http://cn.fujitsu.com/fsp/>

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