Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

ABSOLUTE MAXIMUM RATINGS

V_{CC}, IN1, IN2, PAEN, RFEN1, RFEN2, REFIN, OUT2, REFBP to AGND .....-0.3V to +6.0V
PAOUT to AGND.....-0.3V to (V_{IN1} + 0.3V)
LDO to AGND .....-0.3V to (V_{OUT2} + 0.3V)
IN1, IN2 to V_{CC}.....-0.3V to +0.3V
IN1 to IN2 .....-0.3V to +0.3V
PGND1, PGND2 to AGND.....-0.3V to +0.3V
LX1 Current .....1A_{RMS}
LX2 Current .....1A_{RMS}
IN1 and PAOUT Current.....1A_{RMS}
PAOUT, OUT2, LDO Short Circuit to PGND1, PGND2 .....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Bump UCSP (derate 12.5mW/°C above +70°C) 1W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)...96°C/W
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Bump Temperature (soldering, reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{IN1} = V_{IN2} = V_{PAEN} = V_{RFEN1} = V_{RFEN2} = 3.6V, V_{REFIN} = 0.72V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage	V_{CC}, V_{IN1}, V_{IN2}		2.7		5.5	V
Input Undervoltage Threshold	V_{CC} rising, 180mV typical hysteresis		2.52	2.63	2.70	V
Shutdown Supply Current	V_{PAEN} = V_{RFEN1} = V_{RFEN2} = 0	T_A = +25°C		0.1	4	µA
		T_A = +85°C		0.1		
LOGIC CONTROL						
PAEN, RFEN1, RFEN2 Logic Input High Voltage	2.7V ≤ V_{CC} ≤ 5.5V		1.3			V
PAEN, RFEN1, RFEN2 Logic Input Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V				0.4	V
PAEN, RFEN1, RFEN2 Internal Pulldown Resistor			400	800	1600	kΩ
PAEN, RFEN1, RFEN2 Logic Input Current	V_{IL} = 0	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
REFBP						
REFBP Output Voltage	0µA ≤ IREFBP ≤ 1µA		1.237	1.250	1.263	V
THERMAL PROTECTION						
Thermal Shutdown	T_A rising, 20°C typical hysteresis			+160		°C
OUT1						
Quiescent Supply Current	VRFEN1 = VRFEN2 = 0V, IPA = 0A, no switching			155		µA
On-Resistance	p-channel MOSFET switch, I_{LX1} = -200mA			0.16	0.40	Ω
	n-channel MOSFET rectifier, I_{LX1} = 500mA			0.17	0.40	
Load Regulation	R_L is the inductor resistance			R_L/2		V/A
LX1 Leakage Current	V_{IN1} = 5.5V, V_{LX1} = 0V	T_A = +25°C		0.1	5	µA
		T_A = +85°C		1		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{IN1} = V_{IN2} = V_{PAEN} = V_{RFEN1} = V_{RFEN2} = 3.6V, V_{REFIN} = 0.72V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Peak Current Limit (p-Channel MOSFET)			1200	1450	1700	mA
Valley Current Limit (n-Channel MOSFET)			1100	1350	1600	mA
Minimum On-Time				70		ns
Minimum Off-Time				50		ns
Power-Up Delay	From V_{PAEN} rising to V_{LX1} rising			50	75	µs
OUT1 REFIN						
Common-Mode Range			0.2		1.7	V
REFIN-to-PAOUT Gain	V_{REFIN} = 0.32V or 1.32V, I_{LX1} = 0A		2.45	2.5	2.55	
Input Resistance				320		kΩ
BYPASS						
Bypass Mode Threshold	V_{REFIN} falling, 150mV hysteresis			0.396 xV_{CC}		V
On-Resistance	p-channel MOSFET I_{OUT} = -90mA	T_A = +25°C		0.14		Ω
		T_A = +85°C		0.3		
Bypass Current Limit	V_{PAOUT} = 1.5V		700	1000	1400	mA
Step-Down Current Limit in Bypass			1200	1450	1700	mA
Total Bypass Current Limit	V_{PAOUT} = V_{LX1} = 1.5V		1900	2450	3100	mA
Bypass Off-Leakage Current	V_{CC} = V_{IN1} = 5.5V, V_{PAOUT} = 0V	T_A = +25°C		0.01	5	µA
		T_A = +85°C		1		
OUT2						
Output Voltage	I_{OUT2} = 0 to 150mA, V_{IN2} = V_{CC} = 3.2V to 4.5V		3.038	3.1	3.162	V
OUT2 Leakage Current	V_{RFEN1} = V_{RFEN2} = 0	T_A = +25°C		0.01	5	µA
		T_A = +85°C		0.1		
No-Load Supply Current	V_{PAEN} = 0V, I_{OUT2} = 0A, switching			2.5		mA
On-Resistance	p-channel MOSFET switch, I_{LX2} = -40mA			300		mΩ
	n-channel MOSFET rectifier, I_{LX2} = 40mA			300		mΩ
p-Channel Current-Limit Threshold			400	450	500	mA
n-Channel Negative Current Limit				400		mA
Maximum Duty Cycle				100		%
Minimum Duty Cycle				16.5		%
PWM Frequency			1.8	2.0	2.2	MHz
Power-Up Delay	From V_{RFEN1} or V_{RFEN2} rising to V_{LX2} rising			35	75	µs

Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{IN1} = V_{IN2} = V_{PAEN} = V_{RFEN1} = V_{RFEN2} = 3.6V, V_{REFIN} = 0.72V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LDO					
Output Voltage, V_{LDO}	V_{OUT2} = 3.1V, I_{LDO} = 1mA to 200mA	2.744	2.800	2.856	V
Current Limit	V_{OUT2} = 3.1V, V_{LDO} = 0V	250	420	750	mA
Dropout Voltage	V_{OUT2} = 3.1V, I_{LDO} = 100mA		70		mV
Line Regulation	V_{OUT2} stepped from 3.5V to 5.5V, I_{LDO} = 100mA		2.4		mV
Load Regulation	V_{OUT2} = 3.1V, I_{LDO} stepped from 50µA to 200mA		25		mV
Power-Supply Rejection $\Delta V_{LDO}/\Delta V_{OUT2}$	V_{OUT2} = 3.1V, 10Hz to 10kHz, C_{LDO} = 1µF, I_{LDO} = 100mA		65		dB
Output Noise	100Hz to 100kHz, C_{LDO} = 1µF, I_{LDO} = 100mA		16		μV_{RMS}
Minimum Output Capacitance for Stable Operation	0 < I_{LDO} < 200mA		1		µF
Output Leakage Current	V_{OUT2} = 3.1V, V_{RFEN1} = V_{RFEN2} = 0V		25		nA
Power-Up Delay	From V_{RFEN1} or V_{RFEN2} rising to V_{LDO} rising		50		µs

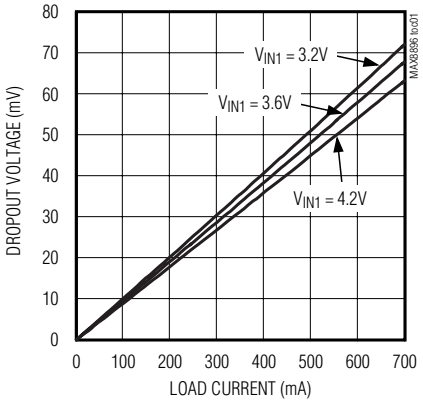
Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

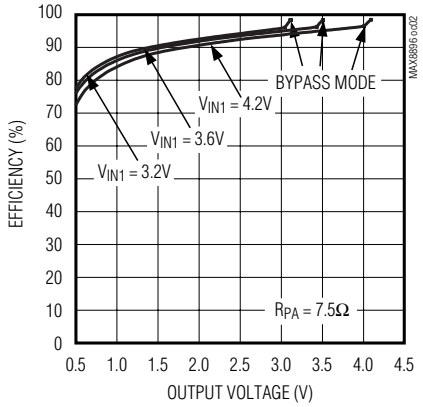
Typical Operating Characteristics

(V_{CC} = V_{IN1} = V_{IN2} = 3.6V, V_{REFIN} = 0.72V, circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

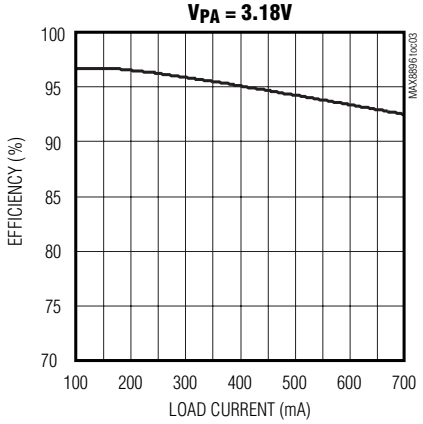
OUT1 PA BYPASS MODE DROPOUT VOLTAGE vs. PA LOAD CURRENT



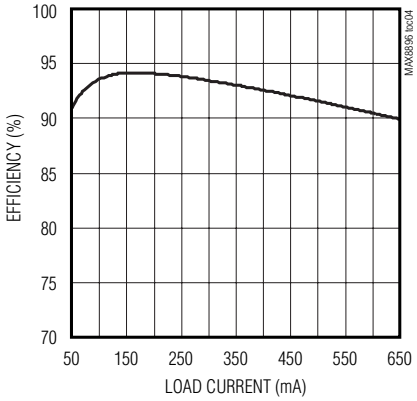
OUT1 PA STEP-DOWN CONVERTER EFFICIENCY vs. OUTPUT VOLTAGE



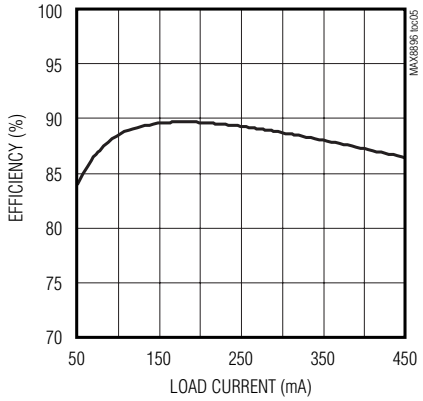
OUT1 PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT V_{PA} = 3.18V



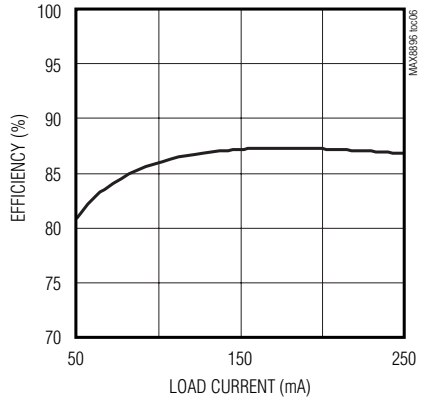
OUT1 PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT V_{PA} = 2.58V



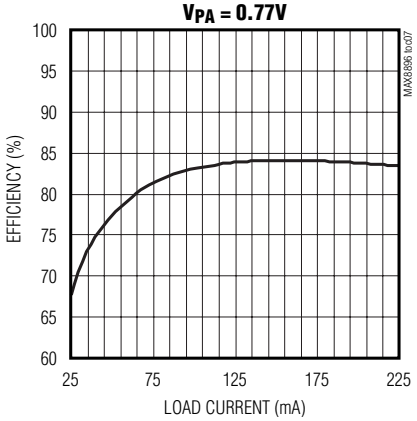
OUT1 PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT V_{PA} = 1.58V



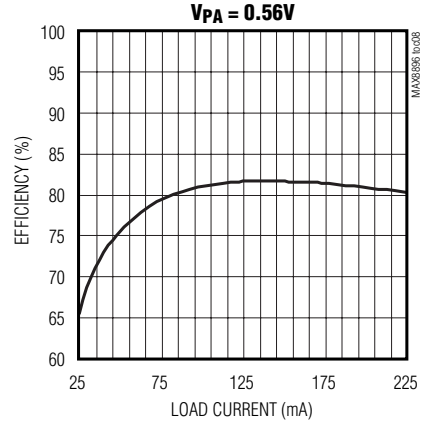
OUT1 PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT V_{PA} = 1.18V



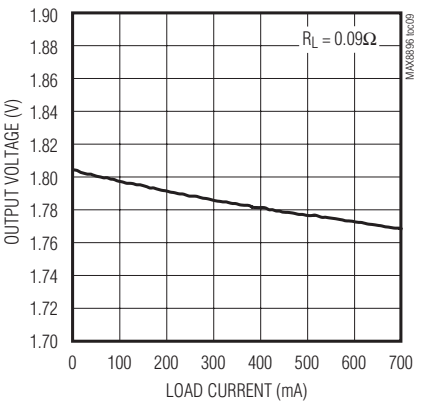
OUT1 PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT V_{PA} = 0.77V



OUT1 PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT V_{PA} = 0.56V



OUT1 PA STEP-DOWN CONVERTER OUTPUT VOLTAGE vs. LOAD CURRENT

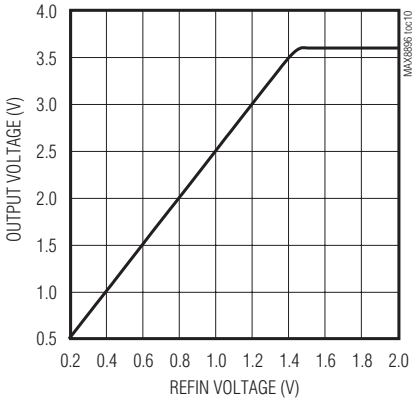


Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

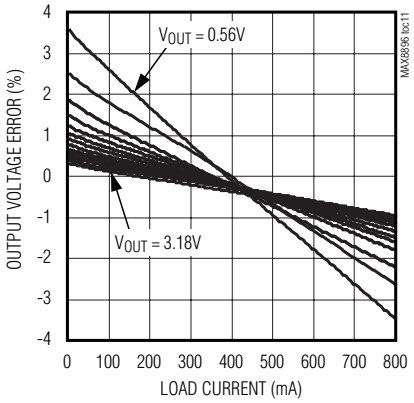
Typical Operating Characteristics (continued)

(V_{CC} = V_{IN1} = V_{IN2} = 3.6V, V_{REFIN} = 0.72V, circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

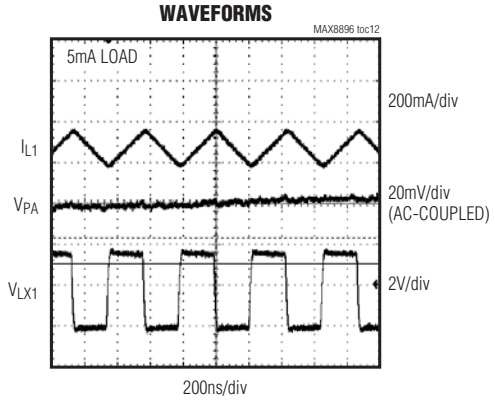
OUT1 PA STEP-DOWN CONVERTER OUTPUT VOLTAGE vs. REFIN VOLTAGE



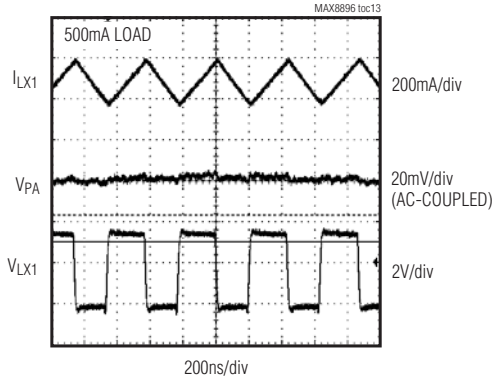
OUTPUT VOLTAGE ERROR vs. LOAD CURRENT



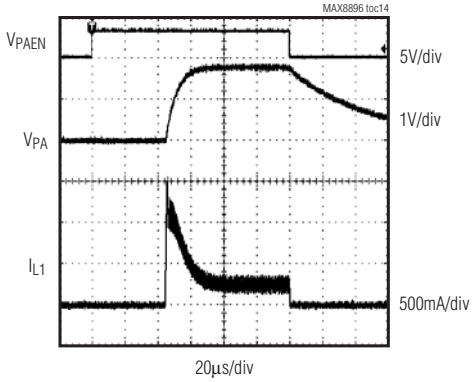
OUT1 LIGHT-LOAD SWITCHING WAVEFORMS



OUT1 HEAVY-LOAD SWITCHING WAVEFORMS



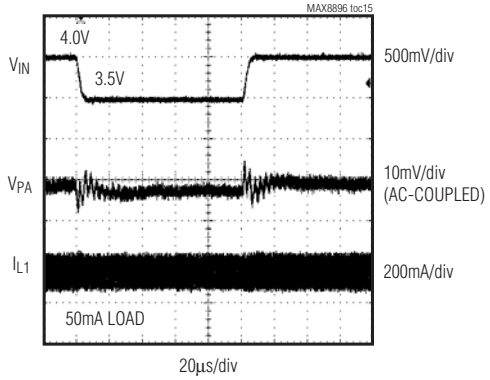
OUT1 STARTUP AND SHUTDOWN



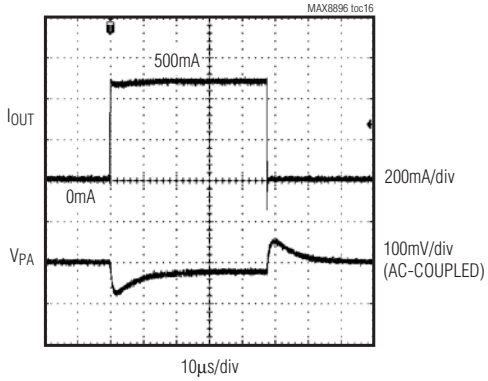
Typical Operating Characteristics (continued)

(V_{CC} = V_{IN1} = V_{IN2} = 3.6V, V_{REFIN} = 0.72V, circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

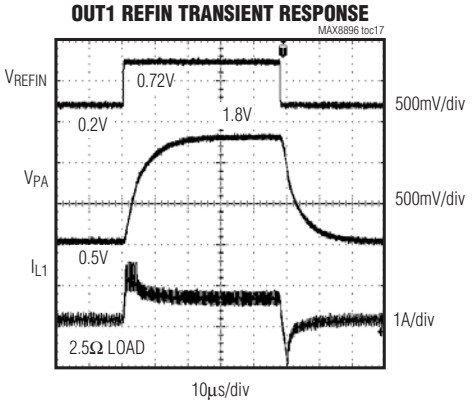
OUT1 LINE TRANSIENT RESPONSE



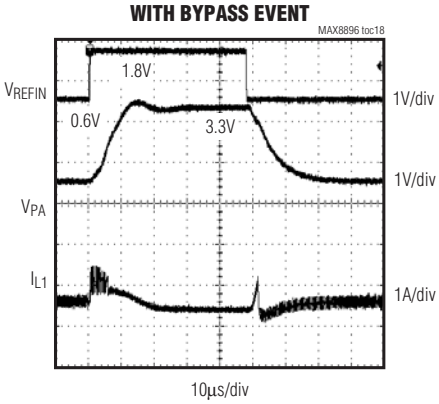
OUT1 LOAD TRANSIENT RESPONSE



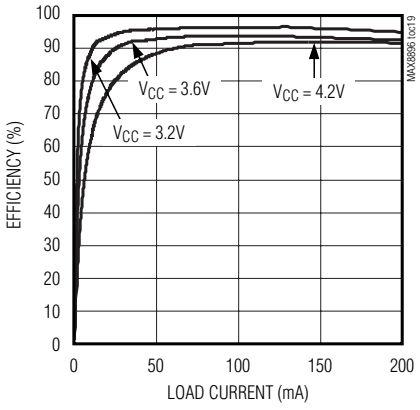
OUT1 REFIN TRANSIENT RESPONSE



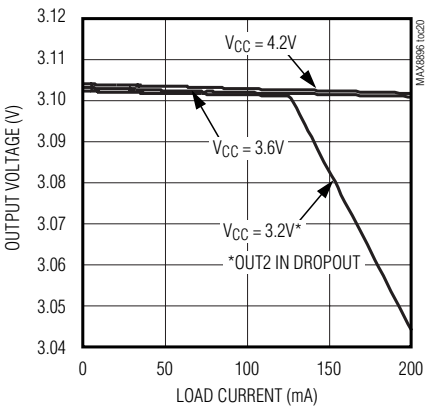
OUT1 REFIN TRANSIENT RESPONSE WITH BYPASS EVENT



OUT2 EFFICIENCY vs. LOAD CURRENT



OUT2 VOLTAGE vs. LOAD CURRENT

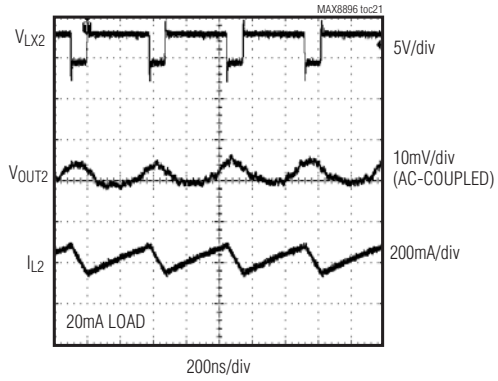


Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

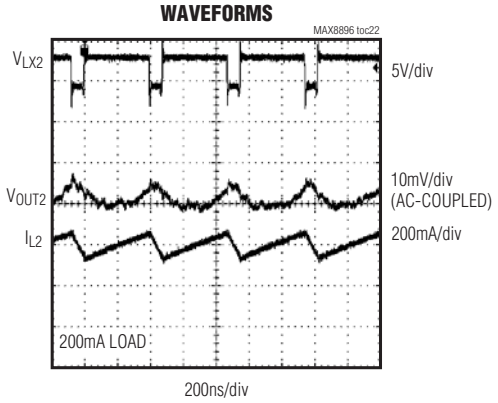
Typical Operating Characteristics (continued)

(V_{CC} = V_{IN1} = V_{IN2} = 3.6V, V_{REFIN} = 0.72V, circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

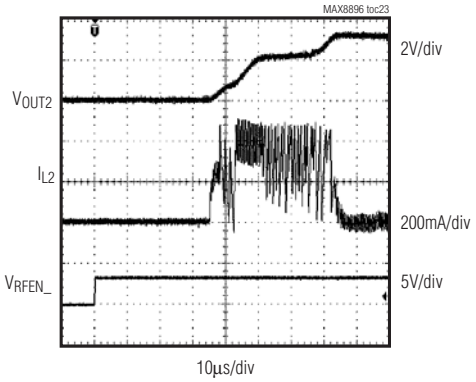
OUT2 LIGHT-LOAD SWITCHING WAVEFORMS



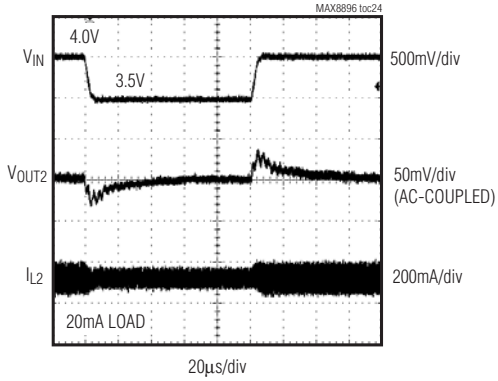
OUT2 HEAVY-LOAD SWITCHING WAVEFORMS



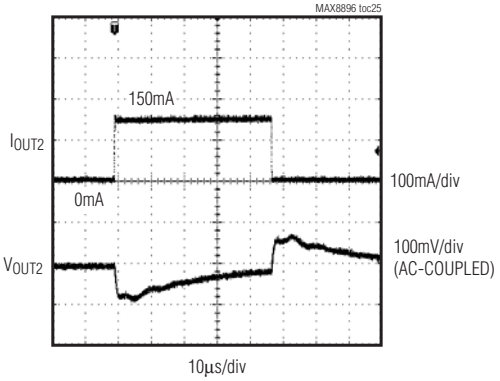
OUT2 STARTUP WAVEFORM



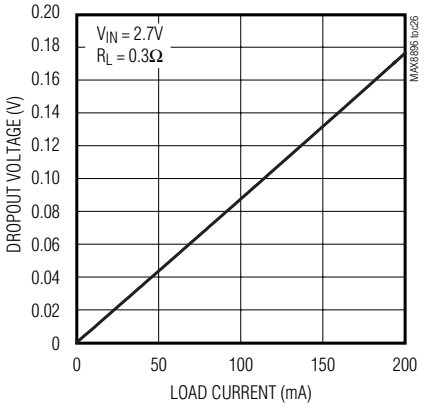
OUT2 LINE TRANSIENT RESPONSE



OUT2 LOAD TRANSIENT RESPONSE



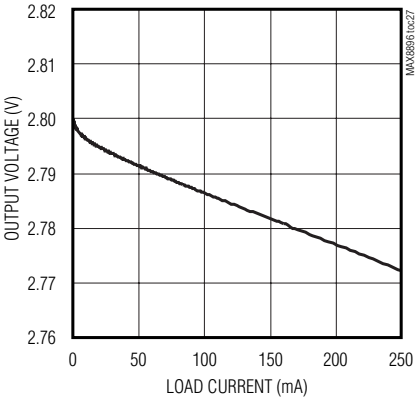
OUT2 DROPOUT VOLTAGE vs. LOAD CURRENT



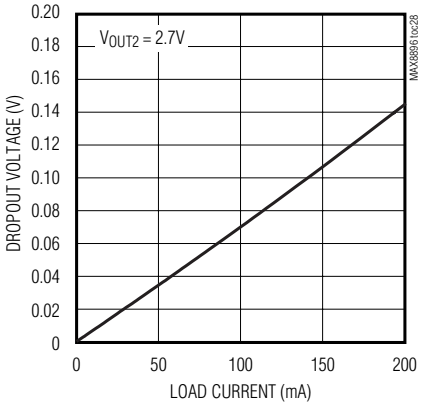
Typical Operating Characteristics (continued)

(V_{CC} = V_{IN1} = V_{IN2} = 3.6V, V_{REFIN} = 0.72V, circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

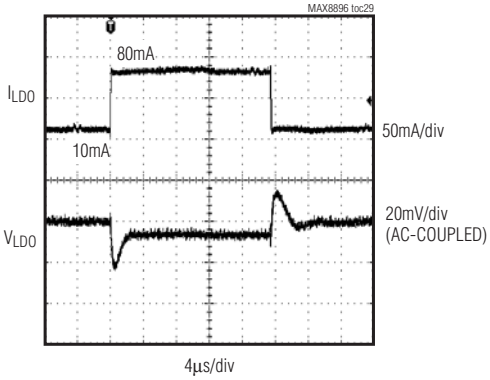
LDO OUTPUT VOLTAGE vs. LOAD CURRENT



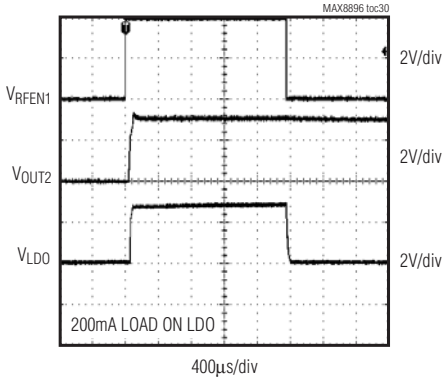
LDO DROPOUT VOLTAGE vs. LOAD CURRENT



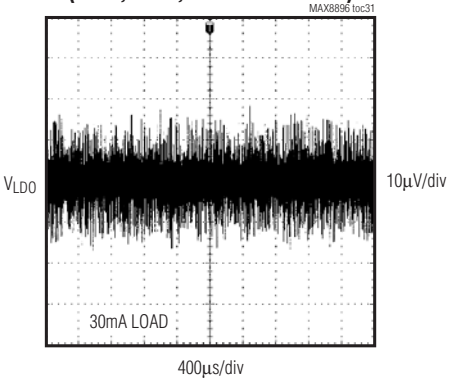
LDO LOAD TRANSIENT RESPONSE



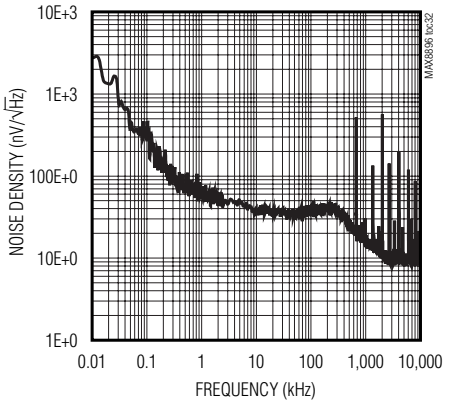
LDO STARTUP WAVEFORM



LDO OUTPUT NOISE (OUT1, OUT2, AND LDO ENABLED)



LDO OUTPUT-NOISE SPECTRAL DENSITY vs. FREQUENCY (OUT1, OUT2, AND LDO ENABLED)



Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

Pin Description

PIN	NAME	FUNCTION
A1	REFBP	Reference Noise Bypass. Bypass REFBP to AGND with a 0.033µF ceramic capacitor to reduce noise on the LDO output. REFBP is internally pulled down through a 1kΩ resistor during shutdown.
A2	AGND	Low-Noise Analog Ground. Connect AGND to the ground plane at a single point away from high switching currents. See the *PCB Layout* section.
A3	REFIN	DAC-Controlled Input. The output of the PA step-down converter is regulated to 2.5 x V_{REFIN}. When V_{REFIN} reaches 0.396 x V_{CC}, bypass mode is enabled.
A4	PGND1	Power Ground for OUT1. Connect PGND1 to the ground plane near the input and output capacitor grounds. See the *PCB Layout* section.
B1	LDO	200mA LDO Regulator Output. Bypass LDO with a 1µF ceramic capacitor as close as possible to LDO and ground. Leave LDO unconnected if not used.
B2	PAEN	OUT1 Enable Input. Connect PAEN to IN1 or logic-high for normal operation. Connect to ground or logic-low to shut down OUT1. Internally connected to ground through an 800kΩ resistor.
B3	RFEN2	OUT2 and LDO Enable Input. Connect RFEN1 or RFEN2 to IN2 or logic-high for normal operation. Connect RFEN1 and RFEN2 to ground or logic-low to shut down OUT2 and the LDO. Internally connected to ground through an 800kΩ resistor.
B4	LX1	Inductor Connection. Connect an inductor from LX1 to the output of OUT1.
C1	OUT2	Output of OUT2. OUT2 is also the supply voltage input for the LDO. Bypass OUT2 with a 2.2µF ceramic capacitor as close as possible to OUT2 and PGND2.
C2	RFEN1	OUT2 and LDO Enable Input. Connect RFEN1 or RFEN2 to IN2 or logic-high for normal operation. Connect RFEN1 and RFEN2 to ground or logic-low to shut down OUT2 and the LDO. Internally connected to ground through an 800kΩ resistor.
C3	V_{CC}	Supply Voltage Input for Internal Reference and Control Circuitry. Connect V_{CC} to a battery or supply voltage from 2.7V to 5.5V. Bypass V_{CC} with a 0.1µF ceramic capacitor as close as possible to V_{CC} and AGND. Connect V_{CC}, IN1, and IN2 to the same source.
C4	IN1	Supply Voltage Input for OUT1. Connect IN1 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN1 with a 4.7µF ceramic capacitor as close as possible to IN1 and PGND1. Connect IN1, V_{CC}, and IN2 to the same source.
D1	PGND2	Power Ground for OUT2. Connect PGND2 to the ground plane near the input and output capacitor grounds. See the *PCB Layout* section.
D2	LX2	Inductor Connection. Connect an inductor from LX2 to the output of OUT2.
D3	IN2	Supply Voltage Input for OUT2. Connect IN2 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN2 with a 2.2µF ceramic capacitor as close as possible to IN2 and PGND2. Connect IN2, V_{CC}, and IN1 to the same source.
D4	PAOUT	PA Connection for Bypass Mode. Internally connected to IN1 using the internal bypass MOSFET during bypass mode. PAOUT is internally connected to the feedback network for OUT1. Bypass PAOUT with a 4.7µF ceramic capacitor as close as possible to PAOUT and PGND1.

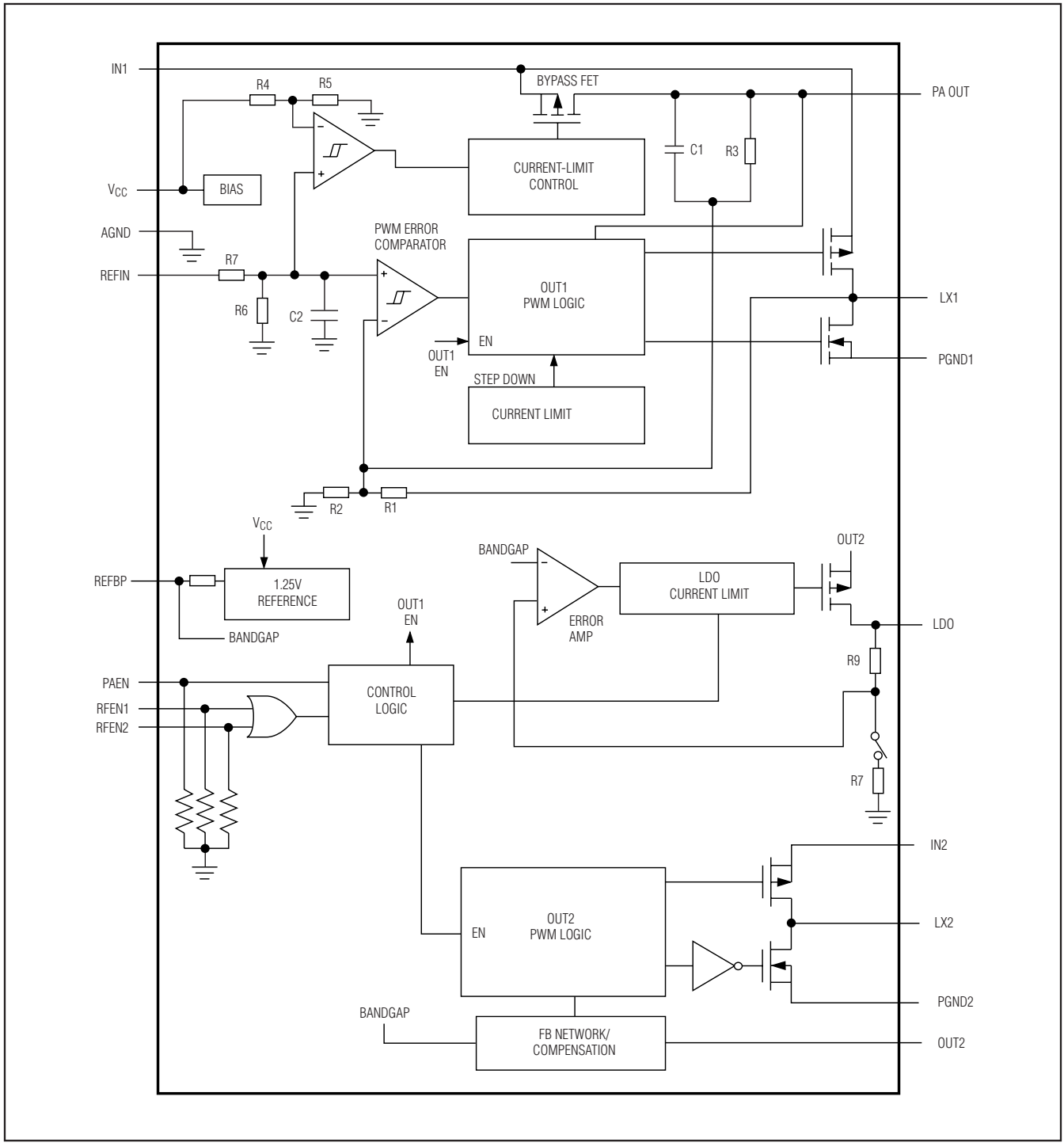


Figure 1. Block Diagram

Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

Detailed Description

The MAX8896 dual step-down converter is optimized for powering the power amplifier (PA) and RF transceiver in WCDMA handsets. This device integrates a high-efficiency PWM step-down converter (OUT1) for medium and low-power transmission, and a 140mΩ (typ) bypass FET to power the PA directly from the battery during high power transmission. A second high-efficiency PWM step-down converter (OUT2) supplies power directly to a high PSRR, low-output noise, 200mA low-dropout linear regulator (LDO) to power the RF transceiver.

OUT1 Step-Down Converter

A hysteretic PWM control scheme ensures high efficiency, fast switching, fast transient response, low output ripple, and physically tiny external components. The control scheme is simple: when the output voltage is below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This high-side switch remains on until the minimum on-time expires and output voltage is within regulation, or the inductor current is above the current-limit threshold. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls again below the regulation threshold. During the off period, the low-side synchronous rectifier turns on and remains on until the high-side switch turns on again. The internal synchronous rectifier eliminates the need for an external Schottky diode.

Voltage-Positioning Load Regulation

The MAX8896 step-down converter utilizes a unique feedback network. By taking DC feedback from the LX node through R1 of Figure 1, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of very small ceramic output capacitors. To improve the load regulation, resistor R3 is included in the feedback. This configuration yields load regulation equal to half the inductor's series resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients or when changing the output voltage from one level to another. However, when calculating the required REFIN voltage, the load regulation should be considered. Because inductor resistance is typically well specified and the typical PA is a resistive load, the V_{REFIN} to V_{OUT1} gain is slightly less than 2.5V/V. The output voltage is approximately:

$$V_{OUT1} = 2.5 \times V_{REFIN} - \frac{1}{2} \times R_L \times I_{LOAD}$$

Automatic Bypass Mode

During high-power transmission, the bypass mode connects IN1 directly to PAOUT with the internal 140mΩ (typ) bypass FET, while the step-down converter is forced into 100% duty-cycle operation. The low on-resistance in this mode provides low dropout, long battery life, and high output current capability. OUT1 enters bypass mode automatically when $V_{REFIN} > 0.396 \times V_{CC}$ (see Figure 2). Current-limit circuitry continuously limits current through the bypass FET to 1000mA (typ). The bypass FET opens up if the voltage at PAOUT drops below 1.25V (typ) in current limit.

OUT2 Step-Down Converter

OUT2 is a high-efficiency, 2MHz current-mode step-down DC-DC converter that outputs 200mA with efficiency up to 94%. The output voltage of the MAX8896 is a fixed 3.1V for powering the LDO. RFEN1 and RFEN2 are dedicated enable inputs for OUT2. Drive RFEN1 or RFEN2 high to enable OUT2, or drive RFEN1 and RFEN2 low to disable OUT2. RFEN1 and RFEN2 have hysteresis so that an RC may be used to implement manual sequencing with respect to other inputs.

OUT2 operates with a constant 2MHz switching frequency regardless of output load. The MAX8896 regulates the output voltage by modulating the switching duty cycle. An internal n-channel synchronous rectifier eliminates the need for an external Schottky diode and improves efficiency. The synchronous rectifier turns on during the second half of each switching cycle (off-time). During this time, the voltage across the inductor is reversed, and the inductor current ramps down. The synchronous rectifier turns off at the end of the switching cycle.

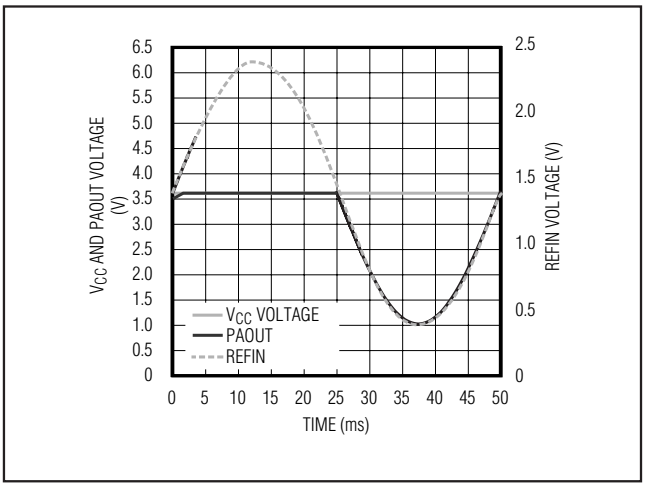


Figure 2. Automatic Bypass

The OUT2 step-down DC-DC converter operates with 100% duty cycle when the supply voltage approaches the output voltage. This allows this converter to maintain regulation until the input voltage falls below the desired output voltage plus the dropout voltage specification of the converter. During 100% duty cycle operation, the high-side p-channel MOSFET turns on constantly, connecting the input to the output through the inductor. The dropout voltage (V_{DO}) is calculated as follows:

$$V_{DO} = I_{LOAD} \times (R_P + R_L)$$

where:

R_P = internal p-channel MOSFET switch on-resistance (see *Electrical Characteristics*)

R_L = external inductor DC resistance

LDO

The LDO provides 200mA at 2.8V and is designed for low noise (16µV_{RMS}, typ) and high PSRR (65dB, typ). The LDO is powered from OUT2 (3.1V) and is enabled or disabled at the same time as OUT2 using RFEN1 or RFEN2.

LDO Dropout Voltage

The regulator's minimum input/output differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the LDO uses a p-channel MOSFET pass transistor, the dropout voltage is drain-to-source on-resistance ($R_{DS(ON)}$) multiplied by the load current (see the *Typical Operating Characteristics*).

Shutdown Mode

Connect PAEN to GND or logic-low to place OUT1 in shutdown mode. In shutdown, the control circuitry, internal switching MOSFET, and synchronous rectifier turn off and LX1 becomes high impedance. Connect PAEN to IN1, V_{CC}, or logic-high for normal operation.

Either RFEN1 or RFEN2 enable OUT2 and the LDO. Connect RFEN1 and RFEN2 to GND or logic-low to place OUT2 and the LDO in shutdown mode. In shutdown, the control circuitry, internal switching MOSFET, and synchronous rectifier turn off and LX2 and the LDO output become high impedance. Connect RFEN1 or RFEN2 to IN2, V_{CC}, or logic-high for normal operation. When PAEN, RFEN1, and RFEN2 are all logic-low, the MAX8896 enter a very low power state, where the input current drops to 0.1µA (typ).

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8896. If the junction temperature exceeds +160°C, the MAX8896 turn off, allowing the IC to cool. The IC turns on and begins soft-start after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal-overload conditions.

Applications Information

Inductor Selection

OUT1 operates with a switching frequency of 2MHz and utilizes a 2.2µH to 4.7µH inductor. OUT2 operates with a switching frequency of 2MHz and utilizes a 2.2µH inductor. This operating frequency allows the use of physically small inductors while maintaining high efficiency.

The OUT1 inductor's DC current rating only needs to match the maximum load of the application because OUT1 features zero current overshoot during startup and load transients. For optimum transient response and high efficiency, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. See Table 1 for suggested inductors and manufacturers.

Using a larger inductance value reduces the ripple current, therefore providing higher efficiency at light load.

Output Capacitor Selection

For OUT1 and OUT2, the output capacitor keeps the output voltage ripple small and ensures regulation loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. A 4.7µF capacitor is recommended for C_{OUT1} and 2.2µF is recommended for C_{OUT2}. For optimum load-transient performance and very low output ripple, the output capacitor value can be increased.

For the LDO, the minimum output capacitance required is dependent on the load currents. For loads lighter than 10mA, it is sufficient to use a 0.1µF capacitor for stable operation over the full temperature range. With rated maximum load currents, a minimum of 1µF is recommended. Larger value output capacitors further reduce output noise and improve load-transient response, stability, and power-supply rejection.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature and DC bias. Ceramic capacitors with Z5U or Y5V temperature characteristics should be avoided. These regulators are optimized for ceramic capacitors. Tantalum capacitors are not recommended.

Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

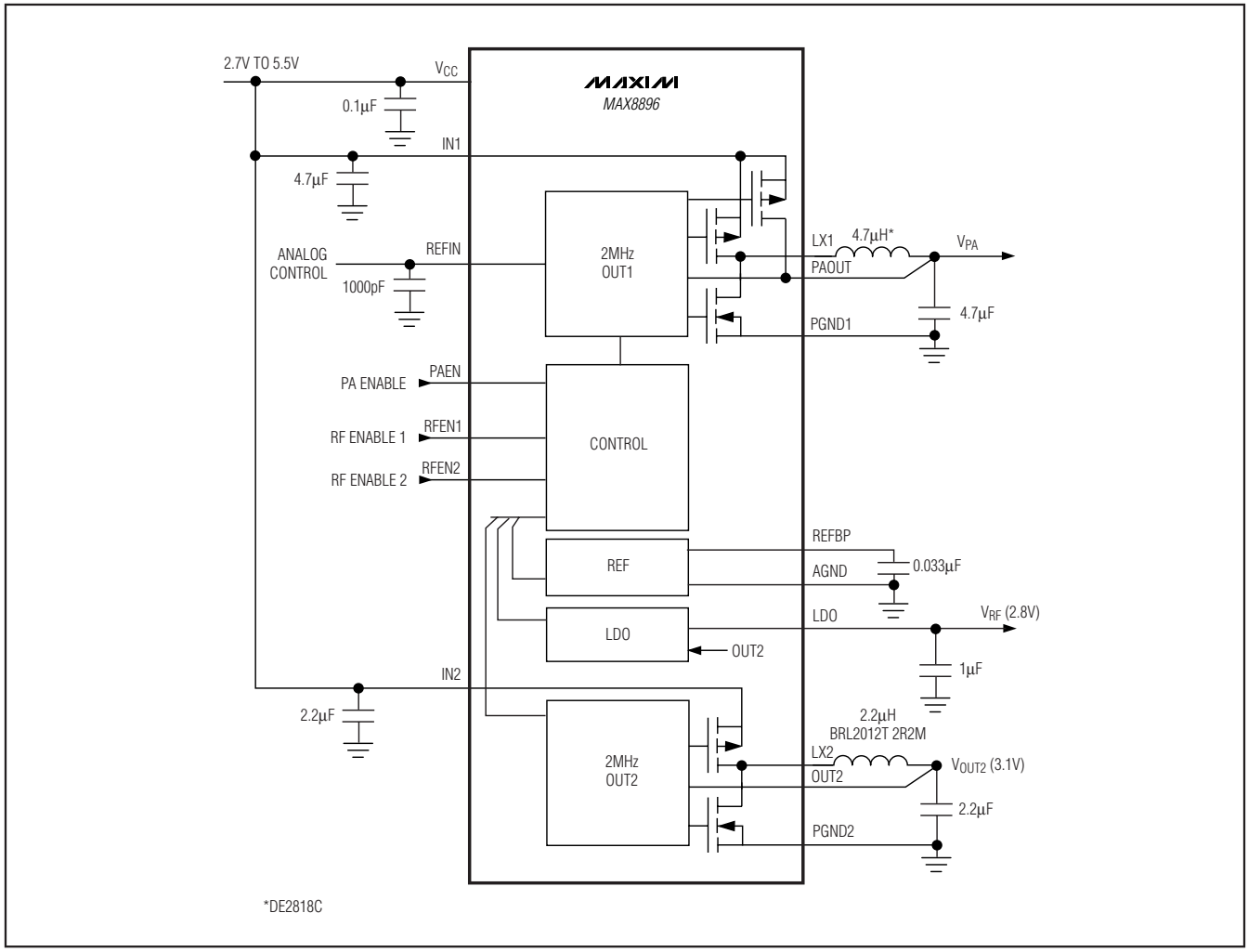


Figure 3. Typical Applications Circuit

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the battery or input power source and reduces switching noise in the MAX8896. The impedance of C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. A 4.7µF capacitor is recommended for C_{IN1} and 2.2µF for C_{IN2}. For optimum noise immunity and low input ripple, the input capacitor value can be increased.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature and DC bias. Ceramic capacitors with Z5U or Y5V temperature characteristics should be avoided.

Thermal Considerations

In most applications, the MAX8896 does not dissipate much heat due to its high efficiency. But in applications where the MAX8896 runs at high ambient temperature with heavy loads, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately +160°C, the thermal-overload protection is activated.

The MAX8896 maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipated in the device is:

$$P_D = P_{OUT1} \times (1/\eta_{OUT1} - 1) + P_{OUT2} \times (1/\eta_{OUT2} - 1) + I_{LDO} \times (V_{OUT2} - V_{LDO})$$

where η is the efficiency of the step-down converter and $P_{OUT\_}$ is the output power of the step-down converter. The maximum allowed power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$$

where $(T_{JMAX} - T_A)$ is the temperature difference between the MAX8896 die junction and the surrounding air, θ_{JA} is the thermal resistance of the junction through the PCB, copper traces, and other materials to the surrounding air.

PCB Layout

High switching frequencies and relatively large peak currents make the PCB layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, resulting in a stable and well regulated output. Connect C_{IN1} close to IN1 and PGND1 and connect C_{IN2} close to IN2 and PGND2. Connect the inductor and output capacitor as close as possible to the IC and keep their traces short, direct, and wide. Keep noisy traces, such as the LX node, as short as possible. Refer to the MAX8896EVKIT for an example layout.

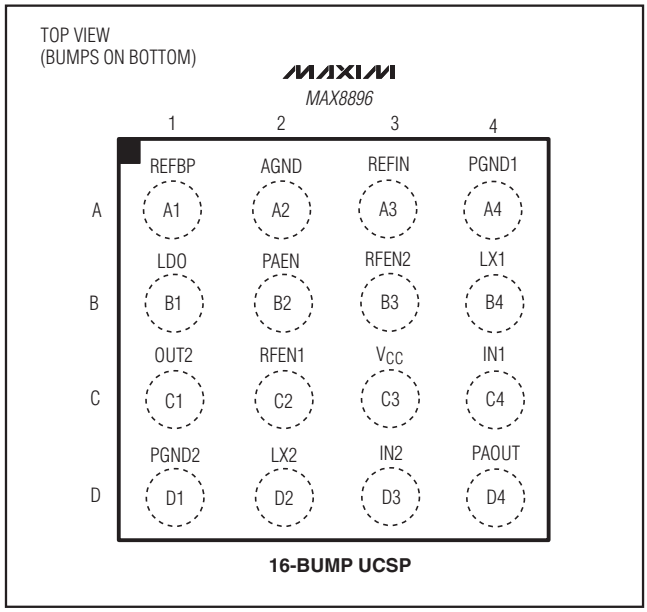
Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

Table 1. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS
Taiyo Yuden	CB2016T	1.0 2.2	0.09 0.13	600 510	2.0mm x 1.6mm x 1.8mm = 5.8mm^3
	CB2518T	2.2 4.7	0.09 0.13	510 340	2.5mm x 1.8mm x 2.0mm = 9mm^3
	BRL2012T	2.2	0.30	550	2.0mm x 1.25mm x 1.0mm = 2.5mm^3
	CKP2520	2.2	0.09	1300	2.5mm x 2.0mm x 1.0mm = 5mm^3
FDK	MIPF2520	1.0 1.5 2.2	0.05 0.07 0.08	1500 1500 1300	2.5mm x 2.0mm x 1.0mm = 5mm^3
	MIPF2016	2.2	0.11	1100	2.0mm x 1.6mm x 1.0mm = 3.2mm^3
Murata	LQH32C_53	1.0 2.2	0.06 0.10	1000 790	3.2mm x 2.5mm x 1.7mm = 14mm^3
TOKO	D3010FB	1.0	0.20	1170	3.0mm x 3.0mm x 1.0mm = 9mm^3
	D2812C	1.2 2.2	0.09 0.15	860 640	3.0mm x 3.0mm x 1.2mm = 11mm^3
	D310F	1.5 2.2	0.13 0.17	1230 1080	3.6mm x 3.6mm x 1.0mm = 13mm^3
	D312C	1.5 2.2	0.10 0.12	1290 1140	3.6mm x 3.6mm x 1.2mm = 16mm^3
	DE2818C	4.7	72	950	3.2mm x 3.0mm x 1.8mm = 17.3mm^3
Sumida	CDRH2D09	1.2 1.5 2.2	0.08 0.09 0.12	590 520 440	3.0mm x 3.0mm x 1.0mm = 9mm^3
	CDRH2D11	1.5 2.2 3.3	0.05 0.08 0.10	680 580 450	3.2mm x 3.2mm x 1.2mm = 12mm^3
Coilcraft	LPO3310	1.0 1.5 2.2	0.07 0.10 0.13	1600 1400 1100	3.3mm x 3.3mm x 1.0mm = 11mm^3
	XPL2010	4.7	0.284	740	1.9mm x 2.0mm x 1.0mm = 3.8mm^3
Panasonic	ELC3FN	1.0 2.2	0.08 0.12	1400 1000	3.2mm x 3.2mm x 1.2mm = 12mm^3
	ELL3GM	1.0 2.2	0.07 0.10	1400 1100	3.2mm x 3.2mm x 1.5mm = 15mm^3

Dual PWM Step-Down Converter in a 2mm x 2mm Package for WCDMA PA and RF Power

Pin Configuration



16-BUMP UCSP

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 UCSP	R162A2+1	**21-0226**