6-Channel High-Speed Logic-Level Translators

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, V_L .....-0.3V to +4V
I/O $V_{CC\_}$, CLK_V_{CC} .....-0.3V to (V_{CC} + 0.3V)
I/O $V_{L\_}$, CLK_V_L, CLK_RET .....-0.3V to (V_L + 0.3V)
EN.....-0.3V to +4V
Short-Circuit Duration I/O $V_{L\_}$, I/O $V_{CC\_}$, CLK_V_{CC}, CLK_V_L, CLK_RET to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Bump UCSP (derate 8.2mW/°C).....660mW
16-Pin TQFN (derate 25.0mW/°C).....2000mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Bump Temperature (soldering).....+235°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
V_L Supply Range	V_L	(Note 2)	1.62		3.20	V
V_{CC} Supply Range	V_{CC}		2.2		3.6	V
Supply Current from V_{CC}	I_{QVCC}	I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L		16	25	µA
Supply Current from V_L	I_{QVL}	I/O $V_{CC\_}$ = V_{CC}, I/O $V_{L\_}$ = V_L		6	10	µA
V_{CC} Shutdown Supply Current	$I_{SHDN-VCC}$	T_A = +25°C, EN = GND or V_L > V_{CC} + 0.7V, MAX13030E–MAX13034E		2	4	µA
		T_A = +25°C, V_L > V_{CC} + 0.7V, MAX13035E,		2	4	
V_L Shutdown Supply Current	$I_{SHDN-VL}$	T_A = +25°C, EN = GND or V_L > V_{CC} + 0.7V, MAX13030E–MAX13034E		0.1	4	µA
		T_A = +25°C, V_L > V_{CC} + 0.7V, MAX13035E		0.1	4	
I/O $V_{CC\_}$, I/O $V_{L\_}$, CLK_V_{CC} Tri-State Leakage Current	I_{LEAK}	T_A = +25°C, EN = GND or V_L > V_{CC} + 0.7V		0.1	2	µA
EN Input Leakage Current	I_{LEAK_EN}	T_A = +25°C, MAX13030E–MAX13034E			1	µA
V_L - V_{CC} Shutdown Threshold High	V_{TH_H}	V_{CC} rising	-0.2	0.05V_L	0.7	V
V_L - V_{CC} Shutdown Threshold Low	V_{TH_L}	V_{CC} falling	-0.2	0.1V_L	0.7	V
I/O $V_{CC\_}$ Pulldown Resistance During Shutdown	$R_{VCC\_PD\_SD}$	EN = GND, MAX13032E/MAX13034E	10	16.5	23	kΩ
I/O $V_{CC\_}$ Pullup Resistance During Shutdown	$R_{VCC\_PU\_SD}$	EN = GND, MAX13031E	10	16.5	23	kΩ
I/O $V_{L\_}$ Pulldown Resistance During Shutdown	$R_{VL\_PD\_SD}$	EN = GND, MAX13033E/MAX13034E	10	16.5	23	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = 1.8V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O V_L_, CLK_V_L, CLK_RET Pullup Resistance During Shutdown	$R_{VL\_PU\_SD}$	(V_L > V_{CC} + 0.7V), MAX13035E	45	75	105	kΩ
I/O V_L_, CLK_V_L, CLK_RET Pullup Current	R_{VL_PU}	EN = V_{CC} or V_L, I/O V_L_ = GND	20			µA
I/O V_{CC}_, CLK_V_{CC} Pullup Current	R_{VCC_PU}	EN = V_{CC} or V_L, I/O V_{CC}_ = GND	20			µA
I/O V_L to I/O V_{CC} DC Resistance	R_{IOVL_IOVCC}	(Note 3)		3		kΩ
ESD PROTECTION (Note 3)						
I/O V_{CC}_, CLK_V_{CC}		Human Body Model, C_{VCC} = 1.0µF		±15		kV
		IEC 61000-4-2 Air-Gap Discharge, C_{VCC} = 1.0µF		±12		
		IEC 61000-4-2 Contact Discharge, C_{VCC} = 1.0µF		±8		
LOGIC-LEVEL THRESHOLDS						
I/O V_L_, CLK_V_L Input-Voltage High Threshold	V_{IHL}	(Note 4)			V_L - 0.2	V
I/O V_L_, CLK_V_L Input-Voltage Low Threshold	V_{ILL}	(Note 4)	0.15			V
I/O V_{CC}_, CLK_V_{CC} Input-Voltage High Threshold	V_{IHC}	(Note 4)			V_{CC} - 0.4	V
I/O V_{CC}_, CLK_V_{CC} Input-Voltage Low Threshold	V_{ILC}	(Note 4)	0.2			V
EN Input-Voltage High Threshold	V_{IH}	MAX13030E–MAX13034E			V_L - 0.4	V
EN Input-Voltage Low	V_{IL}	MAX13030E–MAX13034E	0.4			V
I/O V_L_, CLK_V_L, CLK_RET Output-Voltage High	V_{OHL}	I/O V_L_, CLK_V_L, CLK_RET source current = 20µA, I/O V_{CC}_ ≥ V_{CC} - 0.4V	2/3 V_L			V
I/O V_L_, CLK_V_L, CLK_RET Output-Voltage Low	V_{OLL}	I/O V_L_, CLK_V_L, CLK_RET sink current = 20µA, I/O V_{CC}_ ≤ 0.2V			1/3 V_L	V
I/O V_{CC}_, CLK_V_{CC} Output-Voltage High	V_{OHC}	I/O V_{CC}_, CLK_V_{CC} source current = 20µA, I/O V_L_ ≥ V_L - 0.2V	2/3 V_{CC}			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, EN = V_L, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = 1.8V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$, CLK_V_{CC} Output-Voltage Low	V_{OLC}	I/O $V_{CC\_}$, CLK_V_{CC} sink current = 20µA, I/O $V_{L\_}$ ≤ 0.15V			1/3 V_{CC}	V
RISE/FALL TIME ACCELERATOR STAGE (Note 3)						
Accelerator Pulse Duration		On falling edge		3		ns
		On rising edge		3		
V_L-Output-Accelerator Source Impedance		V_L = 1.62V		11		Ω
		V_L = 3.2V		6		
V_{CC}-Output-Accelerator Source Impedance		V_{CC} = 2.2V		9		Ω
		V_{CC} = 3.6V		8		
V_L-Output-Accelerator Sink Impedance		V_L = 1.62V		9		Ω
		V_L = 3.2V		8		
V_{CC}-Output-Accelerator Sink Impedance		V_{CC} = 2.2V		10		Ω
		V_{CC} = 3.6V		9		

TIMING CHARACTERISTICS

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, $C_{I/OVL}$ ≤ 15pF, $C_{I/OVCC}$ ≤ 15pF, R_{SOURCE} = 150Ω, EN = V_L, I/O $V_{L\_}$ to I/O $V_{CC\_}$ rise/fall time = 3ns, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = 1.8V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O $V_{CC\_}$, CLK_V_{CC} Rise Time	t_{RVCC}	R_S = 150Ω, $C_{I/OVCC}$ = 10pF, C_{CLK_VCC} = 10pF, push-pull drivers (Figure 1)			2.5	ns
I/O $V_{CC\_}$, CLK_V_{CC} Fall Time	t_{FVCC}	R_S = 150Ω, $C_{I/OVCC}$ = 10pF, C_{CLK_VCC} = 10pF (Figures 1, 2)			2.5	ns
I/O $V_{L\_}$, CLK_V_L Rise Time	t_{RVL}	R_S = 150Ω, $C_{I/OVL}$ = 15pF, C_{CLK_VL} = 15pF, push-pull drivers (Figure 3)			2.5	ns
I/O $V_{L\_}$, CLK_V_L Fall Time	t_{FVL}	R_S = 150Ω, $C_{I/OVL}$ = 15pF, C_{CLK_VL} = 15pF (Figures 3, 4)			2.5	ns
Propagation Delay (Driving I/O $V_{L\_}$, CLK_V_L)	$t_{PVL-VCC}$	R_S = 150Ω, $C_{I/OVCC}$ = 10pF, C_{CLK_VCC} = 10pF, push-pull drivers (Figure 1)			6.5	ns
Propagation Delay (Driving I/O $V_{CC\_}$, CLK_V_{CC})	$t_{PVCC-VL}$	R_S = 150Ω, $C_{I/OVL}$ = 15pF, C_{CLK_VL} = 15pF, push-pull drivers (Figure 3)			6.5	ns
Channel-to-Channel Skew	t_{SKEW}	R_S = 150Ω, $C_{I/OVCC}$ = 10pF, $C_{I/OVL}$ = 15pF			0.8	ns
Propagation Delay from I/O $V_{L\_}$ to I/O $V_{CC\_}$ after EN	t_{EN-VCC}	R_{LOAD} = 1MΩ, $C_{I/OVCC}$ = 10pF (Figure 5) (MAX13030E–MAX13034E)		5		µs

TIMING CHARACTERISTICS (continued)

(V_{CC} = +2.2V to +3.6V, V_L = +1.62V to +3.2V, $C_{I/OVL}$ ≤ 15pF, $C_{I/OVCC}$ ≤ 15pF, R_{SOURCE} = 150Ω, EN = V_L, I/O $V_{L\_}$ to I/O $V_{CC\_}$ rise/fall time = 3ns, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = 1.8V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from I/O $V_{CC\_}$ to I/O $V_{L\_}$ after EN	t_{EN-VL}	R_{LOAD} = 1MΩ, $C_{I/OVL}$ = 15pF (Figure 5) (MAX13030E–MAX13034E)		5		µs
Maximum Data Rate		Push-pull operation, R_{SOURCE} = 150_, $C_{I/OVCC\_}$ = 10pF, $C_{I/OVL\_}$ = 15pF, C_{CLK_VCC} = 10pF, C_{CLK_VL} = 15pF	100			Mbps

Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 2: V_L must be less than or equal to V_{CC} - 0.2V during normal operation. However, V_L can be greater than V_{CC} during startup and shutdown conditions and the part will not latch-up or be damaged.

Note 3: Guaranteed by design.

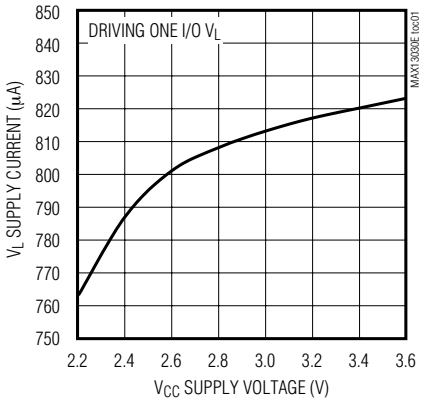
Note 4: Input thresholds are referenced to the boost circuit.

6-Channel High-Speed Logic-Level Translators

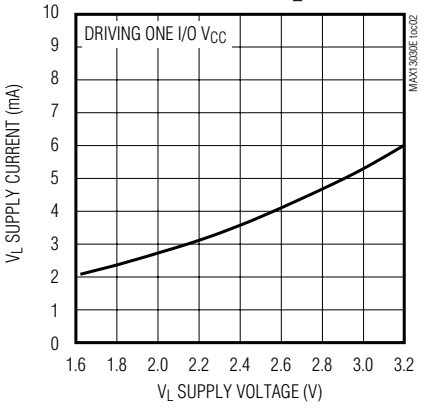
Typical Operating Characteristics

(V_{CC} = 3.3V, V_L = 1.8V, C_L = 15pF, R_{SOURCE} = 150Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

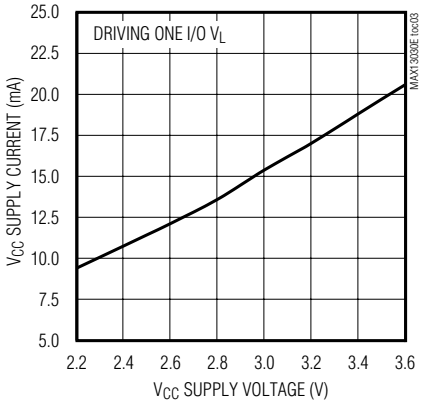
V_L SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING I/O V_L_, V_L = 1.8V)



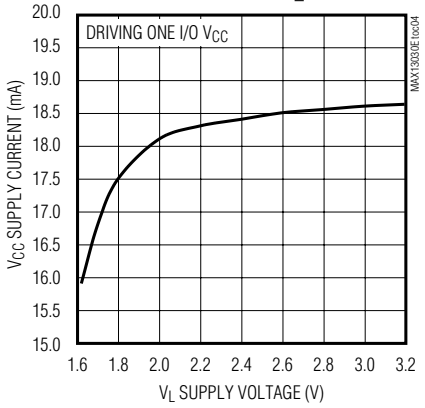
V_L SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING I/O V_{CC}_, V_{CC} = 3.6V)



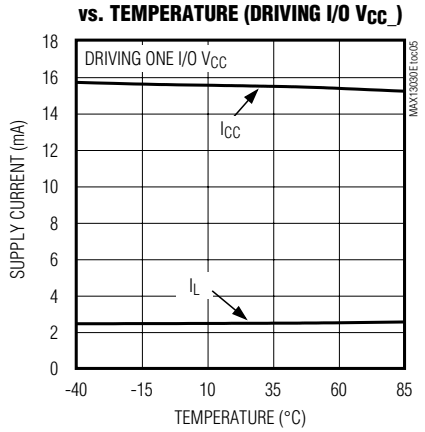
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE (DRIVING I/O V_L_, V_L = 1.8V)



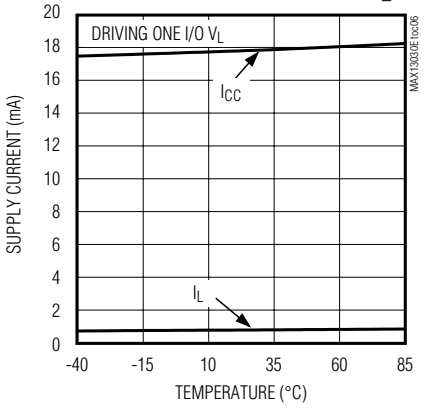
V_{CC} SUPPLY CURRENT vs. V_L SUPPLY VOLTAGE (DRIVING I/O V_{CC}_, V_{CC} = 3.6V)



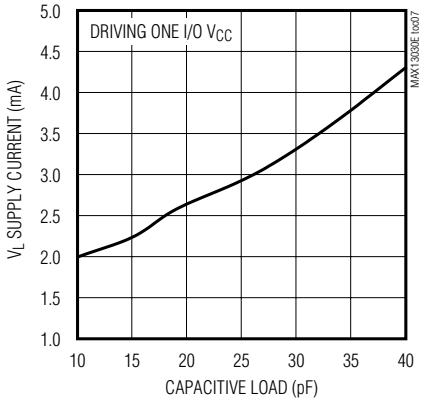
SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/O V_{CC}_)



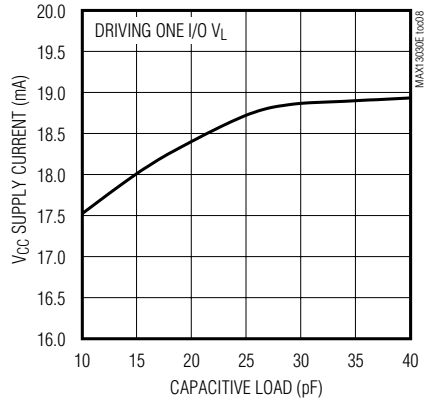
SUPPLY CURRENT vs. TEMPERATURE (DRIVING I/O V_L_)



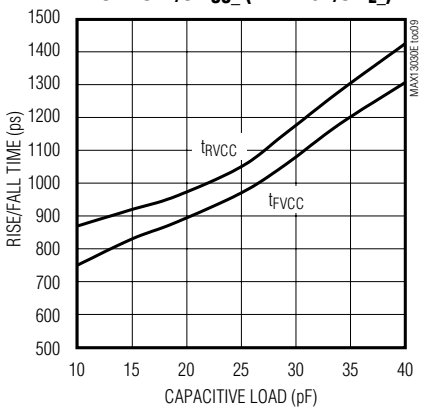
V_L SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_L_ (DRIVING I/O V_{CC}_)



V_{CC} SUPPLY CURRENT vs. CAPACITIVE LOAD ON I/O V_{CC}_ (DRIVING I/O V_L_)



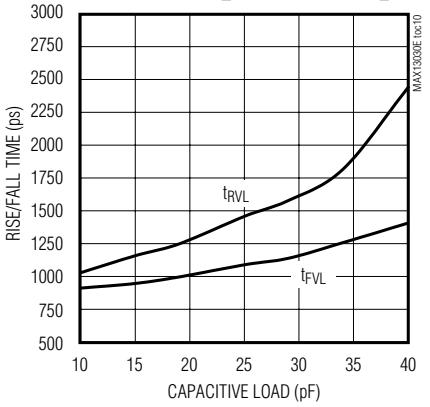
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O V_{CC}_ (DRIVING I/O V_L_)



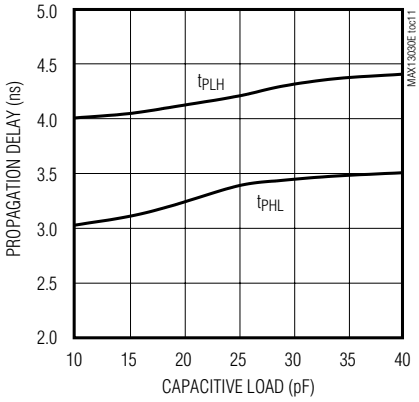
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, V_L = 1.8V, C_L = 15pF, R_{SOURCE} = 150Ω, data rate = 100Mbps, push-pull driver, T_A = +25°C, unless otherwise noted.)

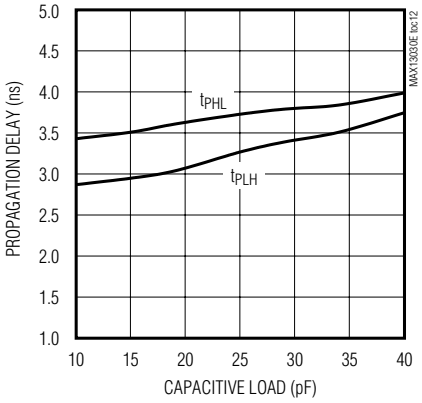
RISE/FALL TIME vs. CAPACITIVE LOAD ON I/O $V_{L\_}$ (DRIVING I/O $V_{CC\_}$)



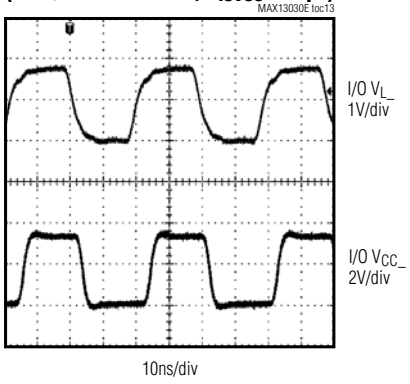
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O $V_{CC\_}$ (DRIVING I/O $V_{L\_}$)



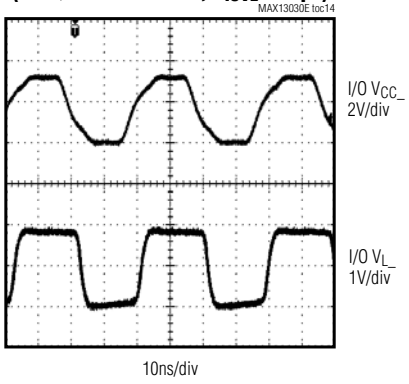
PROPAGATION DELAY vs. CAPACITIVE LOAD ON I/O $V_{L\_}$ (DRIVING I/O $V_{CC\_}$)



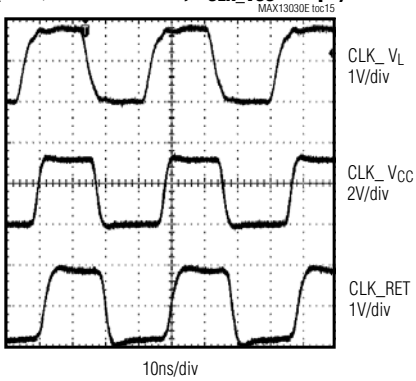
TYPICAL I/O $V_{L\_}$ DRIVING (FREQUENCY = 26MHz, C_{IOVCC} = 40pF)



TYPICAL I/O $V_{CC\_}$ DRIVING (FREQUENCY = 26MHz, C_{IOVL} = 15pF)



TYPICAL CLK_ V_L DRIVING (FREQUENCY = 26MHz, C_{CLK_VCC} = 40pF)



6-Channel High-Speed Logic-Level Translators

Pin Description

PIN				NAME	FUNCTION
MAX13030E–MAX13034E		MAX13035E			
UCSP	TQFN	UCSP	TQFN		
A1	4	A1	4	I/O V_L3	Input/Output 3. Referenced to V_L.
A2	6	A2	6	I/O $V_{CC}3$	Input/Output 3. Referenced to V_{CC}.
A3	7	A3	7	I/O $V_{CC}4$	Input/Output 4. Referenced to V_{CC}.
A4	9	A4	9	I/O V_L4	Input/Output 4. Referenced to V_L.
B1	3	B1	3	I/O V_L2	Input/Output 2. Referenced to V_L.
B2	5	B2	5	I/O $V_{CC}2$	Input/Output 2. Referenced to V_{CC}.
B3	8	B3	8	I/O $V_{CC}5$	Input/Output 5. Referenced to V_{CC}.
B4	10	B4	10	I/O V_L5	Input/Output 5. Referenced to V_L.
C1	2	C1	2	V_L	Logic-Supply Voltage, +1.62V to +3.2V. Bypass V_L to GND with a 0.1µF capacitor placed as close as possible to the device.
C2	16	C2	16	V_{CC}	Power-Supply Voltage, +2.2V to +3.6V. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor. For full ESD protection, connect a 1µF ceramic capacitor from V_{CC} to GND as close as possible to the V_{CC} input.
C3	13	C3	13	GND	Ground
C4	11	—	—	EN	Enable Input. Drive EN to GND for shutdown mode, or drive EN to V_L or V_{CC} for normal operation.
D1	1	D1	1	I/O V_L1	Input/Output 1. Referenced to V_L.
D2	15	D2	15	I/O $V_{CC}1$	Input/Output 1. Referenced to V_{CC}.
D3	14	—	—	I/O $V_{CC}6$	Input/Output 6. Referenced to V_{CC}.
D4	12	—	—	I/O V_L6	Input/Output 6. Referenced to V_L.
—	—	C4	11	CLK_RET	Clock Return Output. CLK_RET is the returned signal of a clock applied to CLK_V_L. CLK_RET is referenced to V_L.
—	—	D3	14	CLK_V_{CC}	Translator Channel for a Clock Applied to V_{CC}
—	—	D4	12	CLK_V_L	Translator Channel for a Clock Applied to V_L
—	EP	—	EP	EP	Exposed Paddle. Connect exposed paddle to GND.

Test Circuits/Timing Diagrams

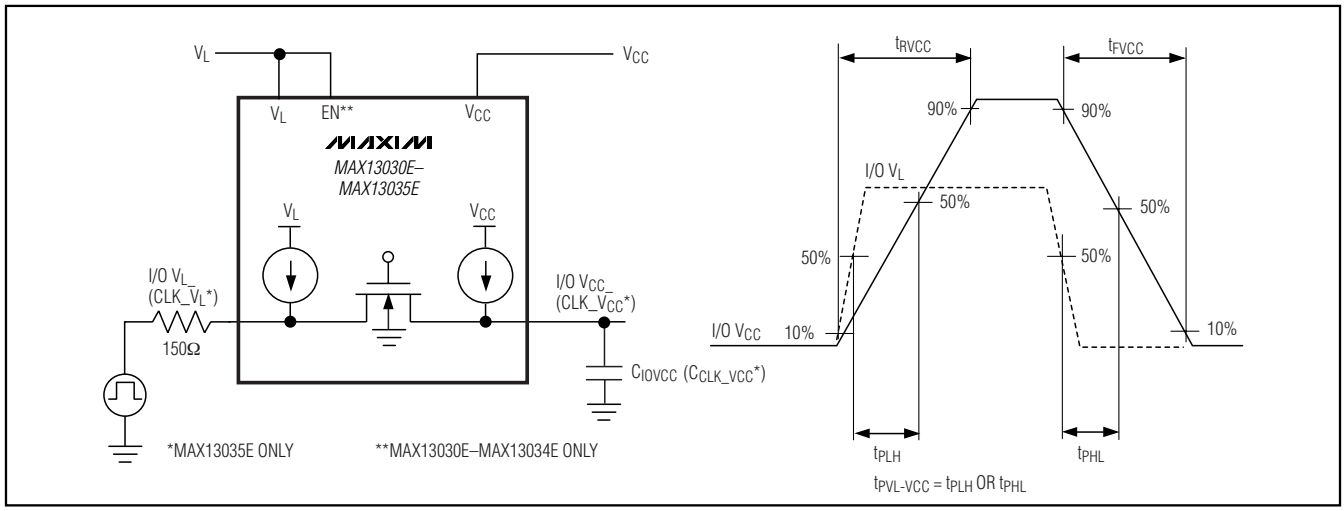


Figure 1. Push-Pull Driving I/O $V_{L\_}$ Test Circuit and Timing

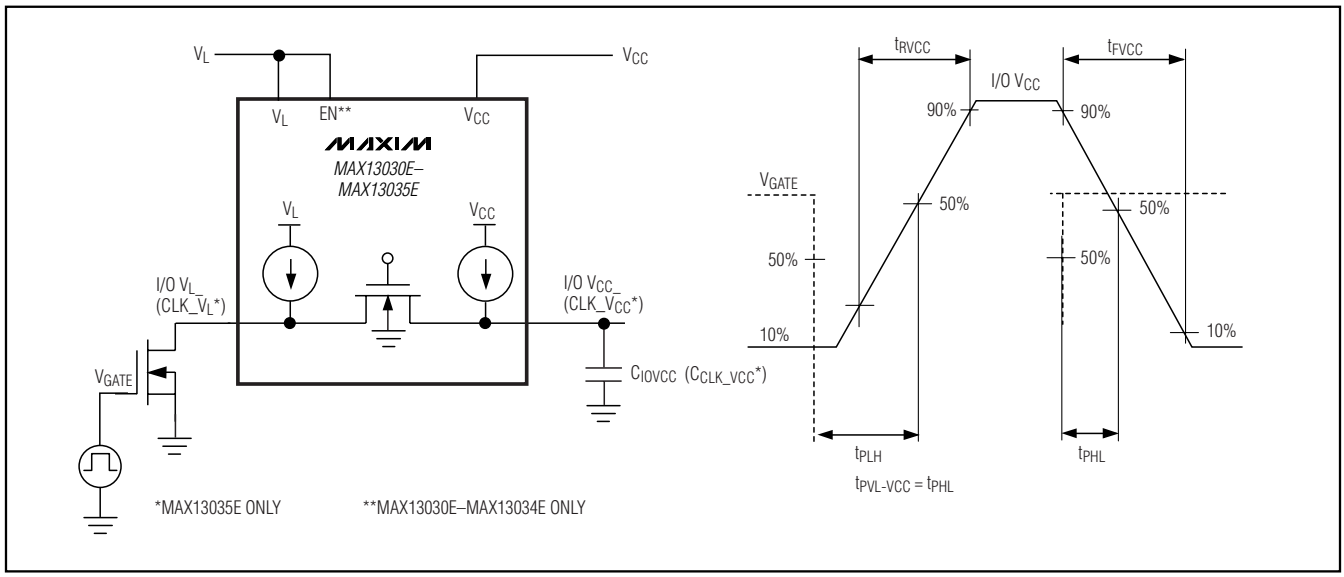


Figure 2. Open-Drain Driving I/O VL_ Test Circuit and Timing

6-Channel High-Speed Logic-Level Translators

Test Circuits/Timing Diagrams (continued)

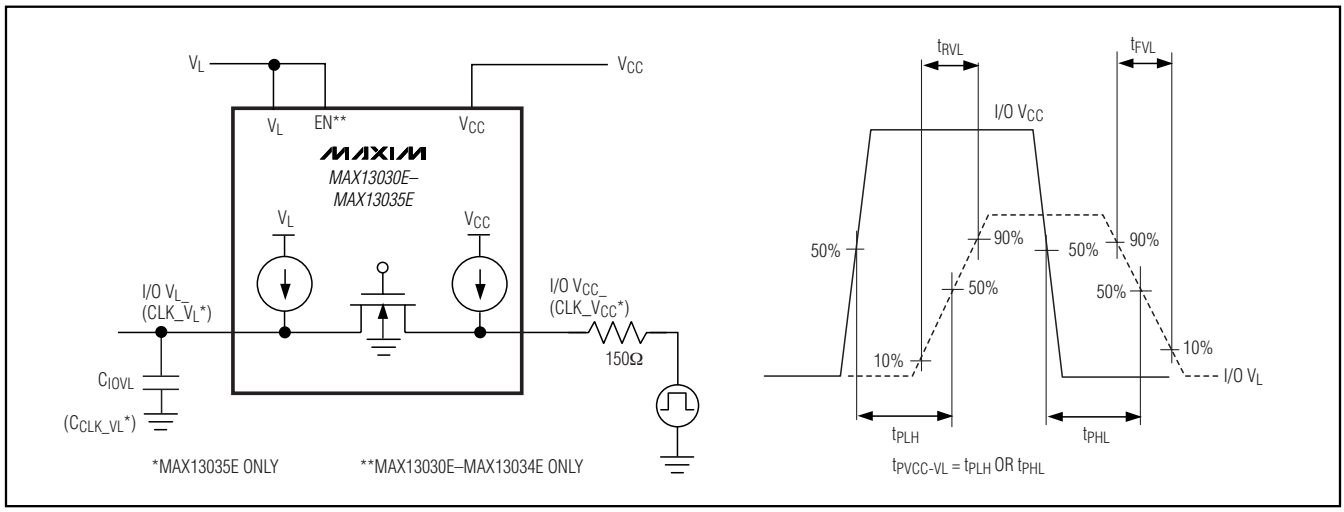


Figure 3. Push-Pull Driving I/O $V_{CC\_}$ Test Circuit and Timing

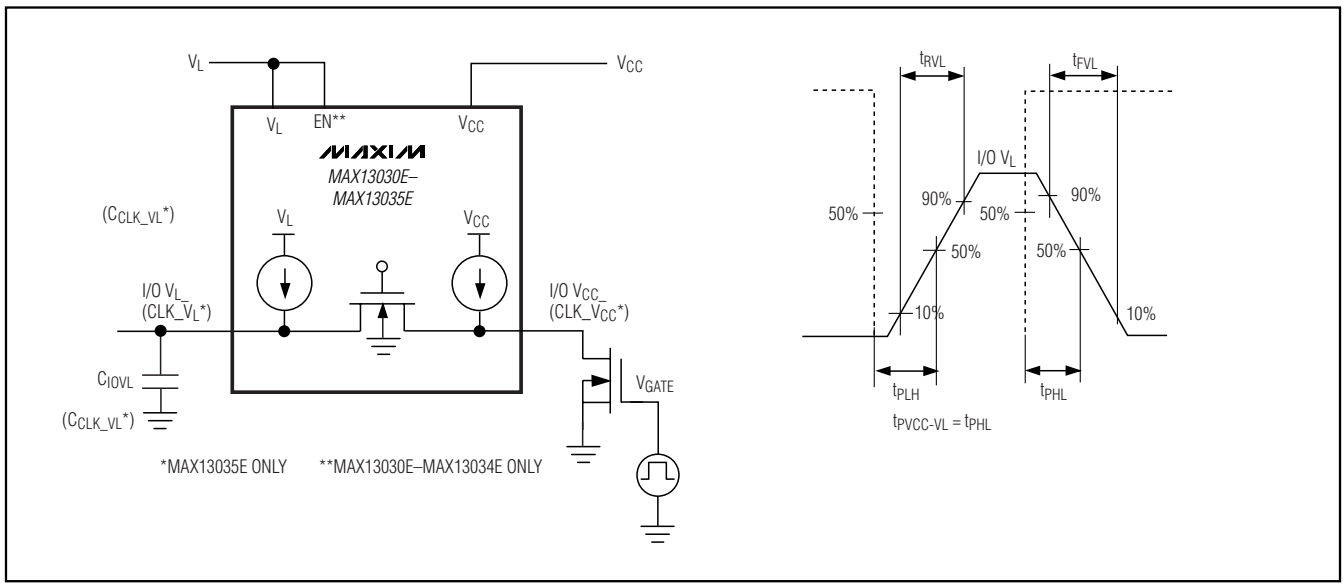


Figure 4. Open-Drain Driving I/O $V_{CC\_}$ Test Circuit and Timing

Test Circuits/Timing Diagrams (continued)

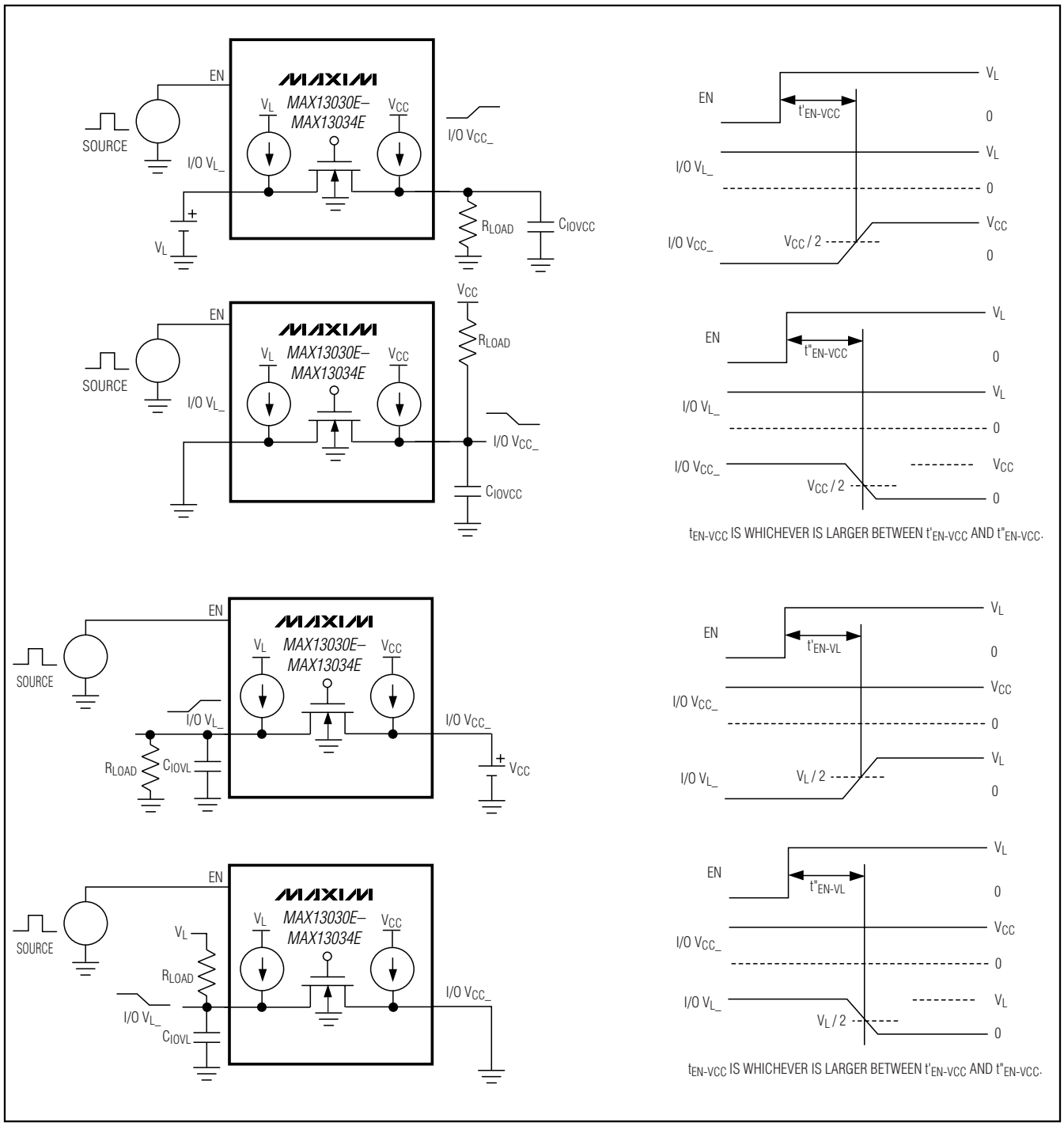


Figure 5. Enable Test Circuit and Timing

6-Channel High-Speed Logic-Level Translators

Detailed Description

The MAX13030E–MAX13035E 6-channel, bidirectional level translators provide the level shifting necessary for 100Mbps data transfer in multivoltage systems. The MAX13030E–MAX13035E are ideally suited for memory card level translation, as well as generic level translation in systems with six channels. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. Logic signals present on the V_L side of the device appear as a higher voltage logic signal on the V_{CC} side of the device, and vice versa. The MAX13035E features a CLK_RET output that returns the same clock signal applied to the CLK_V_L input.

The MAX13030E–MAX13035E operate at full speed with external drivers that source as little as 4mA output current. Each I/O channel is pulled up to V_{CC} or V_L by an internal 30µA current source, allowing the MAX13030E–MAX13035E to be driven by either push-pull or open-drain drivers.

The MAX13030E–MAX13034E feature an enable (EN) input that places the device into a low-power shutdown mode when driven low. The MAX13030E–MAX13035E features an automatic shutdown mode that disables the part when V_{CC} is less than V_L. The state of I/O $V_{CC\_}$ and I/O $V_{L\_}$ during shutdown is chosen by selecting the appropriate part version (see *Ordering Information/ Selector Guide*).

The MAX13030E–MAX13035E accept V_{CC} voltages from +2.2V to +3.6V and V_L voltages from +1.62V to +3.2V.

Level Translation

For proper operation, ensure that +2.2V ≤ V_{CC} ≤ +3.6V, and +1.62V ≤ V_L ≤ V_{CC} - 0.2V. When power is supplied to V_L while V_{CC} is either missing or less than V_L, the MAX13030E–MAX13035E automatically enters a low- power mode. In addition, the MAX13030E–MAX13034E enters a low-power mode if EN = 0V. This allows V_{CC} to be disconnected and still have a known state on I/O $V_{L\_}$. The maximum data rate depends heavily on the load capacitance (see the *Typical Operating Characteristics Rise/Fall Times*), output impedance of the driver, and the operating voltage range.

Input Driver Requirements

The MAX13030E–MAX13035E architecture is based on an nMOS pass gate and output accelerator stages (see Figure 6). Output accelerator stages are always in tri-state mode except when there is a transition on any of the translators on the input side, either I/O $V_{L\_}$, CLK_V_L, I/O $V_{CC\_}$, or CLK_V_{CC}. A short pulse is then generated during which the output accelerator stages become active and charge/discharge the capacitances at the I/Os. Due to its architecture, both input stages become active during the one-shot pulse. This can lead to some current feeding into the external source that is driving the translator. However, this behavior helps to speed up the transition on the driven side.

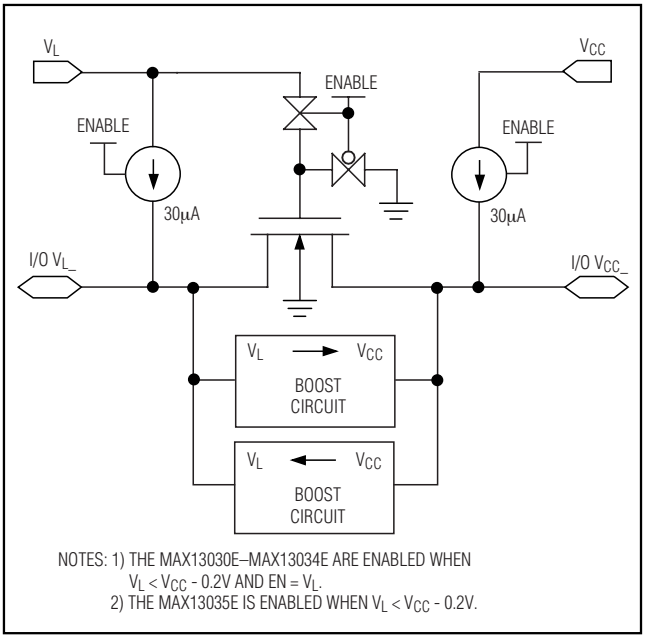


Figure 6. Simplified Functional Diagram for One I/O Line

The MAX13030E–MAX13035E have internal current sources capable of sourcing 30µA to pullup the I/O lines. These internal pullup current sources allow the inputs to be driven with open-drain drivers, as well as push-pull drivers. It is not recommended to use external pullup resistors on the I/O lines. The architecture of the MAX13030E–MAX13035E permit either side to be driven with a minimum of 4mA drivers or larger.

Output Load Requirements

The MAX13030E–MAX13035E I/O are designed to drive CMOS inputs. Do not load the I/O lines with a resistive load less than 25kΩ and do not place an RC circuit at the input of these devices to slow down the edges. If a slower rise/fall time is required, refer to the MAX3000E/ MAX3001E logic-level translator datasheet. For I²C level translation, refer to the MAX3372E–MAX3379E/ MAX3390E–MAX3393E datasheet.

Shutdown Mode

The MAX13030E–MAX13034E feature an enable (EN) input that places the device into a low-power shutdown mode when driven low. The MAX13030E–MAX13035E features an automatic shutdown mode that disables the part when V_{CC} is missing or less than V_L.

Clock Return (CLK_RET)

The MAX13035E features a CLK_RET output that returns the clock signal applied to CLK_V_L. CLK_V_L and CLK_V_{CC} are identical to the other I/O channels, the only difference being that CLK_V_{CC} is internally tied to the V_{CC} side of CLK_RET (see the *Functional Diagram*).

Application Information

Layout Recommendations

Use standard high-speed layout practices when laying out a board with the MAX13030E–MAX13035E. For example, to minimize line coupling, place all other signal lines not connected to the MAX13030E–MAX13035E at least 1x the substrate height of the PCB away from the input and output lines of the MAX13030E–MAX13035E.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_L and V_{CC} to ground with 0.1µF ceramic capacitors. Place all capacitors as close as possible to the power-supply inputs. For full ESD protection, bypass V_{CC} with a 1µF ceramic capacitor located as close as possible to the V_{CC} input.

Unidirectional vs. Bidirectional Level Translator

The MAX13030E–MAX13035E bidirectional level translators can operate as a unidirectional device to translate signals without inversion. These devices provide the smallest solution (UCSP package) for unidirectional level translation without inversion.

Use with External Pullup/Pulldown Resistors

Due to the architecture of the MAX13030E–MAX13035E, it is not recommended to use external pullup or pulldown resistors on the bus. In certain applications, the use of external pullup or pulldown resistors is desired to have a known bus state when there is no active driver on the bus. For example, this may happen when interfacing to a memory card slot with no memory card inserted. The MAX13030E–MAX13035E include internal pullup current sources that set the bus state when the device is enabled. In shutdown mode, the state of I/O V_{CC}_ and I/O V_L_ is dependent on the selected part version (see *Ordering Information/ Selector Guide* for further information).

Open-Drain Signaling

The MAX13030E–MAX13035E are designed to pass open-drain as well as CMOS push-pull signals. When used with open-drain signaling, the rise time is dominated by the interaction of the internal pullup current source and the parasitic load capacitance. The MAX13030E–MAX13035E include internal rise time accelerators to speed up transitions, eliminating any need for external pullup resistors.

SD Card Detection

SD, MiniSD, MMC and similar types of cards provide detection of a card through a pullup resistor on one of the DAT lines, or by use of a mechanical switch. This pullup resistor is internal to the memory card itself. The MAX13030E–MAX13035E only support detection of a memory card through a mechanical switch, and it is recommended that the internal resistor for card detection be switched off by the command interface. For example, when using SD cards, the command SET_CLR_CARD_DETECT (ACMD42) disables this resistor.

UCSP Applications Information

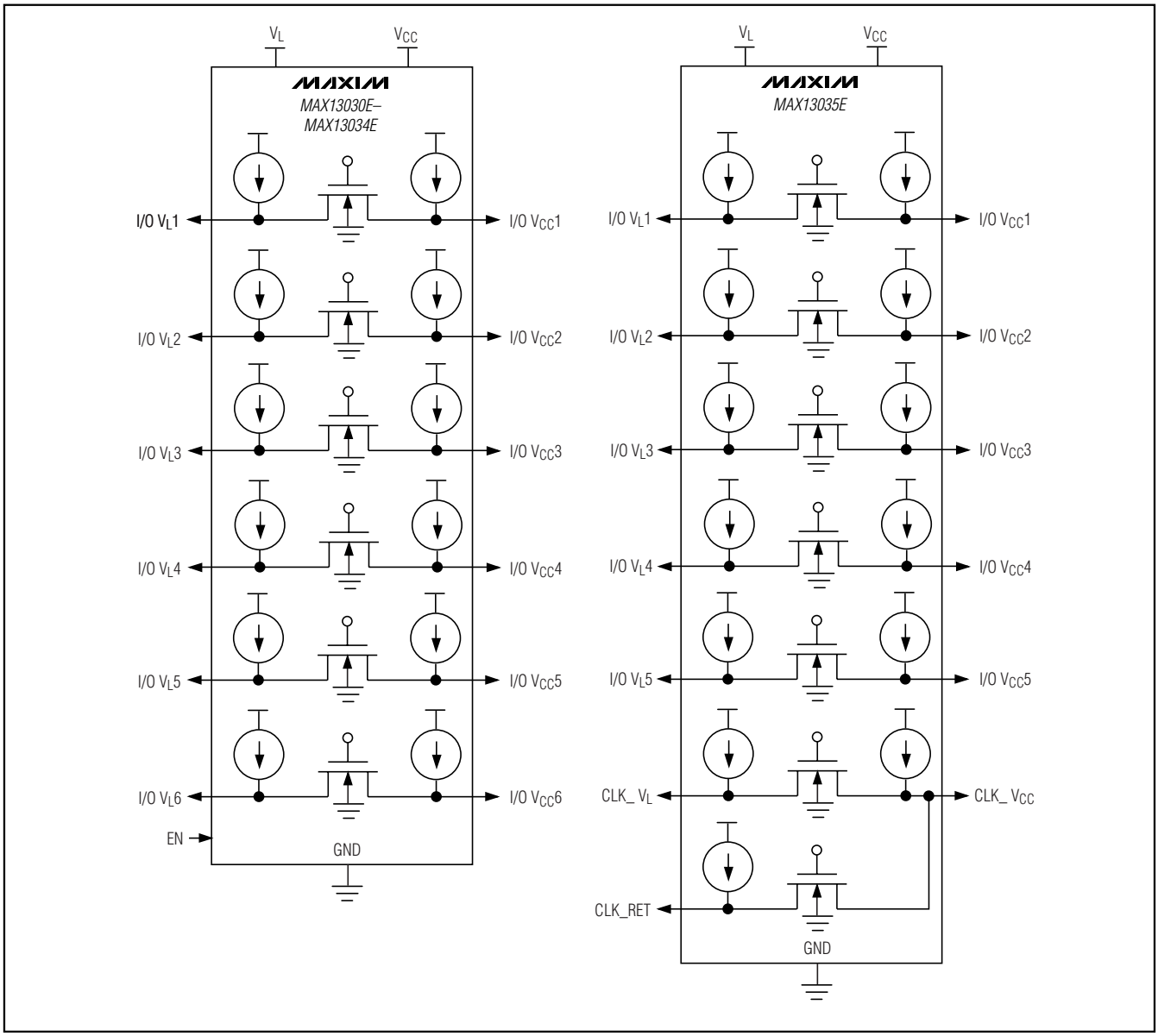
For the latest application details on UCSP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profiles, as well as the latest information on reliability testing results, go to Maxim's web site at www.maxim-ic.com/ucsp to find the Application Note: *UCSP – A Wafer-Level Chip-Scale Package.*

Chip Information

Process: BiCMOS

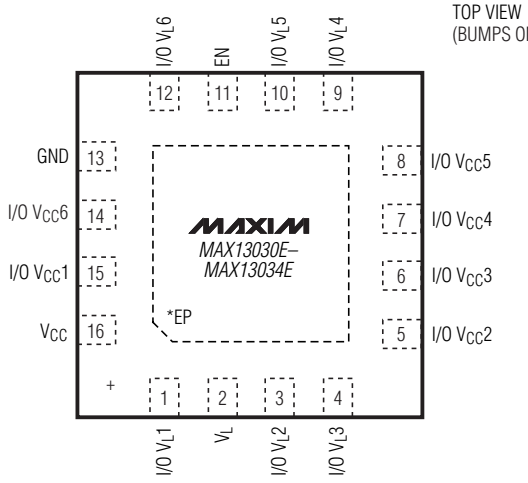
6-Channel High-Speed Logic-Level Translators

Functional Diagram



Pin Configurations

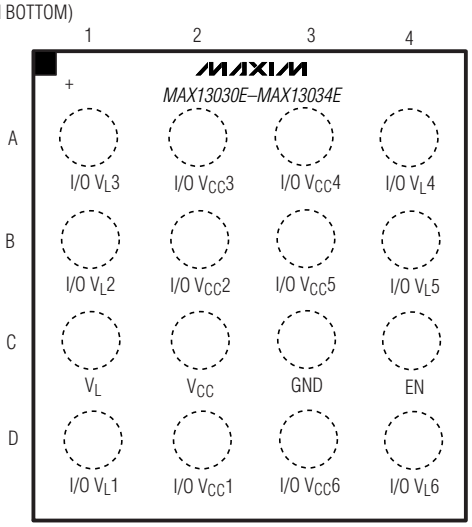
TOP VIEW



16 TQFN (4mm x 4mm)

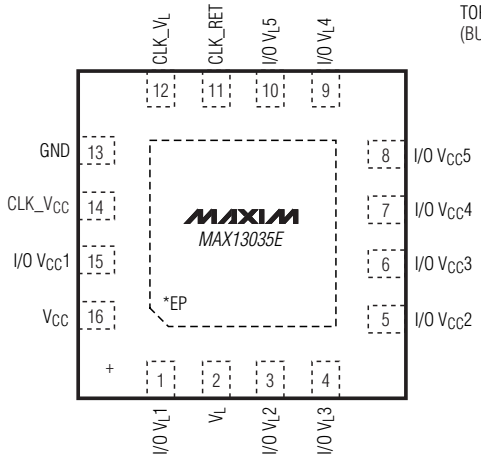
*CONNECT EXPOSED PADDLE TO GROUND

TOP VIEW
(BUMPS ON BOTTOM)



16 UCSP (2mm x 2mm)

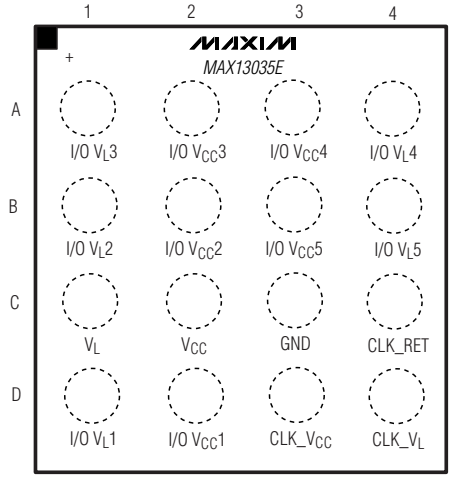
TOP VIEW



16 TQFN (4mm x 4mm)

*CONNECT EXPOSED PADDLE TO GROUND

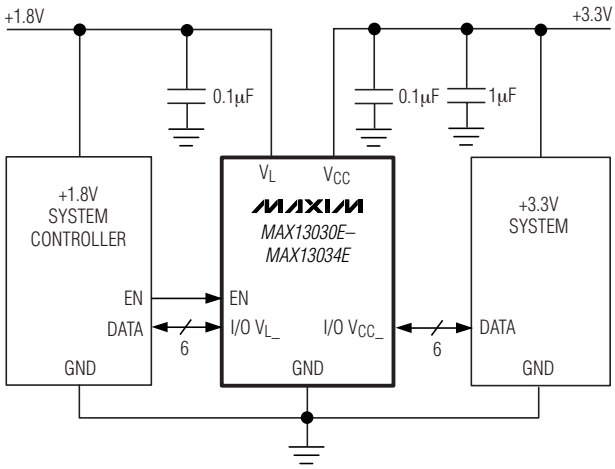
TOP VIEW
(BUMPS ON BOTTOM)



16 UCSP (2mm x 2mm)

6-Channel High-Speed Logic-Level Translators

Typical Operating Circuits (continued)



Ordering Information/Selector Guide (continued)

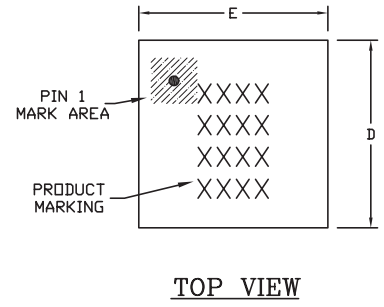
PART	PIN-PACKAGE	I/O $V_{L\_}$ STATE DURING SHUTDOWN	I/O $V_{CC\_}$ STATE DURING SHUTDOWN	PKG CODE
MAX13031EEBE+*	16 UCSP	High impedance	16.5kΩ to V_{CC}	B16-1
MAX13031EETE+*	16 TQFN-EP**	High impedance	16.5kΩ to V_{CC}	T1644-4
MAX13032EEBE+	16 UCSP	High impedance	16.5kΩ to GND	B16-1
MAX13032EETE+	16 TQFN-EP**	High impedance	16.5kΩ to GND	T1644-4
MAX13033EEBE+*	16 UCSP	16.5kΩ to GND	High impedance	B16-1
MAX13033EETE+*	16 TQFN-EP**	16.5kΩ to GND	High impedance	T1644-4
MAX13034EEBE+*	16 UCSP	16.5kΩ to GND	16.5kΩ to GND	B16-1
MAX13034EETE+*	16 TQFN-EP**	16.5kΩ to GND	16.5kΩ to GND	T1644-4
MAX13035EEBE+	16 UCSP	75kΩ to V_L	High impedance	B16-1
MAX13035EETE+	16 TQFN-EP**	75kΩ to V_L	High impedance	T1644-4

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*
+Denotes a lead-free package.
***EP = Exposed paddle.*

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

16L,UCSP.EPS

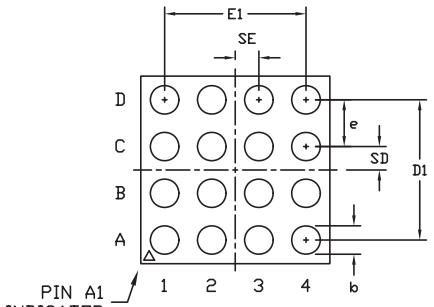


TOP VIEW

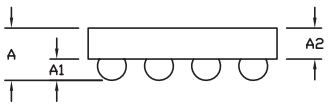
COMMON DIMENSIONS	
A	0.62±0.05–0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B16-1	2.02±0.05	2.02±0.05	NONE
B16-2	2.02±0.05	2.02±0.05	B3, C3
B16-3	2.02±0.05	2.02±0.05	B3, C2
B16-4	2.02±0.05	2.02±0.05	B2, C3
B16-5	2.02±0.05	2.02±0.05	B2, B3, C2, C3
B16-6	2.02±0.05	2.02±0.05	C3

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

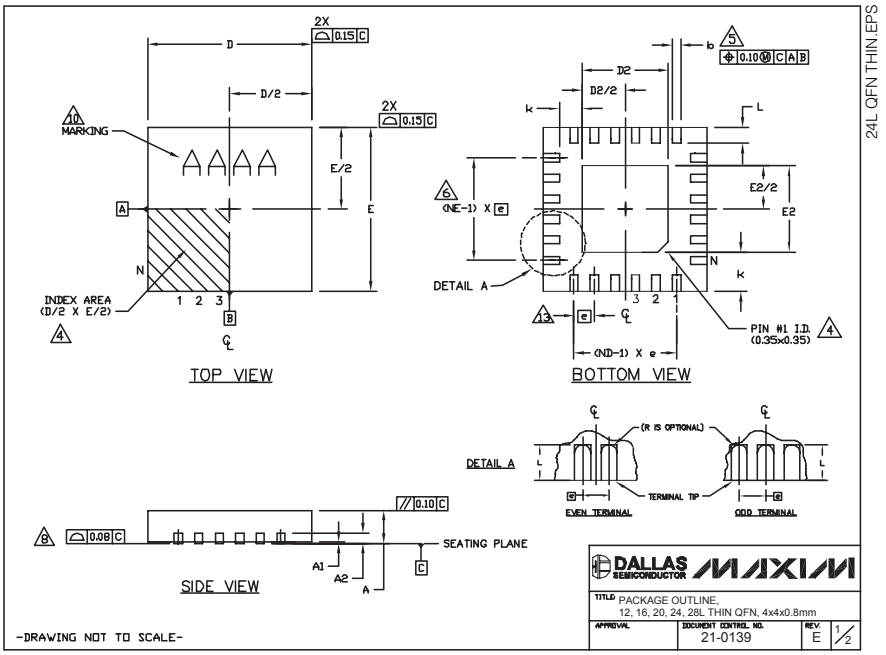
TITLE: PACKAGE OUTLINE, 4x4 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0101	H	1/1

6-Channel High-Speed Logic-Level Translators

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
JEDEC VAR.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444–3, T2444–4 AND T2844–1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0139
REV. E
2/2