400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

ABSOLUTE MAXIMUM RATINGS

$V_{DD\_}$ to GND ..... -0.3V to +6V
V_{DD1} to V_{DD2} ..... -0.3V to +0.3V
CH0–CH7, COM to GND..... -0.3V to (V_{DD1} + 0.3V)
REF, REFADJ to GND ..... -0.3V to (V_{DD1} + 0.3V)
Digital Inputs to GND ..... -0.3V to +6V
Digital Outputs to GND ..... -0.3V to (V_{DD2} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 7.0mW/°C above +70°C) 559mW
Operating Temperature Ranges
MAX128_BCUP..... 0°C to +70°C
MAX128_BEUP ..... -40°C to +85°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX1280

(V_{DD1} = V_{DD2} = +4.5V to +5.5V, COM = GND, f_{SCLK} = 6.4MHz, 50% duty cycle, 16 clocks/conversion cycle (400ksps), external +2.5V at REF, REFADJ = V_{DD1}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL				±1.0	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1.0	LSB
Offset Error					±6.0	LSB
Gain Error (Note 3)					±7.0	LSB
Gain-Error Temperature Coefficient				±0.8		ppm/°C
Channel-to-Channel Offset-Error Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (100kHz sine-wave input, 2.5Vp-p, 400ksps, 6.4MHz clock, bipolar input mode)						
Signal-to-Noise plus Distortion Ratio	SINAD			70		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-81		dB
Spurious-Free Dynamic Range	SFDR			80		dB
Intermodulation Distortion	IMD	f_{IN1} = 99kHz, f_{IN2} = 102kHz		76		dB
Channel-to-Channel Crosstalk (Note 4)		f_{IN} = 200kHz, V_{IN} = 2.5Vp-p		-78		dB
Full-Power Bandwidth		-3dB point		6		MHz
Full-Linear Bandwidth		SINAD > 68dB		350		kHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}		2.5			µs
Track/Hold Acquisition Time	t_{ACQ}				468	ns
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Serial Clock Frequency	f_{SCLK}		0.5		6.4	MHz
Duty Cycle			40		60	%

ELECTRICAL CHARACTERISTICS—MAX1280 (continued)

(V_{DD1} = V_{DD2} = +4.5V to +5.5V, COM = GND, f_{SCLK} = 6.4MHz, 50% duty cycle, 16 clocks/conversion cycle (400ksps), external +2.5V at REF, REFADJ = V_{DD1}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS (CH7–CH0, COM)						
Input Voltage Range, Single-Ended and Differential (Note 6)	$V_{CH\_}$	Unipolar, V_{COM} = 0			V_{REF}	V
		Bipolar, V_{COM} or $V_{CH\_}$ = $V_{REF}/2$, referenced to COM or CH_			$\pm V_{REF}/2$	
Multiplexer Leakage Current		On/off leakage current, $V_{CH\_}$ = 0 or V_{DD1}		±0.001	±1	µA
Input Capacitance				18		pF
INTERNAL REFERENCE						
REF Output Voltage	V_{REF}	T_A = +25°C	2.480	2.500	2.520	V
REF Short-Circuit Current				30		mA
REF Output Temperature Coefficient	TC V_{REF}			±15		ppm/°C
Load Regulation (Note 7)		0 to 1mA output load		0.1	2.0	mV/mA
Capacitive Bypass at REF			4.7		10	µF
Capacitive Bypass at REFADJ			0.01		10	µF
REFADJ Output Voltage				1.22		V
REFADJ Input Range		For small adjustments, from 1.22V		±50		mV
REFADJ Buffer Disable Threshold		To power down the internal reference	1.33		V_{DD1}	V
Buffer Voltage Gain				2.05		V/V
EXTERNAL REFERENCE (Reference buffer disabled, reference applied to REF)						
REF Input Voltage Range		(Note 8)	1.0		V_{DD1} + 50mV	V
REF Input Current		V_{REF} = 2.500V, f_{SCLK} = 6.4MHz		200	350	µA
		V_{REF} = 2.500V, f_{SCLK} = 0			320	
		In power-down, f_{SCLK} = 0			5	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
Input High Voltage	V_{INH}		3.0			V
Input Low Voltage	V_{INL}				0.8	V
Input Hysteresis	V_{HYST}			0.2		V
Input Leakage	I_{IN}	V_{IN} = 0 or V_{DD2}			±1	µA
Input Capacitance	C_{IN}			15		pF
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 5V		15		pF

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

ELECTRICAL CHARACTERISTICS—MAX1280 (continued)

(V_{DD1} = V_{DD2} = +4.5V to +5.5V, COM = GND, f_{SCLK} = 6.4MHz, 50% duty cycle, 16 clocks/conversion cycle (400ksps), external +2.5V at REF, REFADJ = V_{DD1}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Positive Supply Voltage (Note 9)	V_{DD1}, V_{DD2}			4.5		5.5	V
Supply Current	I_{VDD1} + I_{VDD2}	V_{DD1} = V_{DD2} = 5.5V	Operating mode (Note 10)		2.5	4.0	mA
			Reduced-power mode (Note 11)		1.3	2.0	
			Fast power-down (Note 11)		0.9	1.5	
			Full power-down (Note 11)		2	10	µA
Power-Supply Rejection	PSR	V_{DD1} = V_{DD2} = 5V ±10%, midscale input			±0.5	±2.0	mV

ELECTRICAL CHARACTERISTICS—MAX1281

(V_{DD1} = V_{DD2} = +2.7V to +3.6V, COM = GND, f_{SCLK} = 4.8MHz, 50% duty cycle, 16 clocks/conversion cycle (300ksps), external +2.5V at REF, REFADJ = V_{DD1}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL				±1.0	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1.0	LSB
Offset Error					±6.0	LSB
Gain Error (Note 3)					±7.0	LSB
Gain-Error Temperature Coefficient				±1.6		ppm/°C
Channel-to-Channel Offset-Error Matching				±0.2		LSB
DYNAMIC SPECIFICATIONS (75kHz sine-wave input, 2.5Vp-p, 300ksps, 4.8MHz clock, bipolar input mode)						
Signal-to-Noise plus Distortion Ratio	SINAD			70		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-81		dB
Spurious-Free Dynamic Range	SFDR			80		dB
Intermodulation Distortion	IMD	f_{IN1} = 73kHz, f_{IN2} = 77kHz		76		dB
Channel-to-Channel Crosstalk (Note 4)		f_{IN} = 150kHz, V_{IN} = 2.5Vp-p		-78		dB
Full-Power Bandwidth		-3dB point		3		MHz
Full-Linear Bandwidth		SINAD > 68dB		250		kHz

ELECTRICAL CHARACTERISTICS—MAX1281 (continued)

(V_{DD1} = V_{DD2} = +2.7V to +3.6V, COM = GND, f_{SCLK} = 4.8MHz, 50% duty cycle, 16 clocks/conversion cycle (300ksps), external +2.5V at REF, REFADJ = V_{DD1}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Normal operating mode	3.3			µs
Track/Hold Acquisition Time	t_{ACQ}	Normal operating mode			625	ns
Aperture Delay				10		ns
Aperture Jitter				< 50		ps
Serial Clock Frequency	f_{SCLK}	Normal operating mode	0.5		4.8	MHz
Duty Cycle			40		60	%
ANALOG INPUTS (CH7–CH0, COM)						
Input Voltage Range, Single-Ended and Differential (Note 6)	$V_{CH\_}$	Unipolar, V_{COM} = 0			V_{REF}	V
		Bipolar, V_{COM} or $V_{CH\_}$ = $V_{REF}/2$, referenced to COM or CH_			$\pm V_{REF}/2$	
Multiplexer Leakage Current		On/off leakage current, $V_{CH\_}$ = 0 or V_{DD1}		±0.001	±1	µA
Input Capacitance				18		pF
INTERNAL REFERENCE						
REF Output Voltage	V_{REF}	T_A = +25°C	2.480	2.500	2.520	V
REF Short-Circuit Current				15		mA
REF Output Temperature Coefficient	TC V_{REF}			±15		ppm/°C
Load Regulation (Note 7)		0 to 0.75mA output load		0.1	2.0	mV/mA
Capacitive Bypass at REF			4.7		10	µF
Capacitive Bypass at REFADJ			0.01		10	µF
REFADJ Output Voltage				1.22		V
REFADJ Input Range		For small adjustments, from 1.22V		±50		mV
REFADJ Buffer Disable Threshold		To power down the internal reference	1.33		V_{DD1} - 1	V
Buffer Voltage Gain				2.05		V/V
EXTERNAL REFERENCE (Reference buffer disabled, reference applied to REF)						
REF Input Voltage Range		(Note 8)	1.0		V_{DD1} + 50mV	V
REF Input Current		V_{REF} = 2.500V, f_{SCLK} = 4.8MHz		200	350	µA
		V_{REF} = 2.500V, f_{SCLK} = 0			320	
		In power-down, f_{SCLK} = 0			5	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
Input High Voltage	V_{INH}		2.0			V
Input Low Voltage	V_{INL}				0.8	V
Input Hysteresis	V_{HYST}			0.2		V
Input Leakage	I_{IN}	V_{IN} = 0 or V_{DD2}			±1	µA
Input Capacitance	C_{IN}			15		pF

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

ELECTRICAL CHARACTERISTICS—MAX1281 (continued)

(V_{DD1} = V_{DD2} = +2.7V to +3.6V, COM = GND, f_{SCLK} = 4.8MHz, 50% duty cycle, 16 clocks/conversion cycle (300ksps), external +2.5V at REF, REFADJ = V_{DD1}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD2} - 0.5V			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 3V				±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 3V			15		pF
POWER SUPPLY							
Positive Supply Voltage (Note 9)	V_{DD1}, V_{DD2}			2.7		3.6	V
Supply Current (Note 10)	I_{VDD1} + I_{VDD2}	V_{DD1} = V_{DD2} = 3.6V	Operating mode		2.5	3.5	mA
			Reduced-power mode (Note 11)		1.3	2.0	
			Fast power-down (Note 11)		0.9	1.5	
			Full power-down (Note 11)		2	10	µA
Power-Supply Rejection	PSR	V_{DD1} = V_{DD2} = 2.7V to 3.6V, midscale input			±0.5	±2.0	mV

TIMING CHARACTERISTICS—MAX1280

(Figures 1, 2, 6, 7; V_{DD1} = V_{DD2} = +4.5V to +5.5V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Period	t_{CP}		156			ns
SCLK Pulse Width High	t_{CH}		62			ns
SCLK Pulse Width Low	t_{CL}		62			ns
DIN to SCLK Setup	t_{DS}		35			ns
DIN to SCLK Hold	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		35			ns
SCLK Rise to $\overline{CS}$ Rise Hold	t_{CSH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Ignore	t_{CSO}		35			ns
$\overline{CS}$ Rise to SCLK Rise Ignore	t_{CS1}		35			ns
SCLK Rise to DOUT Hold	t_{DOH}	C_{LOAD} = 20pF	10	20		ns
SCLK Rise to SSTRB Hold	t_{STH}	C_{LOAD} = 20pF	10	20		ns
SCLK Rise to DOUT Valid	t_{DOV}	C_{LOAD} = 20pF			80	ns
SCLK Rise to SSTRB Valid	t_{STV}	C_{LOAD} = 20pF			80	ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 20pF	10		65	ns
$\overline{CS}$ Rise to SSTRB Disable	t_{STD}	C_{LOAD} = 20pF	10		65	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 20pF			65	ns
$\overline{CS}$ Fall to SSTRB Enable	t_{STE}	C_{LOAD} = 20pF			65	ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

TIMING CHARACTERISTICS—MAX1281

(Figures 1, 2, 6, 7; V_{DD1} = V_{DD2} = +2.7V to +3.6V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Period	t_{CP}		208			ns
SCLK Pulse Width High	t_{CH}		83			ns
SCLK Pulse Width Low	t_{CL}		83			ns
DIN to SCLK Setup	t_{DS}		45			ns
DIN to SCLK Hold	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		45			ns
SCLK Rise to $\overline{CS}$ Rise Hold	t_{CSH}		0			ns
SCLK Rise to $\overline{CS}$ Fall ignore	t_{CSO}		45			ns
$\overline{CS}$ Rise to SCLK Rise Ignore	t_{CS1}		45			ns
SCLK Rise to DOUT Hold	t_{DOH}	C_{LOAD} = 20pF	13	20		ns
SCLK Rise to SSTRB Hold	t_{STH}	C_{LOAD} = 20pF	1	20		ns
SCLK Rise to DOUT Valid	t_{DOV}	C_{LOAD} = 20pF			100	ns
SCLK Rise to SSTRB Valid	t_{STV}	C_{LOAD} = 20pF			100	ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 20pF	13		85	ns
$\overline{CS}$ Rise to SSTRB Disable	t_{STD}	C_{LOAD} = 20pF	13		85	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 20pF			85	ns
$\overline{CS}$ Fall to SSTRB Enable	t_{STE}	C_{LOAD} = 20pF			85	ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: MAX1280 tested at V_{DD1} = V_{DD2} = +5V, MAX1281 tested at V_{DD1} = V_{DD2} = +3V; COM = GND; unipolar single-ended input mode.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain error and offset error have been nulled.

Note 3: Offset nulled.

Note 4: Ground “on” channel; sine wave applied to all “off” channels.

Note 5: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.

Note 6: The absolute voltage range for the analog inputs (CH7–CH0, and COM) is from GND to V_{DD1}.

Note 7: External load should not change during conversion for specified accuracy. Guaranteed specification of 2mV/mA is a result of production test limitations.

Note 8: ADC performance is limited by the converter’s noise floor, typically 300µVp-p.

Note 9: Electrical characteristics are guaranteed from $V_{DD1(MIN)}$ = $V_{DD2(MIN)}$ to $V_{DD1(MAX)}$ = $V_{DD2(MAX)}$. For operations beyond this range, see the *Typical Operating Characteristics*. For guaranteed specifications beyond the limits, contact the factory.

Note 10: A_{IN} = midscale. Unipolar mode. MAX1280 tested with 20pF on DOUT, 20pF on SSTRB, and f_{SCLK} = 6.4MHz, 0 to 5V. MAX1281 tested with same loads, f_{SCLK} = 4.8MHz, 0 to 3V. DOUT = FFF hex.

Note 11:

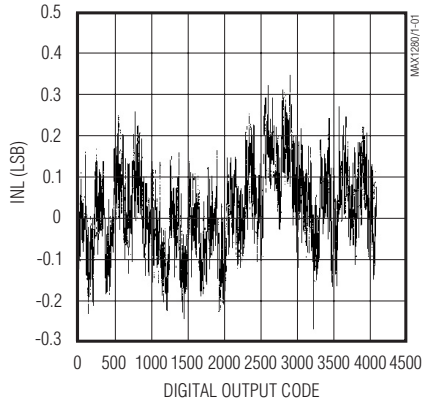
PD1	PD0	MODE
0	0	Full power-down.
0	1	Fast power-down.
1	0	Reduced power mode.
1	1	Normal operation (operating mode).

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

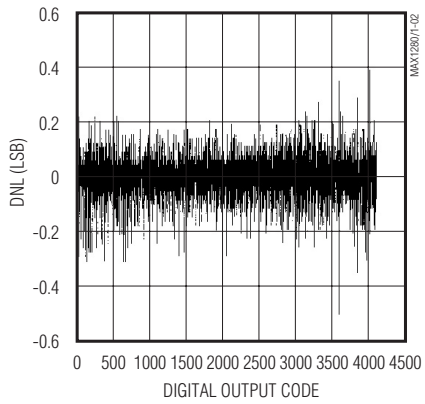
Typical Operating Characteristics

(MAX1280: V_{DD1} = V_{DD2} = 5.0V, f_{SCLK} = 6.4MHz; MAX1281: V_{DD1} = V_{DD2} = 3.0V, f_{SCLK} = 4.8MHz; C_{LOAD} = 20pF, 4.7µF capacitor at REF, 0.01µF capacitor at REFADJ, T_A = +25°C, unless otherwise noted.)

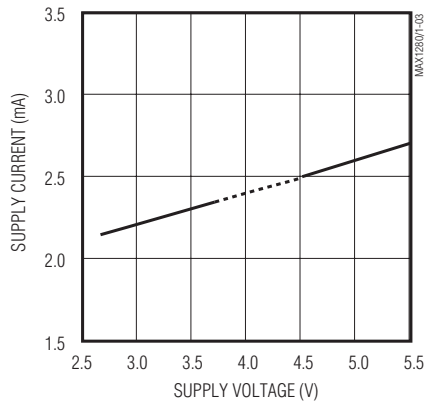
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



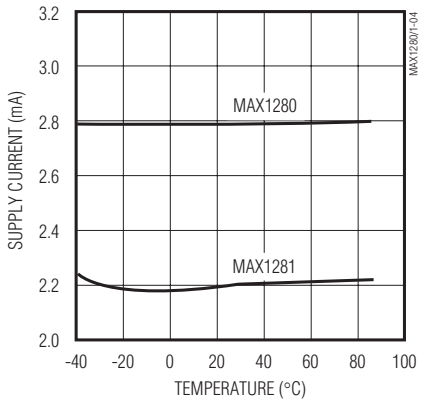
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



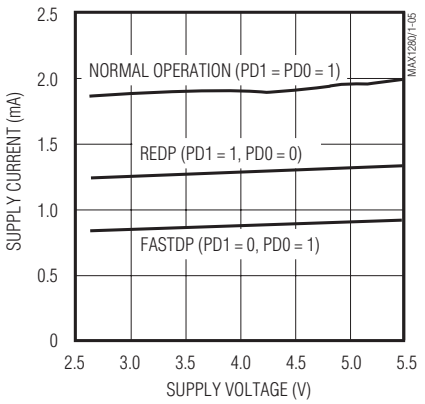
SUPPLY CURRENT vs. SUPPLY VOLTAGE (CONVERTING)



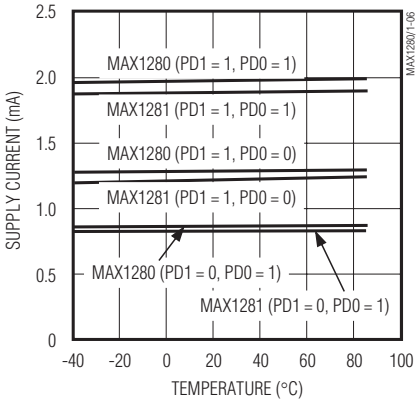
SUPPLY CURRENT vs. TEMPERATURE



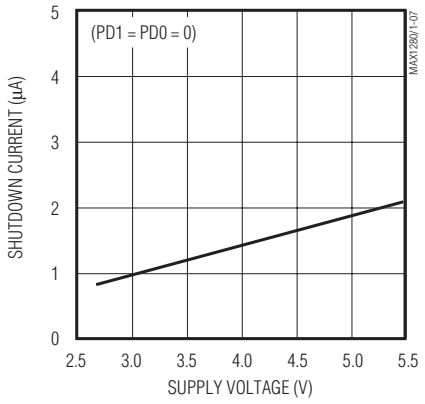
SUPPLY CURRENT vs. SUPPLY VOLTAGE (STATIC)



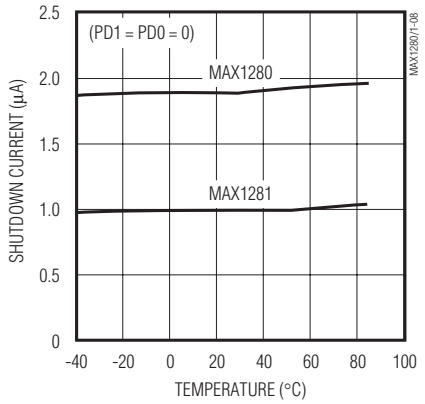
SUPPLY CURRENT vs. TEMPERATURE (STATIC)



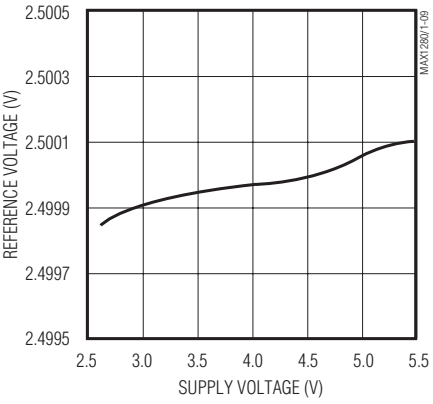
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



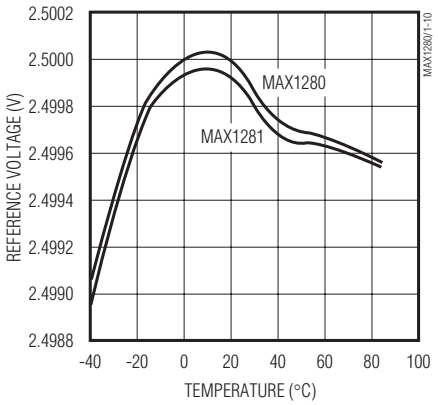
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



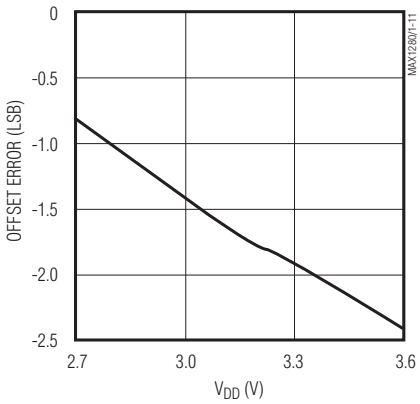
Typical Operating Characteristics (continued)

(MAX1280: $V_{DD1} = V_{DD2} = 5.0V$, $f_{SCLK} = 6.4MHz$; MAX1281: $V_{DD1} = V_{DD2} = 3.0V$, $f_{SCLK} = 4.8MHz$; $C_{LOAD} = 20pF$, 4.7µF capacitor at REF, 0.01µF capacitor at REFADJ, $T_A = +25°C$, unless otherwise noted.)

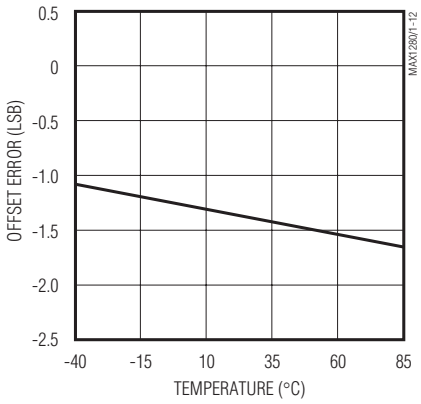
REFERENCE VOLTAGE vs. TEMPERATURE



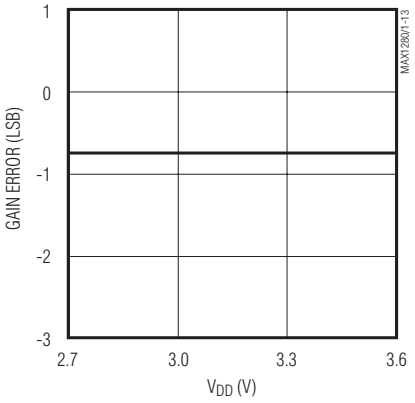
OFFSET ERROR vs. SUPPLY VOLTAGE



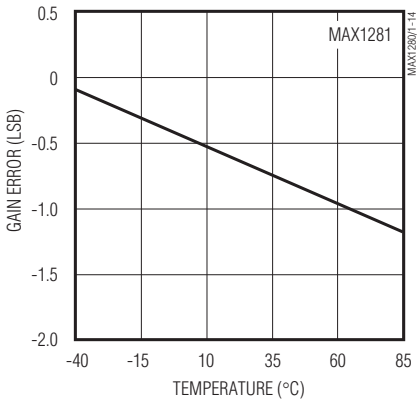
OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE



400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	COM	Ground Reference for Analog Inputs. COM sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	$\overline{SHDN}$	Active-Low Shutdown Input. Pulling $\overline{SHDN}$ low shuts down the device, reducing supply current to 2µA (typ).
11	REF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode, the reference buffer provides a +2.500V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD1}.
12	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD1}.
13	GND	Analog and Digital Ground
14	DOUT	Serial Data Output. Data is clocked out at SCLK's rising edge. High impedance when $\overline{CS}$ is high.
15	SSTRB	Serial Strobe Output. SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high.
16	DIN	Serial Data Input. Data is clocked in at SCLK's rising edge.
17	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT and SSTRB are high impedance.
18	SCLK	Serial Clock Input. Clocks data in and out of the serial interface and sets the conversion speed. (Duty cycle must be 40% to 60%.)
19	V_{DD2}	Positive Supply Voltage
20	V_{DD1}	Positive Supply Voltage

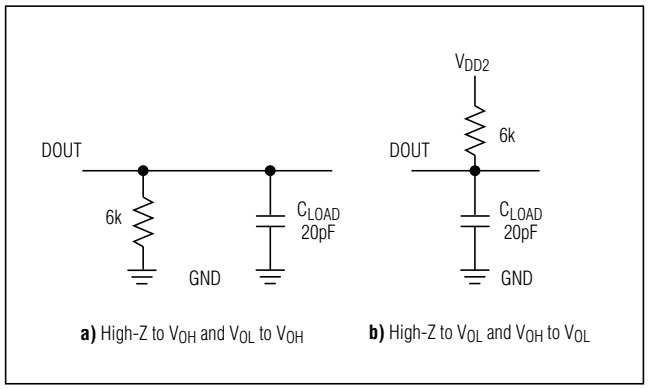


Figure 1. Load Circuits for Enable Time

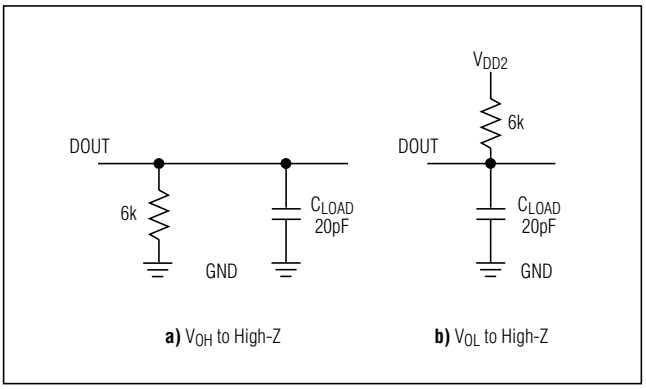


Figure 2. Load Circuits for Disable Time

Detailed Description

The MAX1280/MAX1281 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 shows a functional diagram of the MAX1280/MAX1281.

Pseudo-Differential Input

The equivalent input circuit of Figure 4 shows the MAX1280/MAX1281's input architecture, which is composed of a T/H, input multiplexer, input comparator, switched-capacitor DAC, and reference.

In single-ended mode, the positive input (IN+) is connected to the selected input channel and the negative input (IN-) is set to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels according to Tables 2 and 3.

The MAX1280/MAX1281 input configuration is pseudo-differential in that only the signal at IN+ is sampled. The return side (IN-) is connected to the sampling capacitor while converting and must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to GND during a conversion.

If a varying signal is applied to the selected IN-, its amplitude and frequency must be limited to maintain accuracy. The following equations determine the relationship between the maximum signal amplitude and its frequency in order to maintain ±0.5LSB accuracy. Assuming a sinusoidal signal at IN-, the input voltage is determined by:

$$v_{IN-} = (V_{IN-}) \sin(2\pi ft)$$

The maximum voltage variation is determined by:

$$\max \frac{dv_{IN-}}{d_t} = (V_{IN-})\, 2\pi f \le \frac{1LSB}{t_{CONV}} = \frac{V_{REF}}{2^{12} t_{CONV}}$$

A 650mVp-p 60Hz signal at IN- will generate ±0.5LSB of error when using a +2.5V reference voltage and a 2.5µs conversion time ($15/f_{SCLK}$). When a DC reference voltage is used at IN-, connect a 0.1µF capacitor to GND to minimize noise at the input.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+. The conversion interval begins with the input multiplexer switching C_{HOLD} from IN+ to IN-. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to $V_{DD1}/2$ within the limits of 12-bit resolution. This action is equivalent to transferring a 12pF x (V_{IN+} - V_{IN-}) charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

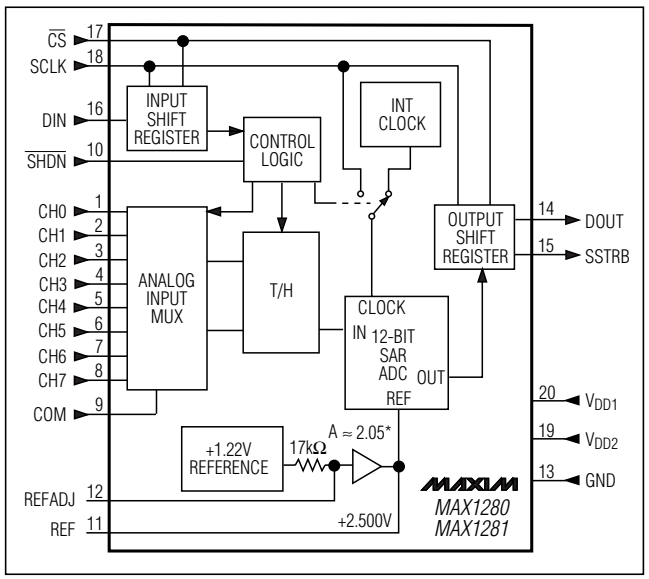


Figure 3. Functional Diagram

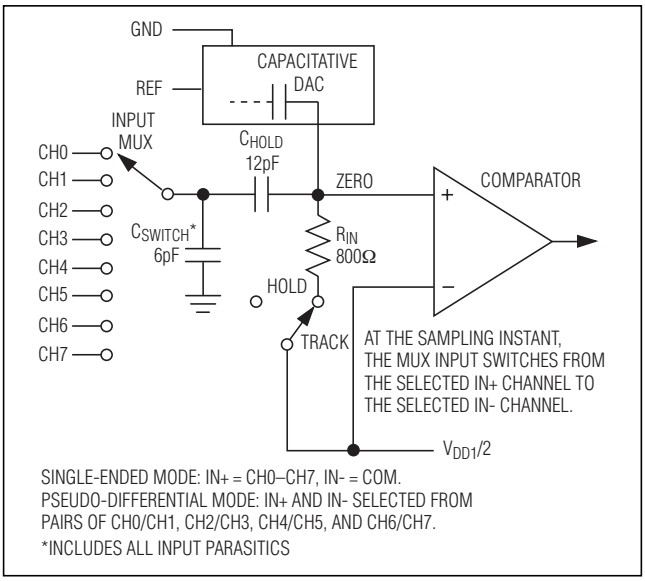


Figure 4. Equivalent Input Circuit

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM and the converter converts the "+" input. If the converter is set up for differential inputs, the difference of [(IN+) - (IN-)] is converted. At the end of the conversion, the positive input connects back to IN+ and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal and is also the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 12pF$$

where R_{IN} = 800Ω, R_S = the source impedance of the input signal; t_{ACQ} is never less than 468ns (MAX1280) or 625ns (MAX1281). Note that source impedances below 2kΩ do not significantly affect the ADC's AC performance.

Input Bandwidth

The ADC's input tracking circuitry has a 6MHz (MAX1280) or 3MHz (MAX1281) small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD1} and GND, allow the channel input pins to swing from GND - 0.3V to V_{DD1} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD1} by more than 50mV or be lower than GND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not allow the input current to exceed 2mA.

Quick Look

To quickly evaluate the MAX1280/MAX1281's analog performance, use the circuit of Figure 5. The MAX1280/MAX1281 require a control byte to be written to DIN before each conversion. Connecting DIN to V_{DD2} feeds in control bytes of $FF (HEX), which trigger single-ended unipolar conversions on CH7 without powering down between conversions. The SSTRB output pulses

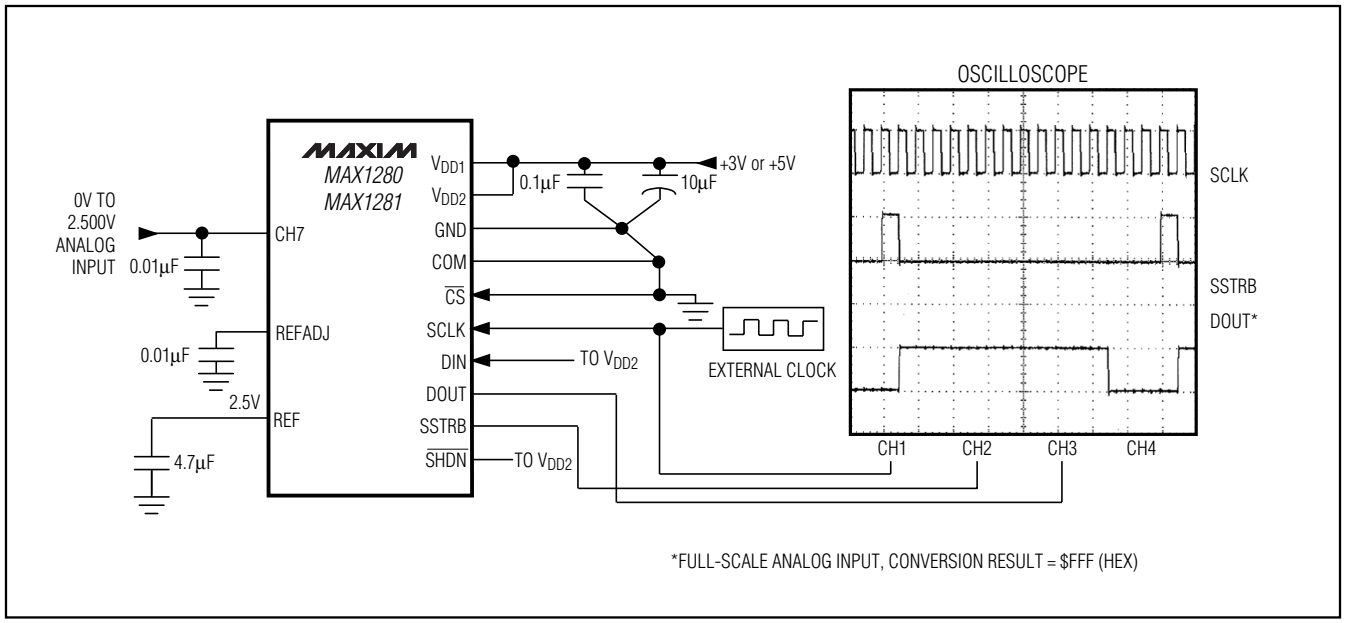


Figure 5. Quick-Look Circuit

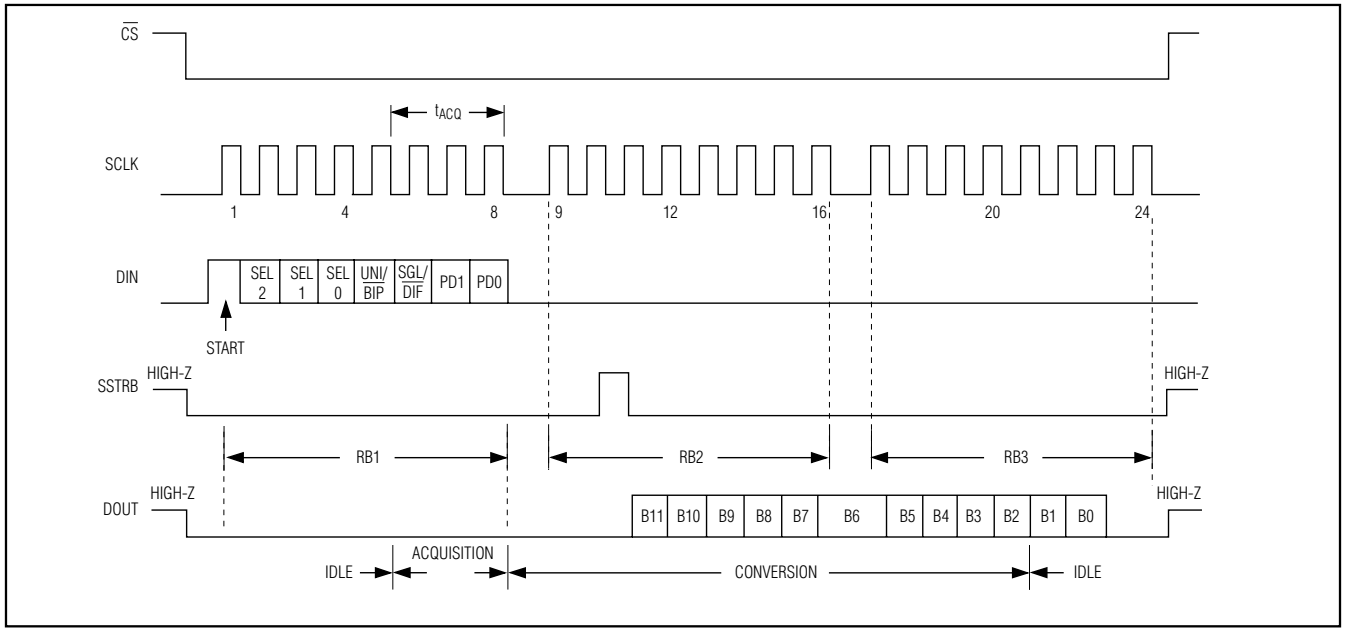


Figure 6. Single-Conversion Timing

high for one clock period before the MSB of the 12-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 will alter the sequence of bits from DOUT. A total of 16 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs typically occur 20ns after the rising edge of SCLK.

Starting a Conversion

Start a conversion by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1280/MAX1281's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1280/MAX1281 are compatible with SPI/QSPI and MICROWIRE devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. MICROWIRE, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result). See Figure 17 for MAX1280/MAX1281 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode, so the CPU generates the serial clock. Choose a clock frequency from 500kHz to 6.4MHz (MAX1280) or 4.8MHz (MAX1281).

1) Set up the control byte and call it TB1. TB1 should be of the format 1XXXXXXX binary, where the Xs denote the particular channel, selected conversion mode, and power mode.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion, padded with three leading zeros and one trailing zero. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 14). For bipolar input mode, the output is two's complement (Figure 15). Data is clocked out on the rising edge of SCLK in MSB-first format.

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/BIP	SGL/DIF	PD1	PD0

BIT	NAME	DESCRIPTION
7 (MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion (Tables 2 and 3).
3	UNI/BIP	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0 to V_{REF} can be converted; in bipolar mode, the differential signal can range from $-V_{REF}/2$ to $+V_{REF}/2$.
2	SGL/DIF	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0 (LSB)	PD1 PD0	Select operating mode. **PD1 PD0 Mode** 0 0 Full power-down 0 1 Fast power-down 1 0 Reduced Power 1 1 Normal Operation

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
0	0	1			+						–
0	1	0					+				–
0	1	1							+		–
1	0	0		+							–
1	0	1				+					–
1	1	0						+			–
1	1	1								+	–

Table 3. Channel Selection in Psuedo-Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

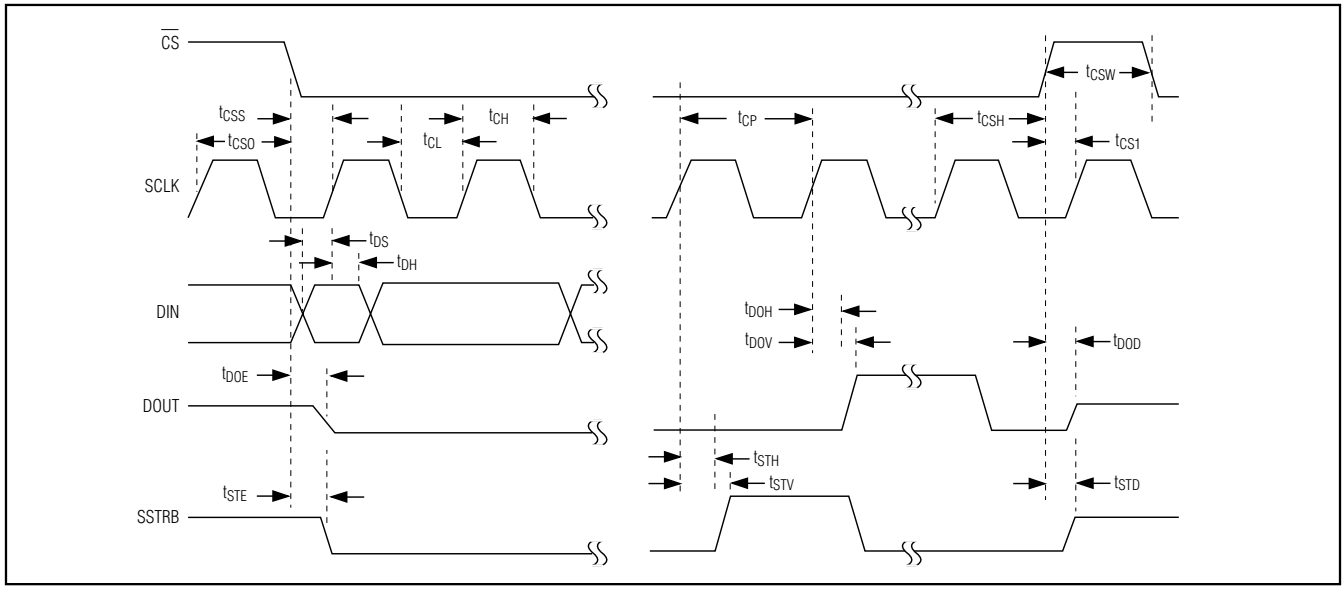


Figure 7. Detailed Serial-Interface Timing

Serial Clock

The external serial clock not only shifts data in and out, but also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ rising edge, SSTRB outputs a logic low. Figure 7 shows the detailed serial-interface timing.

The conversion must complete in 120µs or less, or droop on the sample-and-hold capacitors may degrade conversion results.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as follows:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle, e.g., after V_{DD1} and V_{DD2} are applied.

OR

The first high bit clocked into DIN after bit 6 of a conversion in progress is clocked onto the DOUT pin.

Once a start bit has been recognized, the current conversion may only be terminated by pulling $\overline{SHDN}$ low.

The fastest the MAX1280/MAX1281 can run with $\overline{CS}$ held low between conversions is 16 clocks per conversion. Figure 8 shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1280/MAX1281 in normal operating mode, ready to convert with SSTRB = low. The MAX1280/MAX1281 require 10µs to reset after the power supplies stabilize; no conversions should be initiated during this time. If $\overline{CS}$ is low, the first logic 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. Additionally, wait for the reference to stabilize when using the internal reference.

Power Modes

You can save power by placing the converter in one of the two low-current operating modes or in full power-down between conversions. Select the power mode through bit 1 and bit 0 of the DIN control byte (Tables 1 and 4), or force the converter into hardware shutdown by driving $\overline{SHDN}$ to GND.

The software power-down modes take effect after the conversion is completed; $\overline{SHDN}$ overrides any software power mode and immediately stops any conversion in

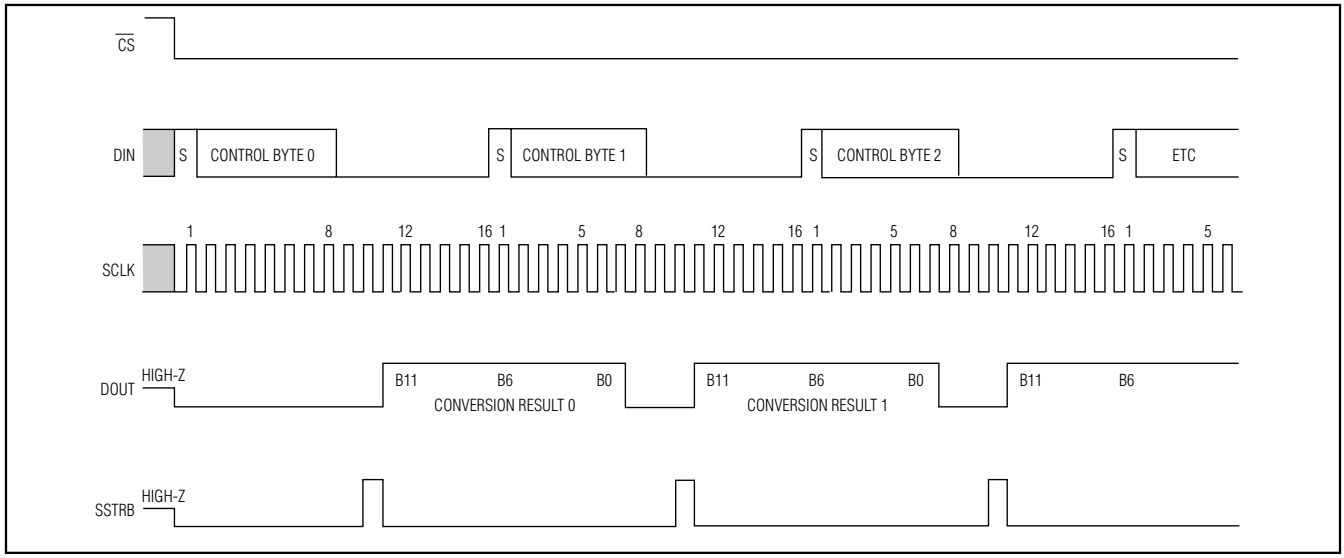


Figure 8. Continuous 16-Clock/Conversion Timing

Table 4. Software-Controlled Power Modes

PD1/PD0	MODE	TOTAL SUPPLY CURRENT		CIRCUIT SECTIONS*	
		CONVERTING	AFTER CONVERSION	INPUT COMPARATOR	REFERENCE
00	Full Power-Down (FULLPD)	2.5mA	2µA	Off	Off
01	Fast Power-Down (FASTPD)	2.5mA	0.9mA	Reduced Power	On
10	Reduced-Power Mode (REDPD)	2.5mA	1.3mA	Reduced Power	On
11	Operating Mode	2.5mA	2.0mA	Full Power	On

**Circuit operation between conversions; during conversion, all circuits are fully powered up.*

progress. In software power-down mode, the serial interface remains active, waiting for a new control byte to start conversion and switch to full-power mode. Once the conversion is completed, the device goes into the programmed power mode until a new control byte is written.

The power-up delay is dependent on the power-down state. Software low-power modes will be able to start conversion immediately when running at decreased clock rates (see *Power-Down Sequencing*). During power-on reset, when exiting software full power-down mode or exiting hardware shutdown, the device goes immediately into full-power mode and is ready to convert after 2µs when using an external reference. When using the internal reference, wait for the typical power-up delay from a full power-down (software or hardware), as shown in Figure 9.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. When software shutdown is asserted, the ADC completes the conversion in progress and powers down into the specified low-quiescent-current state (2µA, 0.9mA, or 1.3mA).

The first logic 1 on DIN is interpreted as a start bit and puts the MAX1280/MAX1281 into their full-power mode. Following the start bit, the data input word or control byte also determines the next power-down state. For example, if the DIN word contains PD1 = 0 and PD0 = 1, a 0.9mA power-down starts after the conversion.

Table 4 details the four power modes with the corresponding supply current and operating sections. For data rates achievable in software power-down modes, see *Power-Down Sequencing* section.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down. Unlike software power-down mode, the conversion is terminated immediately. When returning to normal operation from $\overline{SHDN}$ with an external reference, the MAX1280/MAX1281 can be considered fully powered-up within 2µs of actively pulling $\overline{SHDN}$ high. When using the internal reference, the conversion should be initiated only after the reference has settled; its recovery time depends on the external bypass capacitors and shutdown duration.

Power-Down Sequencing

The MAX1280/MAX1281's automatic power-down modes can save considerable power when operating at less than maximum sample rates. Figures 10 and 11 show the average supply current as a function of the sampling rate.

Using Full Power-Down Mode

Full power-down mode (FULLPD) achieves the lowest power consumption at up to 1000 conversions per channel per second. Figure 10a shows the MAX1281's power consumption for 1- or 8-channel conversions using full power-down mode (PD1 = PD0 = 0), with the internal reference and the maximum clock speed. A 0.01µF bypass capacitor plus the internal 17kΩ reference resistor at REFADJ forms an RC filter with a 200µs time constant. To achieve full 12-bit accuracy, 10 time constants or 2ms are required after power-up if the bypass capacitor is fully discharged between conversions. Waiting this 2ms in FASTPD mode or reduced-power mode (REDP) instead of full power-down mode can further reduce power consumption. This is achieved by using the sequence shown in Figure 12a.

Figure 10b shows the MAX1281's power consumption for 1- or 8-channel conversions using FULLPD mode (PD1 = PD0 = 0), an external reference, and the maximum clock speed. One dummy conversion to power-up the device is needed, but no wait-time is necessary to start the second conversion, thereby achieving lower power consumption at up to the full sampling rate.

Using Fast Power-Down and Reduced-Power Modes

FASTPD and REDP modes achieve the lowest power consumption at speeds close to the maximum sample rate. Figure 11 shows the MAX1281's power consumption in FASTPD mode (PD1 = 0, PD0 = 1), REDP mode (PD1 = 1, PD0 = 0), and (for comparison) normal operating mode (PD1 = 1, PD0 = 1). The figure shows

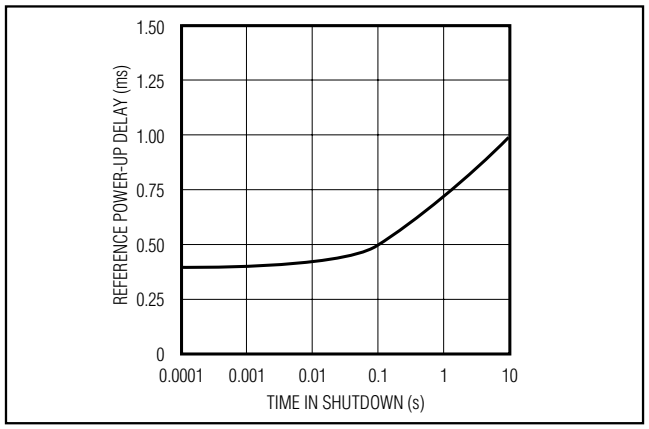


Figure 9. Reference Power-Up Delay vs. Time in Shutdown

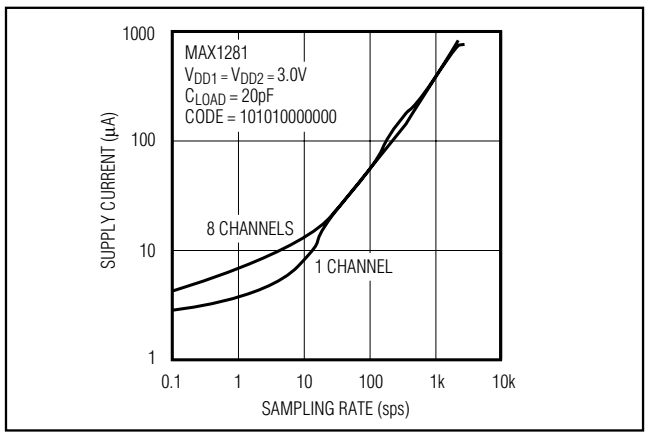


Figure 10a. Average Supply Current vs. Sample Rate (Using FULLPD and Internal Reference)

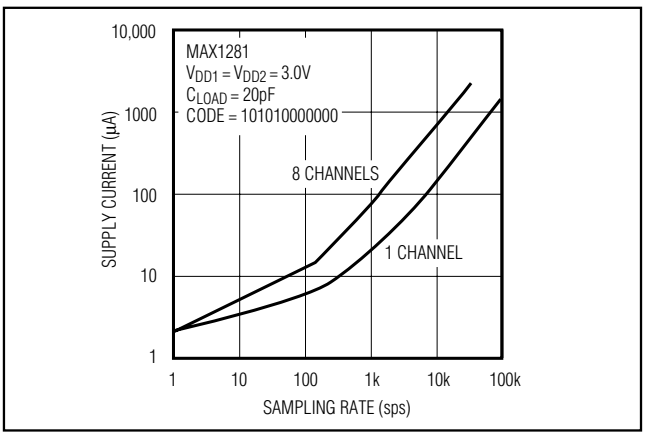


Figure 10b. Average Supply Current vs. Sampling Rate (Using FULLPD and External Reference)

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

power consumption using the specified power-down mode, with the internal reference and the maximum clock speed. The clock speed in FASTPD or REDP should be limited to 4.8MHz for the MAX1280/MAX1281. FULLPD mode may provide increased power savings in applications where the MAX1280/MAX1281 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

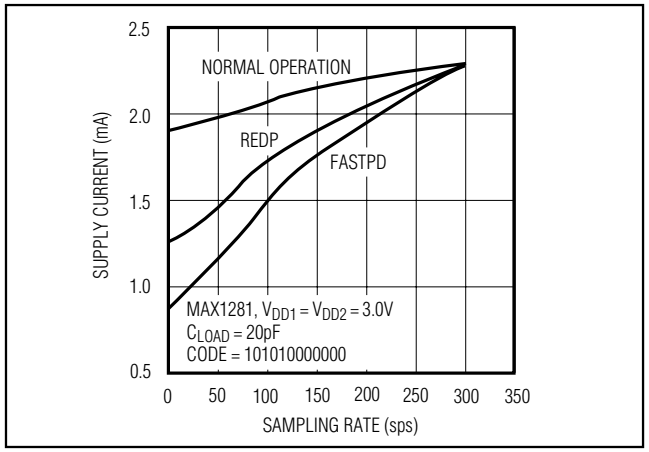


Figure 11. Average Supply Current vs. Sampling Rate (Using REPD, FASTPD, and Normal Operation and Internal Reference)

Internal and External References

The MAX1280/MAX1281 can be used with an internal or external reference. An external reference can be connected directly at REF or at the REFADJ pin.

An internal buffer is designed to provide 2.5V at REF for both the MAX1280/MAX1281. The internally trimmed 1.22V reference is buffered with a gain of +2.05V/V.

Internal Reference

The MAX1280/MAX1281's full-scale range with the internal reference is 2.5V for unipolar inputs and ±1.25V for bipolar inputs. The internal reference voltage is adjustable to ±100mV with the circuit of Figure 13.

External Reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 17kΩ. At REF, the DC input resistance is a minimum of

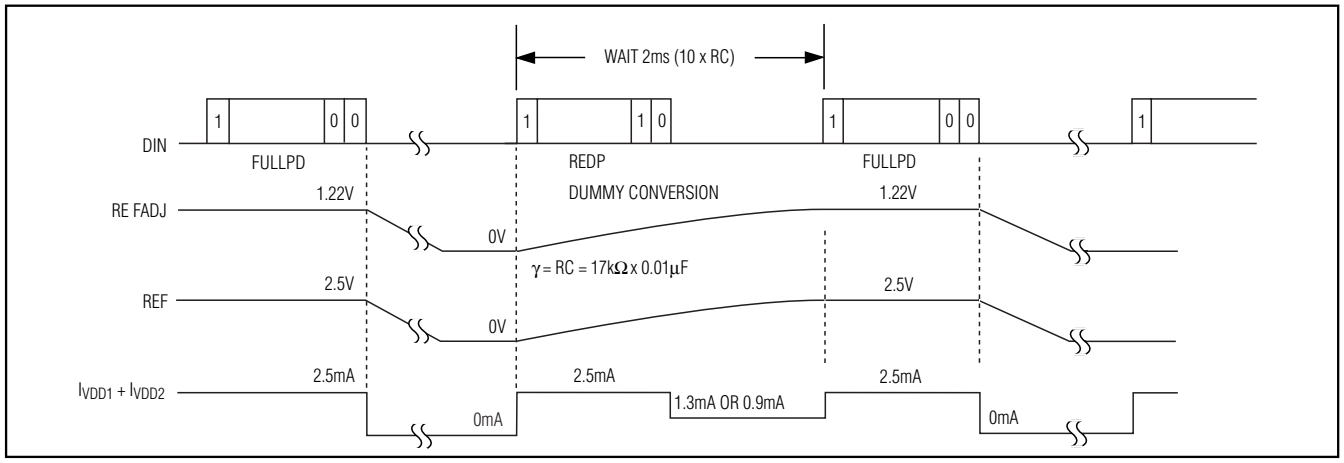


Figure 12a. Full Power-Down Timing

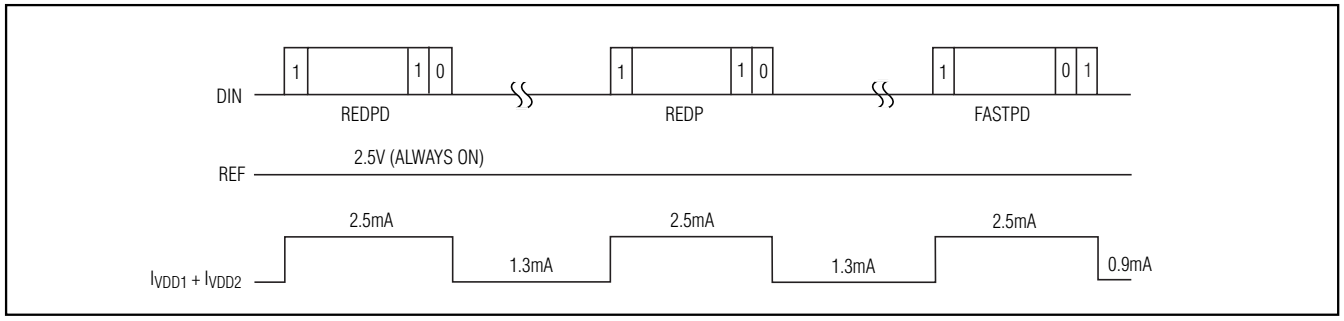


Figure 12b. Reduced-Power/Fast Power-Down Timing

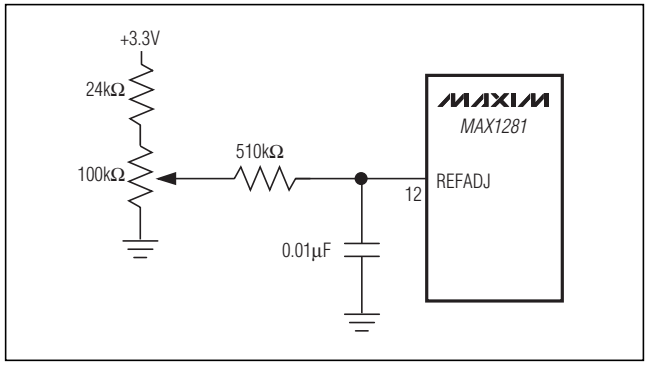


Figure 13. MAX1281 Reference-Adjust Circuit

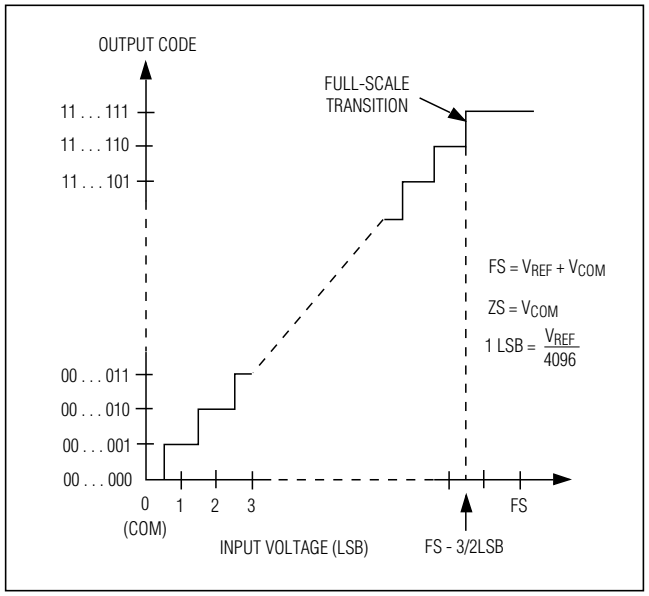


Figure 14. Unipolar Transfer Function, Full Scale (FS) = V_{REF} + V_{COM}, Zero Scale (ZS) = V_{COM}

18kΩ. During conversion, an external reference at REF must deliver up to 350µA DC load current and have 10Ω or less output impedance. If the reference has a higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

Using the REFADJ input makes buffering the external reference unnecessary. To use the direct REF input, disable the internal buffer by connecting REFADJ to V_{DD1}.

Transfer Function

Table 5 shows the full-scale voltage ranges for unipolar and bipolar modes. Figure 14 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 15 shows the bipolar I/O transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 610µV for unipolar and bipolar operation.

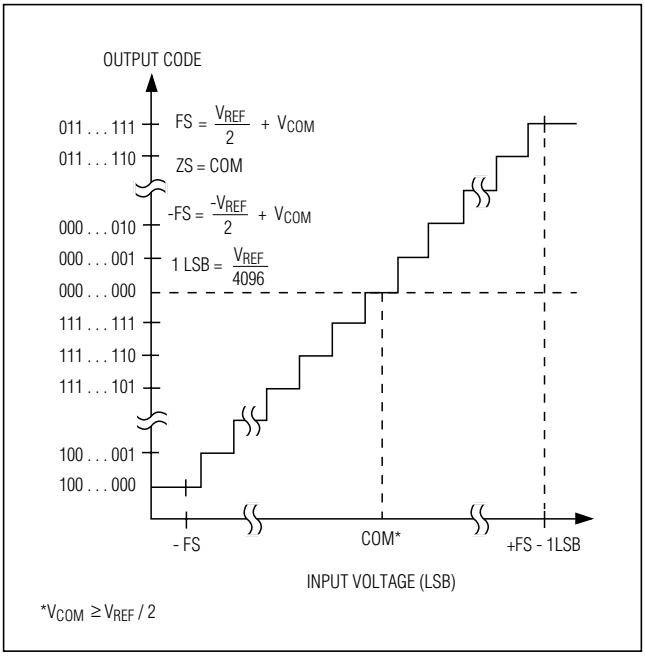


Figure 15. Bipolar Transfer Function, Full Scale (FS) = V_{REF} / 2 + V_{COM}, Zero Scale (ZS) = V_{COM}

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards; wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 16 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at GND. Connect all analog grounds to the star ground. Connect the digital system ground to star ground at this point only. For lowest-noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

High-frequency noise in the V_{DD1} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 10µF capacitors, located close to pin 20 of the MAX1280/MAX1281. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 16).

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

Table 5. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
$V_{REF} + V_{COM}$	COM	$V_{REF} / 2 + V_{COM}$	V_{COM}	$-V_{REF} / 2 + V_{COM}$

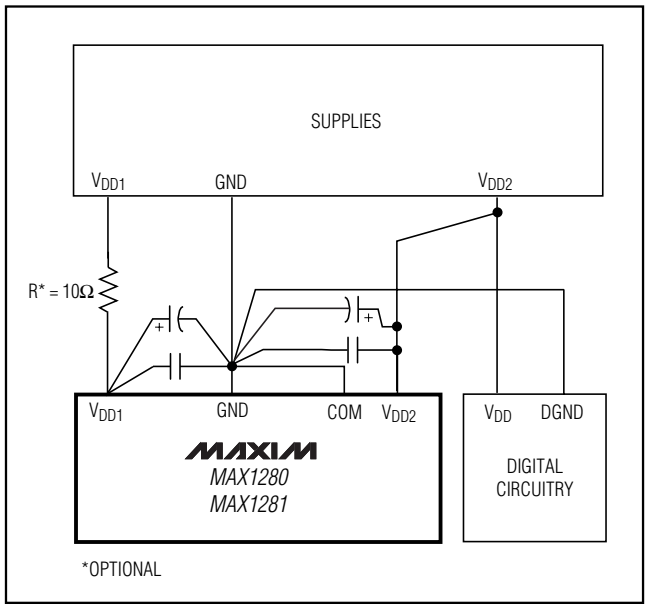


Figure 16. Power-Supply Grounding Connection

High-Speed Digital Interfacing with QSPI

The MAX1280/MAX1281 can interface with QSPI using the circuit in Figure 17 (f_{SCLK} = 4.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own microsequencer.

TMS320LC3x Interface

Figure 18 shows an application circuit that interfaces the MAX1280/MAX1281 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 19.

Use the following steps to initiate a conversion in the MAX1280/MAX1281 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and with CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are connected with the MAX1280/MAX1281's SCLK input.
2) The MAX1280/MAX1281's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX1280/MAX1281's DIN pin.
3) An 8-bit word (1XXXXX11) should be written to the MAX1280/MAX1281 to initiate a conversion and place the device into normal operating mode. See Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1280/MAX1281's SSTRB output is monitored through the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1280/MAX1281.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1280/MAX1281 until the next conversion is initiated.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1280/MAX1281 are measured using the endpoint method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

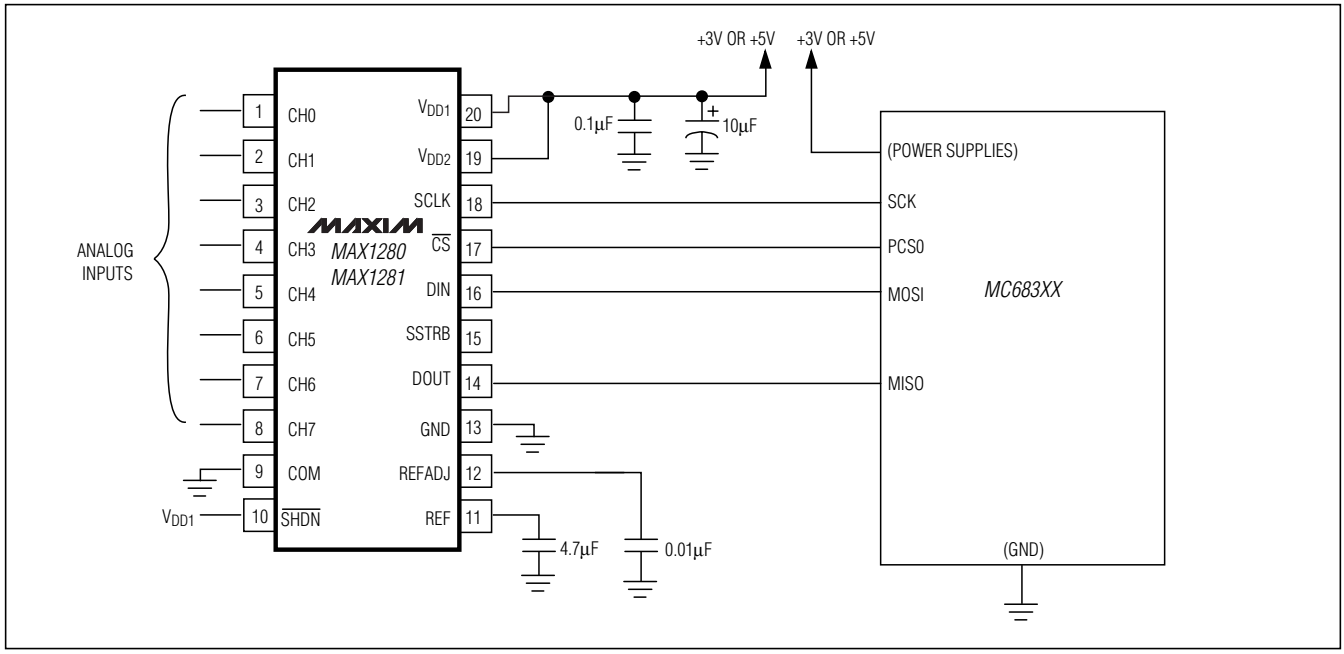


Figure 17. QSPI Connections

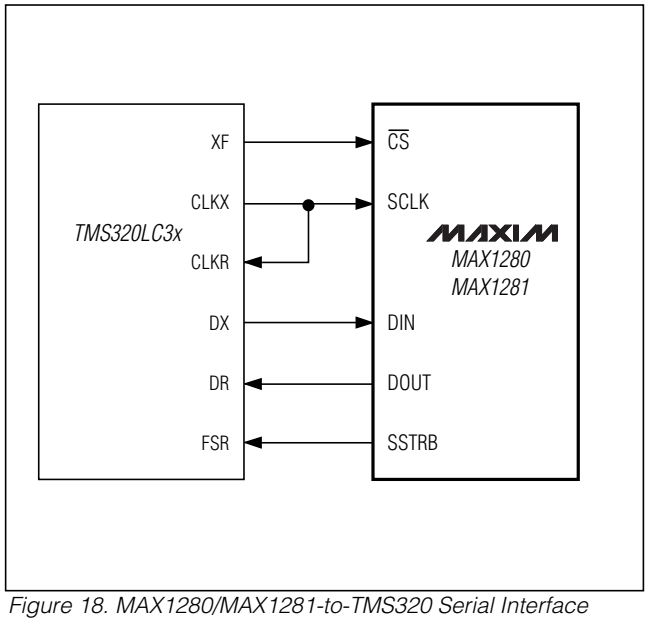


Figure 18. MAX1280/MAX1281-to-TMS320 Serial Interface

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, Signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is calculated by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise ratio plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD\ (dB) = 20 \times \log\ (Signal_{RMS} / Noise_{RMS})$$

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

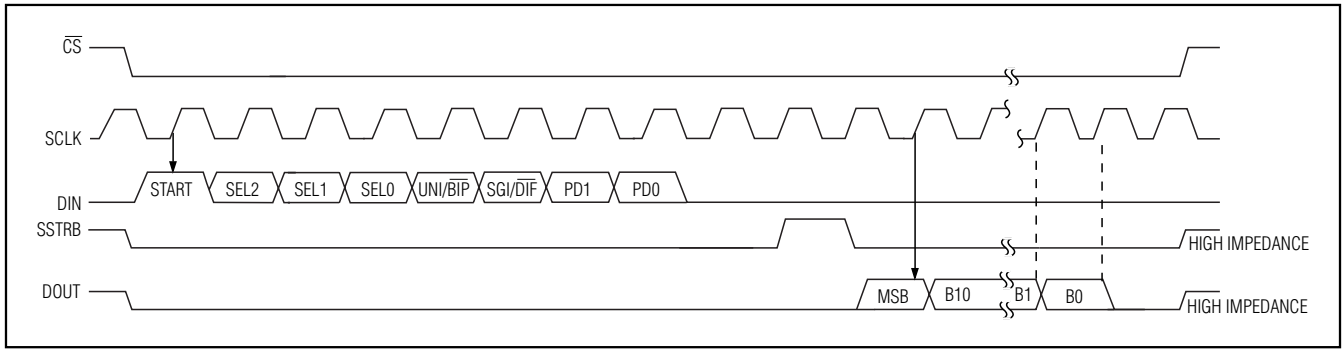


Figure 19. MAX1280/MAX1281-to-TMS320 Serial Interface

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

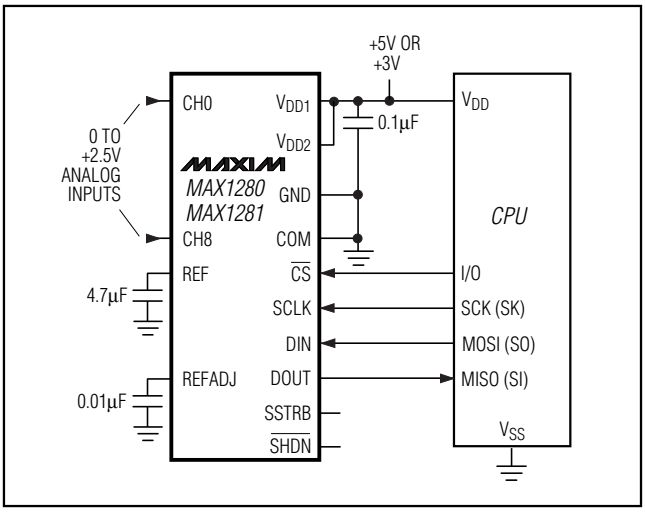
$$THD = 20 \times \log \frac{\left(\sqrt{V_2^2 + V_3^2 + V_4^2 + V_4^2 + V_5^2}\right)}{V_1}$$

where V_1 is the fundamental amplitude, and V_2 through V5 are the amplitudes of the 2nd- through 5th-order harmonics, respectively.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
20 TSSOP	U20+2	21-0066

400ksps/300ksps, Single-Supply, Low-Power, 8-Channel, Serial 12-Bit ADCs with Internal Reference

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/00	Initial release	—
1	4/10	Changed specifications due to single pass flow qualifications and added lead-free information	1–5
2	10/10	Changed multiplexer leakage current condition, added note to supply current condition, changed Note 11, changed Figures 4 and 12b	5, 6, 7, 11, 18