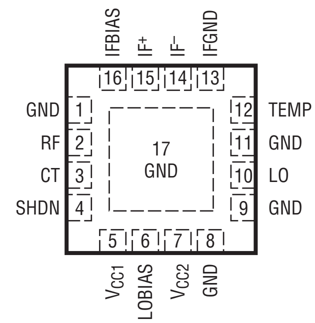
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Mixer Supply Voltage (V_{CC1}, V_{CC2})..........................4.0V
IF Supply Voltage (IF^+, IF^-) 5.5V
Shutdown Voltage (SHDN)................–0.3V to V_{CC} +0.3V
IF Bias Adjust Voltage (IFBIAS).........–0.3V to V_{CC} +0.3V
LO Bias Adjust Voltage (LOBIAS)......–0.3V to V_{CC} +0.3V
LO Input Power (4GHz to 6GHz)..........................+9dBm
LO Input DC Voltage...±0.1V
RF Input Power (4GHz to 6GHz)........................ +15dBm
RF Input DC Voltage...±0.1V
TEMP Diode Continuous DC Input Current............10mA
TEMP Diode Input Voltage ....±1V
Operating Temperature Range (T_C)........–40°C to 105°C
Storage Temperature Range ....–65°C to 150°C
Junction Temperature (T_J) .... 150°C

PIN CONFIGURATION

TOP VIEW



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5544IUF#PBF	LTC5544IUF#TRPBF	5544	16-Lead (4mm x 4mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_C = 25°C, P_{LO} = 2dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LO Input Frequency Range			4200 to 5800		MHz
RF Input Frequency Range	Low Side LO High Side LO		4200 to 6000 4000 to 5800		MHz MHz
IF Output Frequency Range	Requires External Matching		5 to 1000		MHz
RF Input Return Loss	Z_O = 50Ω, 4000MHz to 6000MHz		>12		dB
LO Input Return Loss	Z_O = 50Ω, 4200MHz to 5800MHz		>12		dB
IF Output Impedance	Differential at 240MHz		332Ω‖1.7pF		R‖C
LO Input Power	f_{LO} = 4200MHz to 5800MHz	–1	2	5	dBm
LO to RF Leakage	f_{LO} = 4200MHz to 5800MHz, Requires C2		<–30		dBm
LO to IF Leakage	f_{LO} = 4200MHz to 5800MHz		<–21		dBm
RF to LO Isolation	f_{RF} = 4000MHz to 6000MHz		>38		dB
RF to IF Isolation	f_{RF} = 4000MHz to 6000MHz		>29		dB

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_C = 25°C, P_{LO} = 2dBm, P_{RF} = –3dBm (–3dBm/tone for 2-tone tests),unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3)

Low Side LO Downmixer Application: RF = 4200MHz to 6000MHz, IF = 240MHz, $f_{LO} = f_{RF} – f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 4900MHz RF = 5250MHz RF = 5800MHz	 6.0 	7.9 7.4 6.4		dB
Conversion Gain Flatness	RF = 5250MHz ±30MHz, LO = 5010MHz, IF = 240 ±30MHz		±0.15		dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, RF = 5250MHz		–0.007		dB/°C
2-Tone Input 3rd Order Intercept (Δf = 2MHz)	RF = 4900MHz RF = 5250MHz RF = 5800MHz		25.4 25.9 25.8		dBm
2-Tone Input 2nd Order Intercept (Δf = 241MHz, $f_{IM2} = f_{RF1} – f_{RF2}$)	f_{RF1} = 5371MHz, f_{RF2} = 5130MHz, f_{LO} = 5010MHz		43.2		dBm
SSB Noise Figure	RF = 4900MHz RF = 5250MHz RF = 5800MHz		10.3 11.3 12.8		dB
SSB Noise Figure Under Blocking	f_{RF} = 5250MHz, f_{LO} = 5010MHz, f_{BLOCK} = 4910MHz, P_{BLOCK} = 5dBm		16.9		dB
2RF – 2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/2$)	f_{RF} = 5130MHz at –10dBm, f_{LO} = 5010MHz, f_{IF} = 240MHz		–58.3		dBc
3RF – 3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/3$)	f_{RF} = 5090MHz at –10dBm, f_{LO} = 5010MHz, f_{IF} = 240MHz		–77		dBc
Input 1dB Compression	RF = 5250MHz, V_{CCIF} = 3.3V RF = 5250MHz, V_{CCIF} = 5V		11.4 14.6		dBm

High Side LO Downmixer Application: RF = 4000MHz to 5800MHz, IF = 240MHz, $f_{LO} = f_{RF} + f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 4500MHz RF = 4900MHz RF = 5250MHz		8.0 7.7 7.3		dB
Conversion Gain Flatness	RF = 4900MHz ±30MHz, LO = 5356MHz, IF = 456 ±30MHz		±0.15		dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C, RF = 4900MHz		–0.005		dB/°C
2-Tone Input 3rd Order Intercept (Δf = 2MHz)	RF = 4500MHz RF = 4900MHz RF = 5250MHz		24.2 25.1 24.0		dBm
2-Tone Input 2nd Order Intercept (Δf = 241MHz, $f_{IM2} = f_{RF2} – f_{RF1}$)	f_{RF1} = 4779MHz, f_{RF2} = 5020MHz, f_{LO} = 5140MHz		39.8		dBm
SSB Noise Figure	RF = 4500MHz RF = 4900MHz RF = 5250MHz		10.7 11.0 11.7		dB
2LO – 2RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF/2}$)	f_{RF} = 5020MHz at –10dBm, f_{LO} = 5140MHz f_{IF} = 240MHz		–55		dBc
3LO – 3RF Output Spurious Product ($f_{RF} = f_{LO} – f_{IF/3}$)	f_{RF} = 5060MHz at –10dBm, f_{LO} = 5140MHz f_{IF} = 240MHz		–75		dBc
Input 1dB Compression	RF = 4900MHz, V_{CCIF} = 3.3V RF = 4900MHz, V_{CCIF} = 5V		11.3 14.5		dBm

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_C = 25°C, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Requirements (V_{CC}, V_{CCIF})					
V_{CC} Supply Voltage (Pins 5 and 7)		3.1	3.3	3.5	V
V_{CCIF} Supply Voltage (Pins 14 and 15)		3.1	3.3	5.3	V
V_{CC} Supply Current (Pins 5 + 7) V_{CCIF} Supply Current (Pins 14 + 15) Total Supply Current (V_{CC} + V_{CCIF})			96 98 194	116 122 238	mA
Total Supply Current – Shutdown	SHDN = High			500	µA
Shutdown Logic Input (SHDN) Low = On, High = Off					
SHDN Input High Voltage (Off)		3.0			V
SHDN Input Low Voltage (On)				0.3	V
SHDN Input Current	–0.3V to V_{CC} + 0.3V	–20		30	µA
Turn On Time			0.6		µs
Turn Off Time			0.6		µs
Temperature Sensing Diode (TEMP)					
DC Voltage at T_J = 25°C	I_{IN} = 10µA I_{IN} = 80µA		726.1 782.5		mV mV
Voltage Temperature Coefficient	I_{IN} = 10µA I_{IN} = 80µA		–1.73 –1.53		mV/°C mV/°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

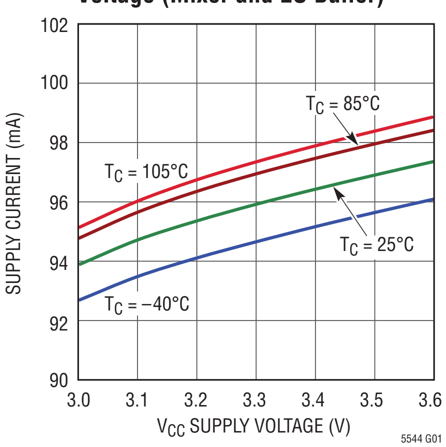
Note 2: The LTC5544 is guaranteed functional over the –40°C to 105°C case temperature range.

Note 3: SSB Noise Figure measurements performed with a small-signal noise source, bandpass filter and 6dB matching pad on RF input, 6dB matching pad on the LO input, bandpass filter on the IF output and no other RF signals applied.

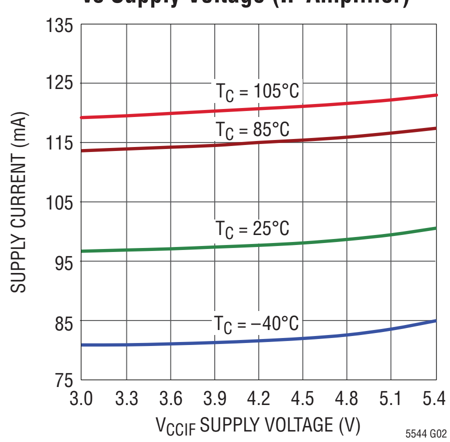
TYPICAL DC PERFORMANCE CHARACTERISTICS

SHDN = Low, Test circuit shown in Figure 1.

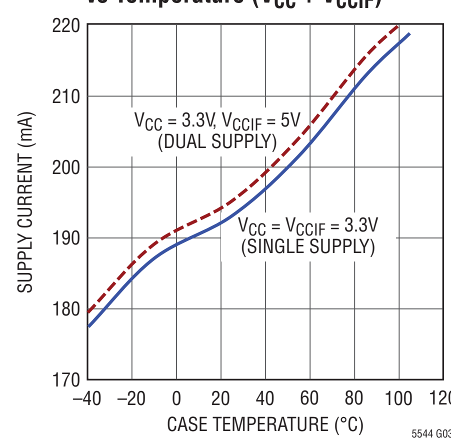
V_{CC} Supply Current vs Supply Voltage (Mixer and LO Buffer)



V_{CCIF} Supply Current vs Supply Voltage (IF Amplifier)



Total Supply Current vs Temperature (V_{CC} + V_{CCIF})

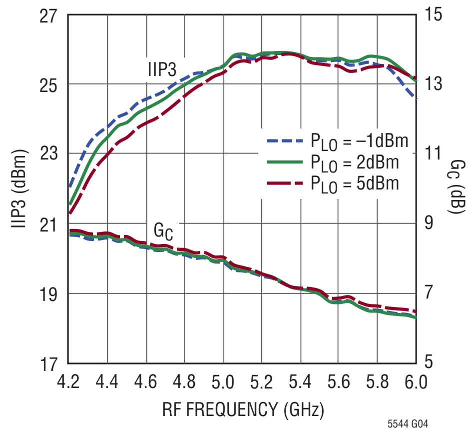


5544f

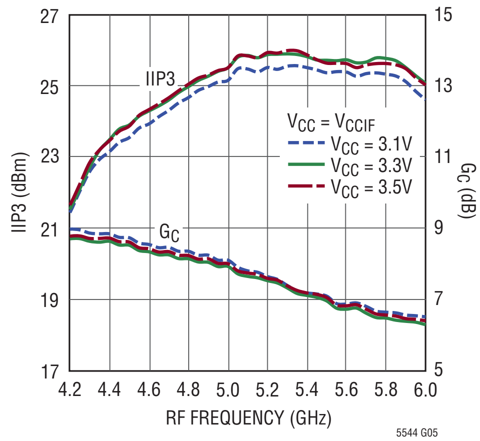
TYPICAL AC PERFORMANCE CHARACTERISTICS Low Side LO

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_C = 25°C, P_{LO} = 2dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, ∆f = 2MHz), IF = 240MHz, unless otherwise noted. Test circuit shown in Figure 1.

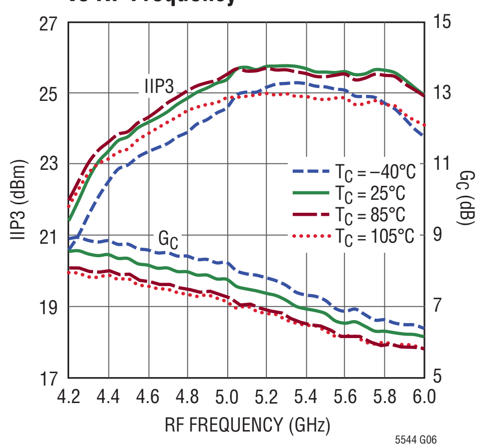
Conversion Gain and IIP3 vs RF Frequency



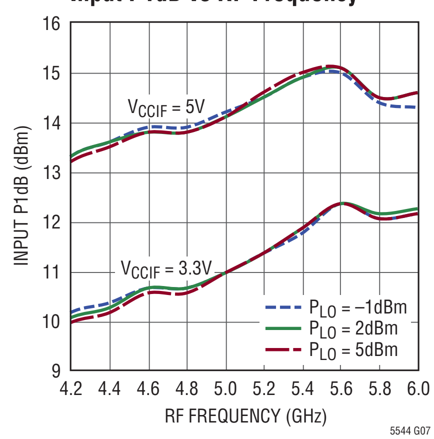
Conversion Gain and IIP3 vs RF Frequency



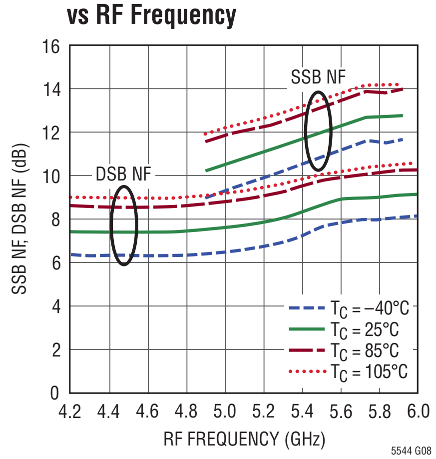
Conversion Gain and IIP3 vs RF Frequency



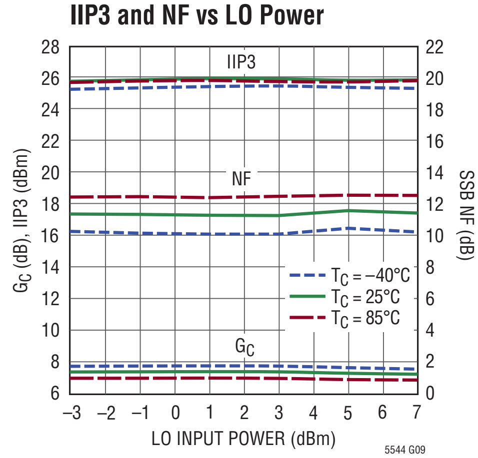
Input P1dB vs RF Frequency



SSB NF and DSB NF vs RF Frequency



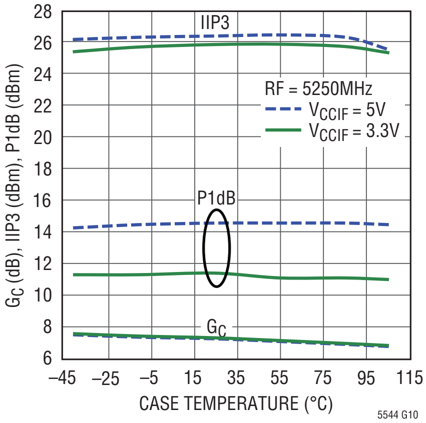
5250MHz Conversion Gain, IIP3 and NF vs LO Power



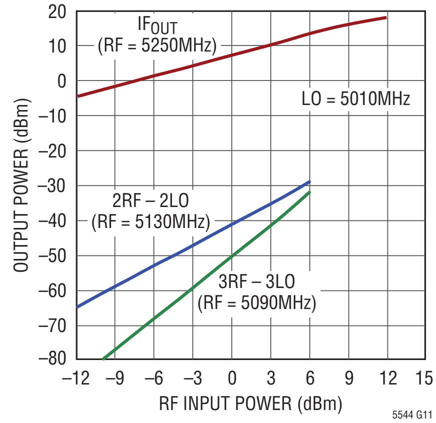
TYPICAL AC PERFORMANCE CHARACTERISTICS Low Side LO (continued)

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_C = 25°C, P_{LO} = 2dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, Δf = 2MHz), IF = 240MHz, unless otherwise noted. Test circuit shown in Figure 1.

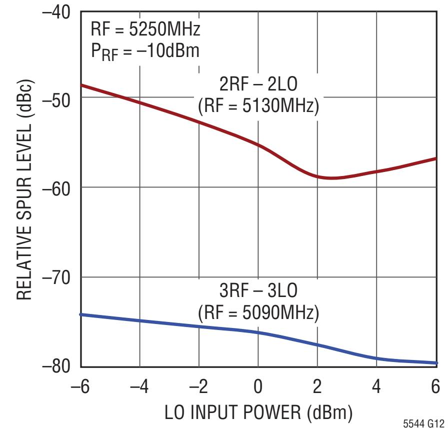
Conversion Gain, IIP3 and RF Input P1dB vs Temperature



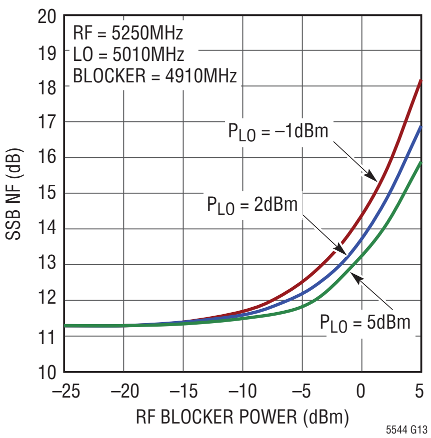
Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



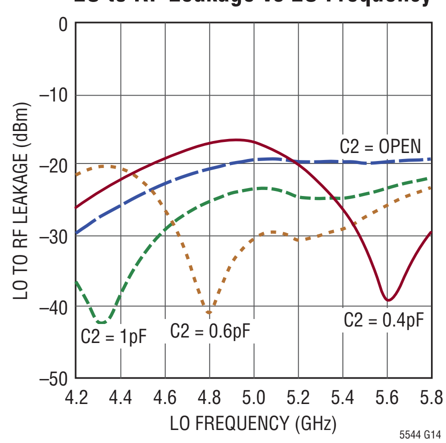
2 × 2 and 3 × 3 Spurs vs LO Power



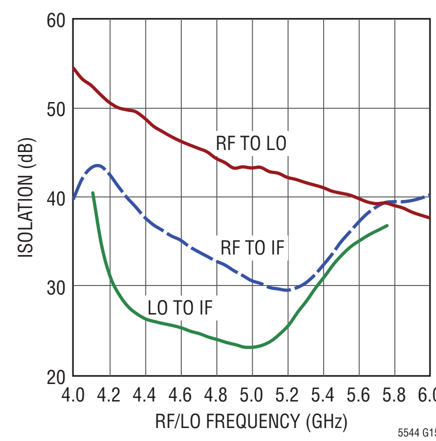
SSB Noise Figure vs RF Blocker Level



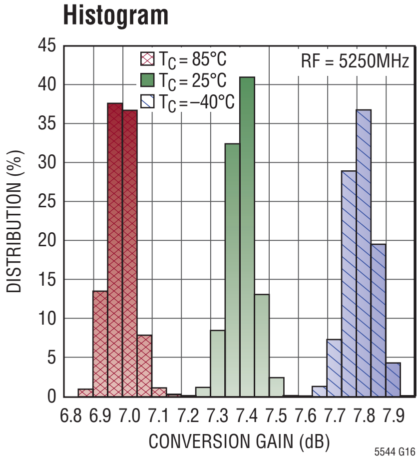
LO to RF Leakage vs LO Frequency



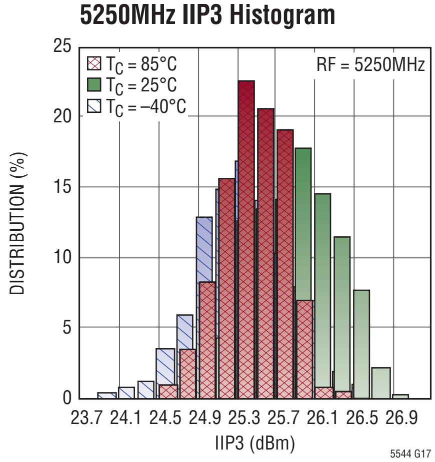
RF/LO Isolation



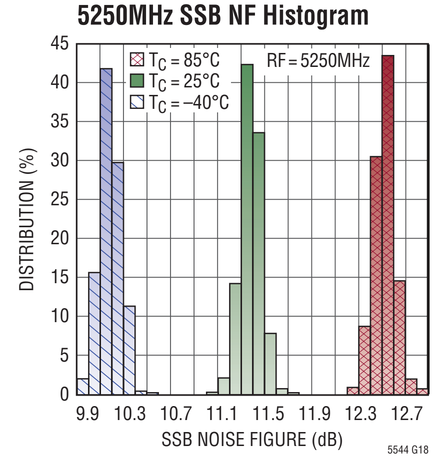
5250MHz Conversion Gain Histogram



5250MHz IIP3 Histogram



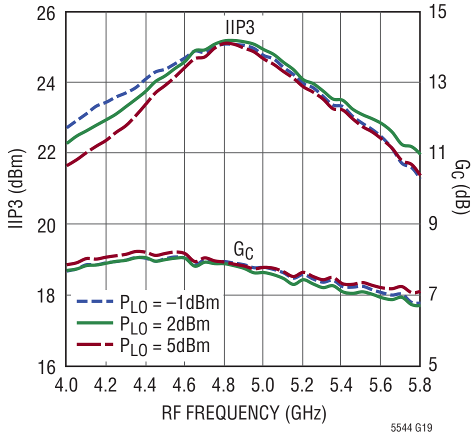
5250MHz SSB NF Histogram



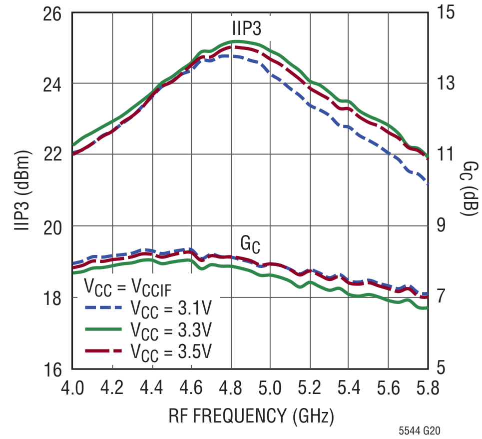
TYPICAL AC PERFORMANCE CHARACTERISTICS High Side LO

V_{CC} = 3.3V, V_{CCIF} = 3.3V, SHDN = Low, T_C = 25°C, P_{LO} = 2dBm, P_{RF} = –3dBm (–3dBm/tone for two-tone IIP3 tests, ∆f = 2MHz), IF = 240MHz, unless otherwise noted. Test circuit shown in Figure 1.

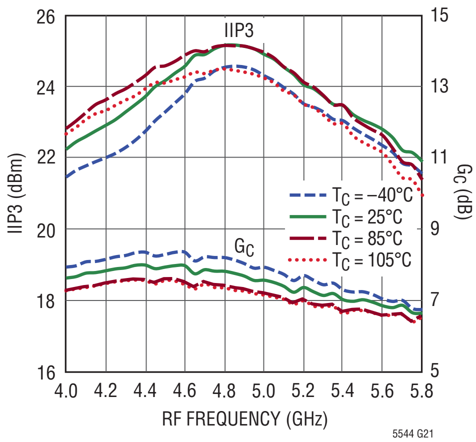
Conversion Gain and IIP3 vs RF Frequency



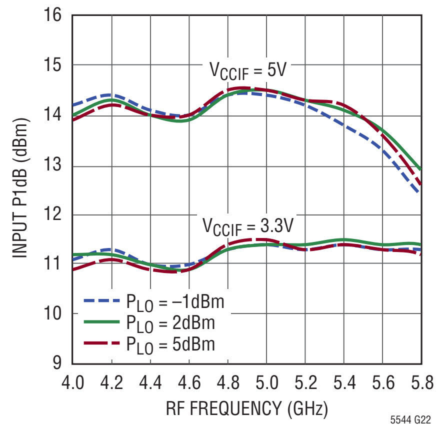
Conversion Gain and IIP3 vs RF Frequency



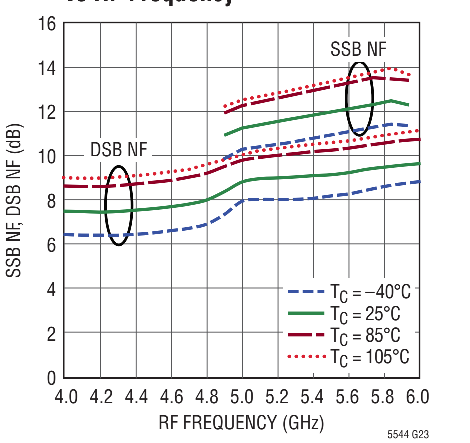
Conversion Gain and IIP3 vs RF Frequency



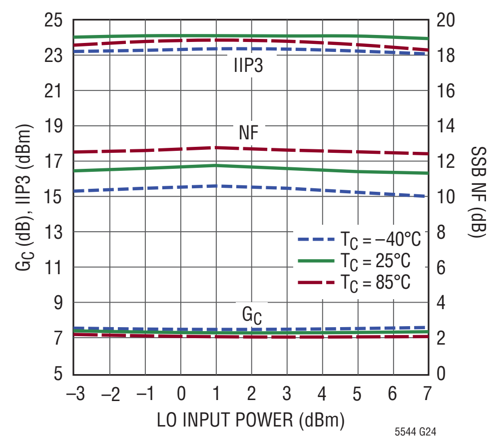
Input P1dB vs RF Frequency



SSB NF and DSB NF vs RF Frequency



5250MHz Conversion Gain, IIP3 and NF vs LO Power



PIN FUNCTIONS

GND (Pins 1, 8, 9, 11, Exposed Pad Pin 17): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

RF (Pin 2): Single-Ended Input for the RF Signal. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. **A series DC-blocking capacitor should be used to avoid damage to the integrated transformer when DC voltage is present at the RF input.** The RF input is impedance matched, as long as the LO input is driven with a 2dBm ±5dB source between 4.2GHz and 5.8GHz.

CT (Pin 3): RF Transformer Secondary Center-Tap. This pin may require a bypass capacitor to ground. See the Applications Information section. This pin has an internally generated bias voltage of 1.2V. It must be DC-isolated from ground and V_{CC}.

SHDN (Pin 4): Shutdown Pin. When the input voltage is less than 0.3V, the IC is enabled. When the input voltage is greater than 3V, the IC is disabled. Typical SHDN pin input current is less than 10μA. This pin must not be allowed to float.

V_{CC1} (Pin 5) and V_{CC2} (Pin 7): Power Supply Pins for the LO Buffer and Bias Circuits. These pins are internally connected and must be externally connected to a regulated 3.3V supply, with bypass capacitors located close to the pins. Typical current consumption is 96mA.

LOBIAS (Pin 6): This Pin Allows Adjustment of the LO Buffer Current. Typical DC voltage is 2.2V.

LO (Pin 10): Single-Ended Input for the Local Oscillator. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. **A series DC blocking capacitor must be used to avoid damage to the integrated transformer if DC voltage is present at the LO input.**

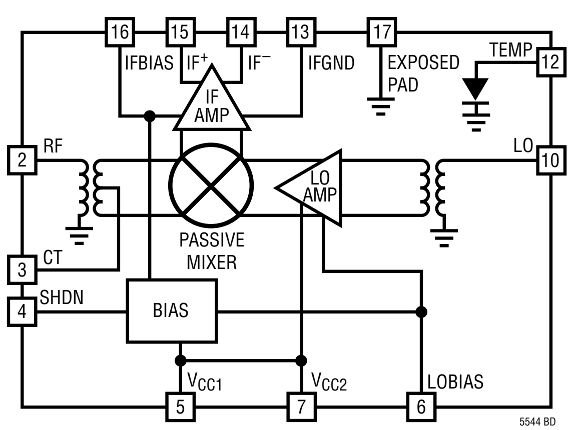
TEMP (Pin 12): Temperature Sensing Diode. This pin is connected to the anode of a diode that may be used to measure the die temperature, by forcing a current and measuring the voltage.

IFGND (Pin 13): DC Ground Return for the IF Amplifier. This pin must be connected to ground to complete the IF amplifier's DC current path. Typical DC current is 98mA.

IF^- (Pin 14) and IF^+ (Pin 15): Open-Collector Differential Outputs for the IF Amplifier. These pins must be connected to a DC supply through impedance matching inductors, or a transformer center-tap. Typical DC current consumption is 49mA into each pin.

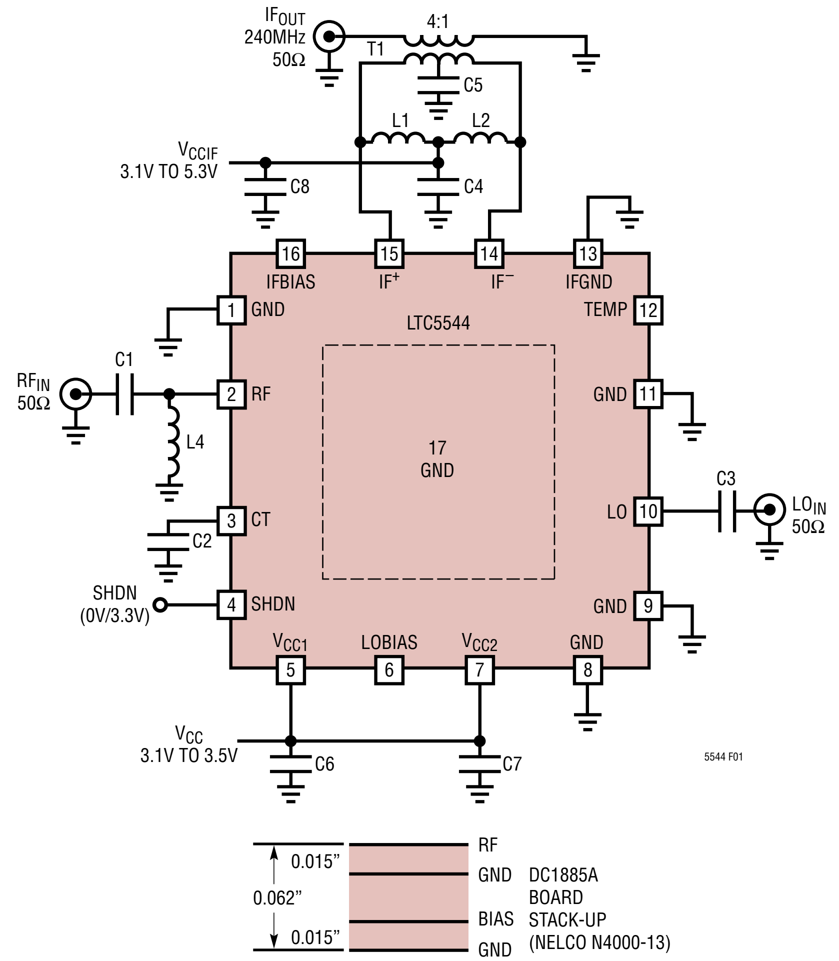
IFBIAS (Pin 16): This Pin Allows Adjustment of the IF Amplifier Current. Typical DC voltage is 2.1V.

BLOCK DIAGRAM



GND PINS ARE NOT SHOWN

TEST CIRCUIT



L1, L2 vs IF Frequencies	
IF (MHz)	**L1, L2 (nH)**
140	220
190	150
240	150
305	82
380	56
456	39

REF DES	VALUE	SIZE	COMMENTS
C1	0.6pF	0402	AVX ACCU-P
C2	Open	0402	
C3	1.2pF	0402	AVX ACCU-P
C4, C6	22pF	0402	AVX
C5	1000pF	0402	AVX
C7, C8	1µF	0603	AVX
L1, L2	150nH	0603	Coilcraft 0603CS
L4	2.2nH	0402	Coilcraft 0402HP
T1	TC4-1W-7ALN+		Mini-Circuits

Note: For IF = 250MHz to 500MHz, use TC4-1W-17LN+ for T1

Figure 1. Standard Downmixer Test Circuit Schematic (240MHz IF)

APPLICATIONS INFORMATION

Introduction

The LTC5544 consists of a high linearity passive double-balanced mixer core, IF buffer amplifier, LO buffer amplifier and bias/shutdown circuits. See the Block Diagram section for a description of each pin function. The RF and LO inputs are single-ended. The IF output is differential. Low side or high side LO injection can be used. The evaluation circuit, shown in Figure 1, utilizes bandpass IF output matching and an IF transformer to realize a 50Ω single-ended IF output. The evaluation board layout is shown in Figure 2.

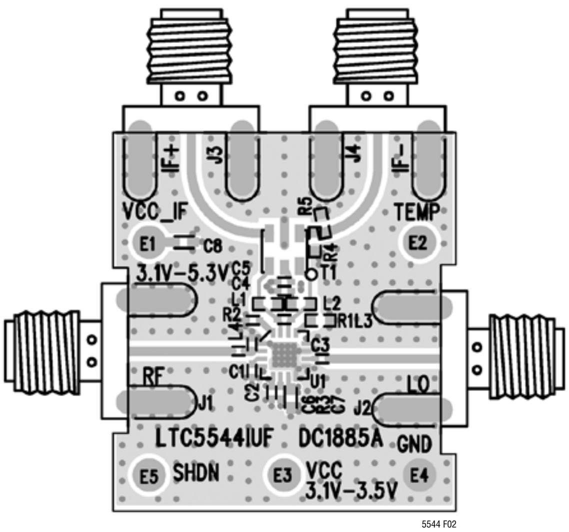


Figure 2. Evaluation Board Layout

RF Input

The mixer's RF input, shown in Figure 3, is connected to the primary winding of an integrated transformer. A 50Ω match is realized with a series capacitor (C1) and a shunt inductor (L4). The primary side of the RF transformer is DC-grounded internally and the DC resistance of the primary is approximately 2.4Ω. A DC blocking capacitor is needed if the RF source has DC voltage present.

The secondary winding of the RF transformer is internally connected to the passive mixer. The center-tap of the transformer secondary is connected to Pin 3 (CT) to allow the connection of bypass capacitor, C2. The value of C2 is LO frequency-dependent and can be tuned for better LO leakage performance. When used, C2 should be located within 2mm of Pin 3 for proper high frequency decoupling. The nominal DC voltage on the CT pin is 1.2V.

For the RF input to be matched, the LO input must be driven. A broadband input match is realized with C1 = 0.6pF and L4 = 2.2nH. The measured RF input return loss is shown in Figure 4 for LO frequencies of 4.4GHz, 5GHz and 5.6GHz. These LO frequencies correspond to the lower, middle and upper values of the LO range. As shown in Figure 4, the RF input impedance is somewhat dependent on LO frequency.

The RF input impedance and input reflection coefficient, versus RF frequency, is listed in Table 1. The reference plane for this data is Pin 2 of the IC, with no external matching, and the LO is driven at 5GHz.

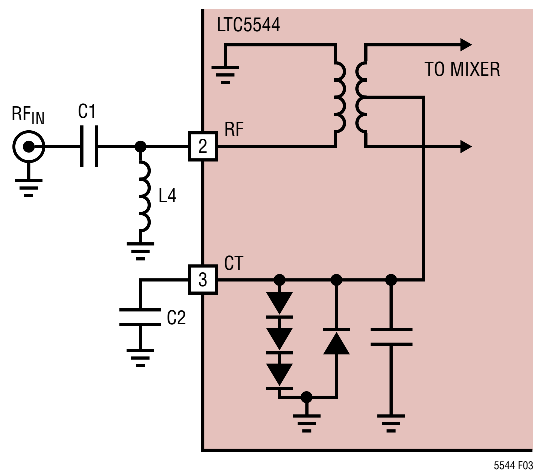


Figure 3. RF Input Schematic

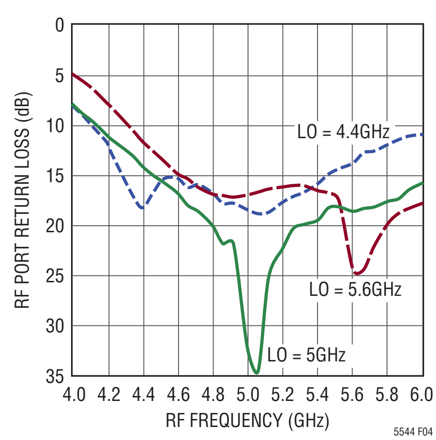


Figure 4. RF Input Return Loss

APPLICATIONS INFORMATION

Table 1. RF Input Impedance and S11 (at Pin 2, No External Matching, LO Input Driven at 5GHz)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
4.0	85.8 + j54.1	0.44	34.8
4.2	89.2 + j45.6	0.41	31.2
4.4	90.9 + j41.3	0.40	29
4.6	95.9 + j33.6	0.38	23.2
4.8	91.4 + j17.1	0.31	15.6
5.0	72.9 + j10.7	0.21	20.1
5.2	66.7 + j24.1	0.25	43.6
5.4	70.8 + j29.1	0.29	40.9
5.6	73.1 + j26.2	0.28	36.6
5.8	69.2 + j23.9	0.25	39.9
6.0	67.3 + j25.7	0.26	43.7

LO Input

The mixer's LO input circuit, shown in Figure 5, consists of a balun transformer and a two-stage high speed limiting differential amplifier to drive the mixer core. The LTC5544's LO amplifiers are optimized for the 4.2GHz to 5.8GHz LO frequency range. LO frequencies above or below this frequency range may be used with degraded performance.

The mixer's LO input is directly connected to the primary winding of an integrated transformer. A 50Ω match is realized with a series 1.2pF capacitor (C3). Measured LO input return loss is shown in Figure 6.

The LO amplifiers are powered through V_{CC1} and V_{CC2} (Pin 5 and Pin 7). When the chip is enabled (SHDN = low), the internal bias circuit provides a regulated 4mA current to the amplifier's bias input, which in turn causes the amplifiers to draw approximately 90mA of DC current. This 4mA reference current is also connected to LOBIAS (Pin 6) to allow modification of the amplifier's DC bias current for special applications. The recommended application circuits require no LO amplifier bias modification, so this pin should be left open-circuited.

The nominal LO input level is +2dBm although the limiting amplifiers will deliver excellent performance over a ±3dB input power range. LO input power greater than +5dBm may be used with slightly degraded performance.

The LO input impedance and input reflection coefficient, versus frequency, is shown in Table 2.

Table 2. LO Input Impedance vs Frequency (at Pin 10, No External Matching)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
4.0	22.7 + j14.7	0.42	140.2
4.2	24.4 + j18.6	0.41	129.9
4.4	28.2 + j22.5	0.39	118.1
4.6	33.2 + j25.3	0.35	106.7
4.8	39.7 + j26.4	0.30	95
5.0	47.4 + j24.3	0.24	82.1
5.2	52.2 + j16.9	0.16	73.3
5.4	52 + j9.4	0.09	72.7
5.6	49.9 + j3.8	0.04	88.8
5.8	47.7 – j1	0.03	–156.5
6.0	44.2 – j6.2	0.09	–129.4

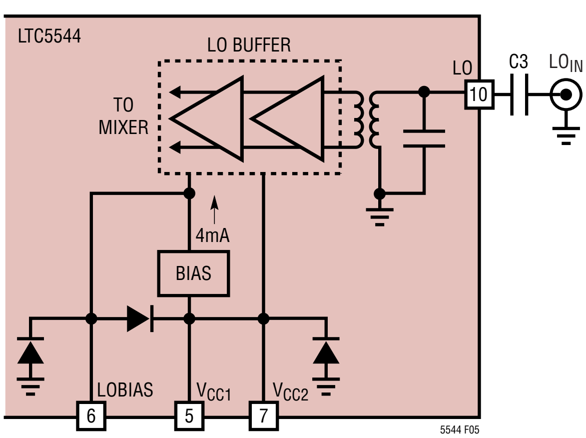


Figure 5. LO Input Schematic

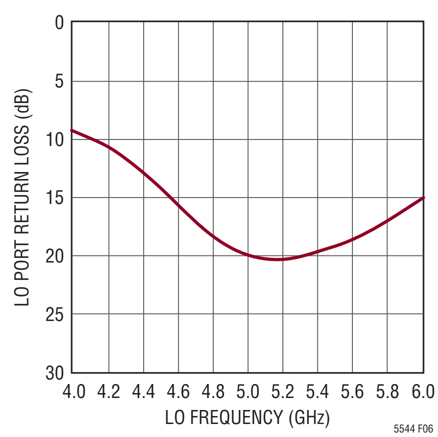


Figure 6. LO Input Return Loss

APPLICATIONS INFORMATION

IF Output

The IF amplifier, shown in Figure 7, has differential open-collector outputs (IF^+ and IF^-), a DC ground return pin (IFGND), and a pin for modifying the internal bias (IFBIAS). The IF outputs must be biased at the supply voltage (V_{CCIF}), which is applied through matching inductors L1 and L2. Alternatively, the IF outputs can be biased through the center tap of a transformer. The common node of L1 and L2 can be connected to the center tap of the transformer. Each IF output pin draws approximately 49mA of DC supply current (98mA total). IFGND (Pin 13) must be grounded or the amplifier will not draw DC current. For the highest conversion gain, high-Q wire-wound chip inductors are recommended for L1 and L2, especially when using V_{CCIF} = 3.3V. Low cost multilayer chip inductors may be substituted, with a slight degradation in performance. Grounding through inductor L3 may improve LO-IF and RF-IF leakage performance in some applications, but is otherwise not necessary. High DC resistance in L3 will reduce the IF amplifier supply current, which will degrade RF performance.

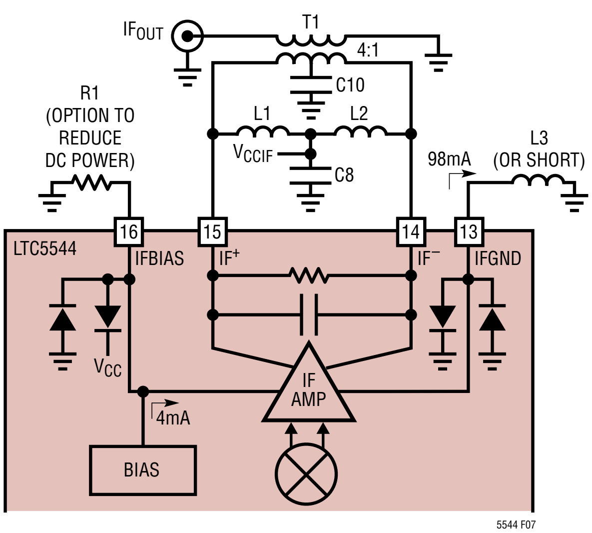


Figure 7. IF Amplifier Schematic with Transformer-Based Bandpass Match

For optimum single-ended performance, the differential IF outputs must be combined through an external IF transformer or discrete IF balun circuit. The evaluation board (see Figures 1 and 2) uses a 4:1 ratio IF transformer for impedance transformation and differential to single-ended transformation. It is also possible to eliminate the IF transformer and drive differential filters or amplifiers directly.

The IF output impedance can be modeled as 332Ω in parallel with 1.7pF at IF frequencies. An equivalent small-signal model is shown in Figure 8. Frequency-dependent differential IF output impedance is listed in Table 3. This data is referenced to the package pins (with no external components) and includes the effects of IC and package parasitics.

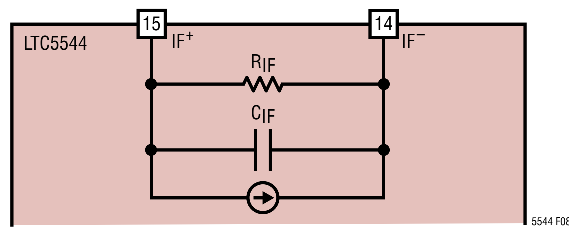


Figure 8. IF Output Small-Signal Model

Table 3. IF Output Impedance vs Frequency

FREQUENCY (MHz)	DIFFERENTIAL OUTPUT IMPEDANCE (R_{IF} || X_{IF} (C_{IF}))
90	351 || –j707 (2.5pF)
140	341 || –j494 (2.3pF)
190	334 || –j441 (1.9pF)
240	332 || –j390 (1.7pF)
300	325 || –j312 (1.7pF)
380	318 || –j246 (1.7pF)
456	304 || –j205 (1.7pF)

Transformer-Based Bandpass IF Matching

The IF output can be matched for IF frequencies as low as 40MHz, or as high as 500MHz, using the bandpass IF matching shown in Figures 1 and 7. L1 and L2 resonate with the internal IF output capacitance at the desired IF frequency. The value of L1, L2 is calculated as follows:

$$L1, L2 = 1/[(2 \pi f_{IF})^2 \bullet 2 \bullet C_{IF}]$$

where C_{IF} is the internal IF capacitance (listed in Table 3).

Values of L1 and L2 are tabulated in Figure 1 for various IF frequencies

APPLICATIONS INFORMATION

Discrete IF Balun Matching

For many applications, it is possible to replace the IF transformer with the discrete IF balun shown in Figure 9. The values of L5, L6, C13 and C14 are calculated to realize a 180° phase shift at the desired IF frequency and provide a 50Ω single-ended output, using the following equations. Inductor L7 is used to cancel the internal capacitance C_{IF} and supplies bias voltage to the IF pin. C15 is a DC blocking capacitor.

$$L5, L6 = \frac{\sqrt{R_{IF} \bullet R_{OUT}}}{\omega_{IF}}$$

$$C13, C14 = \frac{1}{\omega_{IF} \bullet \sqrt{R_{IF} \bullet R_{OUT}}}$$

$$L7 = \frac{|X_{IF}|}{\omega_{IF}}$$

These equations give a good starting point, but it is usually necessary to adjust the component values after building and testing the circuit. The final solution can be achieved with less iteration by considering the parasitics of L7 in the previous calculation.

The typical performances of the LTC5544 using a discrete IF balun matching and a transformer-based IF matching are shown in Figure 10. With an IF frequency of 456MHz, the actual components values for the discrete balun are:

L5, L6 = 36nH, L7 = 82nH and C13, C14 = 3.3pF

Measured IF output return losses for transformer-based bandpass IF matching and discrete balun IF matching (456MHz IF frequency) are plotted in Figure 11. A discrete balun has less insertion loss than a balun transformer, but the IF bandwidth of a discrete balun is less than that of a transformer.

IF Amplifier Bias

The IF amplifier delivers excellent performance with V_{CCIF} = 3.3V, which allows the V_{CC} and V_{CCIF} supplies to be common. With V_{CCIF} increased to 5V, the RF input P1dB increases by more than 3dB, at the expense of higher power consumption. Mixer performance at 5250MHz is shown in Table 4 with V_{CCIF} = 3.3V and 5V.

Table 4. Performance Comparison with V_{CCIF} = 3.3V and 5V (RF = 5250MHz, Low Side LO, IF = 240MHz)

V_{CCIF} (V)	I_{CCIF} (mA)	G_C (dB)	P1dB (dBm)	IIP3 (dBm)	NF (dB)
3.3	98	7.4	11.4	25.9	11.3
5.0	101	7.4	14.6	26.5	11.4

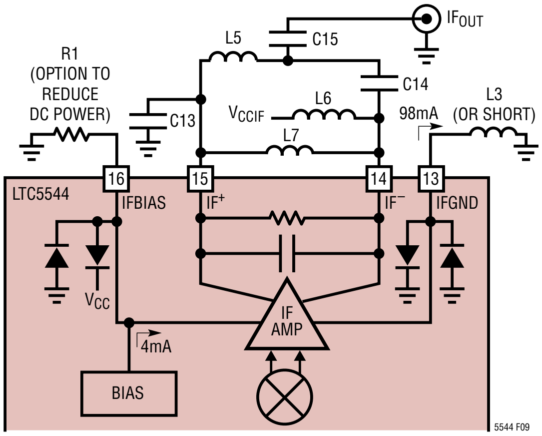


Figure 9. IF Amplifier Schematic with Discrete IF Balun

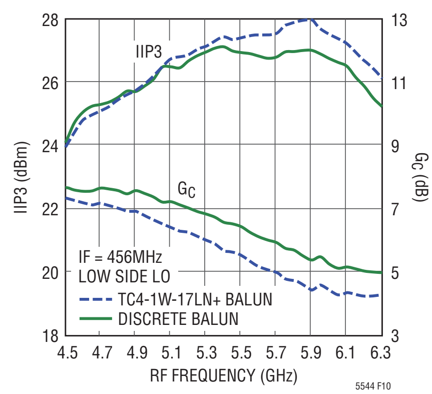


Figure 10. Conversion Gain and IIP3 vs RF Frequency

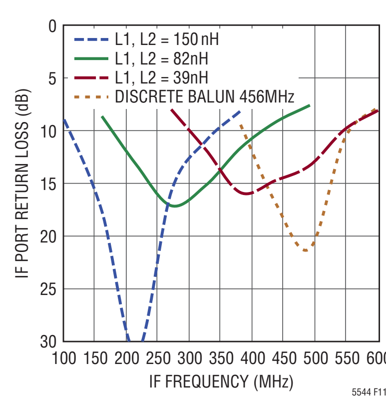


Figure 11. IF Output Return Loss

APPLICATIONS INFORMATION

The IFBIAS pin (Pin 16) is available for reducing the DC current consumption of the IF amplifier, at the expense of reduced performance. This pin should be left open-circuited for optimum performance. The internal bias circuit produces a 4mA reference for the IF amplifier, which causes the amplifier to draw approximately 98mA. If resistor R1 is connected to Pin 16 as shown in Figure 6, a portion of the reference current can be shunted to ground, resulting in reduced IF amplifier current. For example, R1 = 1kΩ will shunt away 1.5mA from Pin 16 and the IF amplifier current will be reduced by 40% to approximately 59mA. The nominal, open-circuit DC voltage at Pin 16 is 2.1V. Table 5 lists RF performance at 5250MHz versus IF amplifier current.

Table 5. Mixer Performance with Reduced IF Amplifier Current (RF = 5250MHz, Low Side LO, IF = 240MHz, V_{CC} = V_{CCIF} = 3.3V)

R1 (kΩ)	I_{CCIF} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	98	7.4	25.9	11.4	11.3
4.7	89	7.2	25.7	11.5	11.4
2.2	77	6.9	25.2	11.6	11.5
1.0	59	6.3	23.8	11.3	11.6

(RF = 5250MHz, High Side LO, IF = 240MHz, V_{CC} = V_{CCIF} = 3.3V)

R1 (kΩ)	I_{CCIF} (mA)	G_C (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	98	7.3	24.0	11.4	11.7
4.7	89	7.0	23.8	11.4	11.9
2.2	77	6.6	23.5	11.4	12.2
1.0	59	5.8	22.6	11.3	12.4

Shutdown Interface

Figure 12 shows a simplified schematic of the SHDN pin interface. To disable the chip, the SHDN voltage must be higher than 3.0V. If the shutdown function is not required, the SHDN pin should be connected directly to GND. The voltage at the SHDN pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

The SHDN pin must be pulled high or low. If left floating, then the on/off state of the IC will be indeterminate. If a three-state condition can exist at the SHDN pin, then a pull-up or pull-down resistor must be used.

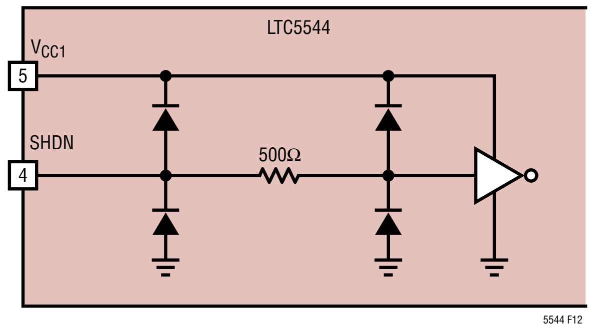


Figure 12. Shutdown Input Circuit

Temperature Diode

The LTC5544 provides an on-chip diode at Pin 12 (TEMP) for chip temperature measurement. Pin 12 is connected to the anode of an internal ESD diode with its cathode connected to internal ground. The chip temperature can be measured by injecting a constant DC current into Pin 12 and measuring its DC voltage. The voltage vs temperature coefficient of the diode is about –1.73mV/°C with 10μA current injected into the TEMP pin. Figure 13 shows a typical temperature-voltage behavior when 10μA and 80μA currents are injected into Pin 12.

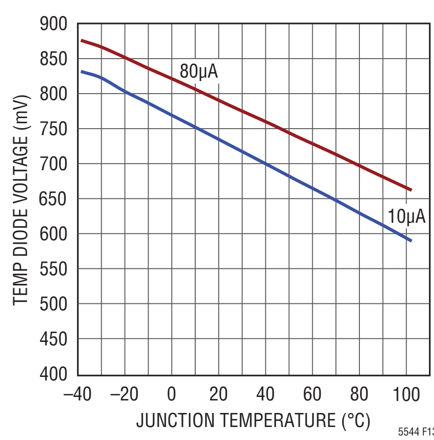


Figure 13. TEMP Diode Voltage vs Junction Temperature (T_J)

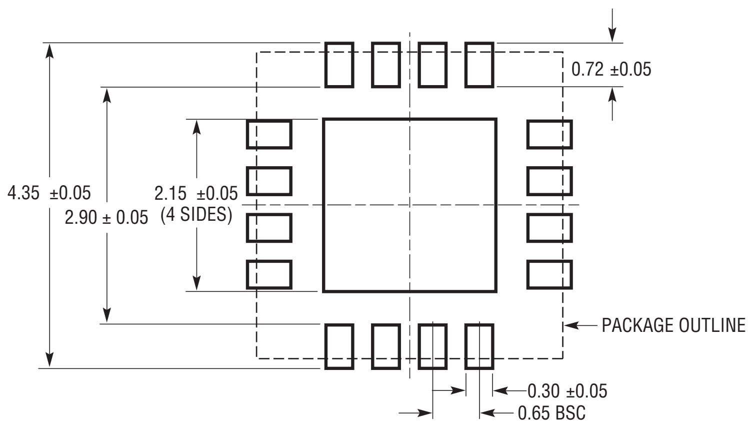
Supply Voltage Ramping

Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

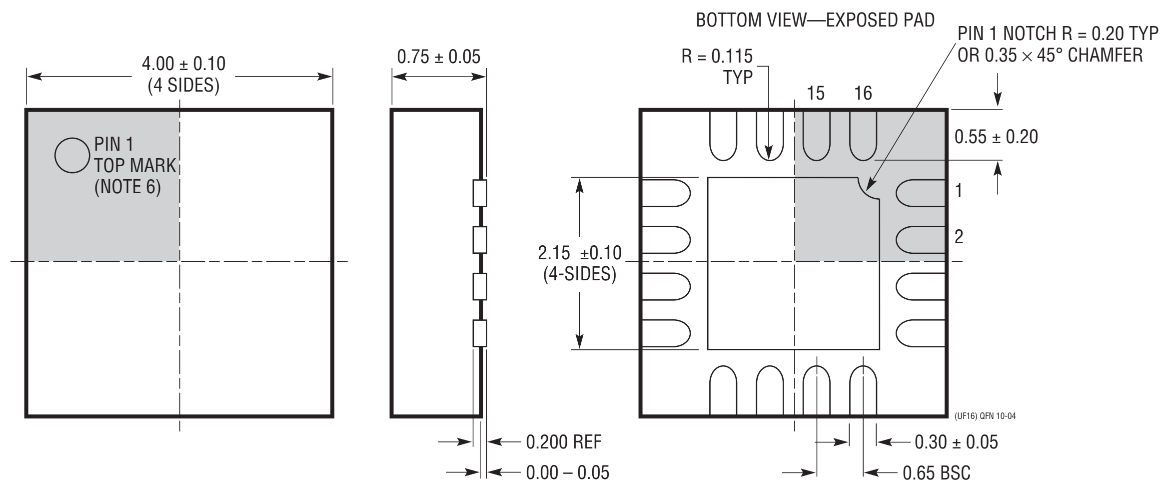
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UF Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



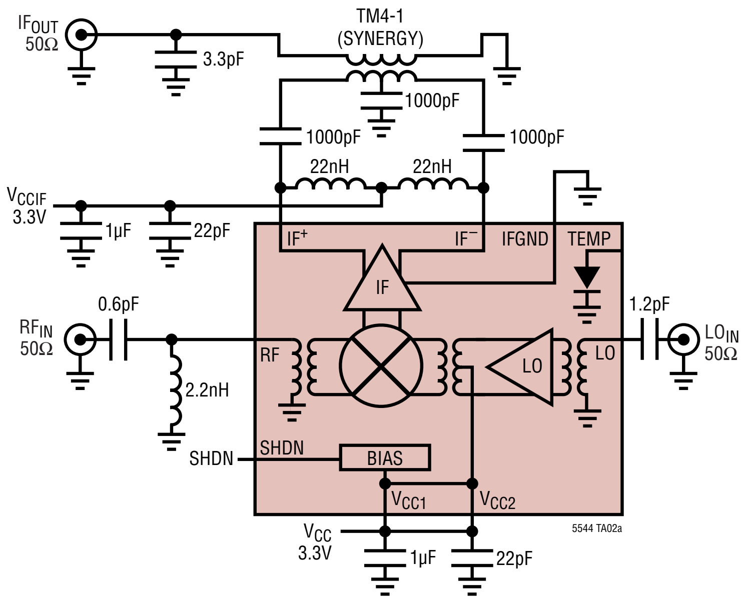
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



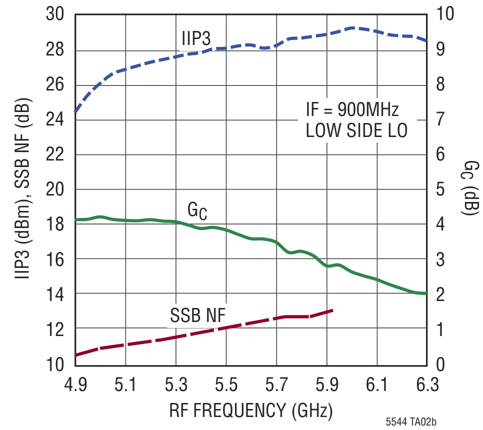
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

900MHz IF Output Matching



Conversion Gain, IIP3 and NF vs RF Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LTC554X	600MHz to 6GHz 3.3V Downconverting Mixers	8dB Gain, 26dBm IIP3, 10dB NF, 3.3V/200mA Supply
LT®5527	400MHz to 3.7GHz, 5V Downconverting Mixer	2.3dB Gain, 23.5dBm IIP3 and 12.5dB NF at 1900MHz, 5V/78mA Supply
LT5557	400MHz to 3.8GHz, 3.3V Downconverting Mixer	2.9dB Gain, 24.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/82mA Supply
LTC559x	600MHz to 4.5GHz Dual Downconverting Mixer Family	8.5dB Gain, 26.5dBm IIP3, 9.9dB NF, 3.3V/380mA Supply
LTC5569	300MHz to 4GHz 3.3V Dual Downconverting Mixer	2dB Gain, 26.8dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/180mA Supply
LTC6400-X	300MHz Low Distortion IF Amp/ADC Driver	Fixed Gain of 8dB, 14dB, 20dB and 26dB; >36dBm OIP3 at 300MHz, Differential I/O
LTC6416	2GHz 16-Bit ADC Buffer	40dBm OIP3 to 300MHz, Programmable Fast Recovery Output Clamping
LTC6412	31dB Linear Analog VGA	35dBm OIP3 at 240MHz, Continuous Variable Gain Range –14dB to 17dB
LT5554	Ultralow Distort IF Digital VGA	48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps
LT5578	400MHz to 2.7GHz Upconverting Mixer	27dBm OIP3 at 900MHz, 24.2dBm at 1.95GHz, Integrated RF Transformer
LT5579	1.5GHz to 3.8GHz Upconverting Mixer	27.3dBm OIP3 at 2.14GHz, NF = 9.9dB, 3.3V Supply, Single-Ended LO and RF Ports
LTC5588-1	200MHz to 6GHz I/Q Modulator	31dBm OIP3 at 2.14GHz, –160.6dBm/Hz Noise Floor
RF Power Detectors		
LTC5587	6GHz RMS Detector with 12-Bit ADC	40dB Dynamic Range, ±1dB Accuracy Over Temperature, 3mA Current, 500ksps
LT5581	6GHz Low Power RMS Detector	40dB Dynamic Range, ±1dB Accuracy Over Temperature, 1.5mA Supply Current
LTC5582	40MHz to 10GHz RMS Detector	57dB Dynamic Range, ±0.5dB Accuracy Over Temperature, ±0.2dB Linearity Error
LTC5583	Dual 6GHz RMS Power Detector	Up to 60dB Dynamic Range, ±0.5dB Accuracy Over Temperature, >50dB Isolation
ADCs		
LTC2208	16-Bit, 130Msps ADC	78dBFS Noise Floor, >83dB SFDR at 250MHz
LTC2285	Dual 14-Bit, 125Msps Low Power ADC	72.4dB SNR, 88dB SFDR, 790mW Power Consumption
LTC2268-14	Dual 14-Bit, 125Msps Serial Output ADC	73.1dB SNR, 88dB SFDR, 299mW Power Consumption

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