

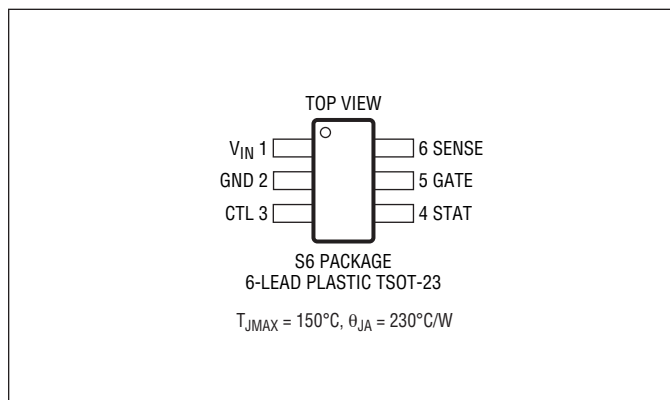
LTC4412

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{IN})	–14V to 36V
Voltage from V_{IN} to SENSE	–28V to 28V
Input Voltage	
CTL	–0.3V to 36V
SENSE	–14V to 36V
Output Voltage	
GATE	–0.3V to the Higher of $V_{IN} + 0.3V$ or SENSE + 0.3V
STAT	–0.3V to 36V
Operating Junction Temperature Range	
(Note 2)	–55°C to 150°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4412ES6#PBF	LTC4412ES6#TRPBF	LTA2	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC4412IS6#PBF	LTC4412IS6#TRPBF	LTA2	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC4412HS6#PBF	LTC4412HS6#TRPBF	LTA2	6-Lead Plastic TSOT-23	–40°C to 150°C
LTC4412MPS6#PBF	LTC4412MPS6#TRPBF	LTA2	6-Lead Plastic TSOT-23	–55°C to 150°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4412ES6	LTC4412ES6#TR	LTA2	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC4412IS6	LTC4412IS6#TR	LTA2	6-Lead Plastic TSOT-23	–40°C to 85°C
LTC4412HS6	LTC4412HS6#TR	LTA2	6-Lead Plastic TSOT-23	–40°C to 150°C
LTC4412MPS6	LTC4412MPS6#TR	LTA2	6-Lead Plastic TSOT-23	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating junction temperature range, unless otherwise noted specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, CTL and GND = 0V. Current into a pin is positive and current out of a pin is negative. All voltages are referenced to GND, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}, V_{SENSE}	Operating Supply Range	V_{IN} and/or V_{SENSE} Must Be in This Range for Proper Operation	●	2.5		28	V
I_{QFL}	Quiescent Supply Current at Low Supply While in Forward Regulation	$V_{IN} = 3.6\text{V}$. Measure Combined Current at V_{IN} and SENSE Pins Averaged with $V_{SENSE} = 3.5\text{V}$ and $V_{SENSE} = 3.6\text{V}$ (Note 3)	●		11	19	μA
I_{QFH}	Quiescent Supply Current at High Supply While in Forward Regulation	$V_{IN} = 28\text{V}$. Measure Combined Current at V_{IN} and SENSE Pins Averaged with $V_{SENSE} = 27.9\text{V}$ and $V_{SENSE} = 28\text{V}$ (Note 3)	●		15	26	μA
I_{QRL}	Quiescent Supply Current at Low Supply While in Reverse Turn-Off	$V_{IN} = 3.6\text{V}$, $V_{SENSE} = 3.7\text{V}$. Measure Combined Current of V_{IN} and SENSE Pins			10	19	μA
I_{QRH}	Quiescent Supply Current at High Supply While in Reverse Turn-Off	$V_{IN} = 27.9\text{V}$, $V_{SENSE} = 28\text{V}$. Measure Combined Current of V_{IN} and SENSE Pins			16	28	μA
I_{QCL}	Quiescent Supply Current at Low Supply with CTL Active	$V_{IN} = 3.6\text{V}$, $V_{SENSE} = 0\text{V}$, $V_{CTL} = 1\text{V}$			7	13	μA
I_{QCH}	Quiescent Supply Current at High Supply with CTL Active	$V_{IN} = 28\text{V}$, $V_{SENSE} = 0\text{V}$, $V_{CTL} = 1\text{V}$			12	20	μA
I_{LEAK}	V_{IN} and SENSE Pin Leakage Currents When Other Pin Supplies Power	$V_{IN} = 28\text{V}$, $V_{SENSE} = 0\text{V}$; $V_{SENSE} = 28\text{V}$, $V_{IN} = 0\text{V}$ $V_{IN} = 14\text{V}$, $V_{SENSE} = -14\text{V}$; $V_{SENSE} = 14\text{V}$, $V_{IN} = -14\text{V}$		-3	0	1	μA

PowerPath Controller

V_{FR}	PowerPath Switch Forward Regulation Voltage	$V_{IN} - V_{SENSE}$, $2.5\text{V} \leq V_{IN} \leq 28\text{V}$	●	10	20	32	mV
V_{RTO}	PowerPath Switch Reverse Turn-Off Threshold Voltage	$V_{SENSE} - V_{IN}$, $2.5\text{V} \leq V_{IN} \leq 28\text{V}$	●	10	20	32	mV

GATE and STAT Outputs

$I_{G(SRC)}$ $I_{G(SNK)}$	GATE Active Forward Regulation Source Current Sink Current	(Note 4)		-1 25	-2.5 50	-5 85	μA μA
$V_{G(ON)}$	GATE Clamp Voltage	Apply $I_{GATE} = 1\mu\text{A}$, $V_{IN} = 12\text{V}$, $V_{SENSE} = 11.9\text{V}$, Measure $V_{IN} - V_{GATE}$		6.3	7	7.7	V
$V_{G(OFF)}$	GATE Off Voltage	Apply $I_{GATE} = -5\mu\text{A}$, $V_{IN} = 12\text{V}$, $V_{SENSE} = 12.1\text{V}$, Measure $V_{SENSE} - V_{GATE}$			0.13	0.25	V
$t_{G(ON)}$	GATE Turn-On Time	$V_{GS} < -3\text{V}$, $C_{GATE} = 1\text{nF}$ (Note 5)			110	175	μs
$t_{G(OFF)}$	GATE Turn-Off Time	$V_{GS} > -1.5\text{V}$, $C_{GATE} = 1\text{nF}$ (Note 6)			13	22	μs
$I_{S(OFF)}$	STAT Off Current	$2.5\text{V} \leq V_{IN} \leq 28\text{V}$ (Note 7)	●	-1	0	1	μA
$I_{S(SNK)}$	STAT Sink Current	$2.5\text{V} \leq V_{IN} \leq 28\text{V}$ (Note 7)	●	6	10	17	μA
$t_{S(ON)}$	STAT Turn-On Time	(Note 8)			4.5	25	μs
$t_{S(OFF)}$	STAT Turn-Off Time	(Note 8)			40	75	μs

CTL Input

V_{IL}	CTL Input Low Voltage	$2.5\text{V} \leq V_{IN} \leq 28\text{V}$	●		0.5	0.35	V
V_{IH}	CTL Input High Voltage	$2.5\text{V} \leq V_{IN} \leq 28\text{V}$	●	0.9	0.635		V
I_{CTL}	CTL Input Pull-Down Current	$0.35\text{V} \leq V_{CTL} \leq 28\text{V}$		1	3.5	5.5	μA
H_{CTL}	CTL Hysteresis	$2.5\text{V} \leq V_{IN} \leq 28\text{V}$			135		mV

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4412 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4412E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature range. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4412I is guaranteed over the –40°C to 85°C operating junction temperature range. The LTC4412MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is degraded for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D \cdot \Theta_{JA})$, where $\Theta_{JA} = 230^\circ\text{C/W}$ for the TSOT-23 package.

Note 3: This results in the same supply current as would be observed with an external P-channel MOSFET connected to the LTC4412 and operating in forward regulation.

Note 4: V_{IN} is held at 12V and GATE is forced to 10.5V. SENSE is set at 12V to measure the source current at GATE. SENSE is set at 11.9V to measure sink current at GATE.

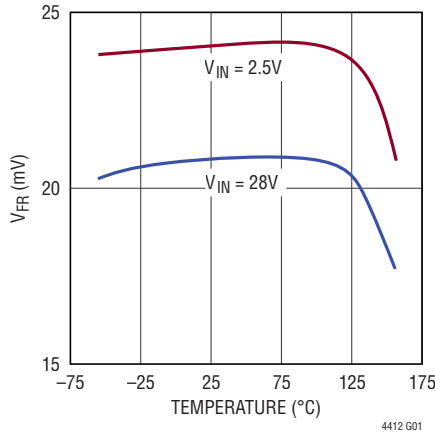
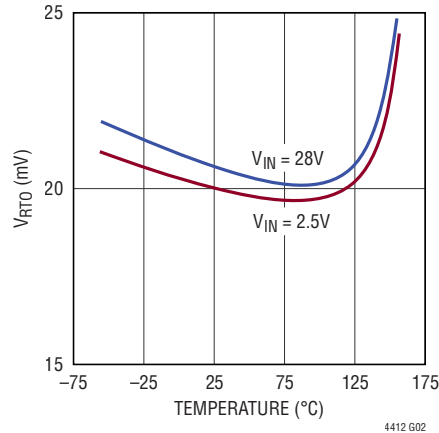
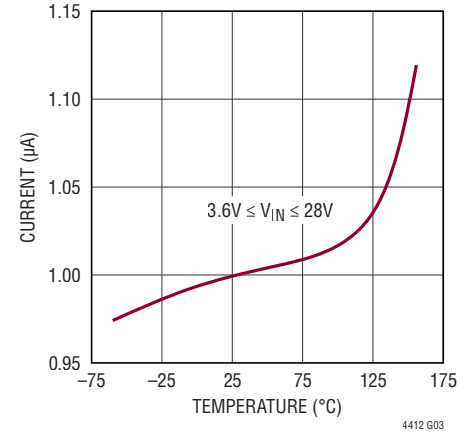
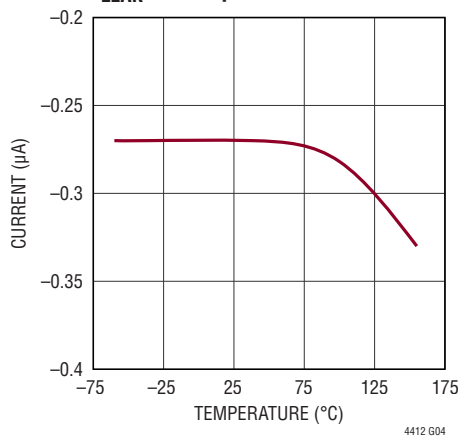
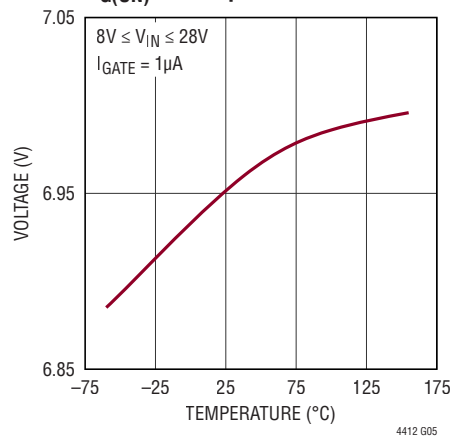
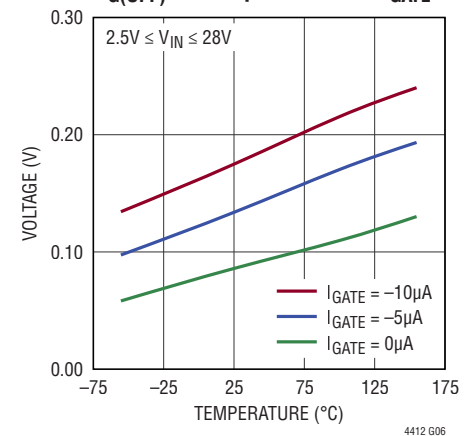
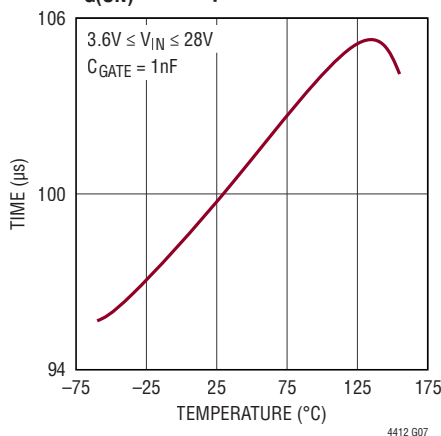
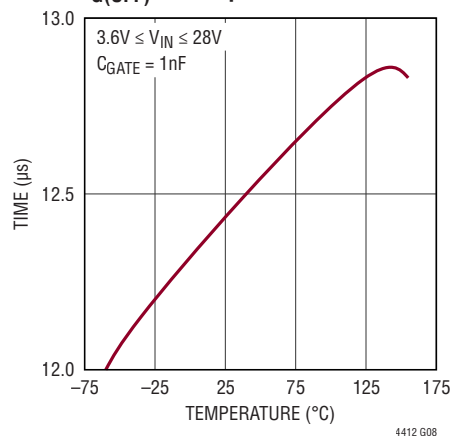
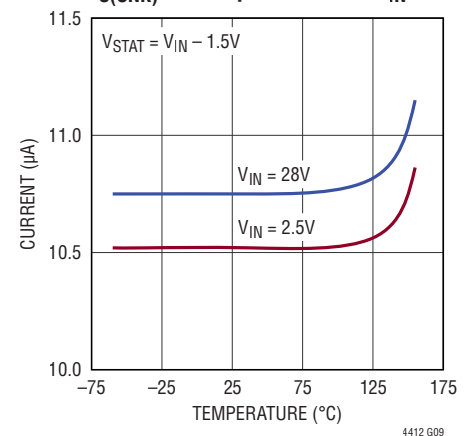
Note 5: V_{IN} is held at 12V and SENSE is stepped from 12.2V to 11.8V to trigger the event. GATE voltage is initially $V_{G(OFF)}$.

Note 6: V_{IN} is held at 12V and SENSE is stepped from 11.8V to 12.2V to trigger the event. GATE voltage is initially internally clamped at $V_{G(ON)}$.

Note 7: STAT is forced to $V_{IN} - 1.5V$. SENSE is set at $V_{IN} - 0.1V$ to measure the off current at STAT. SENSE is set $V_{IN} + 0.1V$ to measure the sink current at STAT.

Note 8: STAT is forced to 9V and V_{IN} is held at 12V. SENSE is stepped from 11.8V to 12.2V to measure the STAT turn-on time defined when I_{STAT} reaches one half the measured $I_{S(SNK)}$. SENSE is stepped from 12.2V to 11.8V to measure the STAT turn-off time defined when I_{STAT} reaches one half the measured $I_{S(SNK)}$.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{FR} vs Temperature and Supply Voltage**V_{RTO} vs Temperature and Supply Voltage****Normalized Quiescent Supply Current vs Temperature****I_{LEAK} vs Temperature****V_{G(ON)} vs Temperature****V_{G(OFF)} vs Temperature and I_{GATE}****t_{G(ON)} vs Temperature****t_{G(OFF)} vs Temperature****I_{S(SNK)} vs Temperature and V_{IN}**

PIN FUNCTIONS

V_{IN} (Pin 1): Primary Input Supply Voltage. Supplies power to the internal circuitry and is one of two voltage sense inputs to the internal analog controller (The other input to the controller is the SENSE pin). This input is usually supplied power from a battery or other power source which supplies current to the load. This pin can be bypassed to ground with a capacitor in the range of 0.1 μ F to 10 μ F if needed to suppress load transients.

GND (Pin 2): Ground. Provides a power return for all the internal circuits.

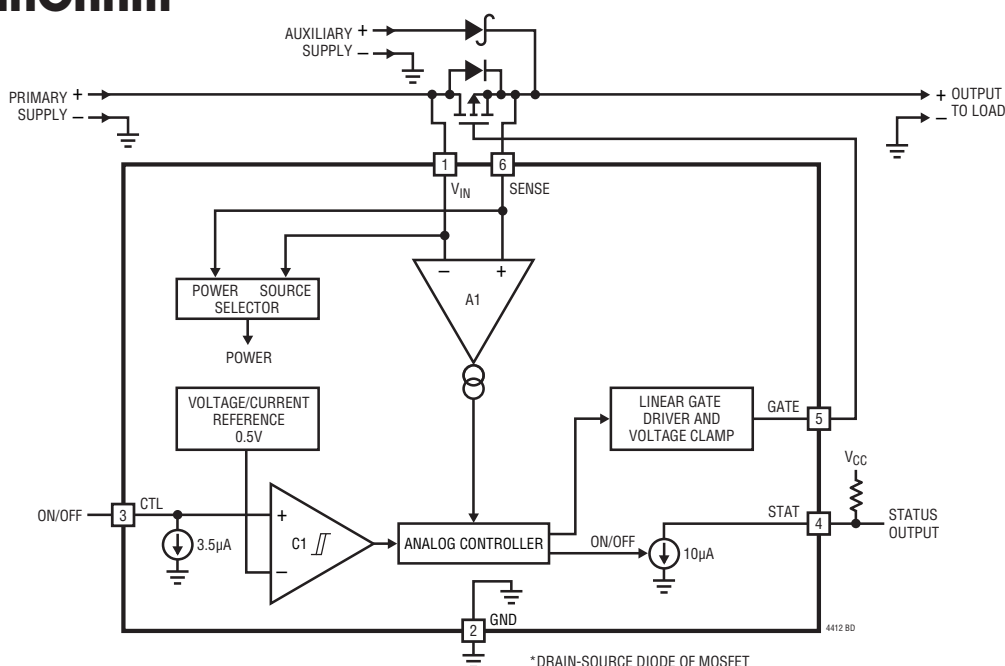
CTL (Pin 3): Digital Control Input. A logical high input (V_{IH}) on this pin forces the gate to source voltage of the primary P-channel MOSFET power switch to a small voltage ($V_{G\text{OFF}}$). This will turn the MOSFET off and no current will flow from the primary power input at V_{IN} if the MOSFET is configured so that the drain to source diode does not forward bias. A high input also forces the STAT pin to sink 10 μ A of current ($I_{S(SNK)}$). If the STAT pin is used to control an auxiliary P-channel power switch, then a second active source of power, such as an AC wall adaptor, will be connected to the load (see Applications Information). An internal current sink will pull the CTL pin voltage to ground (logical low) if the pin is open.

STAT (Pin 4): Open-Drain Output Status Pin. When the SENSE pin is pulled above the V_{IN} pin with an auxiliary power source by about 20mV or more, the reverse turn-off threshold (V_{RTO}) is reached. The STAT pin will then go from an open state to a 10 μ A current sink ($I_{S(SNK)}$). The STAT pin current sink can be used, along with an external resistor, to turn on an auxiliary P-channel power switch and/or signal the presence of an auxiliary power source to a microcontroller.

GATE (Pin 5): Primary P-Channel MOSFET Power Switch Gate Drive Pin. This pin is directed by the power controller to maintain a forward regulation voltage (V_{FR}) of 20mV between the V_{IN} and SENSE pins when an auxiliary power source is not present. When an auxiliary power source is connected, the GATE pin will pull up to the SENSE pin voltage, turning off the primary P-channel power switch.

SENSE (Pin 6): Power Sense Input Pin. Supplies power to the internal circuitry and is a voltage sense input to the internal analog controller (The other input to the controller is the V_{IN} pin). This input is usually supplied power from an auxiliary source such as an AC adaptor or back-up battery which also supplies current to the load.

BLOCK DIAGRAM



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OPERATION

Operation can best be understood by referring to the Block Diagram, which illustrates the internal circuit blocks along with the few external components, and the graph that accompanies Figure 1. The terms primary and auxiliary are arbitrary and may be changed to suit the application. Operation begins when either or both power sources are applied and the CTL control pin is below the input low voltage of 0.35V (V_{IL}). If only the primary supply is present, the Power Source Selector will power the LTC4412 from the V_{IN} pin. Amplifier A1 will deliver a current to the Analog Controller block that is proportional to the voltage difference in the V_{IN} and SENSE pins. While the voltage on SENSE is lower than $V_{IN} - 20\text{mV}$ (V_{FR}), the Analog Controller will instruct the Linear Gate Driver and Voltage Clamp block to pull down the GATE pin voltage and turn on the external P-channel MOSFET. The dynamic pull-down current of $50\mu\text{A}$ ($I_{G(SNK)}$) stops when the GATE voltage reaches ground or the gate clamp voltage. The gate clamp voltage is 7V ($V_{G(ON)}$) below the higher of V_{IN} or V_{SENSE} . As the SENSE voltage pulls up to $V_{IN} - 20\text{mV}$, the LTC4412 will regulate the GATE voltage to maintain a 20mV difference between V_{IN} and V_{SENSE} which is also the V_{DS} of the MOSFET. The system is now in the forward regulation mode and the load will be powered from the primary supply. As the load current varies, the GATE voltage will be controlled to maintain the 20mV difference. If the load current exceeds the P-channel MOSFET's ability to deliver the current with a 20mV V_{DS} the GATE voltage will clamp, the MOSFET will behave as a fixed resistor and the forward voltage will increase slightly. While the MOSFET is on the STAT pin is an open circuit.

When an auxiliary supply is applied, the SENSE pin will be pulled higher than the V_{IN} pin through the external diode.

The Power Source Selector will power the LTC4412 from the SENSE pin. As the SENSE voltage pulls above $V_{IN} - 20\text{mV}$, the Analog Controller will instruct the Linear Gate Driver and Voltage Clamp block to pull the GATE voltage up to turn off the P-channel MOSFET. When the voltage on SENSE is higher than $V_{IN} + 20\text{mV}$ (V_{RTO}), the Analog Controller will instruct the Linear Gate Driver and Voltage Clamp block to rapidly pull the GATE pin voltage to the SENSE pin voltage. This action will quickly finish turning off the external P-channel MOSFET if it hasn't already turned completely off. For a clean transition, the reverse turn-off threshold has hysteresis to prevent uncertainty. The system is now in the reverse turn-off mode. Power to the load is being delivered through the external diode and no current is drawn from the primary supply. The external diode provides protection in case the auxiliary supply is below the primary supply, sinks current to ground or is connected reverse polarity. During the reverse turn-off mode of operation the STAT pin will sink $10\mu\text{A}$ of current ($I_{S(SNK)}$) if connected. Note that the external MOSFET is wired so that the drain to source diode will momentarily forward bias when power is first applied to V_{IN} and will become reverse biased when an auxiliary supply is applied.

When the CTL (control) input is asserted high, the external MOSFET will have its gate to source voltage forced to a small voltage $V_{G(OFF)}$ and the STAT pin will sink $10\mu\text{A}$ of current if connected. This feature is useful to allow control input switching of the load between two power sources as shown in Figure 4 or as a switchable high side driver as shown in Figure 7. A $3.5\mu\text{A}$ internal pull-down current (I_{CTL}) on the CTL pin will insure a low level input if the pin should become open.

APPLICATIONS INFORMATION

Introduction

The system designer will find the LTC4412 useful in a variety of cost and space sensitive power control applications that include low loss diode OR'ing, fully automatic switchover from a primary to an auxiliary source of power, microcontroller controlled switchover from a primary to an auxiliary source of power, load sharing between two or more batteries, charging of multiple batteries from a single charger and high side power switching.

External P-Channel MOSFET Transistor Selection

Important parameters for the selection of MOSFETs are the maximum drain-source voltage $V_{DS(MAX)}$, threshold voltage $V_{GS(VT)}$ and on-resistance $R_{DS(ON)}$.

The maximum allowable drain-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the maximum drain-source voltage seen in the application.

The maximum gate drive voltage for the primary MOSFET is set by the smaller of the V_{IN} supply voltage or the internal clamping voltage $V_{G(ON)}$. A logic level MOSFET is commonly used, but if a low supply voltage limits the gate voltage, a sub-logic level threshold MOSFET should be considered. The maximum gate drive voltage for the auxiliary MOSFET, if used, is determined by the external resistor connected to the STAT pin and the STAT pin sink current.

As a general rule, select a MOSFET with a low enough $R_{DS(ON)}$ to obtain the desired V_{DS} while operating at full load current and an achievable V_{GS} . The MOSFET normally operates in the linear region and acts like a voltage controlled resistor. If the MOSFET is grossly undersized, it can enter the saturation region and a large V_{DS} may result. However, the drain-source diode of the MOSFET, if forward biased, will limit V_{DS} . A large V_{DS} , combined with the load current, will likely result in excessively high MOSFET power dissipation. Keep in mind that the LTC4412 will regulate the forward voltage drop across the primary MOSFET at 20mV if $R_{DS(ON)}$ is low enough. The required $R_{DS(ON)}$ can be calculated by dividing 0.02V by the load current in amps. Achieving forward regulation will minimize power loss and heat dissipation, but it is not a necessity.

If a forward voltage drop of more than 20mV is acceptable then a smaller MOSFET can be used, but must be sized compatible with the higher power dissipation. Care should be taken to ensure that the power dissipated is never allowed to rise above the manufacturer's recommended maximum level. The auxiliary MOSFET power switch, if used, has similar considerations, but its V_{GS} can be tailored by resistor selection. When choosing the resistor value consider the full range of STAT pin current ($I_{S(SNK)}$) that may flow through it.

V_{IN} and SENSE Pin Bypass Capacitors

Many types of capacitors, ranging from 0.1 μ F to 10 μ F and located close to the LTC4412, will provide adequate V_{IN} bypassing if needed. Voltage droop can occur at the load during a supply switchover because some time is required to turn on the MOSFET power switch. Factors that determine the magnitude of the voltage droop include the supply rise and fall times, the MOSFET's characteristics, the value of C_{OUT} and the load current. Droop can be made insignificant by the proper choice of C_{OUT} , since the droop is inversely proportional to the capacitance. Bypass capacitance for the load also depends on the application's dynamic load requirements and typically ranges from 1 μ F to 47 μ F. In all cases, the maximum droop is limited to the drain source diode forward drop inside the MOSFET.

Caution must be exercised when using multilayer ceramic capacitors. Because of the self resonance and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions such as connecting a supply input to a hot power source. To reduce the Q and prevent these transients from exceeding the LTC4412's absolute maximum voltage rating, the capacitor's ESR can be increased by adding up to several ohms of resistance in series with the ceramic capacitor. Refer to Application Note 88.

The selected capacitance value and capacitor's ESR can be verified by observing V_{IN} and SENSE for acceptable voltage transitions during dynamic conditions over the full load current range. This should be checked with each power source as well. Ringing may indicate an incorrect bypass capacitor value and/or too low an ESR.

APPLICATIONS INFORMATION

V_{IN} and SENSE Pin Usage

Since the analog controller's thresholds are small ($\pm 20\text{mV}$), the V_{IN} and SENSE pin connections should be made in a way to avoid unwanted $I \cdot R$ drops in the power path. Both pins are protected from negative voltages.

GATE Pin Usage

The GATE pin controls the external P-channel MOSFET connected between the V_{IN} and SENSE pins when the load current is supplied by the power source at V_{IN} . In this mode of operation, the internal current source, which is responsible for pulling the GATE pin up, is limited to a few microamps ($I_{G(SRC)}$). If external opposing leakage currents exceed this, the GATE pin voltage will reach the clamp voltage (V_{GON}) and V_{DS} will be smaller. The internal current sink, which is responsible for pulling the GATE pin down, has a higher current capability ($I_{G(SNK)}$). With an auxiliary supply input pulling up on the SENSE pin and exceeding the V_{IN} pin voltage by 20mV (V_{RTO}), the device enters the reverse turn-off mode and a much stronger current source is available to oppose external leakage currents and turn off the MOSFET (V_{GOFF}).

While in forward regulation, if the on resistance of the MOSFET is too high to maintain forward regulation, the GATE pin will maximize the MOSFET's V_{GS} to that of the clamp voltage (V_{GON}). The clamping action takes place between the higher of V_{IN} or V_{SENSE} and the GATE pin.

Status Pin Usage

During normal operation, the open-drain STAT pin can be biased at any voltage between ground and 28V regardless of the supply voltage to the LTC4412. It is usually connected to a resistor whose other end connects to a voltage source. In the forward regulation mode, the STAT pin will be open ($I_{S(OFF)}$). When a wall adaptor input or other auxiliary supply is connected to that input, and the voltage on SENSE is higher than $V_{IN} + 20\text{mV}$ (V_{RTO}), the system is in the reverse turn-off mode. During this mode of operation the STAT pin will sink $10\mu\text{A}$ of current ($I_{S(SNK)}$). This will result in a voltage change across the resistor, depending on the resistance, which is useful to turn on an auxiliary P-channel MOSFET or signal to a microcontroller that an auxiliary power source is connected. External

leakage currents, if significant, should be accounted for when determining the voltage across the resistor when the STAT pin is either on or off.

Control Pin Usage

This is a digital control input pin with low threshold voltages (V_{IL}, V_{IH}) for use with logic powered from as little as 1V . During normal operation, the CTL pin can be biased at any voltage between ground and 28V , regardless of the supply voltage to the LTC4412. A logical high input on this pin forces the gate to source voltage of the primary P-channel MOSFET power switch to a small voltage (V_{GOFF}). This will turn the MOSFET off and no current will flow from the primary power input at V_{IN} if the MOSFET is configured so that the drain to source diode is not forward biased. The high input also forces the STAT pin to sink $10\mu\text{A}$ of current ($I_{S(SNK)}$). See the Typical Applications for various examples on using the STAT pin. A $3.5\mu\text{A}$ internal pull-down current (I_{CTL}) on the CTL pin will insure a logical low level input if the pin should be open.

Protection

Most of the application circuits shown provide some protection against supply faults such as shorted, low or reversed supply inputs. The fault protection does not protect shorted supplies but can isolate other supplies and the load from faults. A necessary condition of this protection is for all components to have sufficient breakdown voltages. In some cases, if protection of the auxiliary input (sometimes referred to as the wall adapter input) is not required, then the series diode or MOSFET may be eliminated.

Internal protection for the LTC4412 is provided to prevent damaging pin currents and excessive internal self heating during a fault condition. These fault conditions can be a result of any LTC4412 pins shorted to ground or to a power source that is within the pin's absolute maximum voltage limits. Both the V_{IN} and SENSE pins are capable of being taken significantly below ground without current drain or damage to the IC (see Absolute Maximum Voltage Limits). This feature allows for reverse-battery condition without current drain or damage. This internal protection is not designed to prevent overcurrent or overheating of external components.

TYPICAL APPLICATIONS

Automatic PowerPath Control

The applications shown in Figures 1, 2 and 3 are automatic ideal diode controllers that require no assistance from a microcontroller. Each of these will automatically connect the higher supply voltage, after accounting for certain diode forward voltage drops, to the load with application of the higher supply voltage.

Figure 1 illustrates an application circuit for automatic switchover of a load between a battery and a wall adapter or other power input. With application of the battery, the load will initially be pulled up by the drain-source diode of the P-channel MOSFET. As the LTC4412 comes into action, it will control the MOSFET's gate to turn it on and reduce the MOSFET's voltage drop from a diode drop to 20mV. The system is now in the low loss forward regulation mode. Should the wall adapter input be applied, the Schottky diode will pull up the SENSE pin, connected to the load, above the battery voltage and the LTC4412 will turn the MOSFET off. The STAT pin will then sink current indicating an auxiliary input is connected. The battery is now supplying no load current and all the load current flows through the Schottky diode. A silicon diode could be used instead of the Schottky, but will result in higher power dissipation and heating due to the higher forward voltage drop.

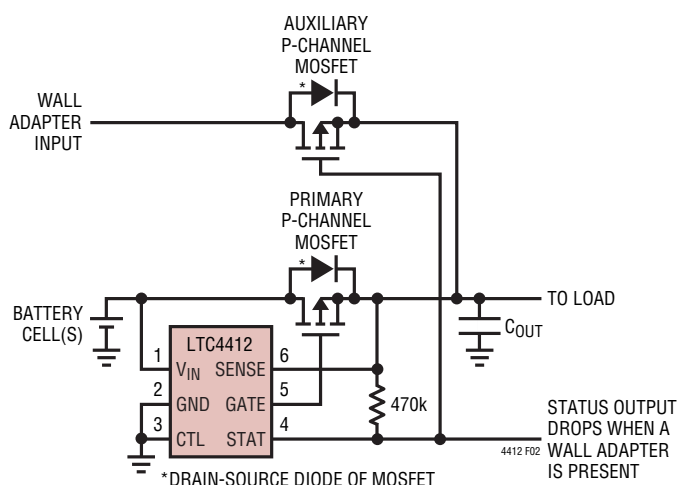


Figure 2. Automatic Switchover of Load Between a Battery and a Wall Adapter with Auxiliary P-Channel MOSFET for Lowest Loss

Figure 2 illustrates an application circuit for automatic switchover of load between a battery and a wall adapter that features lowest power loss. Operation is similar to Figure 1 except that an auxiliary P-channel MOSFET replaces the diode. The STAT pin is used to turn on the MOSFET once the SENSE pin voltage exceeds the battery voltage by 20mV. When the wall adapter input is applied, the drain-source diode of the auxiliary MOSFET will turn on first to pull up the SENSE pin and turn off the primary MOSFET followed by turning on of the auxiliary MOSFET. Once the auxiliary MOSFET has turned on the voltage drop across it can be very low depending on the MOSFET's characteristics.

Figure 3 illustrates an application circuit for the automatic switchover of a load between a battery and a wall adapter in the comparator mode. It also shows how a battery charger can be connected. This circuit differs from Figure 1 in the way the SENSE pin is connected. The SENSE pin is connected directly to the auxiliary power input and not the load. This change forces the LTC4412's control circuitry to operate in an open-loop comparator mode. While the battery supplies the system, the GATE pin voltage will be forced to its lowest clamped potential, instead of being regulated to maintain a 20mV drop across the MOSFET. This has the advantages of minimizing power loss in the MOSFET by minimizing its R_{ON} and not having the influence of a linear control loop's dynamics. A possible disadvantage is if the auxiliary input ramps up slow enough the load voltage will initially droop before rising. This is due to the

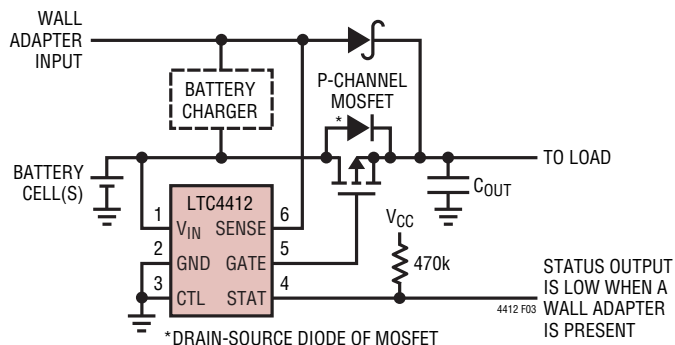


Figure 3. Automatic Switchover of Load Between a Battery and a Wall Adapter in Comparator Mode

TYPICAL APPLICATIONS

Multiple Battery Charging

Figure 6 illustrates an application circuit for automatic dual battery charging from a single charger. Whichever battery has the lower voltage will receive the charging current until both battery voltages are equal, then both will be charged. When both are charged simultaneously, the higher capacity battery will get proportionally higher current from the charger. For Li-Ion batteries, both batteries will achieve the float voltage minus the forward regulation voltage of 20mV. This concept can apply to more than two batteries. The STAT pins provide information as to which batteries are being charged. For intelligent control, the CTL pin input can be used with a microcontroller and back-to-back MOSFETs as shown in Figure 4. This allows complete control for disconnection of the charger from either battery.

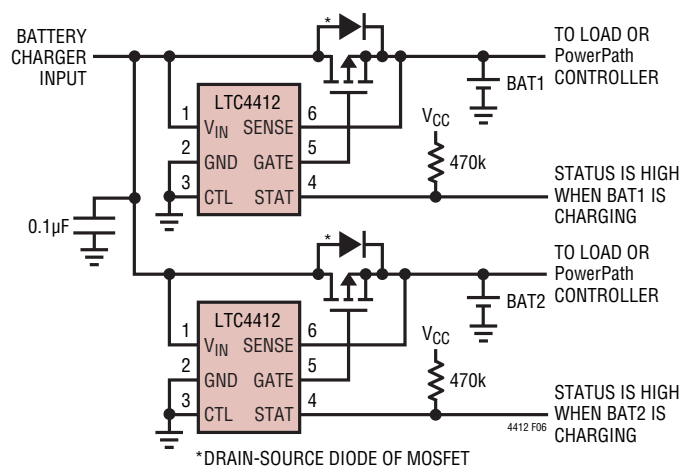


Figure 6. Automatic Dual Battery Charging from Single Charging Source

High Side Power Switch

Figure 7 illustrates an application circuit for a logic controlled high side power switch. When the CTL pin is a logical low, the LTC4412 will turn on the MOSFET. Because the SENSE pin is grounded, the LTC4412 will apply maximum clamped gate drive voltage to the MOSFET. When the CTL pin is a logical high, the LTC4412 will turn off the MOSFET by pulling its gate voltage up to the supply input voltage and thus deny power to the load. The MOSFET is connected with its source connected to the power source. This disables the drain-source diode from supplying voltage to the load when the MOSFET is off. Note that if the load is powered from another source, then the drain-source diode can forward bias and deliver current to the power supply connected to the VIN pin.

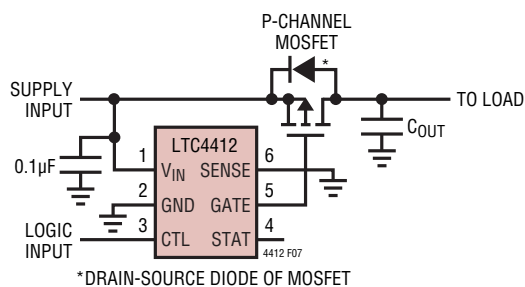


Figure 7. Logic Controlled High Side Power Switch

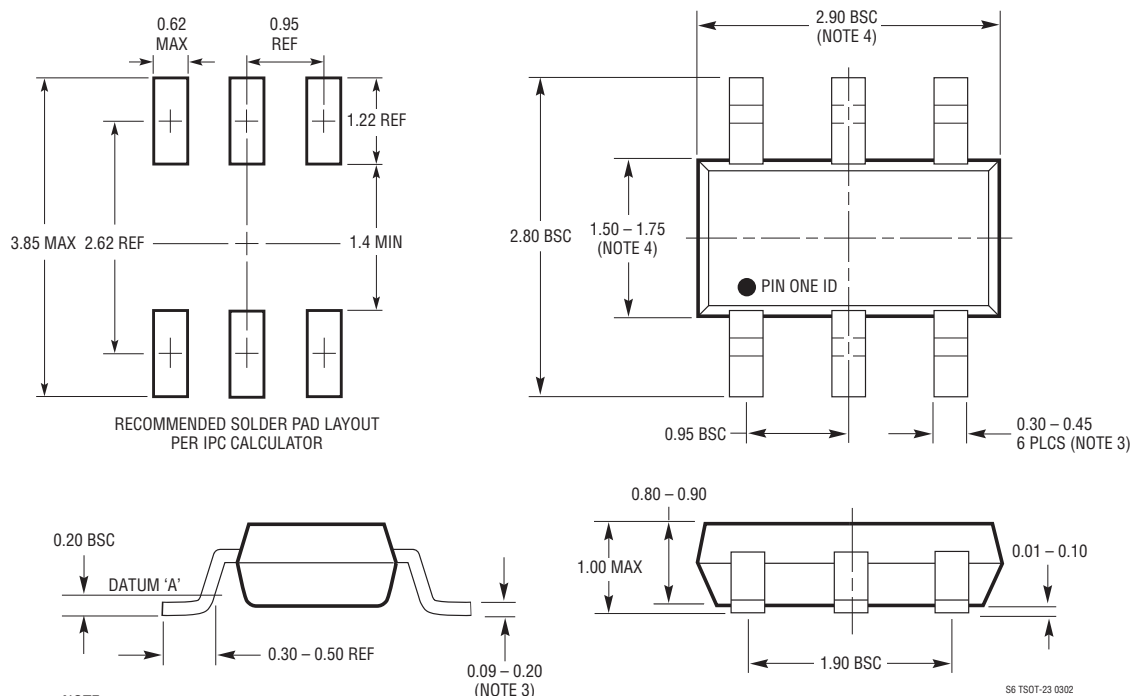
REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	02/15	Added H and MP-grade options.	Throughout

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
 (Reference LTC DWG # 05-08-1636)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1473	Dual PowerPath Switch Driver	Switches and Isolates Sources Up to 30V
LTC1479	PowerPath Controller for Dual Battery Systems	Complete PowerPath Management for Two Batteries; DC Power Source, Charger and Backup
LTC1558/LTC1559	Back-Up Battery Controller with Programmable Output	Adjustable Backup Voltage from 1.2V NiCd Button Cell, Includes Boost Converter
LT[®]1579	300mA Dual Input Smart Battery Back-Up Regulator	Maintains Output Regulation with Dual Inputs, 0.4V Dropout at 300mA
LTC1733/LTC1734	Monolithic Linear Li-Ion Chargers	Thermal Regulation, No External MOSFET/Sense Resistor
LTC1960	Dual Battery Charger Selector with SPI	Complete Dual Battery Charger/Selector System, 36-Lead SSOP
LTC1998	2.5μA, 1% Accurate Programmable Battery Detector	Adjustable Trip Voltage/Hysteresis, ThinSOT
LTC4350	Hot Swappable Load Share Controller	Allows N + 1 Redundant Supply, Equally Loads Multiple Power Supplies Connected in Parallel
LTC4410	USB Power Manager in ThinSOT	Enables Simultaneous Battery Charging and Operation of USB Component Peripheral Devices