

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ( $V_{CCn}$ )	17V
SENSE $n$ Pins	-0.3V to ( $V_{CC} + 0.3V$ )
FB $n$ , ON Pins	-0.3V to ( $V_{CC} + 0.3V$ )
TIMER Pin	-0.3V to 2V
GATE $n$ Pins	Internally Limited (Note 3)
RESET $n$ , FAULT, FILTER Pins	-0.3V to 17V
Operating Temperature Range	
LTC4230C	0°C to 70°C
LTC4230I	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

## PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
FB3	1	20 FB2
RESET 3	2	19 RESET 2
GATE 3	3	18 GATE 2
SENSE 3	4	17 SENSE 2
$V_{CC3}$	5	16 $V_{CC2}$
$V_{CC1}$	6	15 ON
SENSE 1	7	14 GND
GATE 1	8	13 FAULT
RESET 1	9	12 TIMER
FB1	10	11 FILTER
GN PACKAGE 20-LEAD PLASTIC SSOP $T_{JMAX} = 125^{\circ}C$ , $\theta_{JA} = 95^{\circ}C/W$		LTC4230CGN LTC4230IGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^{\circ}C$ .  $V_{CC1} = 3.3V$ ,  $V_{CC2} = 2.5V$ ,  $V_{CC3} = 1.8V$  unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V <sub>CC</sub>	Supply Voltage (V <sub>CC1</sub> )		●	2.700		16.5	V
	Supply Voltage (V <sub>CC2</sub> )	V <sub>CC2</sub> ≤ V <sub>CC1</sub>	●	2.375		16.5	V
	Supply Voltage (V <sub>CC3</sub> )	V <sub>CC3</sub> ≤ (V <sub>CC1</sub> − 1V)	●	1.700		15.5	V
I <sub>CC</sub>	Supply Current (I <sub>CC1</sub> )	ON = V <sub>CC1</sub> , FB1 = High	●		1.8	3	mA
	Supply Current (I <sub>CC2</sub> )	ON = V <sub>CC1</sub> , FB2 = High	●		75	150	μA
	Supply Current (I <sub>CC3</sub> )	ON = V <sub>CC1</sub> , FB3 = High	●		65	150	μA
V <sub>LK01</sub>	Undervoltage Lockout , Channel 1	V <sub>CC1</sub> Low to High Transition	●	2.15	2.35	2.52	V
V <sub>LK02</sub>	Undervoltage Lockout , Channel 2	V <sub>CC2</sub> Low to High Transition	●	1.98	2.15	2.32	V
V <sub>LK03</sub>	Undervoltage Lockout , Channel 3	V <sub>CC3</sub> Low to High Transition	●	1.09	1.19	1.29	V
V <sub>LKOHST1</sub>	Undervoltage Lockout Hysteresis, Channel 1				100		mV
V <sub>LKOHST2</sub>	Undervoltage Lockout Hysteresis, Channel 2				45		mV
V <sub>LKOHST3</sub>	Undervoltage Lockout Hysteresis, Channel 3				35		mV
I <sub>IN</sub> , FB <sub>n</sub>	FB <sub>n</sub> Pin Input Current	0V ≤ V <sub>FB<sub>n</sub></sub> ≤ V <sub>CC<sub>n</sub></sub>	●		±0.1	±10	μA
I <sub>IN</sub> , ON	ON Pin Input Current	0V ≤ V <sub>ON</sub> ≤ V <sub>CC1</sub>	●		±0.1	±10	μA
I <sub>IN</sub> , SENSE <sub>n</sub>	Input Current for SENSE <sub>n</sub>	0V ≤ V <sub>SENSE<sub>n</sub></sub> ≤ V <sub>CC<sub>n</sub></sub>	●		±0.1	±15	μA
V <sub>CB(FAST)</sub>	Circuit Breaker <sub>n</sub> Trip Voltage	Fast Comparator	●	135	150	165	mV
V <sub>CB(SLOW)</sub>		Slow Comparator	●	40	50	60	mV
I <sub>GATE<sub>n</sub></sub> , UP	GATE <sub>n</sub> Pull-Up Current	Charge Pump On, 0 ≤ V <sub>GATE<sub>n</sub></sub> < 0.2V	●	−12.5	−10	−6.5	μA
I <sub>GATE<sub>n</sub></sub> , DN	Normal GATE <sub>n</sub> Pull-Down Current	ON Low, V <sub>GATE<sub>n</sub></sub> = 5V			200		μA
	Fast GATE <sub>n</sub> Pull-Down Current	FAULT Latched and Circuit Breaker Tripped or in UVLO, V <sub>GATE<sub>n</sub></sub> = 5V			16		mA
I <sub>LEAK</sub>	RESET <sub>n</sub> Leakage Current	V <sub>RESET<sub>n</sub></sub> = 15V, Pull-Down Device Off	●		±0.1	±2.5	μA

**ELECTRICAL CHARACTERISTICS**

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  $V_{CC1} = 3.3\text{V}$ ,  $V_{CC2} = 2.5\text{V}$ ,  $V_{CC3} = 1.8\text{V}$  unless otherwise noted. (Note 2)

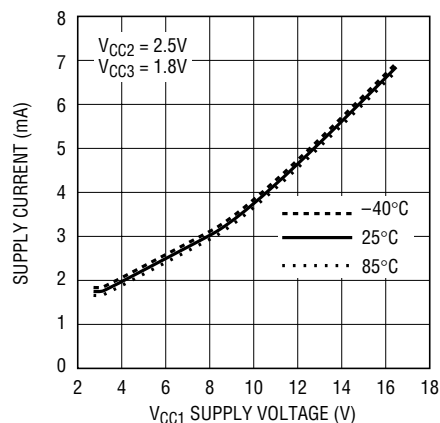
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\Delta V_{GATEn}$	External N-Channel Gate Drive	$V_{GATE1,2} - V_{CC1,2}$ (for $V_{CC1,2} = 2.7\text{V}$ , $V_{CC3} = V_{CC1} - 1\text{V}$ ) $V_{GATE3} - V_{CC3}$ (for $V_{CC1,2} = 2.7\text{V}$ , $V_{CC3} = V_{CC1} - 1\text{V}$ ) $V_{GATE1,2} - V_{CC1,2}$ (for $V_{CC1,2} = 3.3\text{V}$ , $V_{CC3} = V_{CC1} - 1\text{V}$ ) $V_{GATE3} - V_{CC3}$ (for $V_{CC1,2} = 3.3\text{V}$ , $V_{CC3} = V_{CC1} - 1\text{V}$ ) $V_{GATEn} - V_{CCn}$ (for $V_{CC1,2} = 5\text{V}$ , $V_{CC3} = V_{CC1} - 1\text{V}$ ) $V_{GATEn} - V_{CCn}$ (for $V_{CC1,2} = 12\text{V}$ or $15\text{V}$ , $V_{CC3} = V_{CC1} - 1\text{V}$ )	● ● ● ● ● ●	4.5 5.5 5 6 9 7		8 9 10 11 16 18	V V V V V V
$V_{GATEn,OV}$	GATE $n$ Overvoltage Lockout Threshold				0.25		V
$V_{FBn}$	FB $n$ Low Threshold Voltage	FB $n$ High to Low Transition	●	1.209	1.234	1.259	V
$\Delta V_{FBn}$	FB $n$ Line Regulation	$2.7\text{V} \leq V_{CC1} \leq 16.5\text{V}$			0.5		mV
$V_{FBn,HST}$	FB $n$ Hysteresis				3		mV
$V_{ONHI}$	ON High Threshold Voltage	ON Low to High Transition	●	1.250	1.314	1.380	V
$V_{ONLO}$	ON Low Threshold Voltage	ON High to Low Transition	●	1.172	1.234	1.270	V
$V_{ONHST}$	ON Hysteresis				80		mV
$I_{FILTER}$	FILTER Pull-Up Current FILTER Pull-Down Current	During Slow Fault Condition During Normal and Reset Conditions	● ●	-2.5 7	-2 10	-1.3 13	$\mu\text{A}$ $\mu\text{A}$
$V_{FILTER}$	FILTER Threshold	Latched Off Threshold, FILTER Low to High	●	1.10	1.26	1.42	V
$V_{FILTERHST}$	FILTER Threshold Hysteresis				-70		mV
$I_{TMR}$	TIMER Pull-Up Current TIMER Pull-Down Current	TIMER On TIMER Off, $V_{FAULT} = \text{Low}$ $V_{TIMER} = 1.5\text{V}$	● ●	-23 0.9	-20 1.6 2.5	-17 2.3	$\mu\text{A}$ $\mu\text{A}$ mA
$V_{TMR}$	TIMER Threshold	TIMER Low to High TIMER High to Low	● ●	1.172	1.234 0.3	1.27 0.5	V V
$V_{FAULT}$	FAULT Low Threshold Voltage	FAULT High to Low	●	1.172	1.234	1.27	V
$V_{FAULT,HST}$	FAULT Hysteresis	FAULT Low to High			50		mV
$I_{FAULT,UP}$	FAULT Pull-Up Current		●	-2.5	-2	-1.5	$\mu\text{A}$
$V_{OLFAULT}$	Output Low Voltage	$I_{FAULT} = 1.6\text{mA}$ , $V_{CC1} = 5\text{V}$	●		0.19	0.4	V
$V_{OLRESETn}$	Output Low Voltage	$I_{RESETn} = 1.6\text{mA}$ , $V_{CC1} = 5\text{V}$	●		0.19	0.4	V
$t_{GATEFC}$	Fast COMP $n$ Trip to GATE $n$ Discharging	$V_{CB} = 0\text{mV}$ to $200\text{mV}$ Step	●		0.5	1	$\mu\text{s}$
$t_{FAULTSC}$	Slow Comparator Trip to FILTER High and FAULT Latched	$V_{CB} = 0\text{mV}$ to $100\text{mV}$ Step, FILTER Floating 10nF at FILTER Pin to GND			10 7		$\mu\text{s}$ ms
$t_{OVPTFR}$	FILTER Comparator Trip to GATE $n$ Discharging	$V_{FILTER} = 0\text{V}$ to $5\text{V}$	●		8	12	$\mu\text{s}$
$t_{EXTFAULT}$	FAULT Low to GATE Discharging	$V_{FAULT} = 5\text{V}$ to $0\text{V}$	●	1.5	3	4.5	$\mu\text{s}$
$t_{RESET}$	Circuit Breaker Reset Time	ON Held Low to Guarantee FAULT High	●		15	30	$\mu\text{s}$
$t_{OFF}$	Turn-Off Time	ON Goes Low to GATE $n$ Off			8		$\mu\text{s}$

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All current into device pins is positive; all current out of device pins is negative; all voltages are referenced to ground unless otherwise specified.

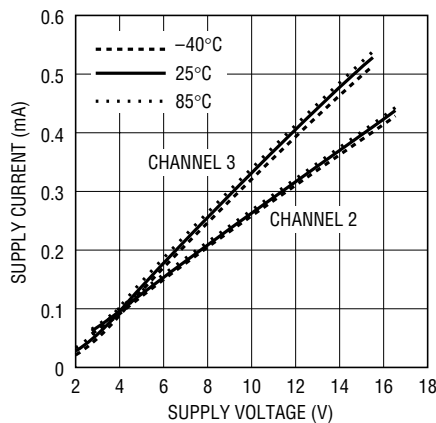
**Note 3:** An internal zener at the GATE $n$  pin clamps the charge pump voltage to a typical maximum operating voltage of 26V. External overdrive of the GATE $n$  pin beyond the internal zener voltage may damage the part. The GATE $n$  capacitance must be  $< 0.15\mu\text{F}$  at maximum  $V_{CC}$ . If a lower GATE $n$  pin voltage is desired, use an external zener diode.

## TYPICAL PERFORMANCE CHARACTERISTICS

Channel 1 Supply Current vs  $V_{CC1}$  Supply Voltage

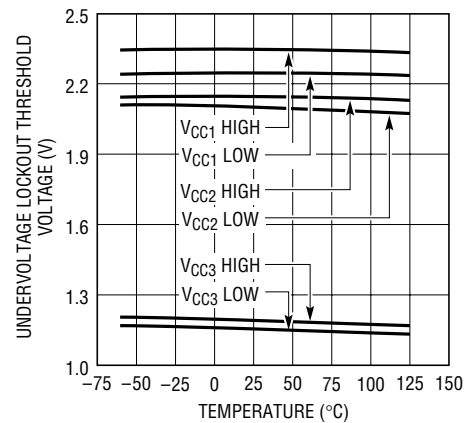
4230 G01

Channels 2 and 3 Supply Current vs Supply Voltage

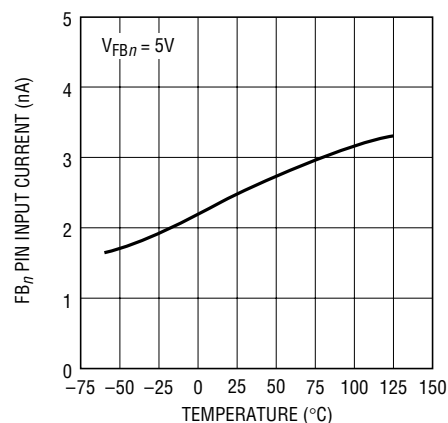


4230 G02

UVLO Threshold Voltage vs Temperature

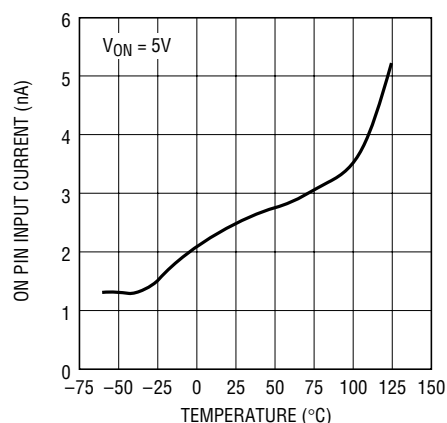


4230 G03

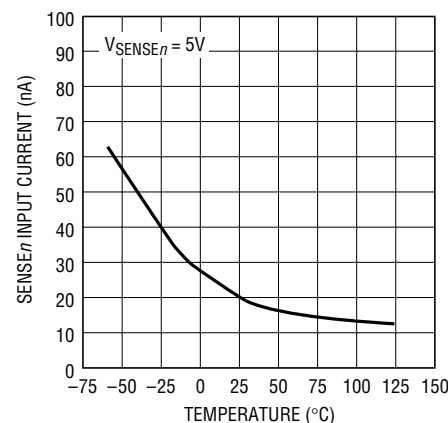
 $FB_n$  Pin Input Current vs Temperature

4230 G04

ON Pin Input Current vs Temperature

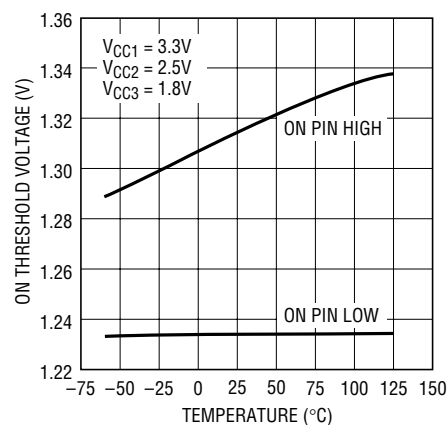


4230 G05

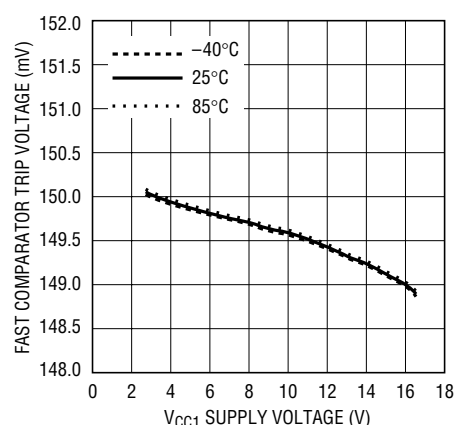
 $SENSE_n$  Input Current vs Temperature

4230 G06

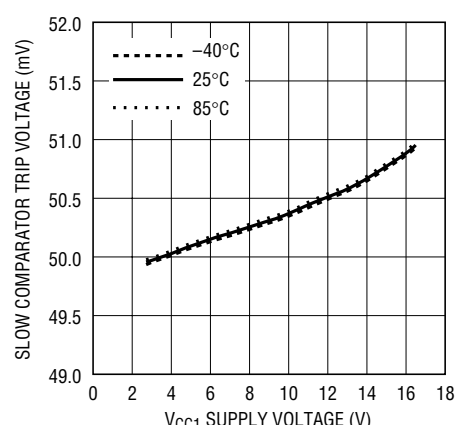
ON Threshold vs Temperature



4230 G07

Fast Comparator Threshold vs  $V_{CC1}$  Supply Voltage

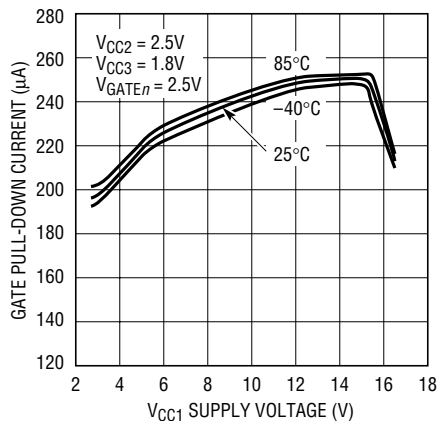
4230 G08

Slow Comparator Threshold vs  $V_{CC1}$  Supply Voltage

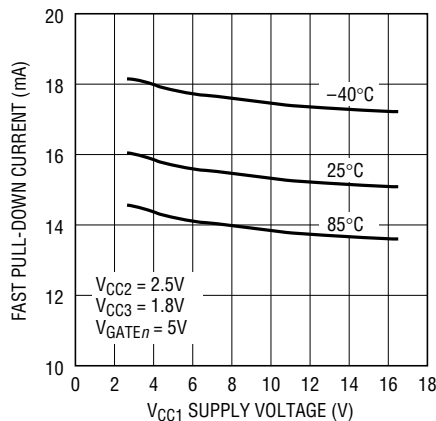
4230 G09

# TYPICAL PERFORMANCE CHARACTERISTICS

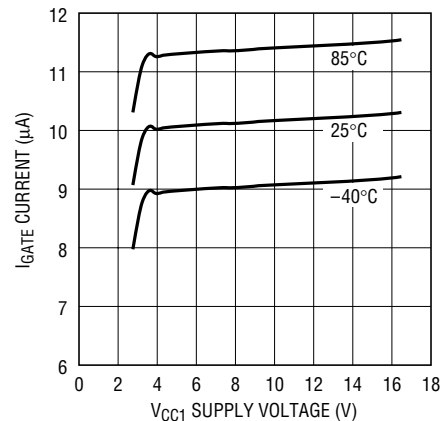
**Normal GATE<sub>n</sub> Pull-Down Current vs V<sub>CC1</sub> Supply Voltage**



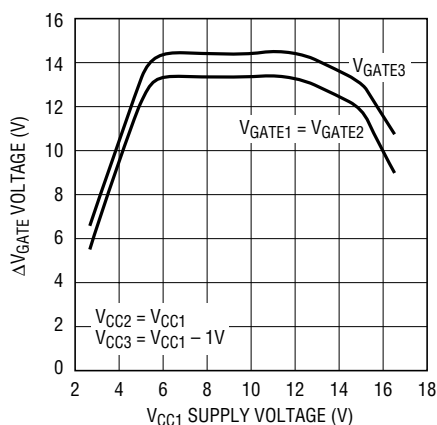
**Fast GATE<sub>n</sub> Pull-Down Current vs V<sub>CC1</sub> Supply Voltage**



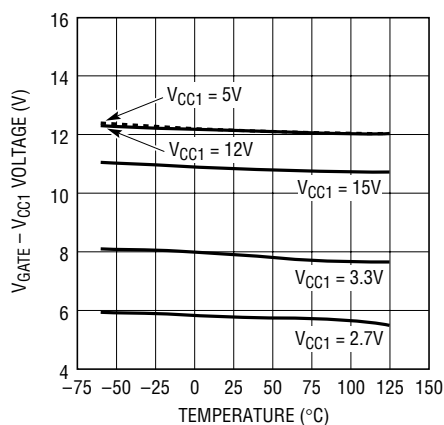
**GATE<sub>n</sub> Output Source Current (Pull-Up) vs V<sub>CC1</sub> Supply Voltage**



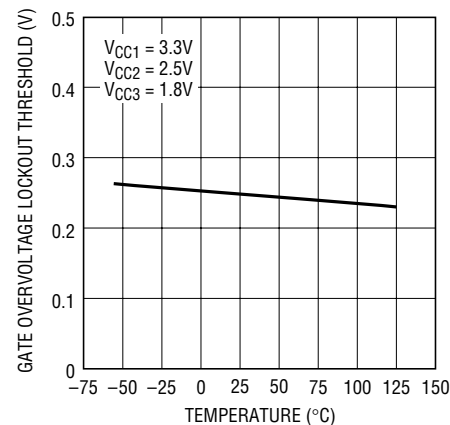
**V<sub>GATE<sub>n</sub></sub> - V<sub>CC<sub>n</sub></sub> vs V<sub>CC1</sub> Supply Voltage**



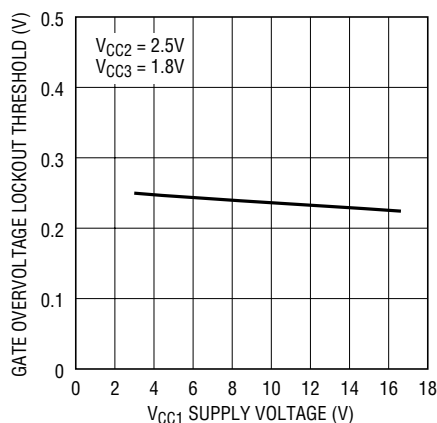
**V<sub>GATE1</sub> - V<sub>CC1</sub> vs Temperature**



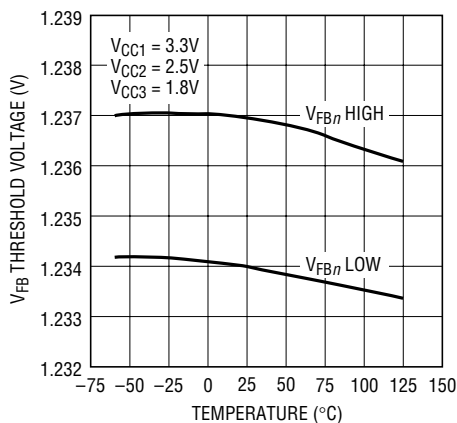
**GATE<sub>n</sub> Overvoltage Lockout Threshold vs Temperature**



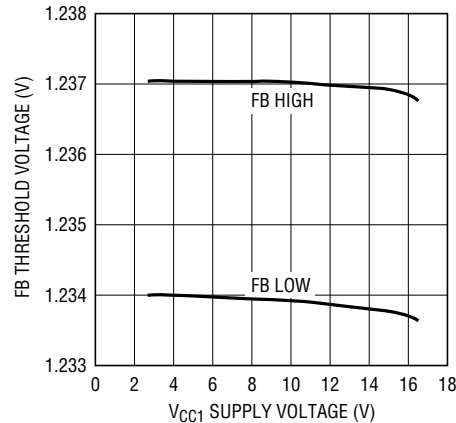
**GATE<sub>n</sub> Overvoltage Lockout Threshold vs V<sub>CC1</sub> Supply Voltage**



**V<sub>FB<sub>n</sub></sub> Threshold Voltage vs Temperature**

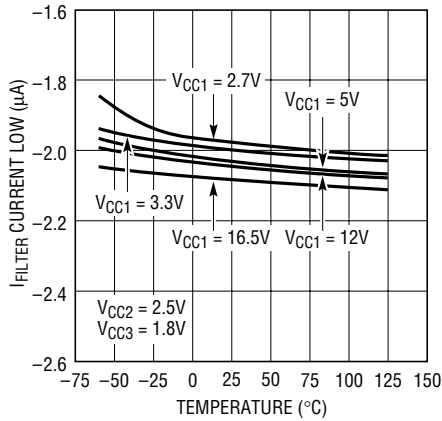


**V<sub>FB<sub>n</sub></sub> Threshold Voltage vs V<sub>CC1</sub> Supply Voltage**

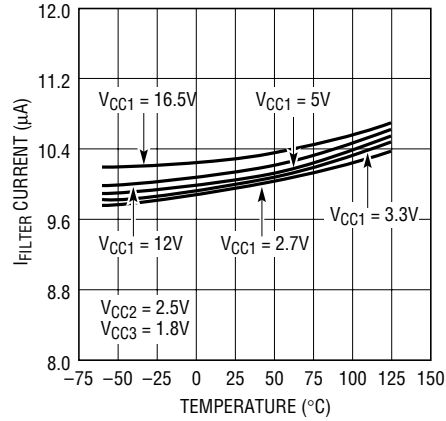


## TYPICAL PERFORMANCE CHARACTERISTICS

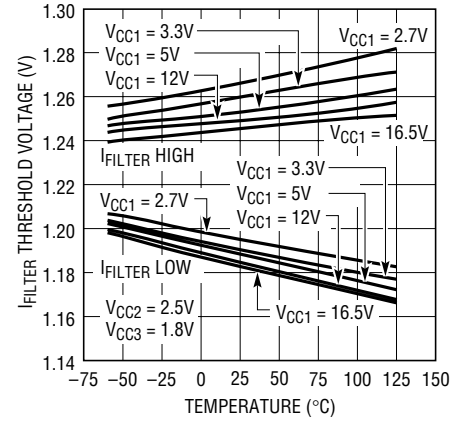
FILTER Pull-Up Current vs Temperature



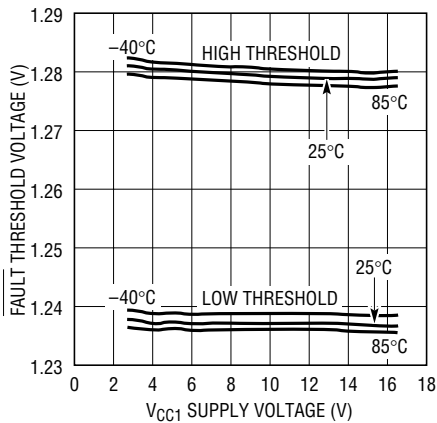
FILTER Pull-Down Current vs Temperature



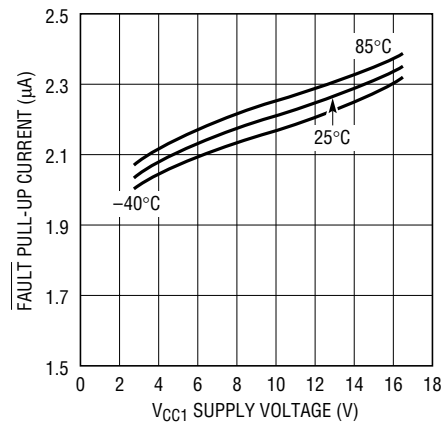
FILTER Threshold Voltage vs Temperature



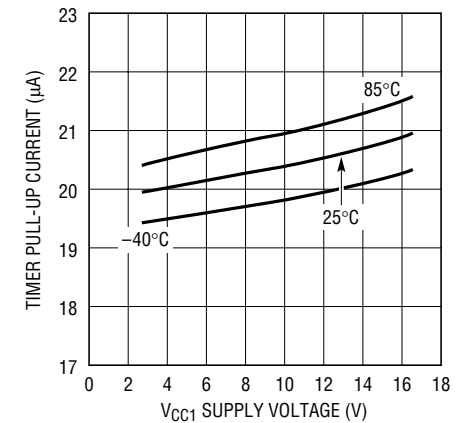
FAULT Threshold Voltage vs VCC1 Supply Voltage



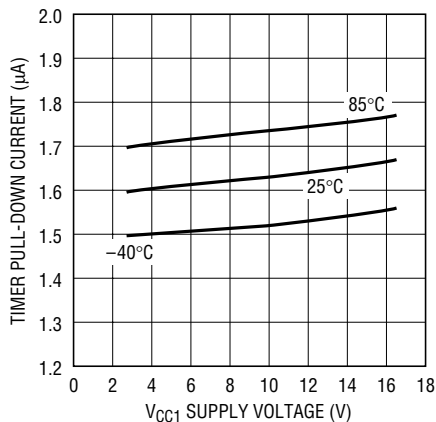
FAULT Pull-Up Current vs VCC1 Supply Voltage



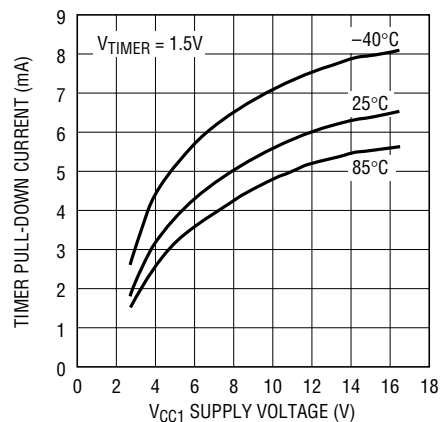
TIMER Pull-Up Current (During First Cycle) vs VCC1 Supply Voltage



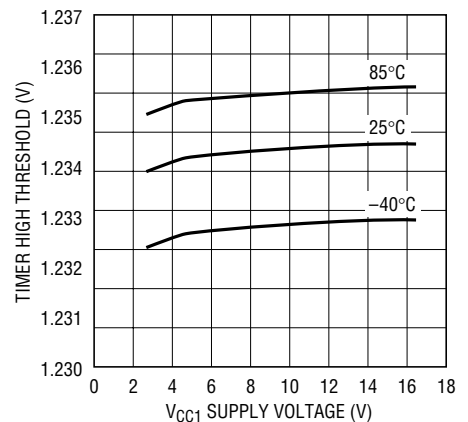
TIMER Pull-Down Current (After Second Cycle) vs VCC1 Supply Voltage



TIMER Fast Pull-Down (End of the First Cycle) Current vs VCC1 Supply Voltage

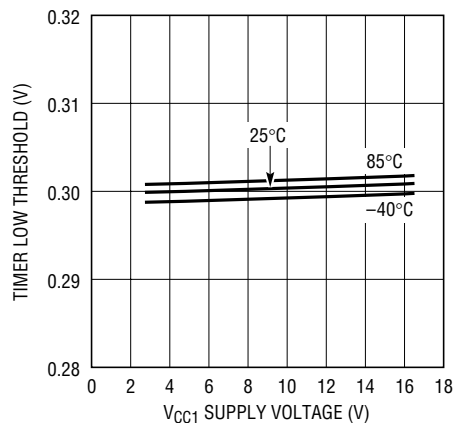


TIMER High Threshold vs VCC1 Supply Voltage



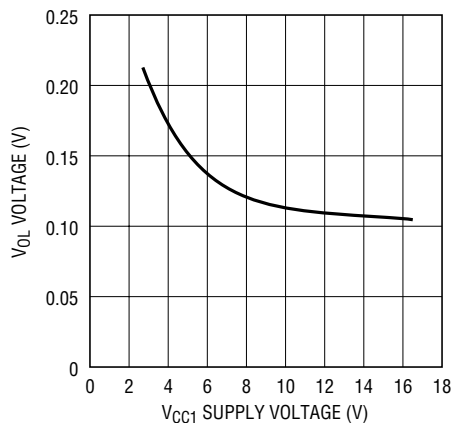
# TYPICAL PERFORMANCE CHARACTERISTICS

**TIMER Low Threshold vs  $V_{CC1}$  Supply Voltage**



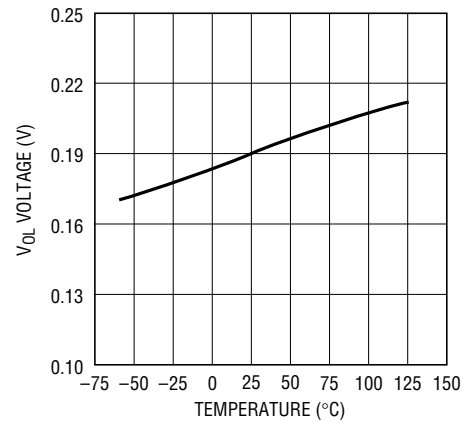
4230 G28

**$V_{OL}$  ( $\overline{\text{RESET}}n$ ,  $\overline{\text{FAULT}}$ ) vs  $V_{CC1}$  Supply Voltage**



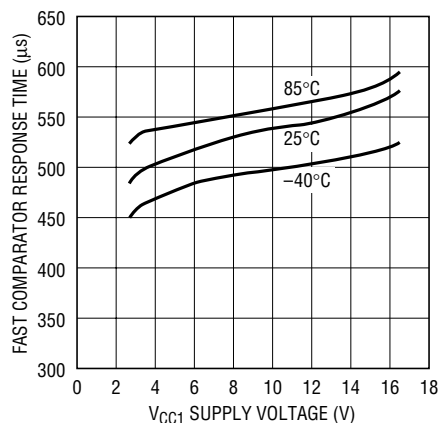
4230 G29

**$V_{OL}$  ( $\overline{\text{RESET}}n$ ,  $\overline{\text{FAULT}}$ ) vs Temperature**



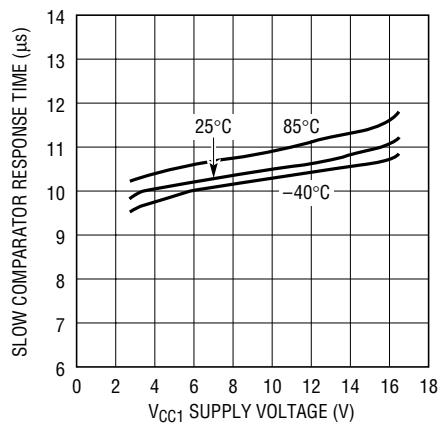
4230 G30

**Fast Comparator Response Time vs  $V_{CC1}$  Supply Voltage**



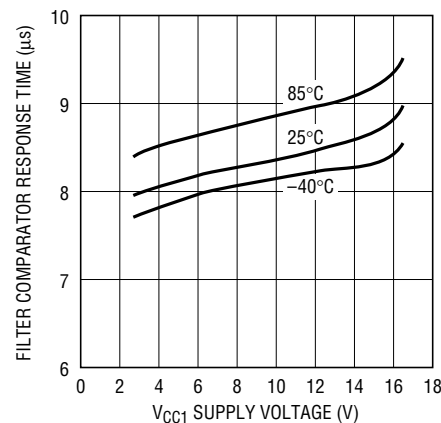
4230 G31

**Slow Comparator Response Time (FILTER Floating) vs  $V_{CC1}$  Supply Voltage**



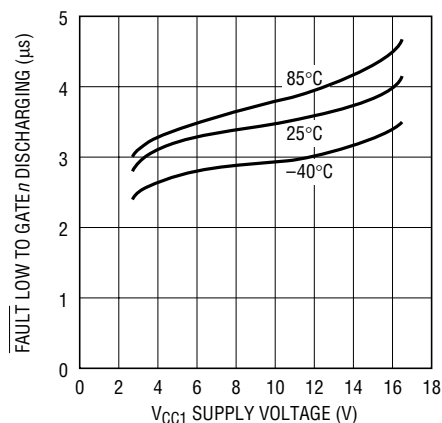
4230 G32

**FILTER Comparator Response Time vs  $V_{CC1}$  Supply Voltage**



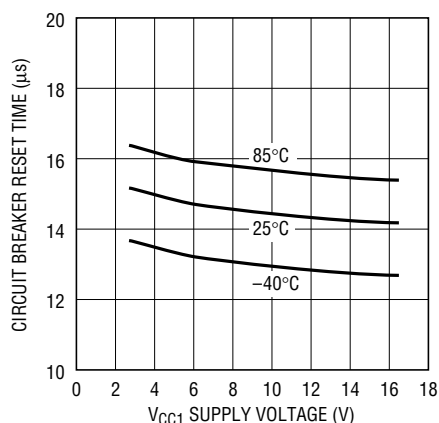
4230 G33

**$\overline{\text{FAULT}}$  Low to  $\text{GATE}n$  Discharging vs  $V_{CC1}$  Supply Voltage**



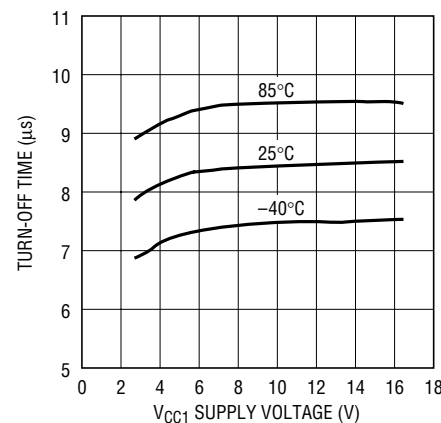
4230 G34

**Circuit Breaker Reset Time vs  $V_{CC1}$  Supply Voltage**



4230 G35

**Turn-Off Time vs  $V_{CC1}$  Supply Voltage**



4230 G36

4230f

## PIN FUNCTIONS

**FB3 (Pin 1):** The FB3 (Feedback) pin is an input to the FBCOMP3 comparator which monitors the  $V_{CC3}$  output supply voltage through an external resistor divider. If  $V_{FB3} < 1.234V$ , RESET 3 pin pulls low. An internal glitch filter at FBCOMP3's output prevents triggering a reset condition due to negative voltage transients. If  $V_{FB3} > 1.237V$ , RESET 3 pin goes high after exiting undervoltage lockout.

**RESET 3 (Pin 2):** An open-drain N-channel device whose source connects to GND (Pin 14). This pin pulls low if the voltage at FB3 (Pin 1) falls below the FB3 threshold (1.234V). This pin requires an external pull-up resistor to  $V_{OUT3}$ . If an undervoltage lockout condition occurs, RESET 3 pulls low independently of FB3 to prevent false glitches.

**GATE3 (Pin 3):** The output signal at this pin is the high side gate drive for Channel 3's external N-channel MOSFET pass transistor. An internal charge pump produces a 4.5V (minimum) to 18V (maximum) gate drive voltage for  $V_{CC1}$  supply voltages from 2.7V to 16.5V, respectively.

As shown in the Block Diagram for each channel, an internal charge pump supplies a 10 $\mu$ A gate current and sufficient gate voltage drive to the external MOSFET. The internal charge pump produces a minimum 4.5V gate drive for  $V_{CC1} < 4.75V$ . For  $V_{CC1} > 4.75V$ , the minimum gate voltage drive is 9V. For  $V_{CC1} \geq 12V$ , the minimum gate voltage drive is 7V which is set by an internal zener diode clamp connected between the GATE 3 pin and GND.

**SENSE 3 (Pin 4):** Circuit Breaker Sense Pin for Channel 3. With a sense resistor placed in the power path between  $V_{CC3}$  and SENSE 3, Channel 3's electronic circuit breaker trips if the voltage across the sense resistor ( $V_{CC3} - V_{SENSE3}$ ) exceeds the thresholds set internally for SLOW COMP3 and FAST COMP3, as shown in the Block Diagram. The threshold for SLOW COMP3 is  $V_{CB(SLOW)} = 50mV$ , and the electronic circuit breaker trips if the voltage across  $R_{SENSE3}$  exceeds 50mV for 10 $\mu$ s, or for the time delay programmed by  $C_{FILTER}$ . To adjust SLOW COMP3's delay, please refer to the section on Adjusting SLOW COMPn's Response Time.

Under transient conditions where large step current changes can and do occur over shorter periods of time, a

second (fast) comparator instead trips the electronic circuit breaker. The threshold for FAST COMP3 is set at  $V_{CB(FAST)} = 150mV$ , and the circuit breaker trips if the voltage across the  $R_{SENSE3}$  exceeds 150mV for more than 500ns. FAST COMP3's delay is fixed in the LTC4230 and cannot be adjusted. To disable Channel 3's electronic circuit breaker, connect the  $V_{CC3}$  and SENSE 3 pins together.

**$V_{CC3}$  (Pin 5):** Positive Supply Input for Channel 3.  $V_{CC3}$  operates from 1.7V to 15.5V ( $V_{CC3} \leq V_{CC1} - 1V$ ) and its supply current,  $I_{CC3}$ , is typically 65 $\mu$ A. The master UVLO circuit disables all three GATE $n$  outputs of the LTC4230 until the voltage at  $V_{CC3}$  exceeds 1.19V.

**$V_{CC1}$  (Pin 6):** This is the positive supply input to the LTC4230, the power supply input for Channel 1, and the power supply input for all three internal charge pumps. The LTC4230 operates from 2.7V to 16.5V, and the  $I_{CC1}$  supply current is typically 1.8mA. The master UVLO circuit disables all three GATE $n$  outputs of the LTC4230 if  $V_{CC1}$  is less than 2.35V. The internal charge pump outputs are enabled when  $V_{CC1} > 2.35V$ ,  $V_{CC2} > 2.15V$ , and  $V_{CC3} > 1.19V$ .

**SENSE 1 (Pin 7):** Circuit Breaker Sense Pin for Channel 1. With a sense resistor placed in the power path between  $V_{CC1}$  and SENSE 1, Channel 1's electronic circuit breaker trips if the voltage across the sense resistor ( $V_{CC1} - V_{SENSE1}$ ) exceeds the thresholds set internally for SLOW COMP1 and FAST COMP1, as shown in the Block Diagram. The threshold for SLOW COMP1 is  $V_{CB(SLOW)} = 50mV$ , and the electronic circuit breaker trips if the voltage across  $R_{SENSE1}$  exceeds 50mV for 10 $\mu$ s, or for the time delay programmed by  $C_{FILTER}$ . To adjust SLOW COMP1's delay, please refer to the section on Adjusting SLOW COMPn's Response Time.

Under transient conditions where large step current changes can and do occur over shorter periods of time, a second (fast) comparator instead trips the electronic circuit breaker. The threshold for FAST COMP1 is set at  $V_{CB(FAST)} = 150mV$ , and the circuit breaker trips if the voltage across the  $R_{SENSE1}$  exceeds 150mV for more than 500ns. FAST COMP1's delay is fixed in the LTC4230 and cannot be adjusted. To disable Channel 1's electronic circuit breaker, connect the  $V_{CC1}$  and SENSE 1 pins together.



## PIN FUNCTIONS

**GATE 1 (Pin 8):** The output signal at this pin is the high side gate drive for Channel 1's external N-channel FET pass transistor. An internal charge pump produces a 4.5V (minimum) to 18V (maximum) gate drive voltage for supplies in the range of  $2.7V \leq V_{CC1} \leq 16.5V$ , respectively.

As shown in the Block Diagram, each channel's internal charge pump is powered by  $V_{CC1}$  and supplies a 10 $\mu$ A gate current and sufficient gate voltage drive to the external FET. The internal charge pump produces a minimum 4.5V gate voltage drive for  $V_{CC1} < 4.75V$ . For  $V_{CC1} > 4.75V$ , the minimum gate voltage drive is 9V. For  $V_{CC1} \geq 12V$ , the minimum gate voltage drive is 7V which is set by an internal zener diode clamp connected between the GATE 1 pin and GND.

**RESET 1 (Pin 9):** An open-drain N-channel device whose source connects to GND (Pin 14). This pin pulls low if the voltage at FB1 (Pin 10) falls below the FB1 threshold (1.234V). During the start-up cycle, RESET 1 goes high impedance at the end of the second timing cycle after FB1 goes above the FB1 threshold. This pin requires an external pull-up resistor to  $V_{OUT1}$ . If an undervoltage lockout condition occurs, RESET 1 pulls low independently of FB1 to prevent false glitches.

**FB1 (Pin 10):** The FB1 (Feedback) pin is an input to the FB1COMP1 comparator which monitors the  $V_{CC1}$  output supply voltage through an external resistor divider. If  $V_{FB1} < 1.234V$ , RESET 1 pin pulls low. An internal glitch filter at FB1COMP1's output prevents triggering a reset condition due to negative voltage transients. If  $V_{FB1} > 1.237V$  after the second timing cycle, RESET 1 goes high.

**FILTER (Pin 11):** Overcurrent Fault Timing Pin and Over-voltage Fault Set Pin. With a capacitor connected from this pin to ground, the response time of all three SLOW COMP comparators can be adjusted. Note that the response time of the SLOW COMP comparators cannot be adjusted individually.

**TIMER (Pin 12):** A capacitor connected from this pin to GND sets the LTC4230's system timing. The LTC4230's initial and second start-up timing cycles and its discharge mode delay time are controlled by this capacitor.

**FAULT (Pin 13):** FAULT is a dual function (an input and an output) internal to the LTC4230. Connected to this pin are an analog comparator (COMP6) and an open-drain N-channel FET. During normal operation, if COMP6 is driven below 1.234V, all electronic circuit breakers trip and each GATE pin pulls low. Referring to the Block Diagram, FAULT incorporates an internal 2 $\mu$ A current source pull up. This allows the LTC4230 to begin a second timing cycle ( $V_{FAULT} > 1.284V$ ) and start up properly. This also allows the use of the FAULT pin as a status output. Under normal operating conditions, the FAULT output is a logic high. Two conditions cause an active low on FAULT: 1) the LTC4230's electronic circuit breakers trip because of an output short circuit ( $V_{OUTn} = 0V$ ) or because of a fast output overcurrent transient (FAST COMP $_n$  trips its circuit breaker); or 2)  $V_{FILTER} > 1.26V$ . The FAULT output is driven to logic low and is latched logic low until the ON pin is driven to logic low for 30 $\mu$ s (the  $t_{RESET}$  duration).

**GND (Pin 14):** Device Ground Connection. Connect this pin to the system's analog ground plane.

**ON (Pin 15):** An active high signal used to enable or disable LTC4230 operation. As shown in the LTC4230 Block Diagram, COMP1's threshold is set at 1.234V and its hysteresis is set at 80mV. If a logic high signal is applied to the ON pin ( $V_{ON} > 1.314V$ ), the first timing cycle begins if an overvoltage condition does not exist on any of the GATE $_n$  pins (Pins 3, 8, and 18). If a logic low signal is applied to the ON pin ( $V_{ON} < 1.234V$ ), each GATE $_n$  pin is pulled low by an internal, dedicated 200 $\mu$ A current sink. The ON pin can also be used to reset all three electronic circuit breakers. If the ON pin is cycled low for more than 1  $t_{RESETn(MAX)}$  period and then high following a circuit breaker trip, all internal circuit breakers are reset and the LTC4230 begins a new start-up cycle.

**V<sub>CC2</sub> (Pin 16):** Positive Supply Input for Channel 2.  $V_{CC2}$  operates from 2.375V to 16.5V and its supply current,  $I_{CC2}$ , is typically 75 $\mu$ A. The master UVLO circuit disables all three GATE $_n$  outputs of the LTC4230 until the voltage at  $V_{CC2}$  exceeds 2.15V.



## PIN FUNCTIONS

**SENSE 2 (Pin 17):** Circuit Breaker Sense Pin for Channel 2. With a sense resistor placed in the power path between  $V_{CC2}$  and SENSE 2, Channel 2's electronic circuit breaker trips if the voltage across the sense resistor ( $V_{CC2} - V_{SENSE2}$ ) exceeds the thresholds set internally for SLOW COMP2 and FAST COMP2, as shown in the Block Diagram. The threshold for SLOW COMP2 is  $V_{CB(SLOW)} = 50\text{mV}$  and the electronic circuit breaker trips if the voltage across  $R_{SENSE2}$  exceeds 50mV for 10 $\mu\text{s}$ , or for the time delay programmed by  $C_{FILTER}$ . To adjust SLOW COMP2's delay, please refer to the section on Adjusting SLOW COMP2's Response Time.

Under transient conditions where large step current changes can and do occur over shorter periods of time, a second (fast) comparator instead trips the electronic circuit breaker. The threshold for FAST COMP2 is set at  $V_{CB(FAST)} = 150\text{mV}$ , and the circuit breaker trips if the voltage across the  $R_{SENSE2}$  exceeds 150mV for more than 500ns. FAST COMP2's delay is fixed in the LTC4230 and cannot be adjusted. To disable Channel 2's electronic circuit breaker, connect the  $V_{CC2}$  and SENSE 2 pins together.

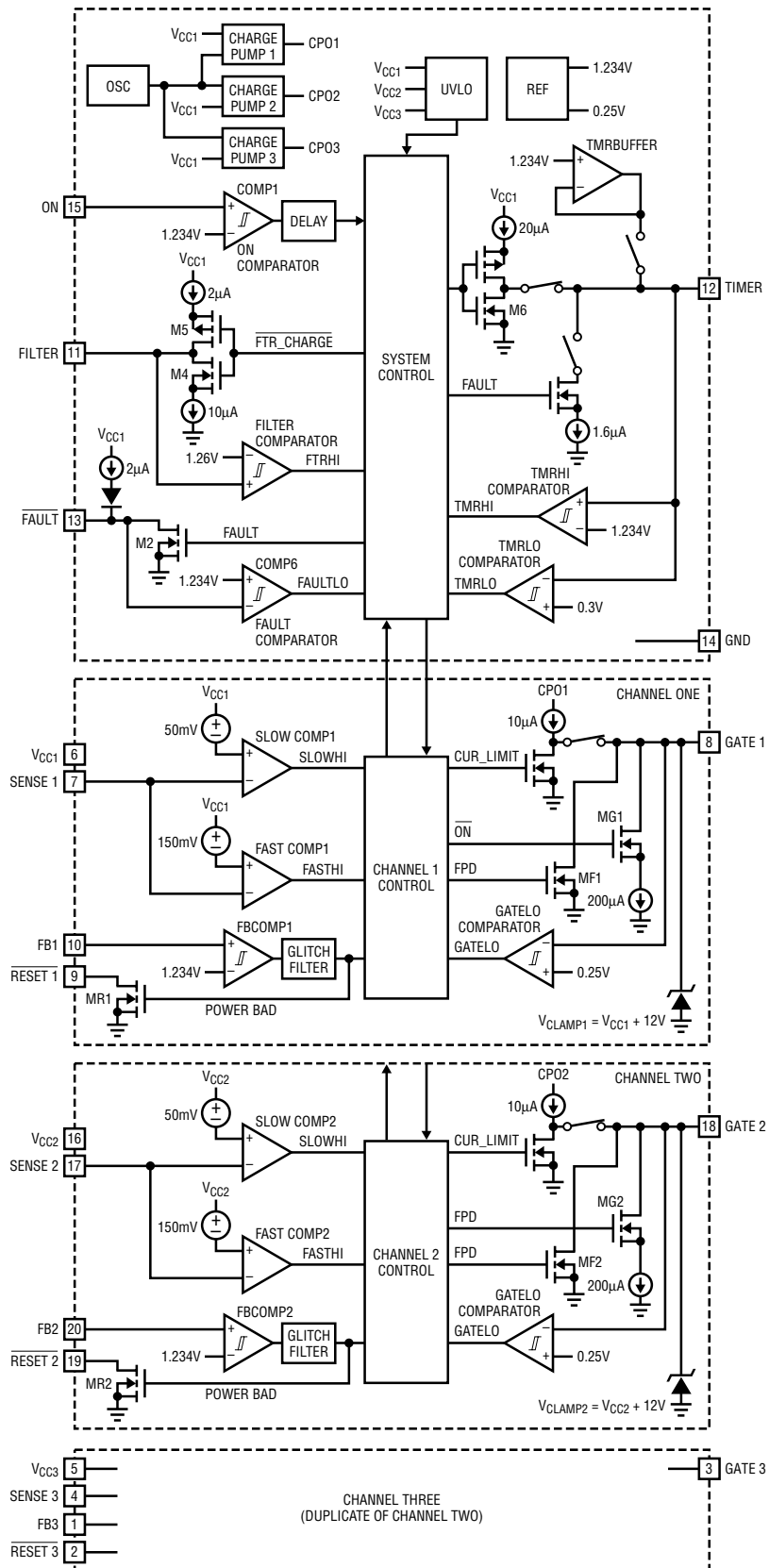
**GATE 2 (Pin 18):** The output signal at this pin is the high side gate drive for Channel 2's external N-channel FET pass transistor. An internal charge pump produces a 4.5V (minimum) to 18V (maximum) gate drive voltage for  $V_{CC1}$  supply voltages from 2.7V to 16.5V, respectively.

As shown in the Block Diagram for each channel, an internal charge pump supplies a 10 $\mu\text{A}$  gate current and sufficient gate voltage drive to the external FET. The internal charge pump produces a minimum 4.5V gate drive for  $V_{CC1} < 4.75\text{V}$ . For  $V_{CC1} > 4.75\text{V}$ , the minimum gate voltage drive is 9V. For  $V_{CC1} \geq 12\text{V}$ , the minimum gate voltage drive is 7V which is set by an internal zener diode clamp connected between the GATE 2 pin and GND.

**RESET 2 (Pin 19):** An open-drain N-channel device whose source connects to GND (Pin 14). This pin pulls low if the voltage at FB2 (Pin 20) falls below the FB2 threshold (1.234V). This pin requires an external pull-up resistor to  $V_{OUT2}$ . If an undervoltage lockout condition occurs, the RESET 2 pin pulls low independently of FB2 to prevent false glitches.

**FB2 (Pin 20):** The FB2 (Feedback) pin is an input to the FBCOMP2 comparator which monitors the  $V_{CC2}$  output supply voltage through an external resistor divider. If  $V_{FB2} < 1.234\text{V}$ , RESET 2 pulls low. An internal glitch filter at FBCOMP3's output prevents triggering a reset condition due to negative voltage transients. If  $V_{FB2} > 1.237\text{V}$ , RESET 2 pin goes high after exiting undervoltage lockout.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### HOT CIRCUIT INSERTION

When circuit boards are inserted into or removed from live backplanes, the supply bypass capacitors can draw huge transient currents from the backplane power bus as they charge. The transient currents can cause permanent damage to the connector pins as well as cause glitches on the system supply, causing other boards in the system to reset.

The LTC4230 is designed to turn a printed circuit board's supply voltages on and off in a controlled manner, allowing the circuit board to be safely inserted or removed from a live backplane. The device provides a system reset signal to indicate when board supply voltage drops below a predetermined level, as well as a dual function fault monitor.

### OUTPUT VOLTAGE MONITOR

The LTC4230 uses a 1.234V bandgap reference, precision voltage comparators and external resistor dividers to monitor the output supply voltages as shown in Figure 1.

The operation of the supply monitor in normal mode is illustrated in Figure 2. RESET 1 pulls low during an undervoltage lockout condition. It remains low until the end of the soft-start cycle (second timing cycle). FB1 then assumes control of RESET 1 status. RESET 2 and RESET 3 also pull low during undervoltage lockout. However, FB2 controls RESET 2 and FB3 controls RESET 3 status immediately after clearing UVLO (Figure 2, Time Points 5 and 6).

If the voltage at FB $n$  drops below its reset threshold (1.234V), the FBCOMP comparator output pulls high. After passing through a glitch filter, RESET $n$  changes state. If the voltage at FB $n$  increases above its reset threshold, the FBCOMP comparator output changes state and RESET $n$  pulls high.

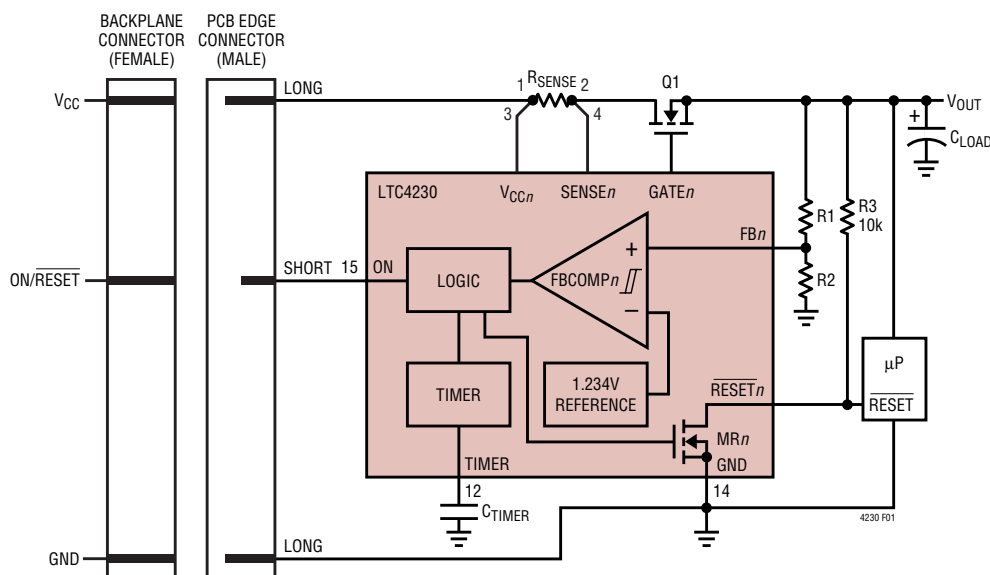
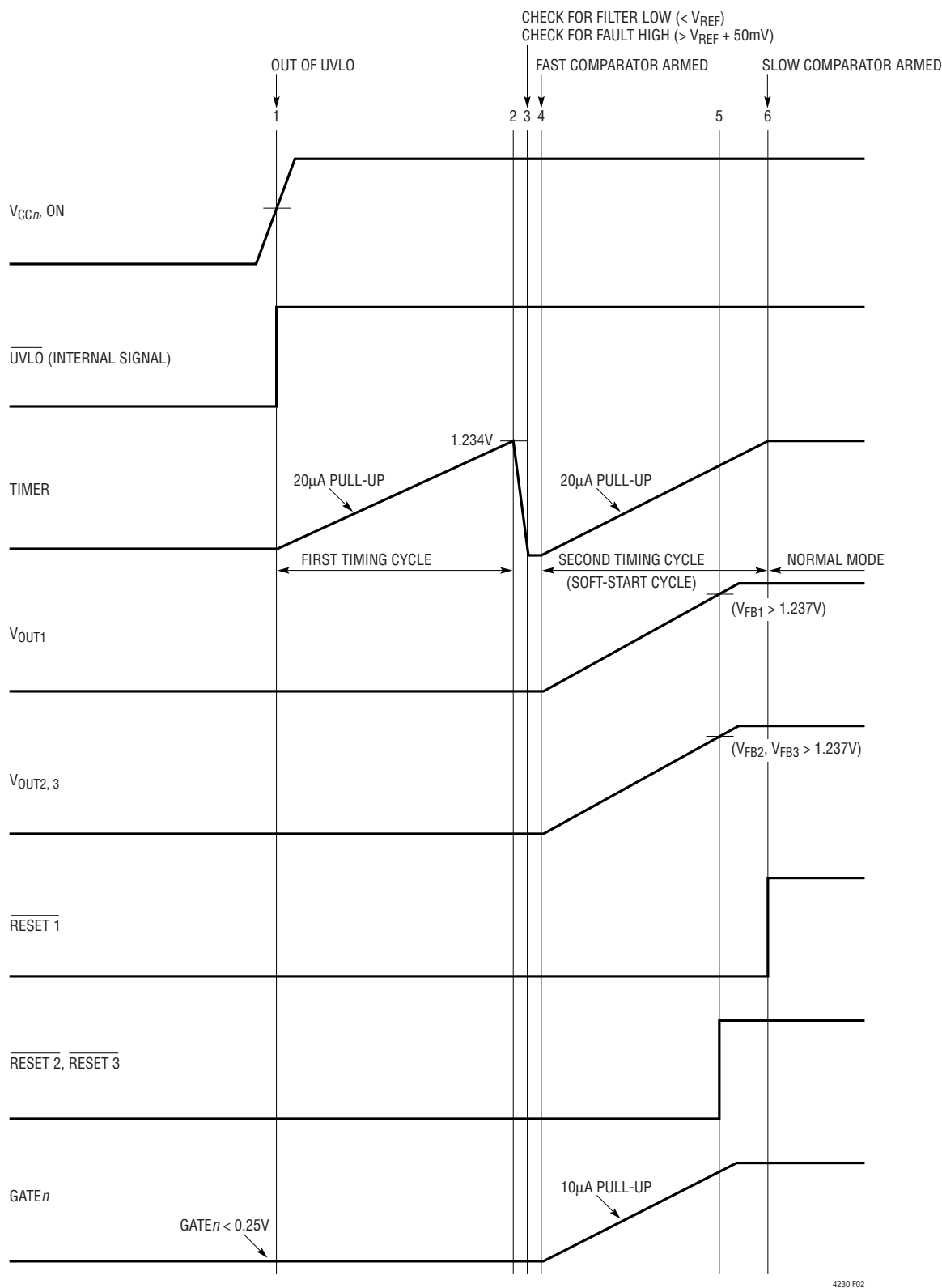


Figure 1. Supply Voltage Monitor Block Diagram

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Figure 2. Supply Monitor Waveforms in Normal Mode

4230f

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### INTERNAL UNDERVOLTAGE LOCKOUT (UVLO)

The LTC4230's power-on reset circuit initializes the start-up condition and ensures the chip is in the proper state if the input supply voltages are too low. If any one of the input supply voltages falls below its corresponding UVLO lower threshold (e.g.,  $V_{CC1} < 2.25V$ ,  $V_{CC2} < 2.105V$  or  $V_{CC3} < 1.155V$ ), the LTC4230 enters UVLO mode and all three  $GATE_n$  pins are each pulled low by internal  $200\mu A$  current sinks. Since the LTC4230's UVLO circuits have hysteresis, the device restarts when all three supply voltages rise above their corresponding UVLO high threshold (e.g.,  $V_{CC1} > 2.35V$ ,  $V_{CC2} > 2.15V$  and  $V_{CC3} > 1.19V$ ) and the ON pin goes high.

In addition, users can utilize the ON comparator (COMP1) or the  $\overline{FAULT}$  comparator (COMP6) to effectively program a higher undervoltage lockout level. If the  $\overline{FAULT}$  comparator is used for this purpose, the system will wait for the input voltage to increase above the level set by the user before starting the second timing cycle. Also, if the input voltage drops below the set level in normal operating mode, the user must cycle the ON pin or  $V_{CC1}$  to restart the system.

### GLITCH FILTER FOR $\overline{RESET}$

Each LTC4230 feedback comparator has a glitch filter to prevent  $\overline{RESET}$  from generating a system reset if there are transients on the  $FB_n$  pin. The relationship between

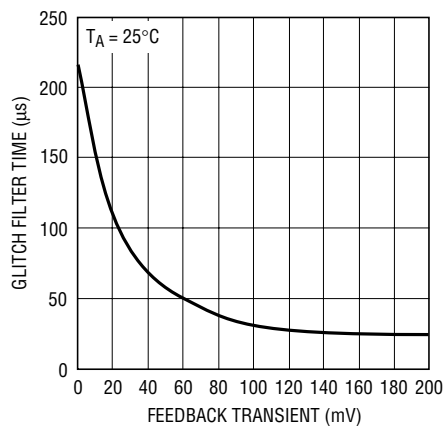


Figure 3. FB Comparator Glitch Filter Time vs Feedback Transient Voltage

glitch filter time and the feedback transient voltage is shown in Figure 3.

### SYSTEM TIMING

System timing for the LTC4230 is generated in the equivalent circuit shown in Figure 4. If the LTC4230's internal timing circuit is off, an internal N-channel FET connects the TIMER pin to GND. If the timing circuit is enabled, an internal  $20\mu A$  current source is then connected to the TIMER pin to charge  $C_{TIMER}$  at a rate given by Equation 1:

$$C_{TIMER} \text{ Charge - Up Rate} = \frac{20\mu A}{C_{TIMER}} \quad (1)$$

When the TIMER pin voltage reaches TMRHI's threshold of  $1.234V$ , the TIMER pin is reset to GND. Equation 2 gives an expression for the timer period:

$$t_{TIMER} = 1.234V \cdot \frac{C_{TIMER}}{20\mu A} \quad (2)$$

As a design aid, the LTC4230's timer period as a function of the  $C_{TIMER}$  using standard values from  $0.1\mu F$  to  $10\mu F$  is shown in Table 1.

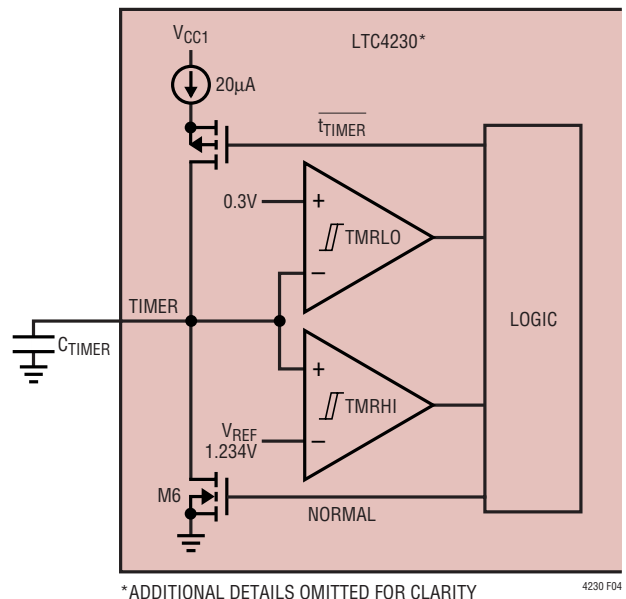


Figure 4. LTC4230 System Timing Block Diagram

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Table 1.  $t_{\text{TIMER}}$  vs  $C_{\text{TIMER}}$

$C_{\text{TIMER}}$	$t_{\text{TIMER}}$
0.1 $\mu\text{F}$	6.2ms
0.22 $\mu\text{F}$	13.6ms
0.33 $\mu\text{F}$	20.4ms
0.47 $\mu\text{F}$	29ms
0.68 $\mu\text{F}$	42ms
0.82 $\mu\text{F}$	50.6ms
1 $\mu\text{F}$	61.7ms
2.2 $\mu\text{F}$	136ms
3.3 $\mu\text{F}$	204ms
4.7 $\mu\text{F}$	290ms
6.8 $\mu\text{F}$	420ms
8.2 $\mu\text{F}$	506ms
10 $\mu\text{F}$	617ms

Ensuring a proper start-up sequence is also dependent on selecting the most appropriate value for  $C_{\text{TIMER}}$  for the application. Long timing periods affect overall system start-up times. A timing period set too short and the system may never start up. A good starting point is to set  $C_{\text{TIMER}} = 1\mu\text{F}$  and then adjust its value accordingly for the application.

## OPERATING SEQUENCE

### Power-Up, Start-Up Check and Plug-In Timing Cycle

The sequence of operations for the LTC4230 is illustrated in the timing diagram of Figure 5. When a PC board is first inserted into a live backplane, the LTC4230 first performs

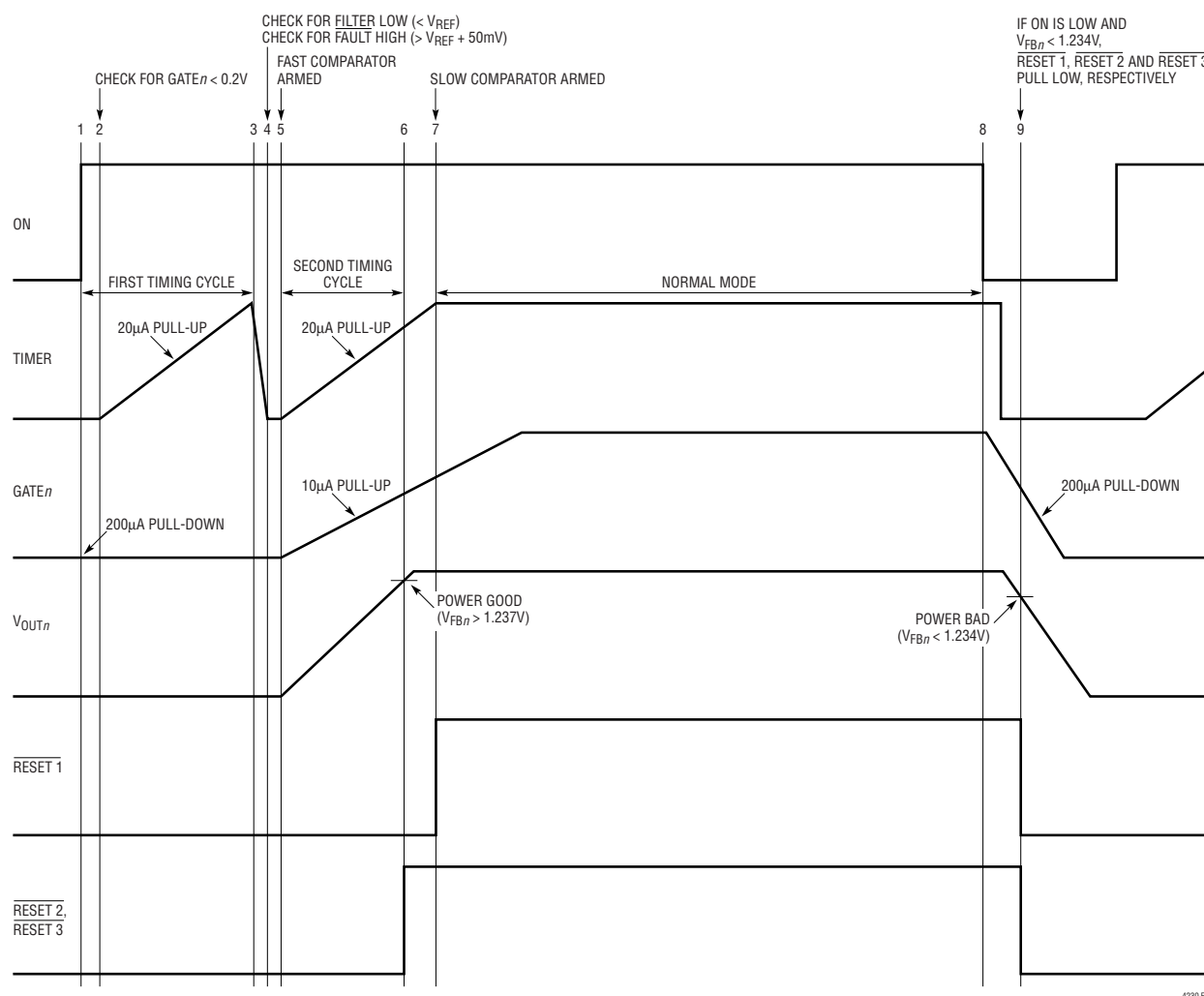


Figure 5. Normal Power-Up Sequence

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## APPLICATIONS INFORMATION

a start-up check to make sure the supply voltage is above its 2.3V UVLO threshold (see Time Point 1). If the input supply voltage is valid, the gate of the external pass transistor is pulled to ground by the internal 200μA current source connected at the GATE<sub>n</sub> pin. The TIMER pin is held low by an internal N-channel pull-down transistor (see M6, LTC4230 Block Diagram) and the FILTER pin voltage is pulled to ground by an internal 10μA current source.

Once V<sub>CCn</sub> and ON (the ON pin is >1.314V) are valid, the LTC4230 checks to make sure that GATE<sub>n</sub> is OFF (V<sub>GATE<sub>n</sub></sub> < 0.25V) at Time Point 2. An internal timing circuit is enabled and the TIMER pin voltage ramps up at the rate described by Equation 1. At Time Point 3 (the timing period programmed by C<sub>TIMER</sub>), the TIMER pin voltage equals V<sub>TMR</sub> (1.234V). Next, the TIMER pin voltage ramps down to Time Point 4 where the LTC4230 performs two checks: (1) FILTER pin voltage is low (V<sub>FILTER</sub> < 1.19V) and (2) FAULT pin voltage is high (V<sub>FAULT</sub> > 1.284V). If both conditions are met, the LTC4230 begins a second timing (soft-start) cycle.

### Second Timing (Soft-Start) Cycle

At the beginning of the second timing cycle (Time Point 5), the LTC4230's FAST COMP<sub>n</sub> is armed and an internal 10μA current source working with an internal charge pump provides the gate drive to the external pass transistor. An expression for the GATE<sub>n</sub> voltage slew rate is given by Equation 3:

$$V_{GATE\,n} \text{ Slew Rate}, \frac{dV_{GATE\,n}}{dt} = \frac{10\mu A}{C_{GATE\,n}} \quad (3)$$

where C<sub>GATE<sub>n</sub></sub> = Power MOSFET gate input capacitance (C<sub>ISS</sub>) for Channel *n*.

For example, a Si4410DY (a 30V N-channel power MOSFET) exhibits an approximate C<sub>GATE</sub> of 3300pF at V<sub>GS</sub> = 10V. The LTC4230's GATE<sub>n</sub> voltage rate-of-change (slew rate) for this example would be:

$$V_{GATE\,n} \text{ Slew Rate}, \frac{dV_{GATE\,n}}{dt} = \frac{10\mu A}{3300pF} = 3.03 \frac{V}{ms}$$

The inrush current being delivered to the load while the GATE<sub>n</sub> is ramping is dependent on C<sub>LOAD<sub>n</sub></sub> and C<sub>GATE<sub>n</sub></sub>.

Equation 4 gives an expression for the inrush current during the second timing cycle:

$$I_{INRUSH} = \frac{dV_{GATE\,n}}{dt} \cdot C_{LOAD\,n} = 10\mu A \cdot \frac{C_{LOAD\,n}}{C_{GATE\,n}} \quad (4)$$

For example, if C<sub>GATE<sub>n</sub></sub> = 3300pF and C<sub>LOAD<sub>n</sub></sub> = 2000μF, the inrush current charging C<sub>LOAD<sub>n</sub></sub> is:

$$I_{INRUSH} = 10\mu A \cdot \frac{2000\mu F}{0.0033\mu F} = 6.06A \quad (5)$$

At Time Point 7, the output voltage trips FBCOMP<sub>n</sub>'s threshold, signaling an output voltage "power good" condition. RESET 2 and RESET 3 pull high. At Time Point 8, RESET 1 asserts high, SLOW COMP is armed and the LTC4230 enters a fault monitor mode.

### SOFT-START WITH CURRENT LIMITING

During the second timing cycle, the inrush current is described by Equation 4. Note that there is a one-to-one correspondence in the inrush current to C<sub>LOAD<sub>n</sub></sub>. If the inrush current is large enough to cause a voltage drop greater than 50mV across the sense resistor, an internal servo loop controls the operation of the 10μA current source at the GATE<sub>n</sub> pin to regulate the load current to:

$$I_{LIMIT(SOFTSTART)\,n} = \frac{50mV}{R_{SENSE\,n}} \quad (6)$$

For example, the inrush current is limited to 5A when R<sub>SENSE<sub>n</sub></sub> = 0.01Ω.

In this fashion, the inrush current is controlled and C<sub>LOAD<sub>n</sub></sub> is charged up slowly during the soft-start cycle.

The timing diagram in Figure 6 illustrates the operation of the LTC4230 in a normal power-up sequence with limited inrush current as described by Equation 6. At Time Point 5, the GATE pin voltage begins to ramp indicating that the power MOSFET is beginning to charge C<sub>LOAD<sub>n</sub></sub>. At Time Point 5, the inrush current causes a 50mV voltage drop across R<sub>SENSE<sub>n</sub></sub> and an internal servo loop engages, limiting the inrush current to a fixed level. At Time Point 6, the GATE<sub>n</sub> pin voltage continues to ramp as C<sub>LOAD<sub>n</sub></sub> charges until V<sub>OUT<sub>n</sub></sub> reaches its final value. The charging current

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reduces, and the internal servo loop disengages. At the end of the soft-start cycle (Time Point 8), all  $\overline{\text{RESET}}_n$  are high and all SLOW COMP $_n$  are armed.

### Power-Off Cycle

As shown at Time Point 9, an external hard reset is initiated by pulling the ON pin low ( $V_{\text{ON}} < 1.234\text{V}$ ). All GATE $_n$  pin voltages are ramped to ground by the internal  $200\mu\text{A}$  current sources, discharging  $C_{\text{GATE}_n}$  and turning off the pass transistors. As  $C_{\text{LOAD}_n}$  discharges, the output voltage crosses FBCOMP $_n$ 's threshold, signaling a "power bad" condition at Time Point 10.  $\overline{\text{RESET}}_n$  then asserts low.

### FREQUENCY COMPENSATION AT SOFT-START

If the external gate input capacitance ( $C_{\text{ISS}}$ ) is greater than  $600\text{pF}$ , no external gate capacitor is required at GATE $_n$  to stabilize the internal current-limiting loop during soft-start. Otherwise, connect an external gate capacitor between the GATE $_n$  and GND pins to increase the total gate capacitance above  $600\text{pF}$ . The servo loop that controls the external MOSFET during current limiting has a unity-gain frequency of about  $105\text{kHz}$  and phase margin of  $80^\circ$  for external MOSFET gate input capacitances to  $2.5\text{nF}$ .

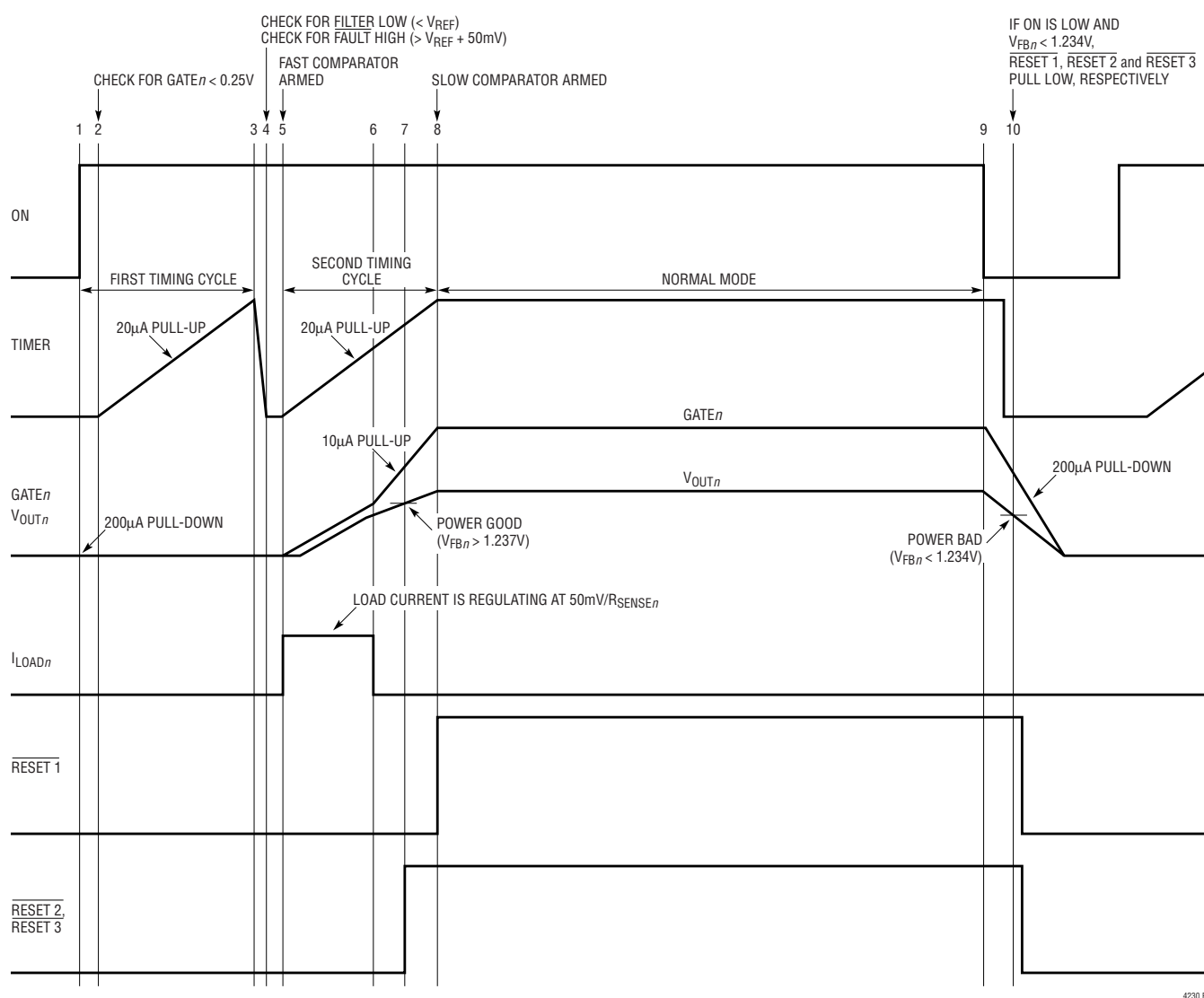


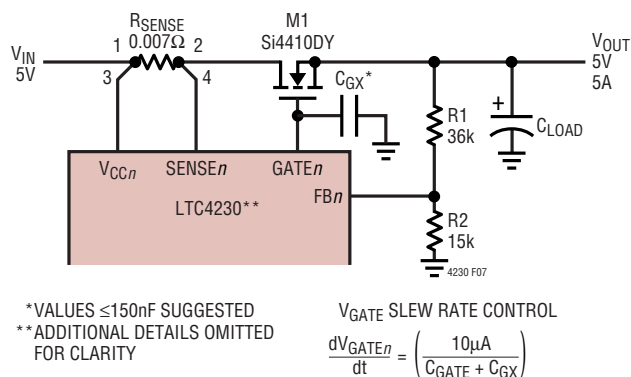
Figure 6. Normal Power-Up Sequence (with Current Limiting in Second Timing Cycle)

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## APPLICATIONS INFORMATION

### USING AN EXTERNAL GATE CAPACITOR

The LTC4230 automatically limits the inrush current in one of two ways: by controlling the GATE<sub>n</sub> pin voltage slew rate or by actively limiting the inrush current. The LTC4230 uses GATE<sub>n</sub> voltage slew rate limiting when C<sub>LOAD<sub>n</sub></sub> is small and/or the inrush current limit is set high. If GATE<sub>n</sub> voltage slew rate control is preferred with large C<sub>LOAD<sub>n</sub></sub>, an external capacitor (C<sub>GX</sub>) can be used from GATE<sub>n</sub> to ground, as shown in Figure 7. According to Equation 3, adding C<sub>GX</sub> slows the GATE<sub>n</sub> voltage slew rate at the expense of slower system turn-on and turn-off time. Should this technique be used, values for C<sub>GX</sub> less than 150nF are recommended.



**Figure 7. Using an External Capacitor at GATE for GATE Voltage Slew Rate Control and Large C<sub>LOAD</sub>**

An external gate capacitor may also be useful to decrease or eliminate current spikes through the MOSFET when power is first applied. At power-up, the instantaneous input voltage step attempts to pull the MOSFET gate up through the MOSFET's drain-to-gate capacitance. If the MOSFET's C<sub>ISS</sub> is small, the gate can be pulled up high enough to turn on the MOSFET, thereby allowing a current spike to the output. This event occurs during the time that the LTC4230 is coming out of UVLO and getting its intelligence to hold the GATE pin low. An external capacitor attenuates the voltage to which the GATE is pulled up and eliminates the current spike. The value required is dependent on the MOSFET capacitance specifications. In typical applications, this capacitor is not required.

### ELECTRONIC CIRCUIT BREAKER

The LTC4230 features an electronic circuit breaker function. It disconnects loads from power supplies when shorts or excessive load current conditions occur on any of the supplies and generates a FAULT signal. If a circuit breaker trips, its GATE<sub>n</sub> pin is immediately pulled to ground, the external N-channel MOSFET is quickly turned OFF and FAULT is latched low.

The circuit breaker trips whenever the voltage across the sense resistor exceeds two different levels, each level set by the LTC4230's SLOW COMP<sub>n</sub> and FAST COMP<sub>n</sub> (see Block Diagram). The SLOW COMP<sub>n</sub> trips the circuit breaker if the voltage across the SENSE<sub>n</sub> resistor (V<sub>CCn</sub> – V<sub>SENSEn</sub> = V<sub>CB</sub>) is greater than 50mV for 10μs. There may be applications where this comparator's response time is not long enough, for example, because of excessive supply voltage noise. To adjust the response time of the SLOW COMP<sub>n</sub>, a capacitor is used at the LTC4230's FILTER pin (see section on Adjusting SLOW COMP<sub>n</sub>'s Response Time). The FAST COMP<sub>n</sub> trips the circuit breaker to protect against fast load overcurrents if the transient voltage across the sense resistor is greater than 150mV for 500ns. The response time of the LTC4230's FAST COMP<sub>n</sub> is fixed.

The timing diagram of Figure 6 illustrates when the LTC4230's electronic circuit breaker is armed. After the first timing cycle, the LTC4230's FAST COMP<sub>n</sub> is armed at Time Point 5. Arming FAST COMP<sub>n</sub> at Time Point 5 ensures that the system is protected against a short-circuit condition during the second timing cycle after C<sub>LOAD<sub>n</sub></sub> has been fully charged. At Time Point 8, SLOW COMP<sub>n</sub> is armed when the internal control loop is disengaged.

The timing diagrams in Figures 8 and 9 illustrate the operation of the LTC4230 when the load current conditions exceed the thresholds of the FAST COMP<sub>n</sub> (V<sub>CB(FAST)</sub> > 150mV) and SLOW COMP<sub>n</sub> (V<sub>CB(SLOW)</sub> > 50mV), respectively.

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### RESETTING THE ELECTRONIC CIRCUIT BREAKER

Once the LTC4230's circuit breaker is tripped,  $\overline{\text{FAULT}}$  is asserted low and the  $\text{GATE}_n$  pin is pulled to ground. The LTC4230 remains latched OFF in this fault state until the external fault is cleared. To clear the internal fault detect

circuitry and to restart the LTC4230, its ON pin must be driven low ( $V_{\text{ON}} < 1.234\text{V}$ ) for at least  $30\mu\text{s}$ , after which time  $\overline{\text{FAULT}}$  goes high. Toggling the ON pin from low to high ( $V_{\text{ON}} > 1.314\text{V}$ ) initiates a restart sequence in the LTC4230. The timing diagram in Figure 10 illustrates a

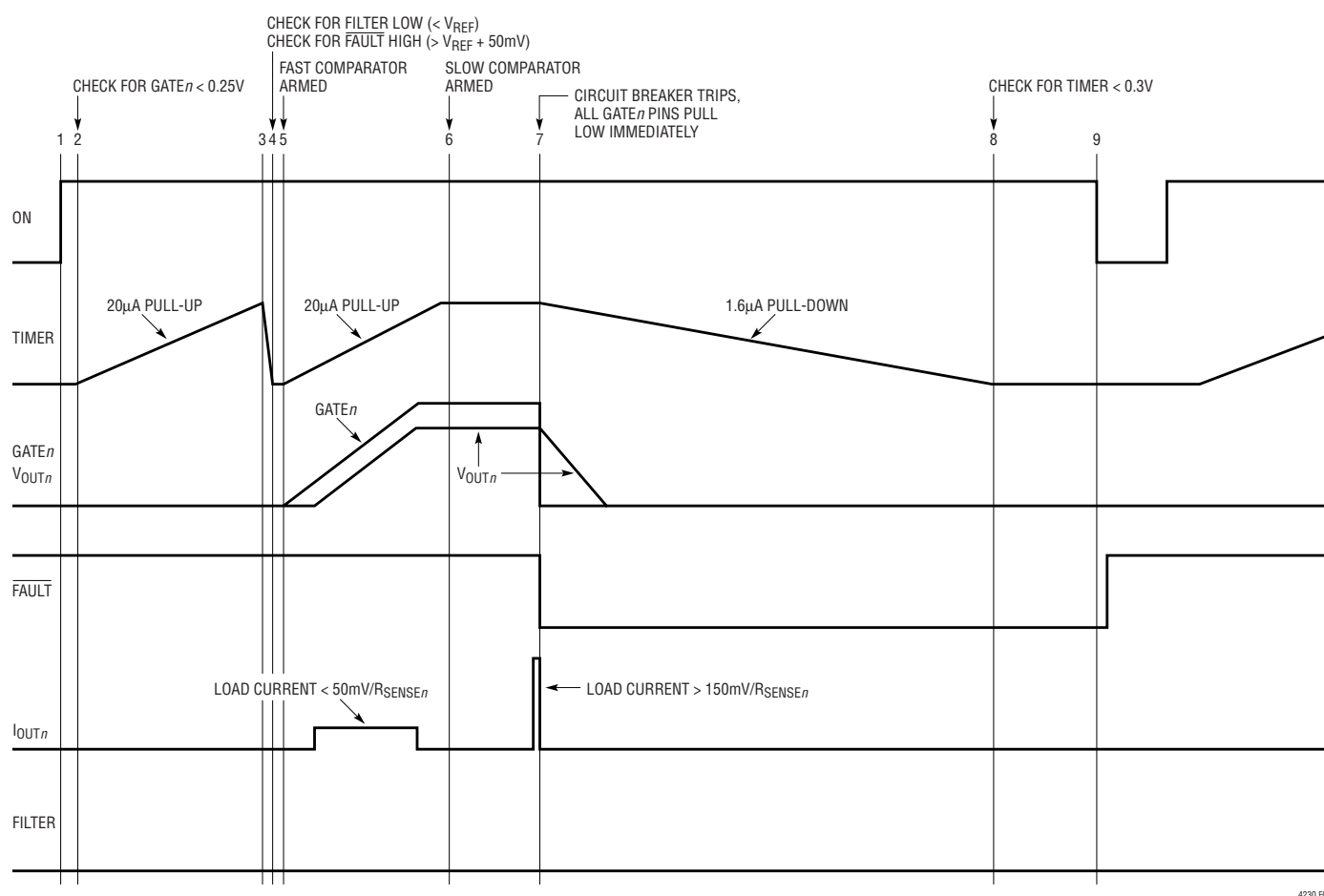


Figure 8. Output Short Circuit Causes Fast Comparator to Trip the Circuit Breaker

4230 F08

APPLICATIONS INFORMATION

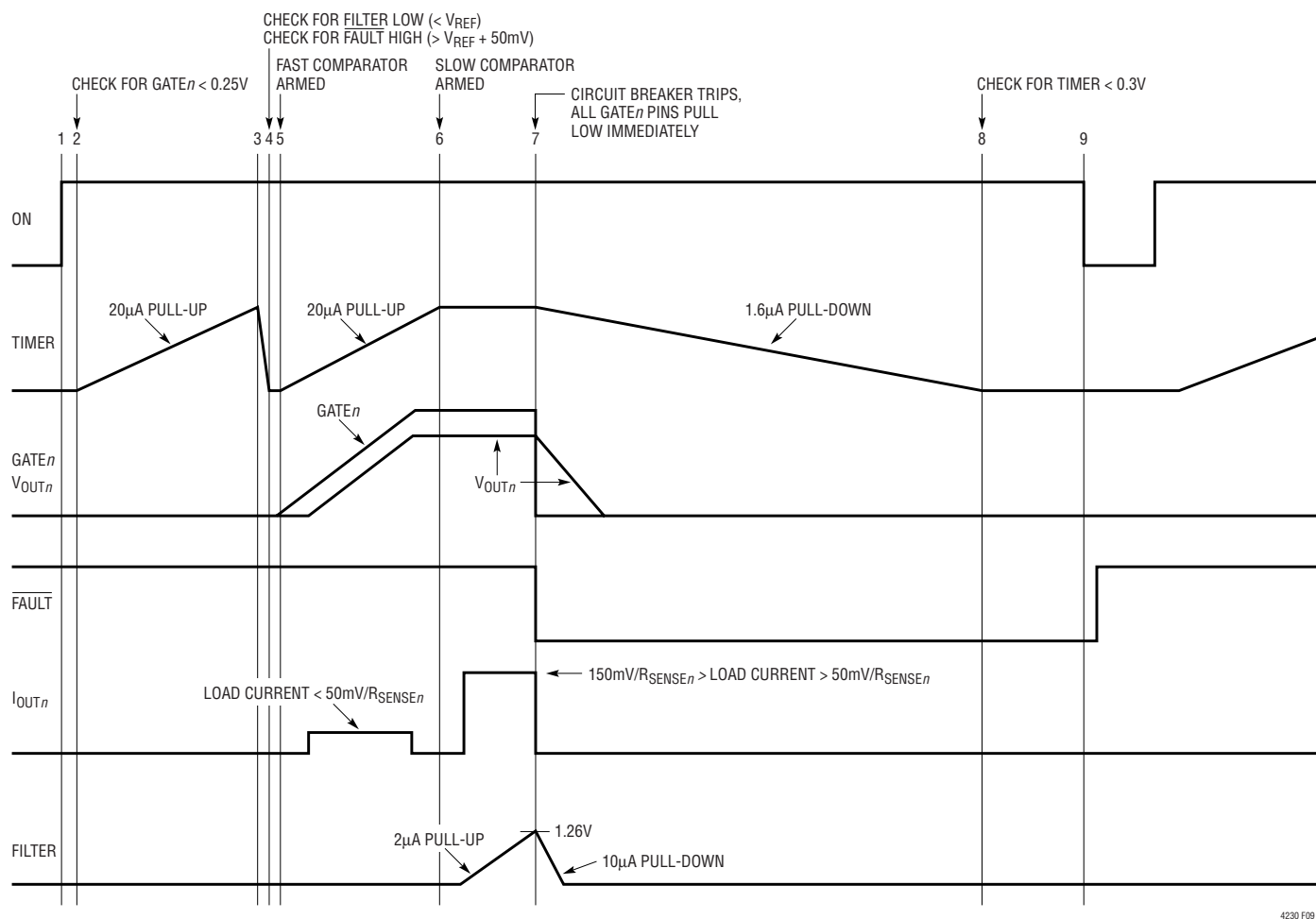


Figure 9. Output Short-Circuit Causes Slow Comparator to Trip Circuit Breaker

## APPLICATIONS INFORMATION

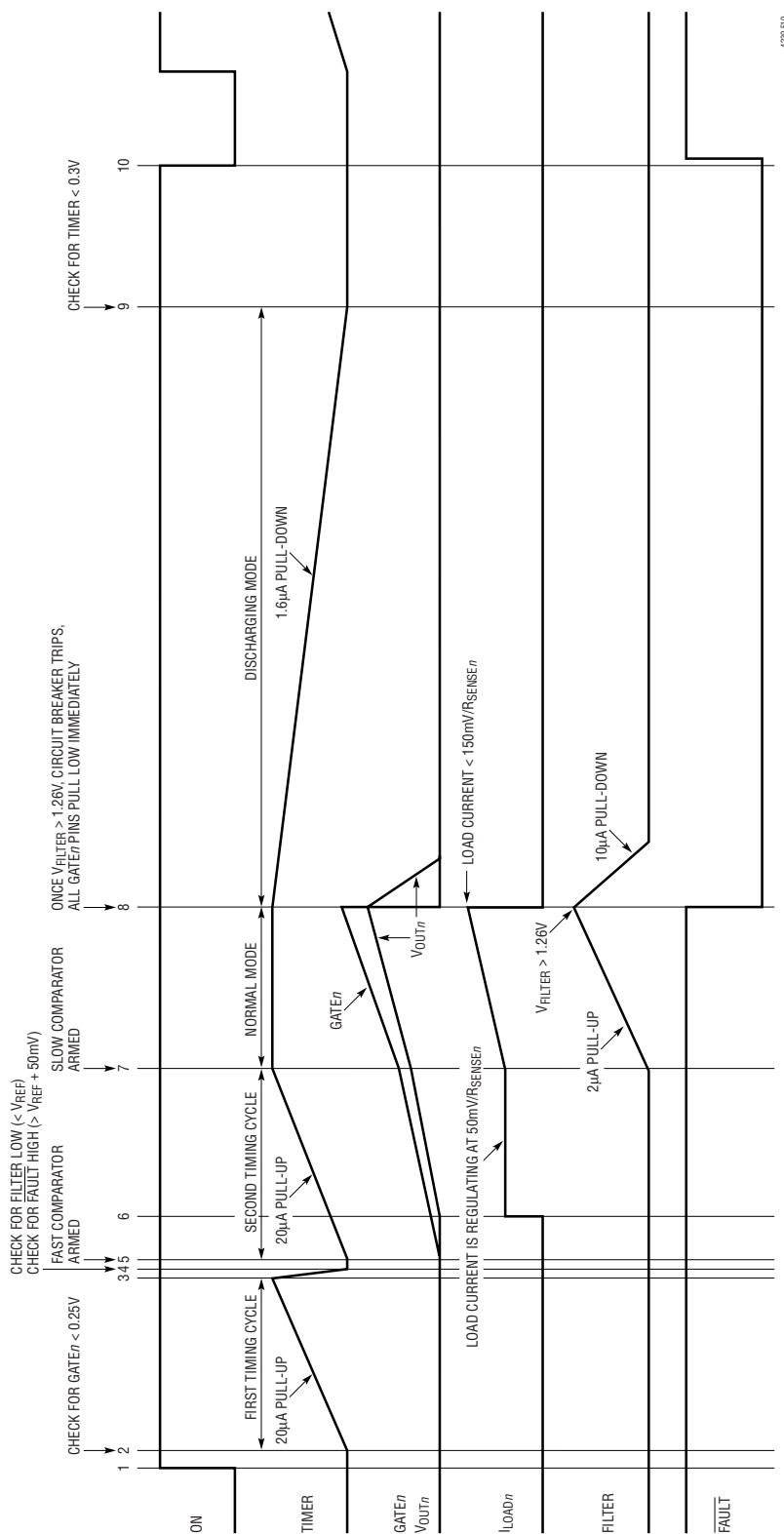


Figure 10. Power-Up into Dead Short in Overcurrent Condition

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start-up sequence where the LTC4230 is powered up into a load overcurrent condition. Note that the circuit breaker trips at Time Point 8 and is reset at Time Point 10.

### ADJUSTING SLOW COMP<sub>n</sub>'S RESPONSE TIME

The response time of SLOW COMP<sub>n</sub> is adjusted using a capacitor connected from the LTC4230's FILTER pin to ground. If this pin is left unused, SLOW COMP<sub>n</sub>'s delay defaults to 10μs. During normal operation, the FILTER output pin is held low as an internal 10μA pull-down current source is connected to this pin by transistor M4. This pull-down current source is turned off when an overcurrent load condition is detected by SLOW COMP<sub>n</sub>. During an overcurrent condition, the internal 2μA pull-up current source is connected to the FILTER pin by transistor M5, thereby charging C<sub>FILTER</sub>. As the charge on the capacitor accumulates, the voltage across C<sub>FILTER</sub> increases. Once the FILTER pin voltage increases to 1.26V, the electronic circuit breaker trips and the LTC4230's GATE<sub>n</sub> pins are switched quickly to ground by transistor MF<sub>n</sub> (refer to the Block Diagram). After the circuit breaker is tripped, M5 is turned off, M4 is turned on and the 10μA pull-down current then holds the FILTER pin voltage low.

SLOW COMP<sub>n</sub>'s response time from an overcurrent fault condition to when the circuit breaker trips (GATE<sub>n</sub> OFF) is given by Equation 7:

$$t_{\text{SLOWCOMP}_n} = 1.26V \cdot \frac{C_{\text{FILTER}}}{2\mu A} + 10\mu s \quad (7)$$

For example, if C<sub>FILTER</sub> = 1000pF, SLOW COMP<sub>n</sub>'s response time = 640μs. As a design aid, SLOW COMP<sub>n</sub>'s delay time (t<sub>SLOW COMP</sub>) versus C<sub>FILTER</sub> for standard values of C<sub>FILTER</sub> from 100pF to 1000pF is illustrated in Table 2.

**Table 2. t<sub>SLOWCOMP<sub>n</sub></sub> vs C<sub>FILTER</sub>**

C <sub>FILTER</sub>	t <sub>SLOWCOMP<sub>n</sub></sub>
100pF	73μs
220pF	149μs
330pF	218μs
470pF	306μs
680pF	438μs
820pF	527μs
1000pF	640μs

### SENSE RESISTOR CONSIDERATIONS

The fault current level at which the LTC4230's internal electronic circuit breakers trip is determined by a sense resistor connected between the LTC4230's V<sub>CC<sub>n</sub></sub> and SENSE<sub>n</sub> pins and two separate trip points. The first trip point is set by the SLOW COMP<sub>n</sub>'s threshold, V<sub>CB(SLOW)</sub> = 50mV, and the trip occurs if a load current fault condition exist for more than 10μs. The current level at which the electronic circuit breaker trips is given by Equation 8:

$$I_{\text{TRIP(SLOW)}_n} = \frac{V_{\text{CB(SLOW)}_n}}{R_{\text{SENSE}_n}} = \frac{50\text{mV}}{R_{\text{SENSE}_n}} \quad (8)$$

The second trip point is set by the FAST COMP<sub>n</sub>'s threshold, V<sub>CB(FAST)</sub> = 150mV, and occurs during fast load current transients that exist for 500ns or longer. The current level at which the circuit breaker trips in this case is given by Equation 9:

$$I_{\text{TRIP(FAST)}_n} = \frac{V_{\text{CB(FAST)}_n}}{R_{\text{SENSE}_n}} = \frac{150\text{mV}}{R_{\text{SENSE}_n}} \quad (9)$$

As a design aid, the currents at which electronic circuit breaker trips for common values for R<sub>SENSE</sub> are shown in Table 3.

**Table 3. I<sub>TRIP(SLOW)</sub> and I<sub>TRIP(FAST)</sub> vs R<sub>SENSE</sub>**

R <sub>SENSE</sub>	I <sub>TRIP(SLOW)</sub>	I <sub>TRIP(FAST)</sub>
0.005Ω	10A	30A
0.006Ω	8.3A	25A
0.007Ω	7.1A	21A
0.008Ω	6.3A	19A
0.009Ω	5.6A	17A
0.01Ω	5A	15A

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4230's V<sub>CC<sub>n</sub></sub> and SENSE<sub>n</sub> pins are strongly recommended. The drawing in Figure 11 illustrates the correct way of making connections between the LTC4230 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

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The power rating of the sense resistor should accommodate steady-state fault current levels so that the component is not damaged before the circuit breaker trips. Table 4 in the Appendix lists suggested sense resistors that can be used with the LTC4230's circuit breaker.

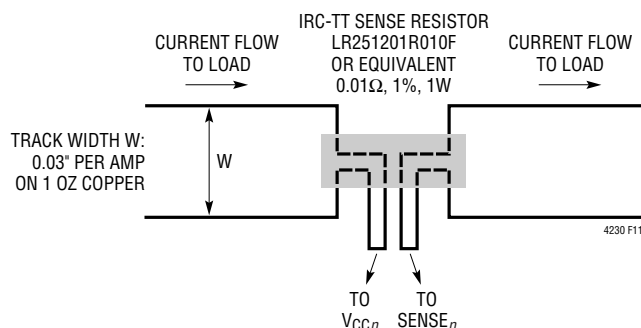


Figure 11. Making PCB Connections to the Sense Resistor

### CALCULATING CIRCUIT BREAKER TRIP CURRENT

For a selected  $R_{SENSE}$  value, the nominal load current that trips the circuit breaker is given by Equation 10:

$$I_{TRIP(NOM)} = \frac{V_{CB(NOM)}}{R_{SENSE(NOM)}} = \frac{50mV}{R_{SENSE(NOM)}} \quad (10)$$

The minimum load current that trips the circuit breaker is given by Equation 11.

$$I_{TRIP(MIN)} = \frac{V_{CB(MIN)}}{R_{SENSE(MAX)}} = \frac{40mV}{R_{SENSE(MAX)}} \quad (11)$$

where

$$R_{SENSE(MAX)} = R_{SENSE(NOM)} \cdot \left[ 1 + \left( \frac{R_{TOL}}{100} \right) \right]$$

The maximum load current that trips the circuit breaker is given in Equation 12.

$$I_{TRIP(MAX)} = \frac{V_{CB(MAX)}}{R_{SENSE(MIN)}} = \frac{60mV}{R_{SENSE(MIN)}} \quad (12)$$

where

$$R_{SENSE(MIN)} = R_{SENSE(NOM)} \cdot \left[ 1 - \left( \frac{R_{TOL}}{100} \right) \right]$$

For example:

If a sense resistor with  $7m\Omega \pm 5\%$   $R_{TOL}$  is used for current limiting, the nominal trip current  $I_{TRIP(NOM)} = 7.1A$ . From Equations 11 and 12,  $I_{TRIP(MIN)} = 5.4A$  and  $I_{TRIP(MAX)} = 9A$  respectively.

For proper operation and to avoid the circuit breaker tripping unnecessarily, the minimum trip current ( $I_{TRIP(MIN)}$ ) must exceed the circuit's maximum operating load current. For reliability purposes, the operation at the maximum trip current ( $I_{TRIP(MAX)}$ ) must be evaluated carefully. If necessary, two resistors with the same  $R_{TOL}$  can be connected in parallel to yield an  $R_{SENSE(NOM)}$  value that fits the circuit requirements.

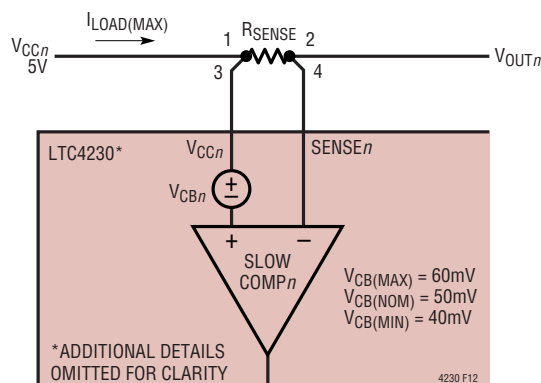


Figure 12. Circuit Breaker Equivalent Circuit for Calculating  $R_{SENSE}$

### POWER MOSFET SELECTION CRITERIA

To start the power MOSFET selection process, choose the maximum drain-to-source voltage,  $V_{DS(MAX)}$ , and the maximum drain current,  $I_{D(MAX)}$  of the MOSFET. The  $V_{DS(MAX)}$  rating must exceed the maximum input supply voltage (including surges, spikes, ringing, etc.) and the  $I_{D(MAX)}$  rating must exceed the maximum short-circuit current in the system during a fault condition. In addition, consider three other key parameters: 1) the required gate-source ( $V_{GS}$ ) voltage drive, 2) the voltage drop across the drain-to-source ON resistance,  $R_{DS(ON)}$  and 3) the maximum junction temperature rating of the MOSFET.

Power MOSFETs are classified into two categories: standard MOSFETs ( $R_{DS(ON)}$  specified at  $V_{GS} = 10V$ ) and logic-level MOSFETs ( $R_{DS(ON)}$  specified at  $V_{GS} = 5V$ ). The absolute

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maximum rating for  $V_{GS}$  is typically  $\pm 20V$  for standard MOSFETs. However, the  $V_{GS}$  maximum rating for logic-level MOSFETs ranges from  $\pm 8V$  to  $\pm 20V$  depending upon the manufacturer and the specific part number. The LTC4230's gate overdrive as a function of  $V_{CC}$  is illustrated in the Typical Performance curves. Logic-level MOSFETs are recommended for low supply voltage applications and standard MOSFETs can be used for applications where supply voltage is greater than 4.75V.

Note that in some applications, the gate of the external MOSFET can discharge faster than the output voltage when the circuit breaker is tripped. This causes a negative  $V_{GS}$  voltage on the external MOSFET. Usually, the selected external MOSFET should have a  $\pm V_{GS(MAX)}$  rating that is higher than the operating input supply voltage to ensure that the external MOSFET is not destroyed by a negative  $V_{GS}$  voltage. In addition, the  $\pm V_{GS(MAX)}$  rating of the MOSFET must be higher than the gate overdrive voltage. Lower  $\pm V_{GS(MAX)}$  rating MOSFETs can be used with the LTC4230 if the  $GATE_n$  overdrive is clamped to a lower voltage. The circuit in Figure 13 illustrates the use of zener diodes to clamp the LTC4230's  $GATE_n$  overdrive signal if lower voltage MOSFETs are used.

The  $R_{DS(ON)}$  of the external pass transistor should be low to make its drain-source voltage ( $V_{DS}$ ) a small percentage of  $V_{CC}$ . At a  $V_{CC} = 2.5V$ ,  $V_{DS} + V_{RSENSE} = 0.1V$  yields 4% error at the output voltage. This restricts the choice of MOSFETs to very low  $R_{DS(ON)}$ . At higher  $V_{CC}$  voltages, the  $V_{DS}$  requirement can be relaxed in which case MOSFET package dissipation ( $P_D$  and  $T_J$ ) may limit the value of  $R_{DS(ON)}$ . Table 5 lists some power MOSFETs that can be used with the LTC4230.

Power MOSFET junction temperature is dependent on four parameters: current delivered to the load,  $I_{LOAD}$ ,  $R_{DS(ON)}$ , junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the maximum ambient temperature to which the circuit will be exposed,  $T_{A(MAX)}$ . For reliable circuit operation, the maximum junction temperature ( $T_{J(MAX)}$ ) for a power MOSFET should not exceed the manufacturer's recommended value.

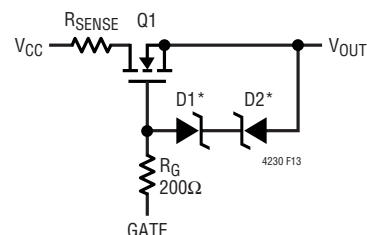
This includes normal mode operation, start-up, current-limit and autoretry mode in a fault condition. For a given set of conditions, the junction temperature of a power MOSFET is given by Equation 13:

$$T_{J(MAX)} \leq (T_{A(MAX)} + \theta_{JA} \cdot P_D) \quad (13)$$

where

$$P_D = (I_{LOAD})^2 \cdot R_{DS(ON)}$$

PCB layout techniques for optimal thermal management of power MOSFET power dissipation help to keep device  $\theta_{JA}$  as low as possible. See the section on PCB Layout Considerations for more information.



\*USER SELECTED VOLTAGE CLAMP  
(A LOW BIAS CURRENT ZENER DIODE IS RECOMMENDED)  
1N4688 (5V)  
1N4692 (7V): LOGIC-LEVEL MOSFET  
1N4695 (9V)  
1N4702 (15V): STANDARD-LEVEL MOSFET

Figure 13. Optional Gate Clamp for Lower  $V_{GS(MAX)}$  MOSFETs

## USING STAGGERED PIN CONNECTORS

The LTC4230 can be used on either a printed circuit board or on the backplane side of the connector, and examples for both are shown in Figure 14. Printed circuit board edge connectors with staggered pins are recommended as the insertion and removal of circuit boards do sequence the pin connections. Supply voltage and ground connections on the printed circuit board should be wired to the edge connector's long pins or blades. Control and status signals (like  $RESET_n$ ,  $FAULT$  and  $ON$ ) passing through the card's edge connector should be wired to short length pins or blades.

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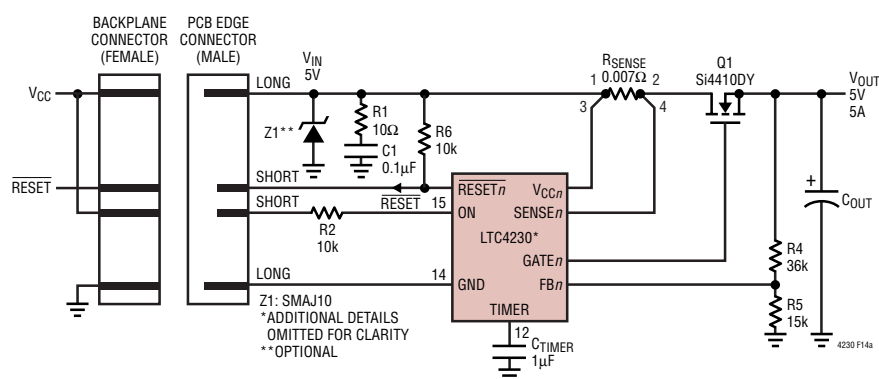
### PCB CONNECTION SENSE

There are a number of ways to use the LTC4230's ON pin to detect whether the printed circuit board has been fully seated in the backplane before the LTC4230 commences a start-up cycle.

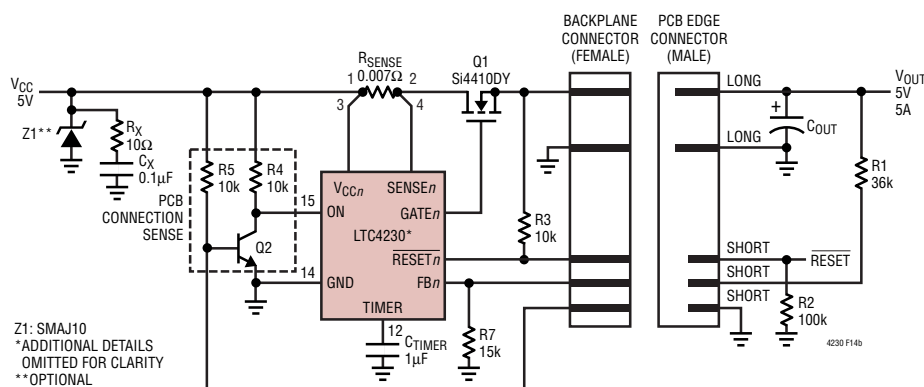
The first example is shown in the schematic on the front page of this data sheet. In this case, the LTC4230 is mounted on the PCB and a 10k resistive divider is connected to the ON pin. On the edge connector, R1 is wired to a short pin. Until the connectors are fully mated, the ON pin is held low, keeping the LTC4230 in an OFF state. Once the connectors are mated, the resistive divider is connected to  $V_{CC1}$ ,  $V_{ON} > 1.314V$  and the LTC4230 begins a start-up cycle.

In Figure 14a, an LTC4230 is illustrated in a basic configuration on a PCB daughter card. The ON pin is connected directly to  $V_{CC}$  on the backplane once the card is seated into the backplane. R2 is provided to bleed off any potential static charge which might exist on the backplane, the connector or during card installation.

A third example is shown in Figure 14b where the LTC4230 is mounted on the backplane. In this example, a 2N2222 transistor and a pair of resistors (R4, R5) form the PCB connection sense circuit. With the card out of the chassis, Q2's base is biased to  $V_{CC}$  through R5, biasing Q2 on and driving the LTC4230's ON pin low. The base of Q2 is also wired to a socket on the backplane connector. When a card is firmly seated into the backplane, the base of Q2 is then grounded through a short pin connection on the card. Q2 is biased off, the LTC4230's ON pin is pulled-up to  $V_{CC}$  and a start-up cycle begins.



(14a) Hot Swap Controller On Daughter Board



(14b) Hot Swap Controller on Backplane

Figure 14. Staggered Pin Connections

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In the previous three examples, the connection sense was hard wired with no processor (low) interrupt capability. As illustrated in Figure 15, the addition of an inexpensive logic-level discrete MOSFET and a couple of resistors offers processor interrupt control to the connection sense. R4 keeps the gate of M2 at  $V_{CC}$  until the card is firmly mated to the backplane. A logic low for the  $\overline{ON/OFF}$  signal turns M2 off, allows the ON pin to pull high and turns on the LTC4230.

A more elaborate connection sense scheme is shown in Figure 16. The bases of Q1 and Q2 are wired to short pins located on opposite ends of the edge connector because the installation/removal of printed circuit cards generally

requires rocking the card back and forth. When  $V_{CC}$  makes connection, the bases of transistors Q1 and Q2 are pulled high, biasing them on. When both are on, the LTC4230's ON pin is held low, keeping the LTC4230 off. When the short base connector pins of Q1 and Q2 finally mate to the backplane, their bases are grounded, biasing the transistors off. The ON pin is then pulled high by R3 enabling the LTC4230 and a power-up cycle begins.

A software-initiated power-down cycle can be started by momentarily driving transistor M1 with a logic high signal. This in turn will drive the LTC4230's ON pin low. If the ON pin is held low for more than  $8\mu s$ , the LTC4230's GATE pin is switched to ground.

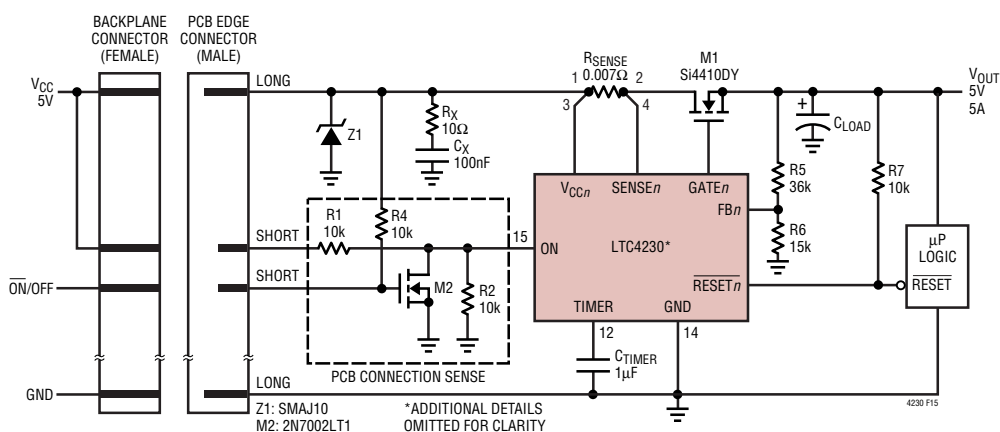


Figure 15. Connection Sense with  $\overline{ON/OFF}$  Control

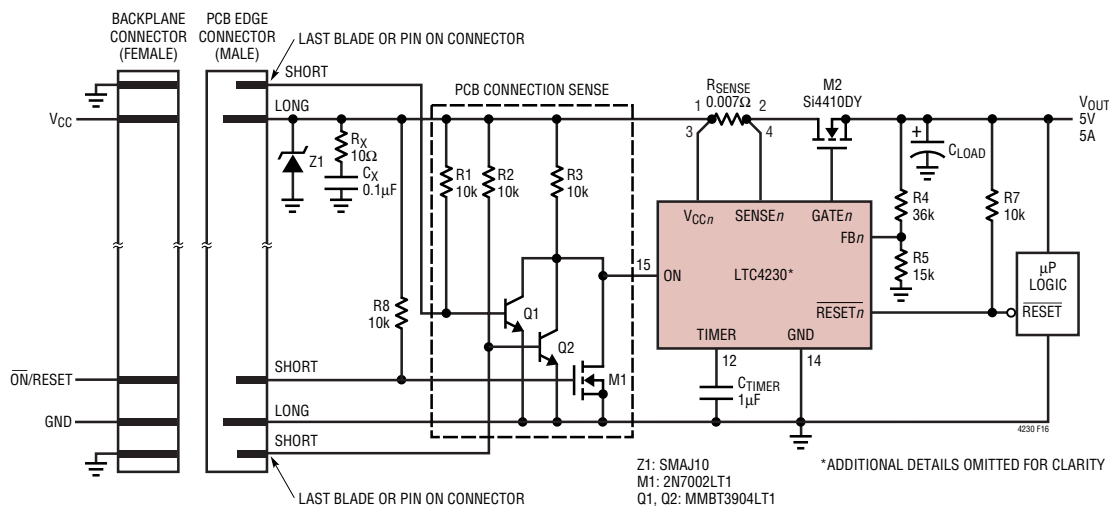


Figure 16. Connection Sense for Rocking the Daughter Board Back and Forth

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### HIGH SUPPLY VOLTAGE OPERATION CONSIDERATIONS

The LTC4230 can be used with supply voltages ranging from 1.7V to 16.5V. At high input supply voltages, the internal charge pump produces a minimum gate drive voltage of 7V for  $V_{CC} > 15V$ . This minimum voltage drive is derived by an internal zener diode clamp circuit, as shown in Figure 17. During PC board insertion or removal, sufficient transient current may flow through this zener diode. To limit the amount of current during transient events, an optional small resistor between the LTC4230's  $GATE_n$  pin and the gate of the external MOSFET can be used, as shown in Figure 17. A secondary benefit of this component is to minimize the possibility of high frequency parasitic oscillations in the power MOSFET.

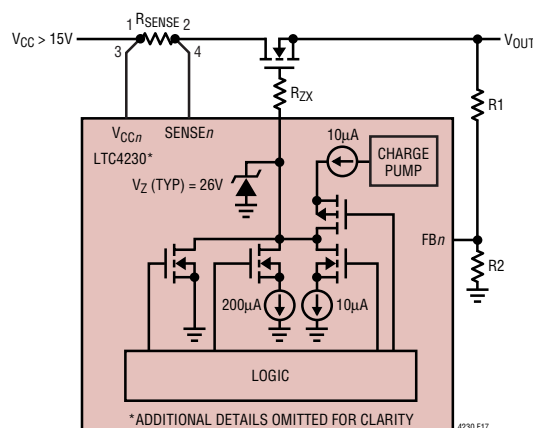


Figure 17. Using an External Resistor to Limit Zener Current in High  $V_{CC}$  Applications

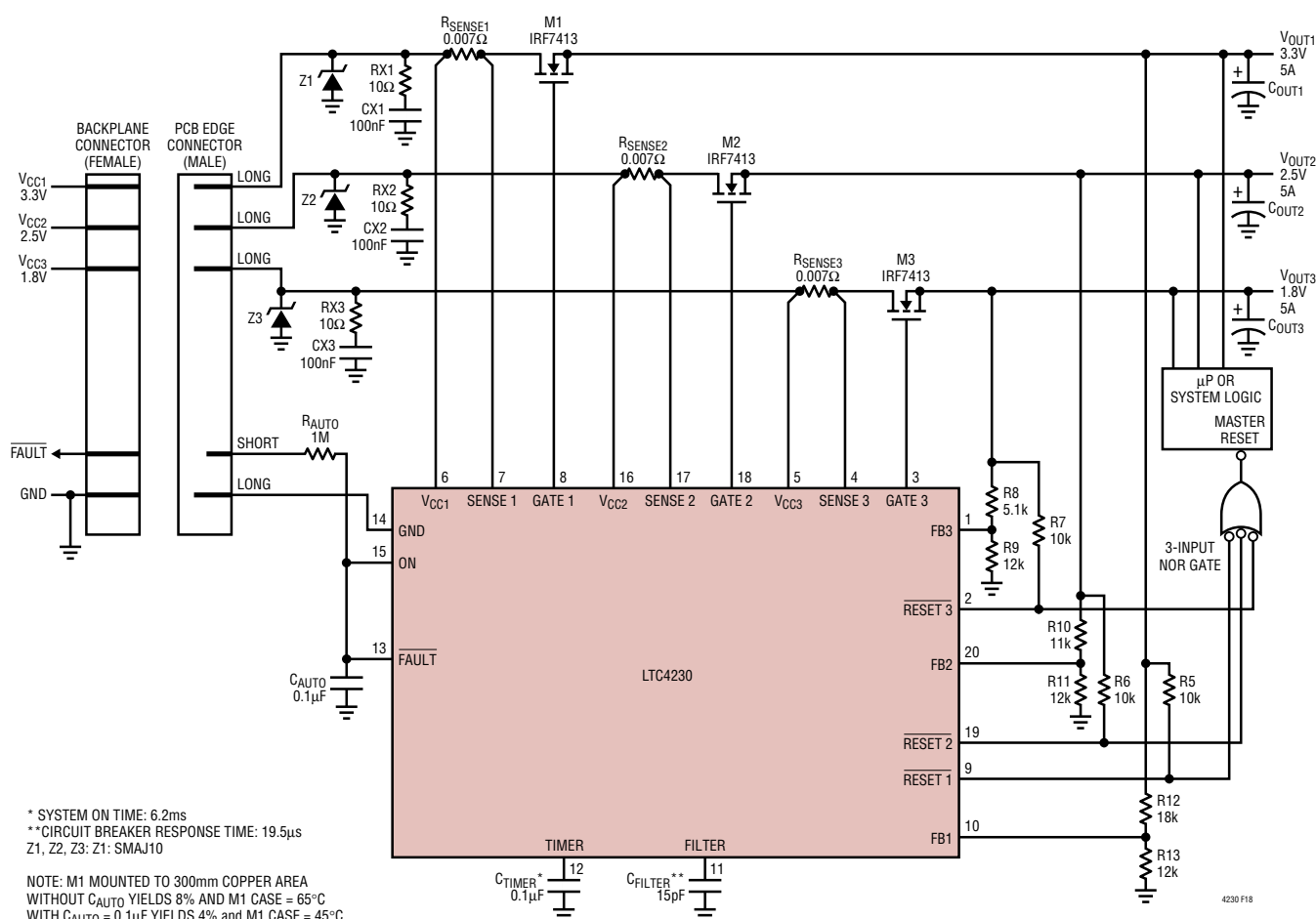


Figure 18. Autotetry Application



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### AUTORETRY AFTER A FAULT

To configure the LTC4230 to automatically retry after a fault condition, the  $\overline{\text{FAULT}}$  (which has an internal  $2\mu\text{A}$  pull-up current source) and ON pins can be connected together, as shown in Figure 18. In this case, the autoretry circuitry will attempt to restart the LTC4230 with an 7% duty cycle, as shown in the timing diagram of Figure 19. To prevent overheating the external MOSFET and other components during the autoretry sequence, adding a capacitor ( $C_{\text{AUTO}}$ ) to the circuit introduces a delay at the ON pin that adjusts the autoretry duty cycle. Equation 14 gives the autoretry duty cycle, modified by the external time constant  $C_{\text{AUTO}}$ :

$$\text{Autoretry Duty Cycle} = \frac{t_{\text{TIMER}}}{t_{\text{OFF}} + 14.5 \cdot t_{\text{TIMER}}} \cdot 100\% \quad (14)$$

where  $t_{\text{TIMER}}$  = LTC4230 system time constant (see TIMER function) and

$$t_{\text{OFF}} = \frac{C_{\text{AUTO}} \cdot 1.314\text{V}}{2\mu\text{A}}$$

For the values shown, the external delay equals 65.7ms and the autoretry duty cycle drops from 7% to 4%.

To increase the RC delay, the user may either increase  $C_{\text{AUTO}}$  or  $R_{\text{AUTO}}$ .

### OVERVOLTAGE TRANSIENT PROTECTION

Good engineering practice calls for bypassing the supply rail of any analog circuit. Bypass capacitors are often placed at the supply connection of every active device, in addition to one or more large value bulk bypass capacitors per supply rail. If power is connected abruptly, the large bypass capacitors slow the rate of rise of the supply voltage and heavily damp any parasitic resonance of lead or PC track inductance working against the supply bypass capacitors.

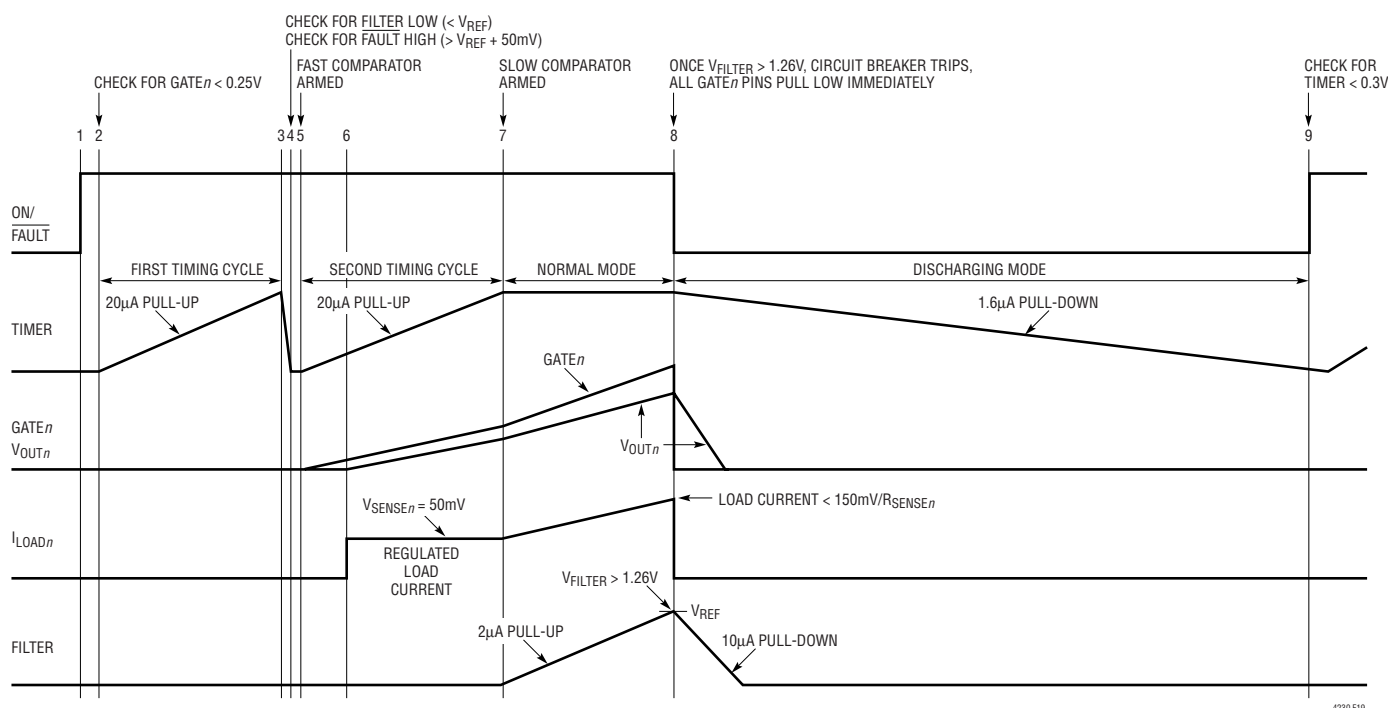


Figure 19. Autoretry Timing

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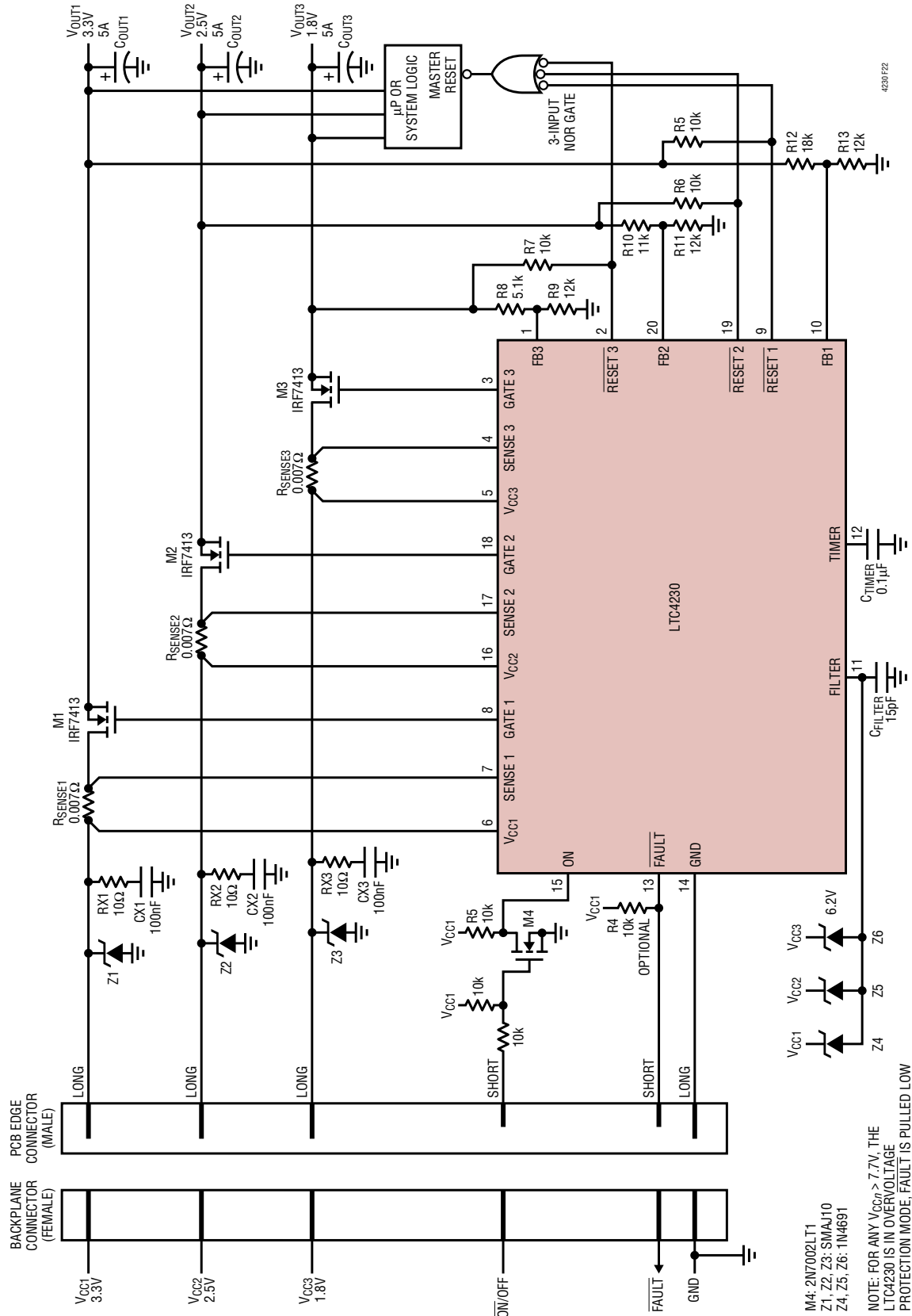


Figure 22. LTC4230 High Side Overvoltage Protection Implementation

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bias current 1N4691 zener diode is chosen to protect the system. Here, the zener diode is connected from  $V_{CC}$  to the LTC4230's FILTER pin. If the input voltage to the system is greater than 6.8V during start-up, the voltage on the FILTER pin is pulled higher than its 1.19V threshold. As a result, the  $GATE_n$  pin is not allowed to ramp and the second timing cycle will not commence until the supply overvoltage condition is removed. Should the supply overvoltage condition occur during normal operation, internal control logic would trip the electronic circuit breaker and the GATE would be pulled to ground, shutting off the external pass transistor. If a lower supply overvoltage threshold is desired, use a zener diode with a smaller breakdown voltage.

A timing diagram for illustrating LTC4230 operation under a high side overvoltage condition is shown in Figure 23. The start-up sequence in this case (between Time Points 1 and 2) is identical to any other start-up sequence under normal operating conditions. At Time Point 2, the input supply voltage causes the zener diode to conduct thereby forcing  $V_{FILTER} > 1.19V$ . At Time Point 3,  $\overline{FAULT}$  is asserted low and the TIMER pin voltage ramps down. At Time Point 4, the LTC4230 checks if  $V_{FILTER} < 1.19V$ .  $\overline{FAULT}$  is asserted low (but not latched) to indicate a start-up failure. Only if the input overvoltage condition is removed before Time Point 5 does the start-up sequence resume at the second timing cycle. At this point in time, the  $GATE_n$  pin voltage is allowed to ramp up,  $\overline{FAULT}$  is pulled to logic high and the circuit breaker is armed. Should, at any time after Time Point 5, a supply overvoltage condition develop ( $V_{FILTER} > 1.26V$ ), the electronic circuit breaker will trip, the  $GATE_n$  will be pulled low to turn off the external MOSFET and  $\overline{FAULT}$  will be asserted low and latched.

### Low Side (Output) Overvoltage Protection

A zener diode can be used in a similar fashion to detect/protect the system against a supply overvoltage condition on the load (or low) side of the pass transistor. In this case, the zener diode is connected from the load to the LTC4230's FILTER pin, as shown in Figure 24. An additional diode, D1, prevents the FILTER pin from pulling low during

output short-circuit. Figure 25 illustrates the timing diagram for a low side output overvoltage condition. In this example, the LTC4230 can only sense the overvoltage supply condition after Time Point 5 and the  $GATE_n$  pin has ramped up to its nominal operating value. After Time Point 5, a supply voltage fault occurs at the load and the zener diode conducts, causing  $V_{FILTER}$  to increase. At Time Point 6,  $V_{FILTER}$  is greater than 1.26V, the circuit breaker trips, GATE pulls to ground and  $\overline{FAULT}$  asserts low and is latched.

In either case, the LTC4230 can be configured to automatically initiate a start-up sequence. Please refer to the section on AutoRetry After a Fault for additional information.

## PCB LAYOUT CONSIDERATIONS

For proper operation of the LTC4230's circuit breaker function, a 4-wire Kelvin connection to the sense resistors is highly recommended. A recommended PCB layout for the sense resistor, the power MOSFET and the GATE drive components around the LTC4230 is illustrated in Figure 26. In Hot Swap applications where load currents can reach 10A or more, narrow PCB tracks exhibit more resistance than wider tracks and operate at more elevated temperatures. Since the sheet resistance of 1 ounce copper foil is approximately  $0.54m\Omega/\text{square}$ , track resistances add up quickly in high current applications. Thus, to keep PCB track resistance and temperature rise to a minimum, PCB track width must be appropriately sized. Consult Appendix A of LTC Application Note 69 for details on sizing and calculating trace resistances as a function of copper thickness.

In the majority of applications, it will be necessary to use plated-through vias to make circuit connections from component layers to power and ground layers internal to the PC board. For 1 ounce copper foil plating, a good starting point is 1A of DC current per via, making sure the via is properly dimensioned so that solder completely fills any void. For other plating thicknesses, check with your PCB fabrication facility.

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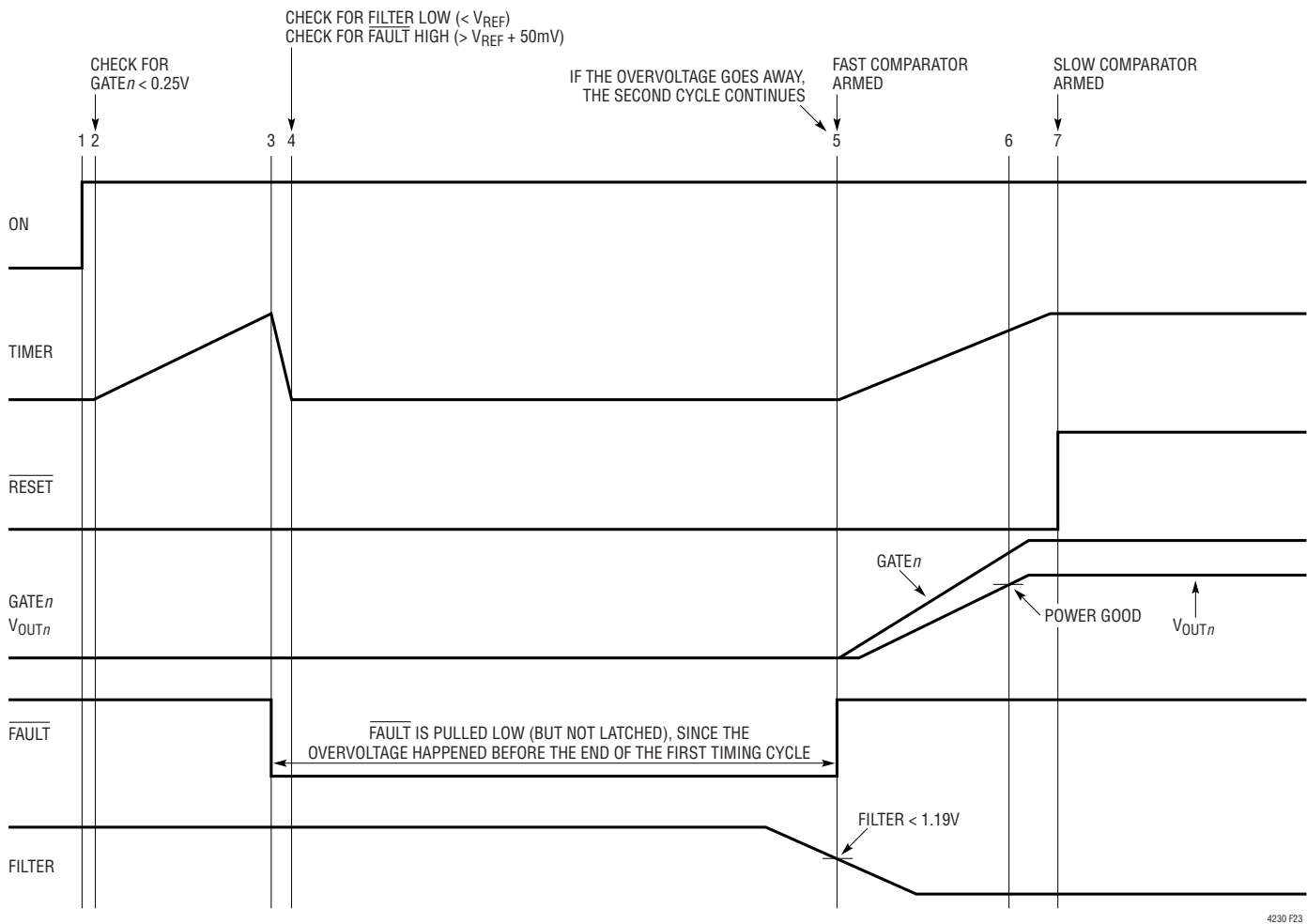
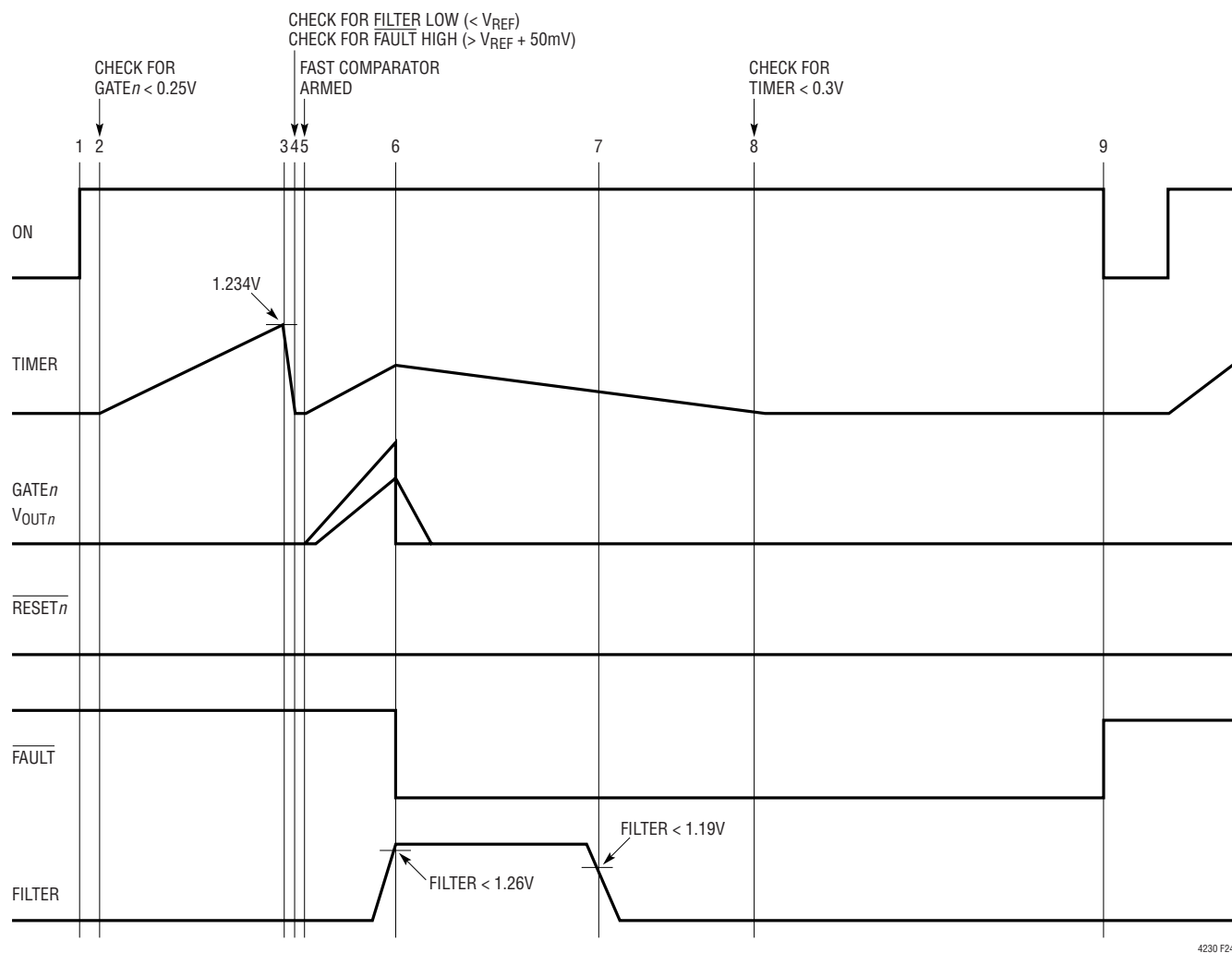


Figure 23. High Side Overvoltage Protection Timing





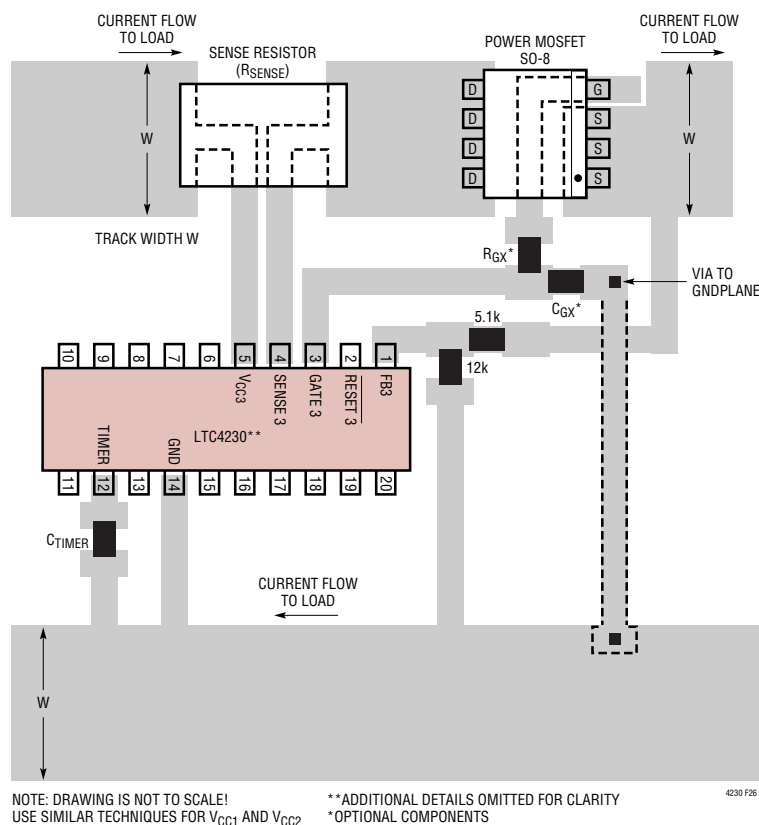
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Figure 25. Low Side Overvoltage Protection Timing

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Figure 26. Recommended Layout for LTC4230  $R_{SENSE}$ , Power MOSFET and Feedback Network

## APPENDIX

Table 4 lists some current sense resistors that can be used with the circuit breaker. Table 5 lists some power MOSFETs that are available. Table 6 lists the web sites of several

manufacturers. Since this information is subject to change, please verify the part numbers with the manufacturer.

Table 4. Sense Resistor Selection Guide

CURRENT LIMIT VALUE	PART NUMBER	DESCRIPTION	MANUFACTURER
1A	LR120601R050	0.05 $\Omega$ 0.5W 1% Resistor	IRC-TT
2A	LR120601R025	0.025 $\Omega$ 0.5W 1% Resistor	IRC-TT
2.5A	LR120601R020	0.02 $\Omega$ 0.5W 1% Resistor	IRC-TT
3.3A	WSL2512R015F	0.015 $\Omega$ 1W 1% Resistor	Vishay-Dale
5A	LR251201R010F	0.01 $\Omega$ 1.5W 1% Resistor	IRC-TT
10A	WSR2R005F	0.005 $\Omega$ 2W 1% Resistor	Vishay-Dale

## APPENDIX

Table 5. N-Channel MOSFET Selection Guide

CURRENT LEVEL (A)	PART NUMBER	DESCRIPTION	MANUFACTURER
0 to 2	M MDF3N02HD	Dual N-Channel SO-8, $R_{DS(ON)} = 0.09\Omega$ , $C_{ISS} = 455\text{pF}$	ON Semiconductor
2 to 5	MMSF5N02HD	Single N-Channel SO-8, $R_{DS(ON)} = 0.025\Omega$ , $C_{ISS} = 1130\text{pF}$	ON Semiconductor
5 to 10	MTB50N06V	Single N-Channel DD Pak, $R_{DS(ON)} = 0.028\Omega$ , $C_{ISS} = 1570\text{pF}$	ON Semiconductor
10 to 20	MTB75N05HD	Single N-Channel DD Pak, $R_{DS(ON)} = 0.0095\Omega$ , $C_{ISS} = 2600\text{pF}$	ON Semiconductor

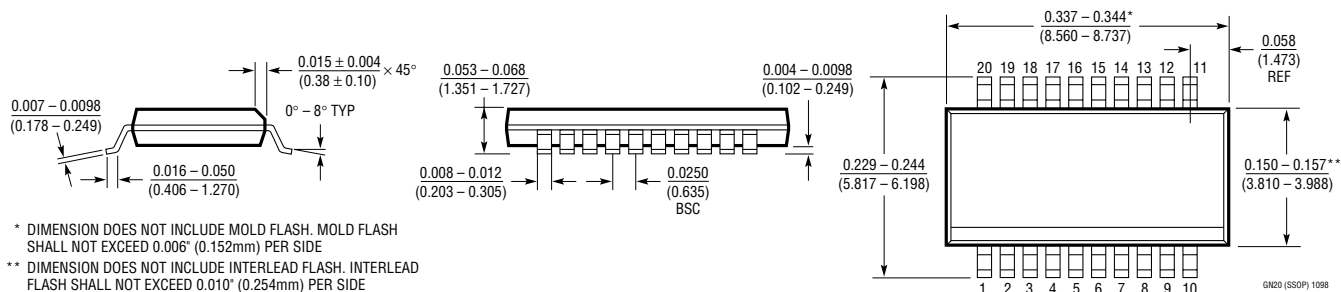
Table 6. Manufacturers' Web Sites

MANUFACTURER	WEB SITE
TEMIC Semiconductor	www.temic.com
International Rectifier	www.irf.com
ON Semiconductor	www.onsemi.com
Intersil	www.intersil.com

MANUFACTURER	WEB SITE
IRC-TT	www.irc tt.com
Vishay-Dale	www.vishay.com
Vishay-Siliconix	www.vishay.com
Diodes, Inc.	www.diodes.com

## PACKAGE DESCRIPTION

GN Package  
20-Lead Plastic SSOP (Narrow .150 Inch)  
(Reference LTC DWG # 05-08-1641)



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	2-Channel Hot Swap Controller	24-Pin, Operates from 3V to 12V and Supports -12V
LTC1422	Single Channel Hot Swap Controller in SO-8	Operates from 2.7V to 12V
LT1641-1/LT1641-2	Positive Voltage Hot Swap Controller	Operates from 9V to 80V
LTC1642	Single Channel Hot Swap Controller	16-Pin, Overvoltage Protection to 33V
LTC1644	PCI Hot Swap Controller	3.3V, 5V and $\pm 12\text{V}$ , 1V Precharge, PCI Reset Logic
LTC1647	Dual Channel Hot Swap Controller	8-Pin, 16-Pin, Operates from 2.7V to 16.5V
LTC4211	Single Hot Swap Controller with Multifunction Current Control	2.5V to 16.5V, Similar Features as LTC4230
LT4250L/LT4250H	Negative Voltage Hot Swap Controllers in SO-8	Operates from -20V to -80V, Active Current Limiting
LTC4251	-48V Hot Swap Controller in SOT-23	-15V to -100V, Active Current Limiting

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