TABLE OF CONTENTS

Features 1
Applications 1
Typical Application 1
Description 1
Table of Contents 2
Absolute Maximum Ratings 4
Pin Configuration 4
Order Information 4
Electrical Characteristics 5
Typical Performance Characteristics 11
Pin Functions 15
Block Diagram 17
Operation 18
Overview 18
Main Control Loop 18
EEPROM 19
Power Up and Initialization 20
Soft-Start 20
Sequencing 21
Voltage-Based Sequencing 21
Shutdown 21
Light Load Current Operation 22
Switching Frequency and Phase 22
Output Voltage Sensing 23
Current Sensing 23
Load Sharing 24
External/Internal Temperature Sense 24
RCONFIG (Resistor Configuration) Pins 25
Fault Detection and Handling 25
Internal Memory with CRC and ECC 26
Serial Interface 27
Communication Failure 27
Device Addressing 27
Responses to V_{OUT} and I_{OUT} Faults 28
Output Overvoltage Fault Response 28
Output Undervoltage Response 28
Peak Output Overcurrent Fault Response 28
Responses to Timing Faults 29
Responses to V_{IN} OV Faults 29
Responses to OT/UT Faults 29
Overtemperature Fault Response—Internal 29
Overtemperature and Undertemperature Fault Response—Externals 29
Responses to External Faults 29
Bus Timeout Failure 30
Similarity Between PMBus, SMBus and I^2C 2-Wire Interface 30
PMBus Serial Digital Interface 31
PMBus Command Summary 34
PMBus Commands 34
*Data Format 39
Applications Information 40
Current Limit Programming 40
I_{SENSE}^+ and I_{SENSE}^- Pins 40
Low Value Resistor Current Sensing 41
Inductor DCR Current Sensing 42
Slope Compensation and Inductor Peak Current 43
Inductor Value Calculation 43
Inductor Core Selection 44
Power MOSFET and Schottky Diode (Optional) Selection 44
Variable Delay Time, Soft-Start and Output Voltage Ramping 45
Digital Servo Mode 46
Soft Off (Sequenced Off) 46
$INTV_{CC}$ Regulator 47
Topside MOSFET Driver Supply (C_B, D_B) 48
Undervoltage Lockout 48
C_{IN} and C_{OUT} Selection 48
Fault Conditions 49
Open-Drain Pins 50
Phase-Locked Loop and Frequency Synchronization 50
Minimum On-Time Considerations 51

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TABLE OF CONTENTS

RCONFIG (External Resistor Configuration Pins) 51
Voltage Selection 51
Frequency and Phase Selection Using RCONFIG 52
Address Selection Using RCONFIG 53
Efficiency Considerations 54
Checking Transient Response 55
PC Board Layout Checklist 56
PC Board Layout Debugging 58
Design Example 59
Connecting the USB to the I²C/SMBus/PMBus Controller to the LTC3880 In System 61
LTpowerPlay: An Interactive GUI for Digital Power . 62
PMBus Communication and Command Processing 63
PMBus Command Details 65
Addressing and Write Protect 65
General Configuration Registers 67
On/Off/Margin 68
PWM Config 70
Voltage 72
Input Voltage and Limits 72
Output Voltage and Limits 73
Current 76
Input Current Calibration 76
Output Current Calibration 76
Input Current 76
Output Current 77
Temperature 78
External Temperature Calibration 78
External Temperature Limits 79
Timing 80
Timing—On Sequence/Ramp 80
Timing—Off Sequence/Ramp 81
Precondition for Restart 81
Fault Response 82
Fault Responses All Faults 82
Fault Responses Input Voltage 82
Fault Responses Output Voltage 83
Fault Responses Output Current 86
Fault Responses IC Temperature 87
Fault Responses External Temperature 88
Fault Sharing 89
Fault Sharing Propagation 89
Fault Sharing Response 91
Scratchpad 91
Identification 92
Fault Warning and Status 93
Telemetry 100
NVM Memory Commands 103
Store/Restore 103
Fault Log Operation 104
Fault Logging 104
Block Memory Write/Read 109
Typical Applications 111
Package Description 116
Revision History 117
Typical Application 118
Related Parts 118

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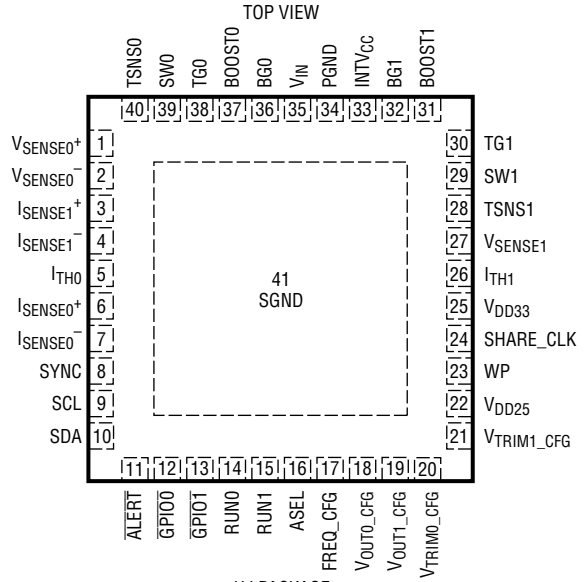
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} Voltage ..... –0.3V to 28V
Topside Driver Voltages
BOOST1, BOOST0 ..... –0.3V to 34V
Switch Voltage (SW1, SW0) ..... –5V to 28V
$EXTV_{CC}$, $INTV_{CC}$, (BOOST1 – SW1),
(BOOST0 – SW0) ..... –0.3V to 6V
V_{SENSE0}^+, V_{SENSE1}, $I_{SENSE0n}$, $I_{SENSE1n}$ ..... –0.3V to 6V
RUN0, RUN1, SDA, SCL, $\overline{ALERT}$ ..... –0.3V to 5.5V
FREQ_CFG, V_{OUTn_CFG}, V_{TRIMn_CFG},
ASEL, V_{DD25} ..... –0.3V to 2.75V
V_{DD33}, $\overline{GPIO0}$, $\overline{GPIO1}$, TSNS0, TSNS1, V_{SENSE0}^-,
SHARE_CLK, WP, SYNC, ITH*n* ..... –0.3V to 3.6V
$INTV_{CC}$ Peak Output Current 100mA
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C*
Storage Temperature Range ..... –65°C to 150°C*

*See Derating EEPROM Retention at Temperature in Applications Information section for junction temperatures in excess of 125°C.

PIN CONFIGURATION

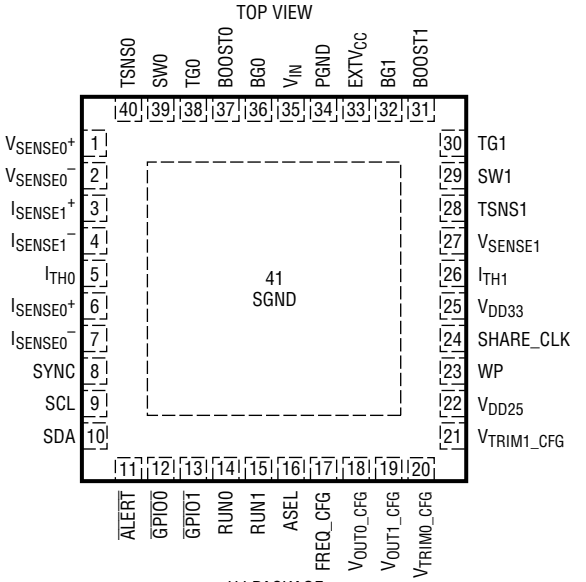
LTC3880



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 33°C/W, θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 41) IS SGND, MUST BE SOLDERED TO PCB

LTC3880-1



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 33°C/W, θ_{JC} = 2.5°C/W
EXPOSED PAD (PIN 41) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC3880EUJ#PBF	LTC3880EUJ#TRPBF	LTC3880UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 105°C
LTC3880IUJ#PBF	LTC3880IUJ#TRPBF	LTC3880UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3880EUJ-1#PBF	LTC3880EUJ-1#TRPBF	LTC3880UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 105°C
LTC3880IUJ-1#PBF	LTC3880IUJ-1#TRPBF	LTC3880UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C

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ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
AUTOMOTIVE PRODUCTS**				
LTC3880EUJ#WPBF	LTC3880EUJ#WTRPBF	LTC3880UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 105°C
LTC3880IUJ#WPBF	LTC3880IUJ#WTRPBF	LTC3880UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3880EUJ-1#WPBF	LTC3880EUJ-1#WTRPBF	LTC3880UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 105°C
LTC3880IUJ-1#WPBF	LTC3880IUJ-1#WTRPBF	LTC3880UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage							
V_{IN}	Input Voltage Range	(Note 12)	●	4.5		24	V
I_Q	Input Voltage Supply Current Normal Operation	(Note 14) $V_{RUN0,1}$ = 3.3V, No Caps on TG and BG $V_{RUN0,1}$ = 0V			 25 20		 mA mA
V_{UVLO}	Undervoltage Lockout Threshold when V_{IN} > 4.3V	V_{INTVCC}/V_{EXTVCC} Falling V_{INTVCC}/V_{EXTVCC} Rising			3.7 3.95		V V
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts			120		ms
Control Loop							
V_{OUT1R0}	Full-Scale Voltage Range 0 Set Point Accuracy (0.6V to 5V) Resolution LSB Step Size	VOUT_COMMAND(1) = 5.500V (Note 9)	● ● 	5.4 –0.5 	 12 1.375	5.6 0.5 	V % Bits mV
V_{OUT1R1}	Full-Scale Voltage Range 1 Set Point Accuracy (0.6V to 2.5V) Resolution LSB Step Size	VOUT_COMMAND(1) = 2.75V (Note 9)	● ● 	2.7 –0.5 	 12 0.6875	2.8 0.5 	V % Bits mV
V_{OUT0R0}	Full-Scale Voltage Range 0 Set Point Accuracy (0.6V to 4.096V) Resolution LSB Step Size	VOUT_COMMAND(0) = 4.095V (Note 9)	● ● 	4.0 –0.5 	 12 1.375	4.2 0.5 	V % Bits mV
V_{OUT0R1}	Full-Scale Voltage Range 1 Set Point Accuracy (0.6V to 2.5V) Resolution LSB Step Size	VOUT_COMMAND(0) = 2.75V (Note 9)	● ● 	2.7 –0.5 	 12 0.6875	2.8 0.5 	V % Bits mV
$V_{LINEREG}$	Line Regulation	6V < V_{IN} < 24V	●			±0.02	%/V
$V_{LOADREG}$	Load Regulation	ΔV_{ITH} = 1.35V – 0.7V ΔV_{ITH} = 1.35V – 2.0V	● ●		0.01 –0.01	0.1 –0.1	% %

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$g_{m0,1}$	Error Amplifier g_m	$I_{TH0,1}$ =1.22V			3		mmho
$I_{ISENSE0,1}$	Input Current	V_{ISENSE} = 5.5V	●		±1	±3	µA
$V_{SENSERIN0}$	V_{SENSE} Input Resistance to Ground	0V ≤ V_{PIN} ≤ 5.5V			41		kΩ
$V_{SENSERIN1}$	V_{SENSE} Input Resistance to Ground	0V ≤ V_{PIN} ≤ 5.5V			37		kΩ
$V_{IILIMIT}$	Resolution				3		bits
	$V_{ILIMMAX}$	Hi Range Lo Range	● ●	68 44	75 50	82 56	mV mV
	V_{ILMMIN}	Hi Range Lo Range			37.5 25		mV mV
Gate Drivers							
TG0,1 t_r t_f	TG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
BG0,1 t_r t_f	BG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Time	(Note 4) C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time				90		ns
OV/UV Output Voltage Supervisor Channel 0							
N	Resolution				8		Bits
$V0_{RANGE0}$	Voltage Monitoring Range	Range Value = 0		1		4.096	V
$V0_{RANGE1}$	Voltage Monitoring Range	Range Value = 1		0.5		2.7	V
$V0_{OUSTP0}$	Threshold Programming Step	Range Value = 0			22		mV
$V0_{OUSTP1}$	Threshold Programming Step	Range Value = 1			11		mV
$V0_{THACC0}$	Threshold Accuracy 2V < V_{OUT0} < 4V	Range Value = 0	●			±2	%
$V0_{THACC1}$	Threshold Accuracy 1V < V_{OUT0} < 2.5V	Range Value = 1	●			±2	%
$t_{PROPOV0}$	OV Comparator to $\overline{GPIO}$ Low Time	V_{OD} = 10% of Threshold				35	µs
$t_{PROPUV0}$	UV Comparator to $\overline{GPIO}$ Low Time	V_{OD} = 10% of Threshold				100	µs
OV/UV Output Voltage Supervisor Channel 1							
N	Resolution				8		bits
$V1_{RANGE0}$	Voltage Range	Range Value = 0		1		5.5	V
$V1_{RANGE1}$	Voltage Range	Range Value = 1		0.5		2.7	V
$V1_{OUSTP0}$	Step Size	Range Value = 0			22		mV
$V1_{OUSTP1}$	Step Size	Range Value = 1			11		mV
$V1_{THACC0}$	Threshold Accuracy 2V < V_{OUT1} < 5V	Range Value = 0	●			±2	%

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V1_{THACC1}$	Threshold Accuracy 1V < V_{OUT1} < 2.5V	Range Value = 1	●			±2	%
$t_{PROPOV1}$	OV Comparator to $\overline{GPIO}$ Low Time	V_{OD} = 10% of Threshold				35	µs
$t_{PROPUV1}$	UV Comparator to $\overline{GPIO}$ Low Time	V_{OD} = 10% of Threshold				100	µs
V_{IN} Voltage Supervisor							
N	Resolution				8		bits
$V_{INRANGE}$	Full-Scale Voltage			4.5		20	V
V_{INSTP}	Step Size				82		mV
$V_{INTHACC}$	Threshold Accuracy 9.0V < V_{IN} < 20V		●			±2.5	%
$V_{INTHACC\M}$	Threshold Accuracy 4.5V < V_{IN} ≤ 9V		●			±5	%
$t_{PROPVIN}$	Comparator Response Time (VIN_ON and VIN_OFF)	V_{OD} = 10% of Threshold				100	µs
Output Voltage Readback							
N	Resolution LSB Step Size				16 244		Bits µV
V_{OFS}	Full-Scale Voltage	(Note 10) V_{RUNn} = 0V (Note 8)			8		V
V_{OUT_TUE}	Total Unadjusted Error	(Note 8) V_{OUTn} > 0.6V	●			0.5	%
V_{OS}	Zero-Code Offset Voltage					±500	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			90		ms
V_{IN} Voltage Readback							
N	Resolution	(Note 5)			10		Bits
V_{IFS}	Full-Scale Voltage	(Note 11)			38.91		V
V_{IN_TUE}	Total Unadjusted Error	V_{VIN} > 4.5V (Note 8)	 ●			0.5 2	% %
$t_{CONVERT}$	Conversion Time	(Note 6)			90		ms
Output Current Readback							
N	Resolution LSB Step Size	(Note 5) 0V ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 16mV 16mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 32mV 32mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 63.9mV 63.9mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 127.9mV			10 15.625 31.25 62.5 125		Bits µV µV µV µV
I_{FS}	Full-Scale Current	(Note 7) R_{ISENSE} = 1mΩ			±128		A
I_{OUT_TUE}	Total Unadjusted Error	(Note 8) V_{ISENSE} > 6mV (Note 15)	●			±1	%
V_{OS}	Zero-Code Offset Voltage					±28	µV
$t_{CONVERT}$	Conversion Time	(Note 6)			90		ms
Input Current and Duty Cycle Readback							
D_RES	Resolution				10		Bits
D_TUE	Total Unadjusted Error	16.3% Duty Cycle		–3		3	%
$t_{CONVERT}$	Update Rate	(Note 6)			90		ms

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Temperature Readback (T0, T1, T2)							
T_{RES_T}	Resolution				0.25		°C
T0,1_TUE	External TSNS TUE	ΔV_{TSNS} = 72mV (Note 8)	●			±3	°C
T2_TUE	Internal TSNS TUE	$V_{RUN0,1}$ = 0.0V, f_{SYNC} = 0kHz (Note 8)			±1		°C
$t_{CONVERT_T}$	Update Rate	(Note 6)			90		ms
$INTV_{CC}$ Regulator							
V_{INTVCC}	Internal V_{CC} Voltage No Load (LTC3380)	6V < V_{IN} < 24V		4.8	5	5.2	V
V_{LDO_INT}	$INTV_{CC}$ Load Regulation (LTC3380)	I_{CC} = 0mA to 50mA			0.5	±2	%
V_{DD33} Regulator							
V_{DD33}	Internal V_{DD33} Voltage	4.5V < V_{INTVCC}/V_{EXTVCC}		3.2	3.3	3.40	V
$I_{LIM(VDD33)}$	V_{DD33} Current Limit	V_{DD33} = GND			70		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold				3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold				3.1		V
V_{DD25} Regulator							
V_{DD25}	Internal V_{DD25} Voltage			2.25	2.5	2.75	V
$I_{LIM(VDD25)}$	V_{DD25} Current Limit	V_{DD25} = GND			50		mA
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency Accuracy	250kHz < f_{SYNC} < 1MHz Measured Falling Edge-to-Falling Edge of SYNC with SWITCH_FREQUENCY = 250.0.and 1000.0	●			±7.5	%
$V_{TH,SYNC}$	SYNC Input Threshold	V_{CLKIN} Falling V_{CLKIN} Rising			1 1.5		V V
$V_{OL,SYNC}$	SYNC Low Output Voltage	I_{LOAD} = 3mA	●		0.2	0.4	V
$I_{LEAKSYNC}$	SYNC Leakage Current in Slave Mode	0V ≤ V_{PIN} ≤ 3.6V				±5	µA
θSYNC-θ0	SYNC to Ch0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	MFR_PWM_CONFIG_LTC3880[2:0] = 0, 2, 3 MFR_PWM_CONFIG_LTC3880[2:0] = 5 MFR_PWM_CONFIG_LTC3880[2:0] = 1 MFR_PWM_CONFIG_LTC3880[2:0] = 4, 6			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1	SYNC to Ch1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	MFR_PWM_CONFIG_LTC3880[2:0] = 3 MFR_PWM_CONFIG_LTC3880[2:0] = 0 MFR_PWM_CONFIG_LTC3880[2:0] = 2, 4, 5 MFR_PWM_CONFIG_LTC3880[2:0] = 1 MFR_PWM_CONFIG_LTC3880[2:0] = 6			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 13)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 13)	T_J < T_{JMAX}	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < TJ < 85°C During EEPROM Write Operations	●		440	4100	ms

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 12V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs SCL, SDA, RUN0, RUN1, $\overline{GPIO0}$, $\overline{GPIO1}$							
V_{IH}	Input High Threshold Voltage	SCL, SDA, RUN0, RUN1, $\overline{GPIO0}$, $\overline{GPIO1}$	●			2.0	V
V_{IL}	Input Low Threshold Voltage	SCL, SDA, RUN0, RUN1, $\overline{GPIO0}$, $\overline{GPIO1}$	●	1.4			V
V_{HYST}	Input Hysteresis	SCL, SDA			0.08		V
C_{PIN}	Input Capacitance					10	pF
Digital Input WP							
I_{PUWP}	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL, SDA, $\overline{GPIO0}$, $\overline{GPIO1}$, $\overline{ALERT}$, RUN0, RUN1, SHARE_CLK							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
Digital Inputs SHARE_CLK, WP							
V_{IH}	Input High Threshold Voltage		●		1.5	1.8	V
V_{IL}	Input Low Threshold Voltage		●	0.6	1		V
Leakage Current SDA, SCL, $\overline{ALERT}$, RUN0, RUN1							
I_{OL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V	●			±5	µA
Leakage Current $\overline{GPIO0}$, $\overline{GPIO1}$							
I_{GL}	Input Leakage Current	0V ≤ V_{PIN} < 3.6V	●			±2	µA
Digital Filtering of $\overline{GPIO0}$, $\overline{GPIO1}$							
I_{FLTG}	Input Digital Filtering $\overline{GPIO}$				3		µs
Digital Filtering of RUN0, RUN1							
I_{FLTG}	Input Digital Filtering RUN				10		µs
PMBus Interface Timing Characteristics							
f_{SMB}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD,STA}$	Hold time After Repeated Start Condition. After this Period, the First Clock is Generated		●	0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		●	0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD,DAT}$	Data Hold Time Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 µs µs
$t_{SU,DAT}$	Data Setup Time Receiving Data		 ●	 0.1			 µs
$t_{TIMEOUT_SMB}$	Stuck PMBus Timer Non-Block Reads Stuck PMBus Timer Block Reads	Measured from the Last PMBus Start Event			32 150		ms ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs

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ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3880/LTC3880-1 are tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3880E/LTC3880E-1 are guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 105°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3880I/LTC388I-1 are guaranteed over the full –40°C to 125°C operating junction temperature range. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 5: The data format in PMBus is 5 bits exponent (signed) and 11 bits mantissa (signed). This limits the output resolution to 10 bits though the internal ADC is 16 bits and the calculations use 32-bit words.

Note 6: The data conversion is done in round robin fashion. All inputs signals are continuously converted for a typical latency of 90ms.

Note 7: The IOUT_CAL_GAIN = 1.0mΩ and MFR_IOUT_CAL_GAIN_TC = 0.0. Value as read from READ_IOUT in amperes.

Note 8: Part tested with PWM disabled. Evaluation in application demonstrates capability. TUE (%) = ADC Gain Error (%) + 100 • [Zero Code Offset + ADC Linearity Error]/Actual Value.

Note 9: All V_{OUT} commands assume the ADC is used to auto-zero the output to achieve the stated accuracy. LTC3880 is tested in a feedback loop that servos V_{OUT} to a specified value.

Note 10: The maximum V_{OUT} voltage is 5.5V.

Note 11: The maximum V_{IN} voltage is 28V.

Note 12: When $V_{IN} < 6V$, $INTV_{CC}$ must be tied to V_{IN}.

Note 13: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification. The RESTORE_USER_ALL command (NVM read) is valid over the entire operating junction temperature range.

Note 14: The LTC3880-1 quiescent current (I_Q) equals the I_Q of V_{IN} plus the I_Q of $EXTV_{CC}$.

Note 15: Guaranteed with a common mode voltage (V_{OUT}) between 0V and 5.5V.

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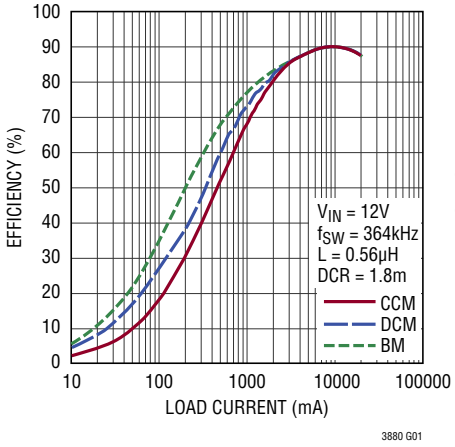
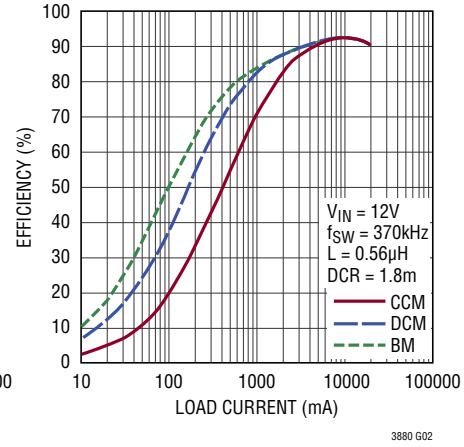
TYPICAL PERFORMANCE CHARACTERISTICS

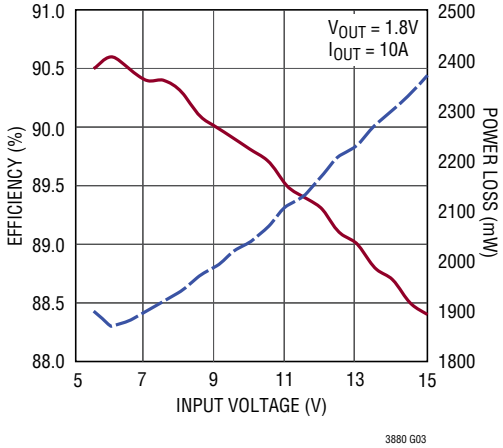
Efficiency vs Load Current, V_{OUT} = 1.8V (LTC3880)



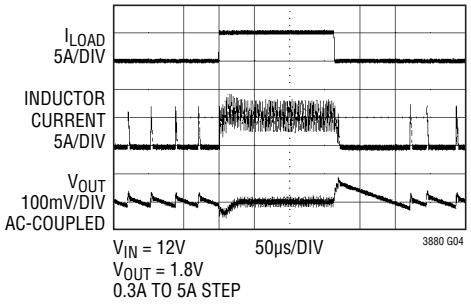
Efficiency vs Load Current, V_{OUT} = 3.3V (LTC3880)



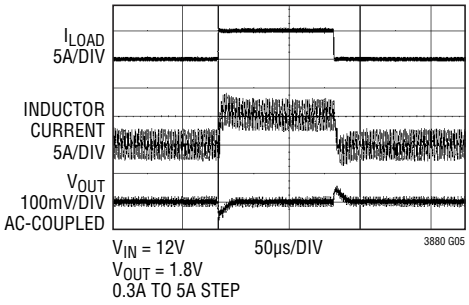
Efficiency and Power Loss vs Input Voltage (LTC3880)



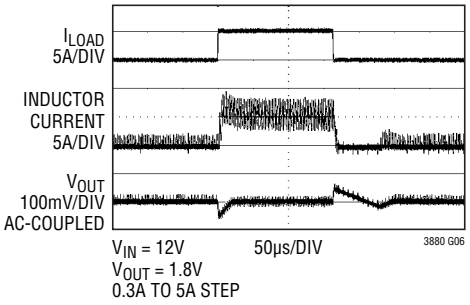
Load Step (Burst Mode Operation)



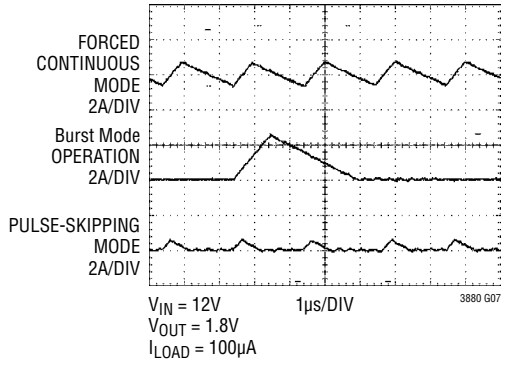
Load Step (Forced Continuous Mode)



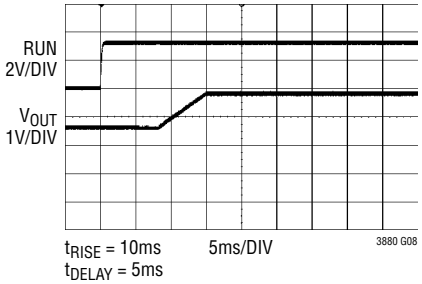
Load Step (Pulse-Skipping Mode)



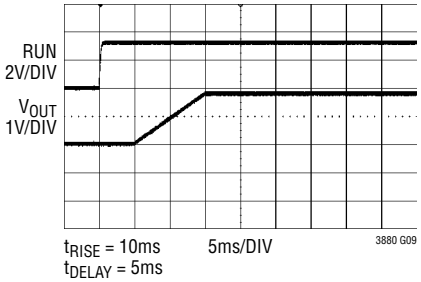
Inductor Current at Light Load



Start-Up into a Pre-Biased Load



Soft-Start Ramp



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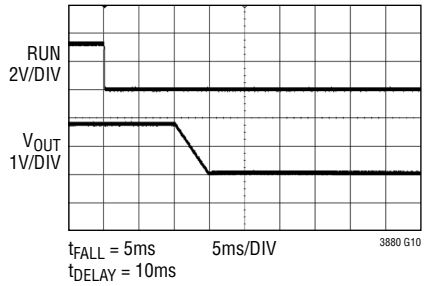
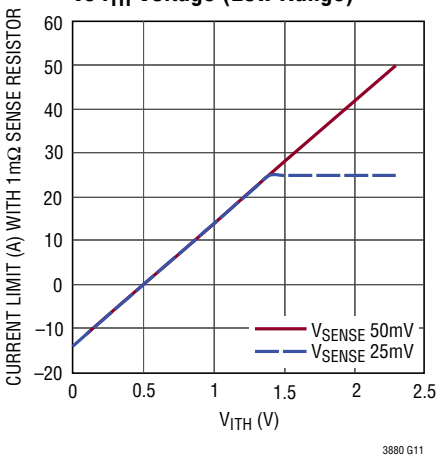
TYPICAL PERFORMANCE CHARACTERISTICS

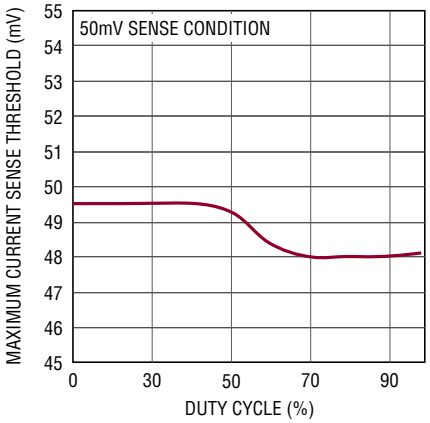
Soft-Off Ramp



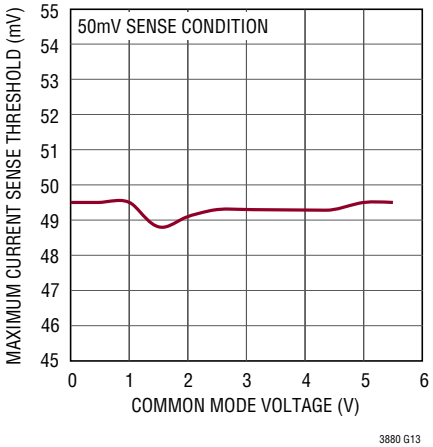
Current Sense Threshold vs I_{TH} Voltage (Low Range)



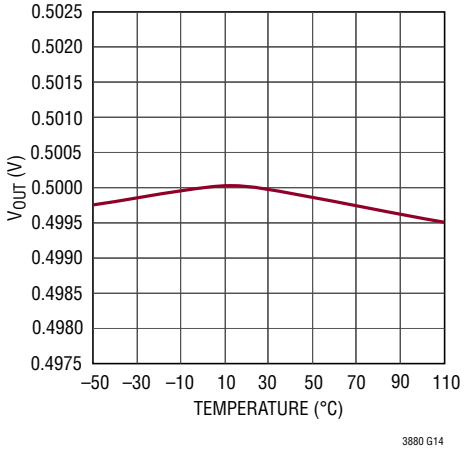
Maximum Current Sense Threshold vs Duty Cycle, V_{OUT} = 0V



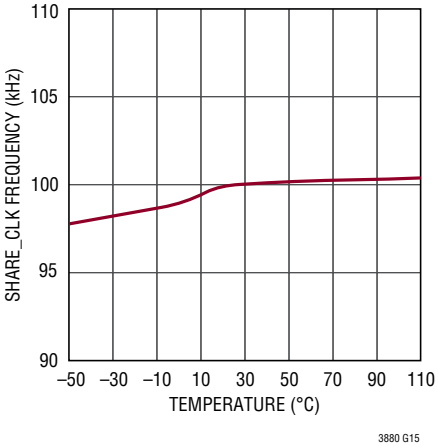
Maximum Current Sense Threshold vs Common Mode Voltage



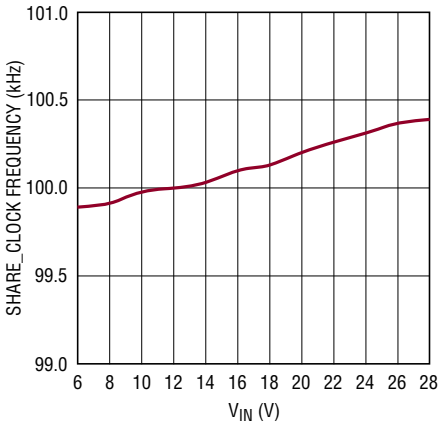
Regulated Output vs Temperature



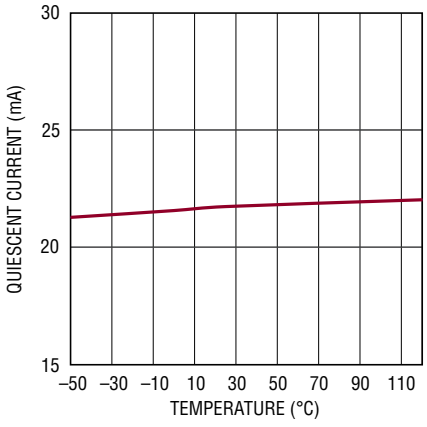
SHARE_CLK Frequency vs Temperature



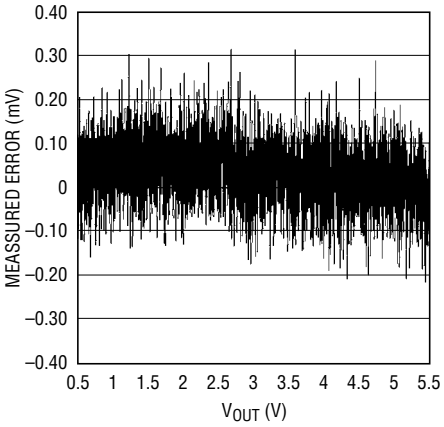
SHARE-CLK Frequency vs V_{IN}



Quiescent Current vs Temperature



V_{OUT} Measurement vs V_{OUT}



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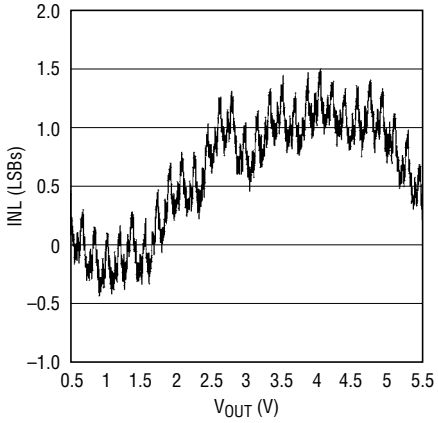
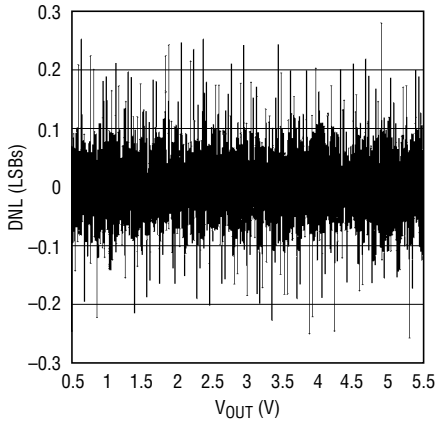
TYPICAL PERFORMANCE CHARACTERISTICS

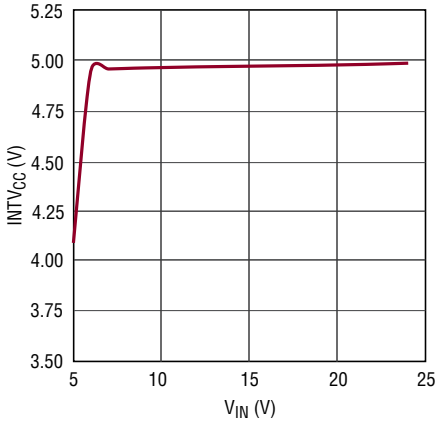
V_{OUT} Command INL



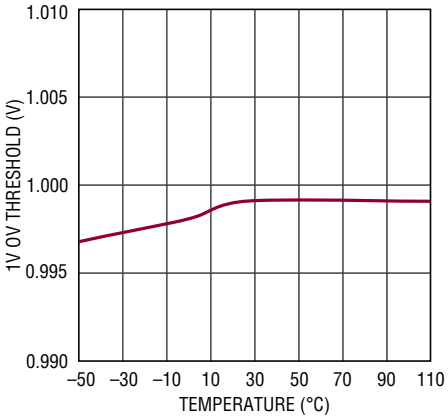
V_{OUT} Command DNL



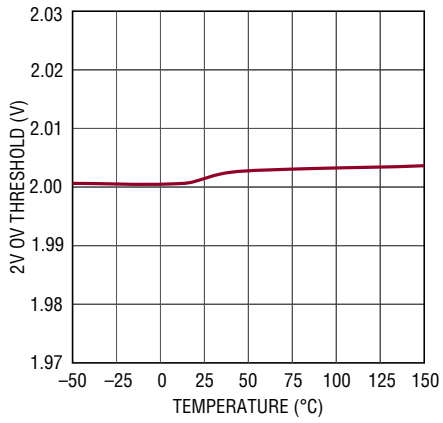
$INTV_{CC}$ Line Regulation



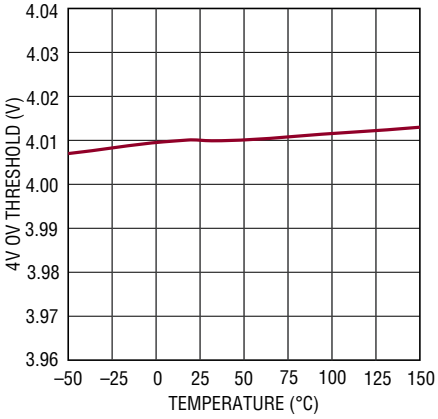
V_{OUT} OV Threshold vs Temperature (1V Target)



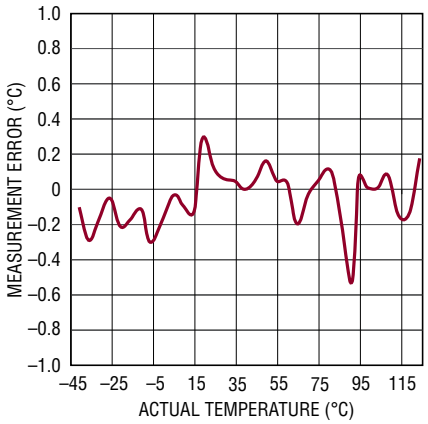
V_{OUT} OV Threshold vs Temperature (2V Target)



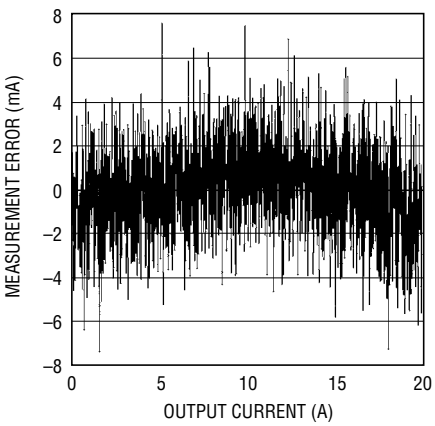
V_{OUT} OV Threshold vs Temperature (4V Target)



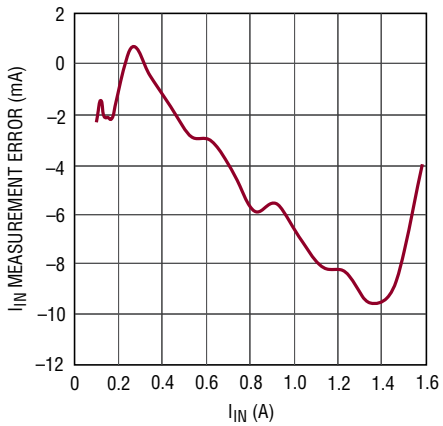
Temperature Error vs Temperature



I_{OUT} Error vs I_{OUT} Room Temperature



I_{IN} Measurement Error vs I_{IN}



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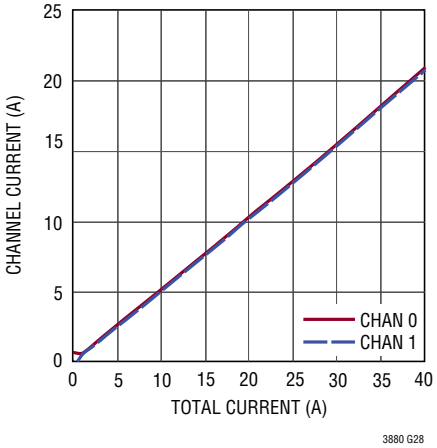
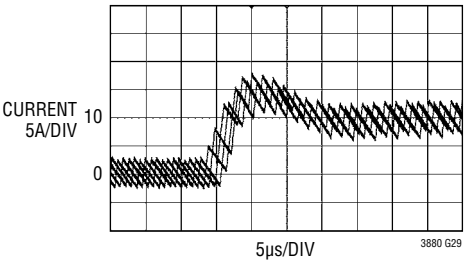
TYPICAL PERFORMANCE CHARACTERISTICS

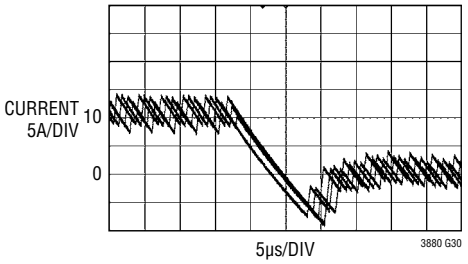
DC Output Current Matching in a 2-Phase System (LTC3880)



Dynamic Current Sharing During a Load Transient in a 4-Phase System



Dynamic Current Sharing During a Load Transient in a 4-Phase System



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PIN FUNCTIONS

V_{SENSE0}^+ (Pin 1): Channel 0 Positive Voltage Sense Input.

V_{SENSE0}^- (Pin 2): Channel 0 Negative Voltage Sense Input.

I_{TH0}/I_{TH1} (Pin 5/Pin 26): Current Control Threshold and Error Amplifier Compensation Nodes. Each associated channel's current comparator tripping threshold increases with its I_{TH} voltage.

I_{SENSE0}^+/I_{SENSE1}^+ (Pins 6/Pin 3): Current Sense Comparator Inputs. The (+) inputs to the current comparators are normally connected to DCR sensing networks or current sensing resistors.

I_{SENSE0}^-/I_{SENSE1}^- (Pin 7/Pin 4): Current Sense Comparator Inputs. The (–) inputs are connected to the low side of the current sense element.

SYNC (Pin 8): External Clock Synchronization Input and Open-Drain Output Pin. If an external clock is present at this pin, the switching frequency will be synchronized to the external clock. If clock master mode is enabled, this pin will pull low at the switching frequency with a 500ns pulse to ground. A resistor pull up to 3.3V is required in the application if the LTC3880 is the master.

SCL (Pin 9): Serial Bus Clock Input. Open-drain output, can hold the output low if clock stretching is enabled. A pull-up resistor to 3.3V is required in the application.

SDA (Pin 10): Serial Bus Data Input and Output. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{ALERT}}$ (Pin 11): Open-Drain Digital Output. Connect the $\overline{\text{SMBALERT}}$ signal to this pin. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{GPIO0}}$/$\overline{\text{GPIO1}}$ (Pin 12/Pin 13): Digital Programmable General Purpose Inputs and Outputs. Open-drain output. A pull-up resistor to 3.3V is required in the application.

RUN0/RUN1 (Pin 14/Pin 15): Enable Run Input. Logic high on these pins enables the controller. Open-drain output holds the pin low until the LTC3880 is out of reset. A pull-up resistor to 3.3V is required in the application.

ASEL (Pin 16): Serial Bus Address Configuration Input. Connect a ±1% resistor divider between the chip V_{DD25} ASEL and SGND in order to select the 4LSBs of the serial bus interface address. A resistor divider on ASEL is recommended if there are more than 1 LTC3880 on the same board to assure the user can independently program each IC. If the pin is left open, the IC will use the value programmed in the NVM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

FREQ_CFG (Pin 17): Frequency or Phase Set/Select Pin. Connect a ±1% resistor divider between the chip V_{DD25} FREQ_CFG and SGND in order to select switching frequency or phase. If the pin is left open, the IC will use the value programmed in the NVM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

V_{OUT0_CFG}/V_{OUT1_CFG} (Pin 18/Pin 19): Output Voltage Select Pin. Connect a ±1% resistor divider between the chip V_{DD25} $V_{OUT}n$_CFG and SGND in order to select output voltage. This voltage can be adjusted with the $V_{TRIM}n$_CFG pins. If the pin is left open, the IC will use the value programmed in the NVM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

V_{TRIM0_CFG}/V_{TRIM1_CFG} (Pin 20/Pin 21): Voltage Trim Select Pin. Connect a ±1% resistor divider between the chip V_{DD25} $V_{TRIM}n$_CFG and SGND in order to adjust the output voltage set point. The $V_{TRIM}n$_CFG settings in conjunction with the $V_{OUT}n$_CFG setting adjusts the voltage set point. If the pin is left open, the IC will either not modify the $V_{OUT}n$_CFG setting or use NVM. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

V_{DD25} (Pin 22): Internally Generated 2.5V power Supply Output Pin. Bypass this pin to SGND with a low ESR 1µF capacitor. Do not load this pin with external current except for the ±1% resistor dividers required for the configuration pins.

WP (Pin 23): Write Protect Pin Active High. An internal 10µA current source pulls the pin to V_{DD33}. If WP is high, the PMBus writes are restricted.

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PIN FUNCTIONS

SHARE_CLK (Pin 24): Share Clock, Bidirectional Open-Drain Clock Sharing Pin. Nominally 100kHz. Used to synchronize the timing between multiple LTC3880s. Tie all SHARE_CLK pins together. All LTC3880s will synchronize to the fastest clock. A pull-up resistor to 3.3V is required.

V_{DD33} (Pin 25): Internally Generated 3.3V Power Supply Output Pin. Bypass this pin to SGND with a low ESR 1µF capacitor. Do not load this pin with external current except for the pull-up resistors required for $\overline{GPIO}n$, SCLK, SYNC and possibly RUN*n*, $\overline{ALERT}$, SDA and SCL.

V_{SENSE1} (Pin 27): Channel 1 Voltage Sense Input. This input voltage is referenced to the SGND pin.

$INTV_{CC}$ (Pin 33): LTC3880: Internal Regulator 5V Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

$EXTV_{CC}$ (Pin 33): LTC3880-1: External Regulator 5V input. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

PGND (Pin 34): Power Ground Pin. Connect this pin closely to the sources of the bottom N-channel MOSFETs, the (–) terminal of C_{VCC} and the (–) terminal of C_{IN}.

V_{IN} (Pin 35): LTC3880: Main Input Supply. Decouple this pin to PGND with a capacitor (0.1µF to 1µF). For applications where the main input power is 5V, tie the V_{IN} and $INTV_{CC}$ pins together. LTC3880-1: Input Voltage Sense. Should be connected to the external power MOSFET supply.

BG0/BG1 (Pin 36/Pin 32): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-Channel MOSFETs between PGND and $INTV_{CC}$.

BOOST0/BOOST1 (Pin 37/Pin 31): Boosted Floating Driver Supplies. The (+) terminal of the booststrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

TG0/TG1 (Pin 38/Pin 30): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltages.

SW0/SW1 (Pin 39/Pin 29): Switch Node Connections to Inductors. Voltage swings at the pins are from a Schottky diode (external) voltage drop below ground to V_{IN}.

TSNS0/TSNS1 (Pin 40/Pin 28): Channel 0,1 External Diode Temperature Sense. Connect to the anode of a diode connected PNP transistor and star connect the cathode to SGND in order to sense remote temperature. If external temperature sense elements are not installed, short pin to ground and set the UT_FAULT_LIMIT to –275°C, IOUT_CAL_GAIN_TC set to zero and the UT_FAULT_RESPONSE to ignore.

SGND (Exposed Pad Pin 41): Signal Ground. All small-signal and compensation components should connect to this ground, which in turn connects to PGND at one point.

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BLOCK DIAGRAM (One of two channels (CH0) shown)

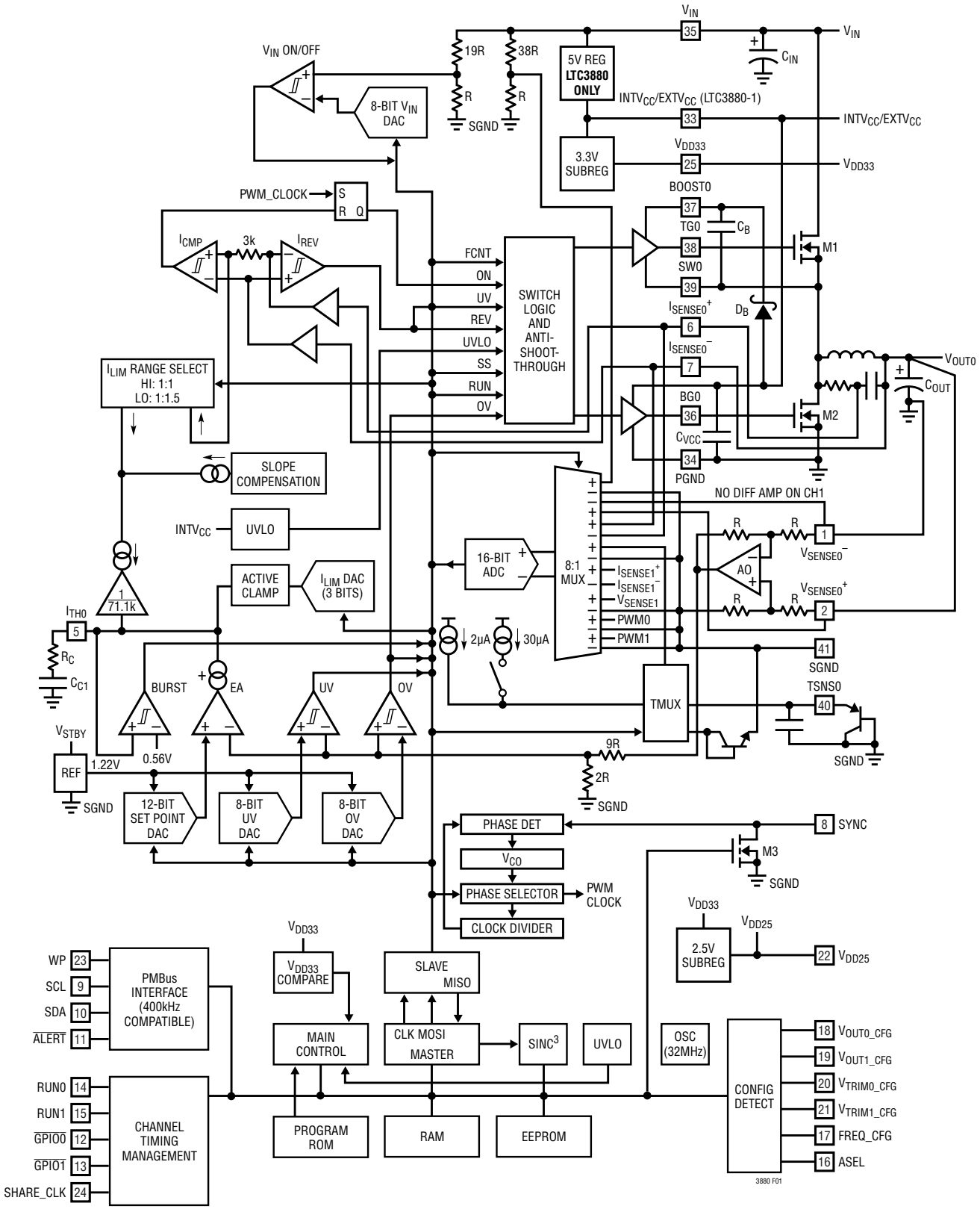

Figure 1. Block Diagram

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OPERATION

OVERVIEW

The LTC3880 is a dual channel/dual phase, constant frequency, analog current mode controller for DC/DC step-down applications with a digital interface. The LTC3880 digital interface is compatible with PMBus which supports bus speeds of up to 400kHz. A typical application circuit is shown on the first page of this data sheet.

Major features include:

- Programmable Output Voltage
- Programmable Input Voltage Comparator
- Programmable Current Limit
- Programmable Switching Frequency
- Programmable OV and UV Comparators
- Programmable On and Off Delay Times
- Programmable Output Rise/Fall Times
- Phase-Locked Loop for Synchronous, Polyphase Operation (2, 3, 4 or 6 Phases)
- Input and Output Voltage/Current, Temperature and Duty Cycle Telemetry
- Fully Differential Load Sense
- Integrated Gate Drivers
- Non-Volatile Configuration Memory with ECC
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time-Base Interconnect for Synchronization Between Multiple Controllers
- Fault Logging
- WP Pin to Protect Internal Configuration
- Standalone Operation After User Factory Configuration
- PMBus, 400kHz Compliant Interface

The PMBus interface provides access to important power management data during system operation including:

- Internal Controller Temperature
- External System Temperature via Optional Diode Sense Elements
- Average Output Current
- Average PWM Duty Cycle
- Average Output Voltage
- Average Input Voltage
- Average Input Current
- Configurable, Latched and Unlatched Individual Fault and Warning Status

Individual channels are accessed through the PMBus using the PAGE command, i.e., PAGE 0 or 1.

Fault reporting and shutdown behavior are fully configurable. Two individual $\overline{\text{GPIO}}$ outputs are provided ($\overline{\text{GPIO0}}$, $\overline{\text{GPIO1}}$), both of which can be masked independently. A dedicated pin for $\overline{\text{ALERT}}$ is provided. The shutdown operation also allows all faults to be individually masked and can be operated in either unlatched (hiccup) or latched modes.

Individual status commands enable fault reporting over the serial bus to identify the specific fault event. Fault or warning detection includes the following:

- Output Undervoltage/Overvoltage
- Input Undervoltage/Overvoltage
- Input and Output Overcurrent
- Internal Overtemperature
- External Overtemperature
- Communication, Memory or Logic (CML) Fault

MAIN CONTROL LOOP

The LTC3880 is a constant frequency, current mode step-down controller containing two channels operating with various user-defined relative phasing. During normal operation each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin which is the output of each error amplifier, EA. The EA negative terminal is equal to the V_{SENSE} voltage divided by 5.5 (2.75 if range = 1). The positive terminal of the EA is

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OPERATION

connected to the output of a 12-bit DAC with values ranging from 0V to 1.024V. The output voltage, through feedback of the EA, will be regulated to 5.5 times the DAC output (2.75 times if range = 1). The DAC value is calculated by the part to synthesize the users desired output voltage. The output voltage is programmed by the user either with the resistor configuration pins detailed in Tables 12 and 13 or by the V_{OUT} command (either from NVM or by PMBus command). Refer to the PMBus command section of the data sheet or the PMBus specification for more details. The output voltage can be modified by the user at any time with a PMBus VOUT_COMMAND. This command will typically have a latency less than 10ms. The user is encouraged to reference the PMBus Power System Management Protocol Specification to understand how to program the LTC3880. This specification can be found at http://www.pmbus.org/specs.html.

Continuing the basic operation description, the current mode controller will turn off the top gate when the peak current is reached. If the load current increases, V_{SENSE} will slightly droop with respect to the DAC reference. This causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on. In continuous conduction mode, the bottom MOSFET stays on until the end of the switching cycle.

EEPROM

The LTC3880 contains internal EEPROM with Error Correction Coding (ECC) or NVM (nonvolatile memory) to store configuration settings and fault log information. EEPROM endurance retention and mass write operation time are specified in the Electrical Characteristics and Absolute Maximum Ratings sections. Write operations above T_J = 85°C are possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded. Read operations performed at temperatures between 85°C and 125°C will not degrade the EEPROM. Writing to the EEPROM above 85°C will result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 85°C, the slight degradation in the data retention characteristics of the fault log will not take away from the usefulness of the function.

It is recommended that the EEPROM not be written when the die temperature is greater than 85°C. If the die temperature exceeds 130°C, the LTC3880 will disable all EEPROM write operations. All EEPROM write operations will be re-enabled when the die temperature drops below 125°C. (The controller will also disable when the die temperature exceeds the internal overtemperature fault limit 160°C with a 10°C hysteresis)

The degradation in EEPROM retention for temperatures >125°C can be approximated by calculating the dimensionless acceleration factor using the following equation:

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

K = $8.617 \bullet 10^{-5}$ eV/°K

T_{USE} = 125°C specified junction temperature

T_{STRESS} = actual junction temperature in °C

Example: Calculate the effect on retention when operating at a junction temperature of 135°C for 10 hours.

T_{STRESS} = 130°C

T_{USE} = 125°C

$AF = e^{[(1.4/8.617 \bullet 10^{-5}) \bullet (1/398 - 1/403)]} = 1.66$

The equivalent operating time at 125°C = 16.6 hours.

Thus the overall retention of the EEPROM was degraded by 16.6 hours as a result of operating at a junction temperature of 130°C for 10 hours. The effect of the overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a maximum junction temperature of 125°C.

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OPERATION

POWER UP AND INITIALIZATION

The LTC3880 is designed to provide standalone supply sequencing and controlled turn-on and turn-off operation. It operates from a single input supply (4.5V to 24V) while three on-chip linear regulators generate internal 2.5V, 3.3V and 5V. If V_{IN} is below 6V, the $INTV_{CC}$ and V_{IN} pins must be tied together. The controller configuration is initialized by an internal threshold based UVLO where V_{IN} must be approximately 4V and the 5V, 3.3V and 2.5V linear regulators must be within approximately 20% of the regulated values. The LTC3880-1 does not have an internal 5V linear regulators. The $EXTV_{CC}$ pin is driven by an external regulator to improve efficiency of the circuit and minimize power on the LTC3880. The $EXTV_{CC}$ pin must exceed approximately 4V before the internal UVLO is exceeded. To minimize application power, the $EXTV_{CC}$ pin can be supplied by a switching regulator.

During initialization, the external configuration resistors are identified and/or contents of the NVM are read into the controller's commands. The $\overline{GPIO}n$ pins are in high impedance (Hi-Z) mode. The TG*n*, BG*n* and RUN*n* pins are held low. The LTC3880 will use the contents of Tables 12 to 15 to determine the resistor defined parameters. See the Resistor Configuration section for more detail. The resistor configuration pins only control some of the preset values of the controller. The remaining values are programmed in NVM either at the factory or by the user.

If the configuration resistors are not inserted or if the ignore RCONFIG bit is asserted (bit 6 of the MFR_CONFIG_ALL_LTC3880 configuration command), the LTC3880 will use only the contents of NVM to determine the DC/DC characteristics. The ASEL value read at power-up or reset is always respected unless the pin is open. The ASEL will use the MSB from NVM and the LSB from the detected threshold. See the Applications Information section for more detail.

After the part has initialized, an additional comparator monitors V_{IN}. The VIN_ON threshold must be exceeded before the output power sequencing can begin. After V_{IN} is initially applied, the part will typically require 120ms to initialize and begin the TON_DELAY timer. The readback of voltages and currents may require an additional 90ms.

SOFT-START

The part must enter the run state prior to soft-start. The run pins are released by the LTC3880 after the part initializes and V_{IN} is greater than the VIN_ON threshold. If multiple LTC3880s are used in an application, they all hold their respective run pins low until all devices initialize and V_{IN} exceeds the VIN_ON threshold for every device. The SHARE_CLK pin assures all the devices connected to the signal use the same time base. The SHARE_CLK pin is held low until the part has initialized after V_{IN} is applied. The LTC3880 can be set to turn off (or remain off) if SHARE_CLK is low (set bit 2 of MFR_CHAN_CONFIG_LTC3880 to a 1). This allows the user to assure synchronization across numerous LTC ICs even if the RUN pins can not be connected together due to board constraints. In general, if the user cares about synchronization between chips it is best to connect all the respective RUN pins together and to connect all the respective SHARE_CLK pins together. This assures all chips begin sequencing at the same time and use the same time base.

After the RUN pin releases and prior to entering a constant output voltage regulation state, the LTC3880 performs a monotonic initial ramp or "soft-start". Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set-point. Once the LTC3880 is commanded to turn on, (after power up and initialization) the controller waits for the user specified turn-on delay (TON_DELAY) prior to initiating this output voltage ramp. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting the value of TON_RISE to any value less than 0.25ms. The LTC3880 PWM always uses discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom gate is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a pre-biased load. When the TON_MAX_FAULT_LIMIT is reached, the part transitions to continuous mode or burst, if so programmed. If TON_MAX_FAULT_LIMIT is set to zero, there is no time limit and the part transitions to the desired conduction mode after TON_RISE completes and V_{OUT} has exceeded

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OPERATION

the VOUT_UV_FAULT_LIMIT and IOUT_OC is not present. Setting TON_MAX_FAULT_LIMIT to a value of 0 is not recommended. This described method of start-up sequencing is time based.

SEQUENCING

The default mode for sequencing the outputs on and off is time based. Each output is enabled after waiting TON_DELAY amount of time following either a RUN pin going high, a PMBus command to turn on or the V_{IN} rising above a preprogrammed voltage. Off sequencing is handled in a similar way. To assure proper sequencing, make sure all ICs connect the SHARE_CLK pin together and RUN pins together. If the RUN pins can not be connected together for some reason, set bit 2 of MFR_CHAN_CONFIG_LTC3880 to a 1. This bit requires the SHARE_CLK pin to be clocking before the power supply output can start. When the RUN pin is pulled low, the LTC3880 will hold the pin low for the MFR_RESTART_DELAY. The minimum MFR_RESTART_DELAY is TOFF_DELAY + TOFF_FALL + 136ms. This delay assures proper sequencing of all rails. The LTC3880 calculates this delay internally and will not process a shorter delay. However, a longer commanded MFR_RESTART_DELAY will be used by the part. The maximum allowed value is 65.52 seconds.

VOLTAGE-BASED SEQUENCING

The $\overline{\text{GPIO}}n$ pins can be asserted when the UV threshold is exceeded for each output. It is possible to feed the $\overline{\text{GPIO}}$ pin from one output into the RUN pin of the next output

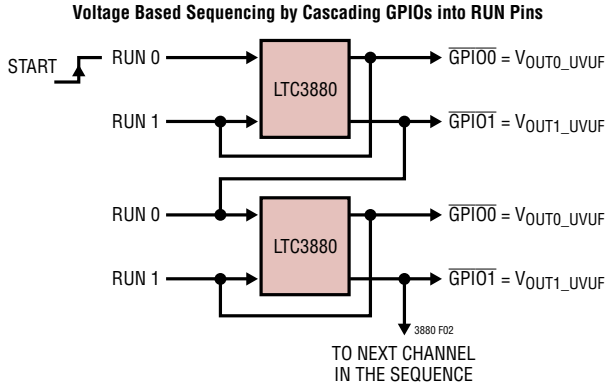

Figure 2. Event (Voltage) Based Sequencing

in the sequence. To use the $\overline{\text{GPIO}}n$ pin for voltage based sequencing, set bit 12 of the MFR_GPIO*n*_PROPAGATE command = 1. Bit 12 is the VOUT_UVUF (PGOOD) which is the unfiltered VOUT_UV comparator. Using the unfiltered VOUT_UV fault limit is recommended because there is little appreciable time delay between the comparator crossing the UV threshold and the $\overline{\text{GPIO}}$ pin releasing This can be implemented across multiple LTC3880s. The VOUT_UVUF (PGOOD) has a 70µs filter. If the V_{OUT} voltage bounces around the UV threshold for a long period of time it is possible for the $\overline{\text{GPIO}}$ output to toggle more than once. To minimize this problem, set the TON_RISE time under 100ms. If a fault in the string of rails is detected, only the faulted rail and downstream rails will fault off. The rails in the string of devices in front of the faulted rail will remain on unless commanded off.

SHUTDOWN

The LTC3880 supports two shutdown modes. The first mode is closed-loop shutdown response, with user-defined turn-off delay (TOFF_DELAY) and ramp down rate (TOFF_FALL). The controller will maintain the mode of operation for TOFF_FALL. In discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current.

The other shutdown mode occurs in response to a fault condition or loss of SHARE_CLK (if bit 2 of MFR_CHAN_CONFIG_LTC3880 is set to a 1) or V_{IN} falling below the VIN_OFF threshold or $\overline{\text{GPIO}}$ pulled low externally (if the MFR_GPIO_RESPONSE is set to inhibit). Under these conditions the power stage is disabled in order to stop the transfer of energy to the load as quickly as possible. The shutdown state can be entered from the soft-start or active regulation states either through user intervention (deasserting RUN*n* or the PMBus OPERATION command) or in response to a detected fault or an external fault via the bidirectional $\overline{\text{GPIO}}n$ pins, or loss of SHARE_CLK (if bit 2 of MFR_CHAN_CONFIG_LTC3880 is set to a 1) or V_{IN} falling below the VIN_OFF threshold.

In hiccup mode, the controller responds to a fault by shutting down and entering the inactive state for a programmable delay time (MFR_RETRY_DELAY).

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OPERATION

This delay minimizes the duty cycle associated with autonomous retries if the fault that caused the shutdown disappears once the output is disabled. The retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If multiple outputs are controlled by the same $\overline{GPIO}$ pin, the decay time of the faulted output determines the retry delay. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG_LTC3880. Alternatively, the controller can be configured so that it remains latched-off following a fault and clearing requires user intervention such as toggling RUN*n* or commanding the part OFF then ON.

LIGHT LOAD CURRENT OPERATION

The LTC3880 has three modes of operation including high efficiency Burst Mode operation, discontinuous conduction mode or forced continuous conduction mode. Mode selection is done using the MFR_PWM_MODE_LTC3880 command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

In Burst Mode operation the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below approximately 0.5V, the internal Burst Mode operation asserts and both external MOSFETs are turned off. In Burst Mode operation, the load current is supplied by the output capacitor. As the output voltage decreases, the EA output begins to rise. When the output voltage drops sufficiently, Burst Mode operation is deasserted, and the controller resumes normal operation by turning on the top external MOSFET on the next PWM cycle.

If a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom gate external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller can operate in discontinuous operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry. Forced continuous conduction mode may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this and turn off the offending channel. However, this fault is based on an ADC read and can take up to 90ms to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction or Burst Mode operation.

If the part is set to Burst Mode operation, as the inductor average current increases, the controller will automatically modify the operation from Burst Mode operation, to discontinuous mode to continuous mode.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the LTC3880's controller can be established with internal clock references or with an external time-base. The LTC3880 can be configured for an external clock input through the programmed value in NVM, a PMBus command or setting the R_{BOTTOM} resistor of the FREQ_CFG pin to 0Ω and the R_{TOP} to open. The PMBus command FREQUENCY_SWITCH is set to external clock. The MFR_PWM_CONFIG_LTC3880 command determines the relative phasing. Using the RCONFIG input, channel 0 and channel 1 have a relative phasing of 0° and 180° with respect to the falling edge of SYNC. The master should be selected to be out of phase with the slave. Both RUN pins must be low or both channels commanded off before the FREQUENCY and MFR_PWM_CONFIG_LTC3880 commands can be written to the LTC3880. The relative phasing of all devices in a PolyPhase rail should be optimally phased. The relative phasing of each rail is 360/n where n is the number of phases in the rail.

If the LTC3880 is configured as the oscillator output on SYNC, the switching frequency source can be selected with

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OPERATION

either external configuration resistors or through serial bus programming. The FREQ_CFG configuration resistor pin can be used to select the FREQUENCY_SWITCH and MFR_PWM_CONFIG_LTC3880 values as outlined in Table 14. Otherwise, the FREQUENCY_SWITCH and MFR_PWM_CONFIG_LTC3880 PMBus commands can be used to select PWM switching frequency and the PWM channel phase relationship. The phase and frequency relationships are completely independent of each other providing the numerous application options for the user. If the LTC3880 is configured to drive the SYNC pin using the programmed FREQUENCY_SWITCH command value, the SYNC pin will pull low at the desired clock rate with 500ns low pulse. Care must be taken in the application to assure the capacitance on SYNC is minimized to assure the pull-up resistor versus the capacitor load has a low enough time constant for the application. In addition, a phase-locked loop (PLL) is available to synchronize the internal oscillator to an external clock source that is connected to the SYNC pin. All phase relationships are between the falling edge of SYNC and the rising edge of the LTC3880 TG outputs. Multiple LTC3880s can be synchronized in order to realize PolyPhase arrays.

OUTPUT VOLTAGE SENSING

The channel 0 differential amplifier allows remote, differential sensing of the load voltage with $V_{SENSE0n}$ pins. The channel 1 sense pin (V_{SENSE1}) is referenced to SGND. The telemetry ADC is fully differential and makes measurements of channels 0 and 1 output voltages at the $V_{SENSE0n}$ and V_{SENSE1}/SGND pins, respectively. Due to head room limitations of the internal amplifier for V_{SENSE0}, the maximum allowed differential sense voltage is 4.096V.

CURRENT SENSING

For DCR current sense applications, a resistor in series with a capacitor is placed across the inductor. In this configuration, the resistor is tied to the FET side of the inductor while the capacitor is tied to the load side of the inductor as shown in Figure 3. If the RC values are chosen such that the RC time constant matches the inductor time constant (L/DCR, where DCR is the inductor series resistance), the resultant voltage (V_{DCR}) appearing across the capacitor will equal the voltage across the inductor series resistance and thus represent the current flowing through the inductor. The RC calculations are based on the room temperature DCR of the inductor.

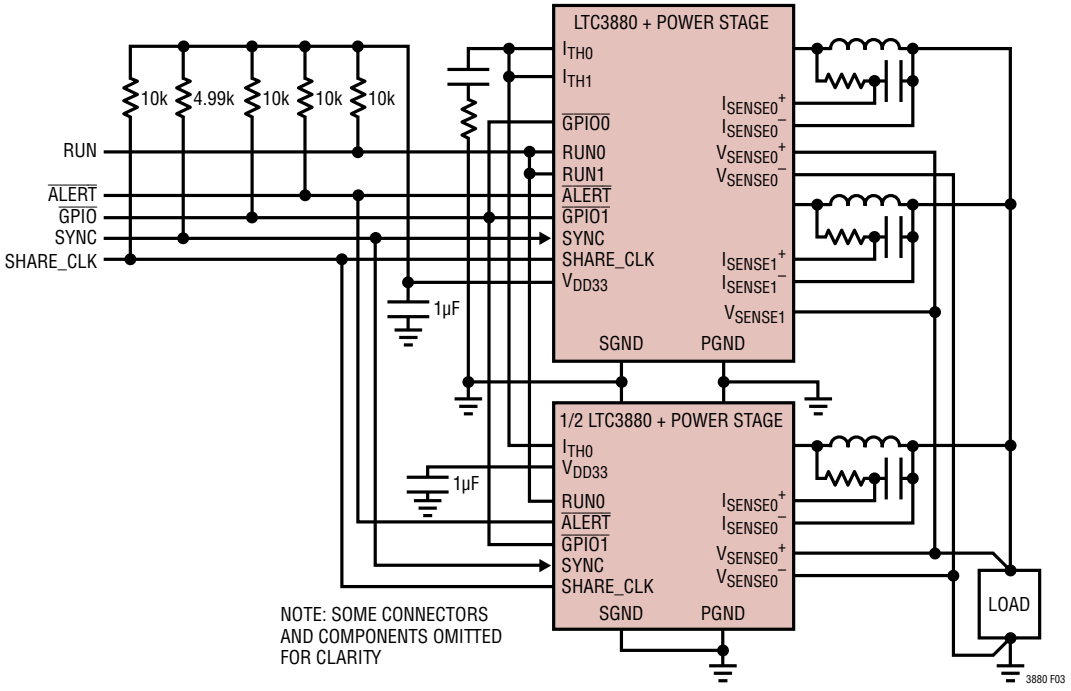

Figure 3. Load Sharing Connections for 3-Phase Operation

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The RC time constant should remain constant, as a function of temperature. This assures the transient response of the circuit is the same regardless of the temperature. The DCR of the inductor has a large temperature coefficient, approximately 3900ppm/°C. The temperature coefficient of the inductor must be written to the MFR_IOUT_CAL_GAIN_TC register. The external temperature is sensed near the inductor and used to modify the internal current limit circuit to maintain an essentially constant current limit with temperature. In this application, the I_{SENSEn}^{+} pin is connected to the FET side of the capacitor while the I_{SENSEn}^{-} pin is placed on the load side of the capacitor. The current sensed from the input is then given by the expression V_{DCR}/DCR. V_{DCR} is digitized by the LTC3880's telemetry ADC with an input range of ±128mV, a noise floor of 7μV_{RMS}, and a peak-peak noise of approximately 46.5µV. The LTC3880 computes the inductor current using the DCR value stored in the IOUT_CAL_GAIN command and the temperature coefficient stored in command MFR_IOUT_CAL_GAIN_TC. The resulting current value is returned by the READ_IOUT command.

LOAD SHARING

Multiple LTC3880's can be arrayed in order to provide a balanced load-share solution by bussing the necessary pins. Figure 3 illustrates the shared connections required for load sharing.

The frequency must only be programmed on one of the LTC3880s. The other(s) must be programmed to External Clock.

EXTERNAL/INTERNAL TEMPERATURE SENSE

External temperature can be best measured using a remote diode-connected PNP transistor such as the MMBT3906. The emitter should be connected to the TSNS*n* pin while the base and collector terminals of the PNP transistor should be returned to the LTC3880's SGND pin, preferably using a star connection. It is possible to connect the collector of the PNP to the source of the bottom MOSFET. This may optimize board layout allowing the PNP closer proximity to the power FETs. The base of the PNP must still be tied to signal ground. For best noise immunity, the connections should be routed differentially and a 10nF capacitor should be placed in parallel with the diode connected PNP. Two different currents are applied to the diode (nominally 2µA and 32µA) and the temperature is calculated from the ΔV_{BE} measurement. The external transistor temperature is digitized by the telemetry ADC, and the value is returned by the PMBus READ_TEMPERATURE_1 (Ch*n*) command.

The READ_TEMPERATURE_2 command returns the junction temperature of the LTC3880 using an on-chip diode. The slope of the external temperature sensor can be modified with the temperature slope coefficient stored in MFR_TEMP_1_GAIN. Typical PNPs require temperature slope adjustments slightly less than 1. The MMBT3906 has a recommended value in this command of approximately MFR_TEMP_1_GAIN = 0.991 based on the ideality factor of 1.01. Simply invert the ideality factor to calculate the MFR_TEMP_1_GAIN. Different manufacturers and different lots may have different ideality factors. Consult with the manufacturer to set this value.

The offset of the external temperature sense can be adjusted by MFR_TEMP_1_OFFSET. A value of 0 in this register sets the temperature offset to –273.15°C.

If the PNP cannot be placed in direct contact with the inductor, the slope or offset can be increased to account for temperature mismatches. If the user is adjusting the slope, the intercept point is at absolute zero, –273.15°C, so small adjustments in slope can change the apparent measured temperature significantly. Another way to artificially increase the slope of the temperature term is to increase the MFR_IOUT_CAL_GAIN_TC term. This will modify the temperature slope with respect to room temperature.

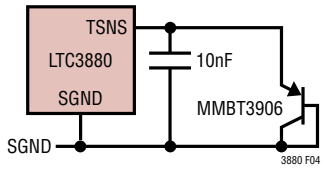

Figure 4. Temperature Sense Circuit

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OPERATION

RCONFIG (RESISTOR CONFIGURATION) PINS

There are six input pins utilizing 1% resistor dividers between V_{DD25} and SGND to select key operating parameters. The pins are ASEL, FREQ_CFG, V_{OUT0_CFG}, V_{OUT1_CFG}, V_{TRIM0_CFG} and V_{TRIM1_CFG}. If pins are floated, the value stored in the corresponding NVM command is used. If bit 6 of the MFR_CONFIG_ALL_LTC3880 configuration command is asserted in NVM, the resistor inputs are ignored upon power-up except for ASEL which is always respected. The resistor configuration pins are only measured during a power-up reset or after an MFR_RESET command is executed.

The V_{OUTn_CFG} and V_{TRIMn} pin settings are described in Tables 12 and 13. These pins select the output voltages for the LTC3880's analog PWM controllers. If both pins are open, the VOUT_COMMAND command is loaded from NVM to determine the output voltage.

The following parameters are set as a percentage of the output voltage if the RCONFIG pins are used to determined output voltage:

- VOUT_OV_FAULT_LIMIT ..... +10%
- VOUT_OV_WARN ..... +7.5%
- VOUT_MAX ..... +7.5%
- VOUT_MARGIN_HI ..... +5%
- POWER_GOOD_ON ..... –7%
- POWER_GOOD_OFF ..... –8%
- VOUT_MARGIN_LO ..... –5%
- VOUT_UV_WARN ..... –6.5%
- VOUT_UV_FAULT_LIMIT ..... –7%

The FREQ_CFG pin settings are described in Table 14. This pin selects the switching frequency and phase relationships between the two channels and SYNC pin. To synchronize to an external clock, the part must be put into external clock mode (FREQ_CFG pin shorted to ground). If no external clock is supplied, the part will clock at the lowest free-running frequency of the internal PWM oscillator. This low clock rate will increase the ripple current of the inductor possibly producing undesirable operation. If the external SYNC signal is missing or misbehaving, a "PLL Lock Status" fault will be indicated in the STATUS_MFR_SPECIFIC command. If the user does not wish to see the PLL_FAULT even if there is not a valid synchronization signal at power up, bit 3 of the MFR_CONFIG_ALL_LTC3880 command must be asserted. If the SYNC pin is connected between multiple ICs only one of the ICs can be the oscillator, all other ICs must be configured to external clock.

The ASEL pin settings are described in Table 15. This pin selects the bottom 4 bits of the slave address for the LTC3880. The 3 most significant bits are retrieved from the NVM MFR_ADDRESS command. If the pin is floating, the 7-bit value stored in NVM MFR_ADDRESS command is used to determine the slave address. For more detail, refer to Table 15a.

Note: Per the PMBus specification, pin programmed parameters can be overridden by commands from the digital interface with the exception of ASEL which is always honored. Do not set any part address to 0x5A or 0x5B because these are global addresses and all parts will respond to them.

FAULT DETECTION AND HANDLING

A variety of fault and warning reporting and handling mechanisms are available. Fault and warning detection capabilities include:

- Input OV/FAULT Protection and UV Warning
- Average Input OC Warn
- Output OV/UV Fault and Warn Protection
- Output OC Fault and Warn Protection
- Internal and External Overtemperature Fault Protection
- External Undertemperature Fault and Warn Protection
- CML Fault (Communication, Memory or Logic)
- External Fault Detection via the Bidirectional $\overline{GPIO}n$ Pins.

In addition, the LTC3880 can map any combination of fault indicators to their respective $\overline{GPIO}n$ pin using the propagate $\overline{GPIO}n$ response commands, MFR_GPIO_PROPAGATE_LTC3880. Typical usage of a $\overline{GPIO}$ pin is as a driver for an external crowbar device, overtemperature alert, overvoltage alert or as an interrupt to cause a microcontroller to poll the fault commands. Alternatively, the $\overline{GPIO}n$ pins can be used as inputs to detect external faults downstream of the controller that require an immediate response. The $\overline{GPIO0}$ and/or

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$\overline{\text{GPIO1}}$ pins can also be configured as power good outputs (by asserting bit 12 of MFR_GPIO_PROPAGATE_LTC3880). Power good indicates the controller output is above the UV threshold. At power-up the pin will initially be three-state. Traditionally PGOOD also includes the OV threshold. Assert bit 0 of MFR_GPIO_PROPAGATE_LTC3880 if this is desired. If it is necessary to have the desired polarity on the pin at power-up in this configuration, attach a Schottky diode between the RUN pin of the propagated power good signal and the $\overline{\text{GPIO}}$ pin. The Cathode must be attached to RUN and the Anode to the $\overline{\text{GPIO}}$ pin. If the $\overline{\text{GPIO}}$ pin is set to a power good status, the MFR_GPIO_RESPONSE must be ignore otherwise there is a latched off condition with the controller.

As described in the Soft-Start section, it is possible to control start-up through concatenated events. If $\overline{\text{GPIO}}n$ is used to drive the RUN pin of another controller, the unfiltered VOUT_UV fault limit (PGOOD) should be mapped to the $\overline{\text{GPIO}}$ pin.

Any fault or warning event will cause the $\overline{\text{ALERT}}$ pin to assert low. The pin will remain asserted low until the CLEAR_FAULTS command is issued, the fault bit is written to a 1 or bias power is cycled or a MFR_RESET command is issued. Channel specific faults are cleared if the RUN pins are toggled OFF/ON or the part is commanded OFF/ON via PMBus. If bit 0 of MFR_CONFIG_ALL_LTC3880 is set to a 1, toggling the RUN pins OFF/ON clears all faults. The MFR_GPIO_PROPAGATE_LTC3880 command determines if the $\overline{\text{GPIO}}$ pins are pulled low when a fault is detected; however, the $\overline{\text{ALERT}}$ pin is always pulled low if a fault or warning is detected and the status bits are updated.

Output and input fault event handling is controlled by the corresponding fault response byte as specified in Tables 5 to 9. Shutdown recovery from these types of faults can either be autonomous or latched. For autonomous recovery, the faults are not latched, so if the fault condition is not present after the retry interval has elapsed, a new soft-start is attempted. If the fault persists, the controller will continue to retry. The retry interval is specified by the MFR_RETRY_DELAY command and prevents damage to the regulator components by repetitive power cycling, assuming the fault condition itself is not immediately destructive. The MFR_RETRY_DELAY must be greater than 120ms. It can not exceed 83.88 seconds.

Channel-to-channel fault dependencies can be created by connecting $\overline{\text{GPIO}}n$ pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed $\overline{\text{GPIO}}n$ pins low. The other channels are then configured to shut down when the $\overline{\text{GPIO}}n$ pins are pulled low. For autonomous group retry, the faulted channel is configured to let go of the $\overline{\text{GPIO}}n$ pin(s) after a retry interval, assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence. If the fault response is LATCH_OFF, the $\overline{\text{GPIO}}$ pin remains asserted low until either the RUN pin is toggled OFF/ON or the part is commanded OFF/ON. The toggling of the RUN either by the pin or OFF/ON command will clear faults associated with the channel. If it is desired to have all faults cleared when either RUN pin is toggled, set bit 0 of MFR_CONFIG_ALL_LTC3880 to a 1.

The status of all faults and warnings is summarized in the STATUS_WORD and STATUS_BYTE commands.

Additional fault detection and handling capabilities are:

Internal Memory with CRC and ECC

The LTC3880 contains internal EEPROM with error correction coding (ECC) to store user configuration settings and fault log information. EEPROM endurance and retention for user space and fault log pages are specified in the Absolute Maximum Ratings and Electrical Characteristics table.

The integrity of the NVM memory is checked with a CRC calculation each time its data is to be read, such as after a power-on reset. A CRC failure will prevent the controller from leaving the inactive state. If a CRC failure occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$ and RUN pins will be pulled low. At that point, the device will respond at special address 0x7C, which is only activated after an invalid CRC has been detected. The chip will also respond to global addresses 0x5A and 0x5B, but all LTC PSM chips will respond to these addresses so users must be careful when using global addresses. NVM repair can be attempted

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by writing the desired configuration to the controller and executing a STORE_USER_ALL command followed by a CLEAR_FAULTS command. Contact the factory if EEPROM repair is unsuccessful.

See the Applications Information section or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming, which the LTC3880 also supports.

SERIAL INTERFACE

The LTC3880 serial interface is a PMBus compliant slave device and can operate at any frequency between 10kHz and 400kHz. The address is configurable using either the NVM or an external resistor divider. In addition the LTC3880 always responds to the global broadcast address of 0x5A (7 bit) or 0x5B (7 bit). Address 0x5A is not paged and is performed on both channels. 0x5B respects the page command. Because address 0x5A does not support page, it can not be used for any paged reading commands.

The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte, 6) read word and 7) read block. All read operations will return a valid PEC if the PMBus master requests it. If the PEC_REQUIRED bit is set in the MFR_CONFIG_ALL_LTC3880 command, the PMBus write operations will not be acted upon until a valid PEC has been received by the LTC3880.

Communication Failure

PEC write errors (if PEC_REQUIRED is active), attempts to access unsupported commands, or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_CML command, and the $\overline{\text{ALERT}}$ pin is pulled low.

DEVICE ADDRESSING

The LTC3880 offers five different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) channel, 4) rail addressing and 5) alert response address (ARA).

Global addressing provides a means of the PMBus master to address all LTC3880 devices on the bus. The LTC3880 global address is fixed 0x5A (7 bit) or 0xB4 (8 bit) and cannot be disabled. Commands sent to the global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global command 0x5B (7 bit) or 0xB6 (8 bit) is paged and allows channel specific command of all LTC3880 devices on the bus.

Device addressing provides the standard means of the PMBus master communicating with a single instance of an LTC3880. The value of the device address is set by a combination of the ASEL configuration pin and the MFR_ADDRESS command. When this addressing means is used, the PAGE command determines the channel being acted upon. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS.

Channel addressing provides a means for the PMBus master addressing a single channel of the LTC3880 without using the PAGE command. The value assigned to the paged MFR_CHANNEL_ADDRESS determines the specific channel the user wishes to act upon. Example: If MFR_CHANNEL_ADDRESS for page 0 is set to 0x57 and the MFR_CHANNEL_ADDRESS for page 1 is set to 0x54, the user can address channel 0 of the device by performing PMBus device commands using address 0x57 (7 bit). The user can address channel 1 of the device by performing PMBus device commands using address 0x54 (7 bit). This eliminates the user from first assigning the PAGE command and then the command to be acted upon.

Rail addressing provides a means for the PMBus master addressing a set of channels connected to the same output rail, simultaneously. This is similar to global addressing, however, the PMBus address can be dynamically assigned by using the MFR_RAIL_ADDRESS command. The MFR_RAIL_ADDRESS is paged, so channels can be independently assigned to a specific rail. It is recommended that rail addressing should be limited to command write operations.

All five means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts.

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OPERATION

RESPONSES TO V_{OUT} AND I_{OUT} FAULTS

V_{OUT} OV and UV conditions are monitored by comparators. The OV and UV limits are set in three ways.

- As a Percentage of the V_{OUT} if Using the Resistor Configuration Pins
- In NVM if Either Programmed at the Factory or Through the GUI
- By PMBus Command

The I_{IN} and I_{OUT} overcurrent monitors are performed by ADC readings and calculations. Thus these values are based on average currents and can have a time latency of up to 90ms. The I_{OUT} calculation accounts for the sense resistor and the temperature coefficient of the resistor. The input current is equal to the sum of output current times the respective channel duty cycle plus the input offset current for each channel. If this calculated input current exceed the IN_OC_WARN_LIMIT the $\overline{\text{ALERT}}$ pin is pulled low and the IIN_OC_WARN bit is asserted in the STATUS_INPUT register.

The digital processor within the LTC3880 provides the ability to ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). The retry interval is set in MFR_RETRY_DELAY and can be from 120ms to 83.88 seconds in 1ms increments. The shutdown for OV/UV and OC can be done immediately or after a user selectable deglitch time.

Output Overvoltage Fault Response

A programmable overvoltage comparator (OV) guards against transient overshoots as well as long-term overvoltages at the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared *regardless of the PMBus VOUT_OV_FAULT_RESPONSE command byte value.* This hardware level fault response delay is typically 2µs from the overvoltage condition to BG asserted high. Using the VOUT_OV_FAULT_RESPONSE command, the user can select any of the following behaviors:

- OV Pull-Down Only (OV cannot be ignored)
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Either the Latch Off or Retry fault responses can be deglitched in increments of (0-7) • 10µs. See Table 5.

Output Undervoltage Response

The response to an undervoltage comparator output can be either:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

The UV responses can be deglitched. See Table 6.

Peak Output Overcurrent Fault Response

Due to the current mode control algorithm, peak output current across the inductor is always limited on a cycle by cycle basis. The value of the peak current limit is specified in sense voltage in the EC table. The current limit circuit operates by limiting the I_{TH} maximum voltage. If DCR sensing is used, the I_{TH} maximum voltage has a temperature dependency directly proportional to the TC of the DCR of the inductor. The LTC3880 automatically monitors the external temperature sensors and modifies the maximum allowed I_{TH} to compensate for this term.

The overcurrent fault processing circuitry can execute the following behaviors:

- Current Limit Indefinitely
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

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OPERATION

The overcurrent responses can be deglitched in increments of (0-7) • 16ms. See Table 7

RESPONSES TO TIMING FAULTS

TON_MAX_FAULT_LIMIT is the time allowed for V_{OUT} to rise and settle at start-up. The TON_MAX_FAULT_LIMIT condition is predicated upon detection of the VOUT_UV_FAULT_LIMIT as the output is undergoing a SOFT_START sequence. The TON_MAX_FAULT_LIMIT time is started after TON_DELAY has been reached and a SOFT_START sequence is started. The resolution of the TON_MAX_FAULT_LIMIT is 10µs. If the VOUT_UV_FAULT_LIMIT is not reached within the TON_MAX_FAULT_LIMIT time, the response of this fault is determined by the value of the TON_MAX_FAULT_RESPONSE command value. This response may be one of the following:

- Ignore
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

This fault response is not deglitched. A value of 0 in TON_MAX_FAULT_LIMIT means the fault is ignored. The TON_MAX_FAULT_LIMIT should be set longer than the TON_RISE time. It is recommended TON_MAX_FAULT_LIMIT always be set to a non-zero value, otherwise the output may never come up and no flag will be set to the user.

See Table 9.

RESPONSES TO V_{IN} OV FAULTS

V_{IN} overvoltage is measured with the MUX'd ADC; therefore, the response is naturally deglitched by the 90ms typical response time of the ADC. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

See Table 9.

RESPONSES TO OT/UT FAULTS

Overtemperature Fault Response—Internal

An internal temperature sensor protects against NVM damage. Above 85°C, no writes to NVM are recommended. Above 130°C, the part disables the NVM and does not re-enable until the temperature has dropped to 120°C. Temperature is measured by the ADC. Internal temperature faults cannot be ignored. Internal temperature limits cannot be adjusted by the user.

See Table 9.

Overtemperature and Undertemperature Fault Response—Externals

Two external temperature sensors can be used to sense critical circuit elements like inductors and power MOSFETs. The OT_FAULT_RESPONSE and UT_FAULT_RESPOSE commands are used to determine the appropriate response to an overtemperature and undertemperature condition, respectively. If no external sense elements are used (not recommended) set the UT_FAULT_RESPONSE to ignore and set the UT_FAULT_LIMIT to –275°C.

The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

See Table 9.

RESPONSES TO EXTERNAL FAULTS

When either $\overline{GPIO}n$ pin is pulled low, the OTHER bit is set in the STATUS_WORD command, the appropriate bit is set in the STATUS_MFR_SPECIFC command, and the $\overline{ALERT}$ pin is pulled low. Responses are not deglitched. Each channel can be configured to ignore or shut down then retry in response to its $\overline{GPIO}n$ pin going low by modifying the MFR_GPIO_RESPONSE command. To avoid the $\overline{ALERT}$ pin asserting low when $\overline{GPIO}$ is pulled low, assert bit 1 of MFR_CHAN_CONFIG_LTC3880.

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OPERATION

FAULT LOGGING

The LTC3880 has fault logging capability. Data is logged into memory in the order shown in Table 11. The data to be stored in the fault log is being continuously stored in internal volatile memory. When a fault event occurs, the recording into internal volatile memory is halted, the fault log information is available from the MFR_FAULT_LOG command, and the contents of the internal memory are copied into NVM. Fault logging is allowed at temperatures above 85°C; however, retention of 10 years is not guaranteed. When the die temperature exceeds 130°C the fault logging is delayed until the die temperature drops below 120°C. After the fault condition that created the fault log event has been removed, clear the fault before the fault log data is erased, or else the part will immediately issue another fault log.

When the LTC3880 powers-up, it checks the NVM for a valid fault log. If a valid fault log exists in NVM, the "Valid Fault Log" bit in the STATUS_MFR_SPECIFIC command will be set and an $\overline{\text{ALERT}}$ event will be generated. Also, fault logging will be blocked until the LTC3880 has received a MFR_FAULT_LOG_CLEAR command before fault logging will be re-enabled.

The information is stored in EEPROM in the event of any fault that disables the controller on either channel. An external $\overline{\text{GPIO}}n$ pulling low will not trigger a fault logging event.

BUS TIMEOUT FAILURE

The LTC3880 implements a timeout feature to avoid hanging the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 25ms or the LTC3880 will three-state the bus and ignore the given data packet. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), all data bytes and the PEC byte if applicable.

The LTC3880 allows longer PMBus timeouts for block read data packets. This timeout is proportional to the length of the block read. The additional block read timeout applies primarily to the MFR_FAULT_LOG command. In no circumstances will the timeout period be less than the $t_{TIMEOUT_SMB}$ specification of 32ms (typical).

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTC3880 supports the full PMBus frequency range from 10kHz to 400kHz.

SIMILARITY BETWEEN PMBUS, SMBUS AND I²C 2-WIRE INTERFACE

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I²C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide time-outs to prevent bus hangs and optional packet error checking (PEC) to ensure data integrity. In general, a master device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general purpose I²C controller is used, check that repeat start is supported.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: Paragraph 5: Transport.

For a description of the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I²C.

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OPERATION

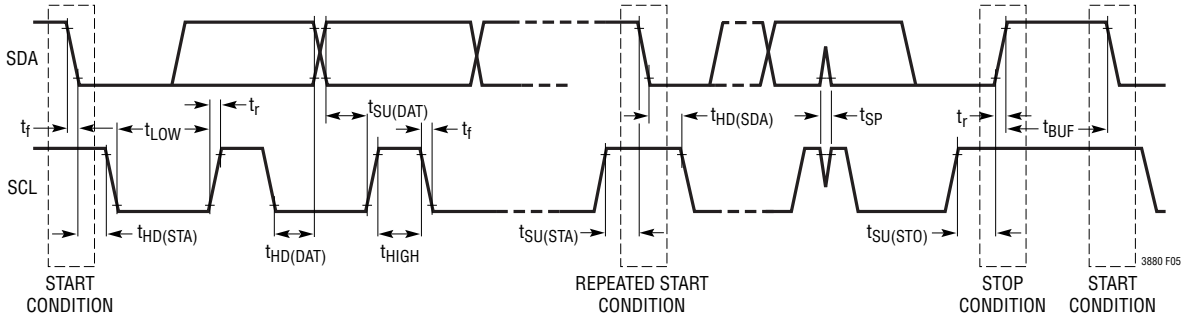


Figure 5. Timing Diagram

PMBUS SERIAL DIGITAL INTERFACE

The LTC3880 communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram, Figure 5, shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC3880 is a slave device. The master can communicate with the LTC3880 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following PMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 7-16 illustrate the aforementioned PMBus protocols. All transactions support PEC (parity error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended when reading the fault log.

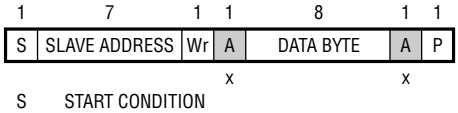
Figure 6 is a key to the protocol diagrams in this section. PEC is optional.

A value shown below a field in the following figures is a mandatory value for that field.

The data formats implemented by PMBus are:

- Master transmitter transmits to slave receiver. The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte. At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format. During a change of direction within a transfer, the master repeats both a start condition and the slave address but with the R/$\overline{W}$ bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

Examples of these formats are shown in Figures 7-16.



S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
x	SHOWN UNDER A FIELD INDICATES THAT THAT FIELD IS REQUIRED TO HAVE THE VALUE OF x
A	ACKNOWLEDGE (THIS BIT POSITION MAY BE 0 FOR AN ACK OR 1 FOR A NACK)
P	STOP CONDITION
PEC	PACKET ERROR CODE
☐	MASTER TO SLAVE
▒	SLAVE TO MASTER
···	CONTINUATION OF PROTOCOL

3880 F06

Figure 6. PMBus Packet Protocol Diagram Element Key

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OPERATION

Table 1. Data Format Terminology

PMBus TERMINOLOGY	MEANING	TERMINOLOGY FOR: SPECS, GUI, APPLICATION NOTES	ABBREVIATIONS FOR SUMMARY COMMAND TABLE	FOR MORE DETAIL REFER TO THE DATA FORMAT SECTION OF TABLE 2
Linear	Linear	Linear_5s_11s	L11	Page 35
Linear (for Voltage Related Commands)	Linear	Linear_16u	L16	Page 35
Direct	Direct-Manufacturer Customized	DirectMfr	CF	Page 35
Hex		Hex	I16	
ASCII		ASCII	ASC	
	Register Fields	Reg	Reg	

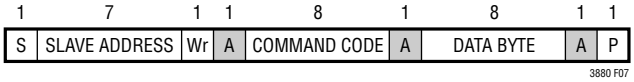

Figure 7. Write Byte Protocol

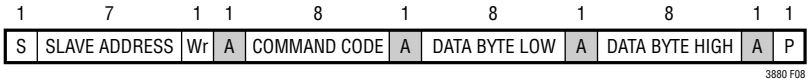

Figure 8. Write Word Protocol

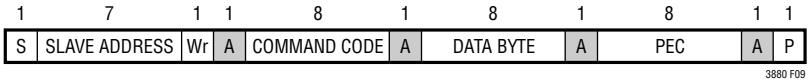

Figure 9. Write Byte Protocol with PEC

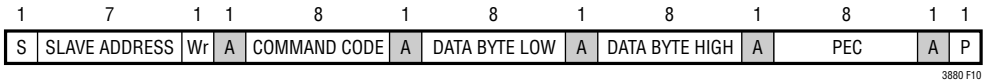

Figure 10. Write Word Protocol with PEC

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OPERATION

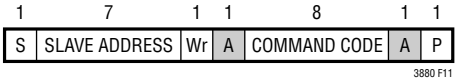

Figure 11. Send Byte Protocol

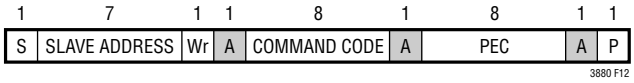

Figure 12. Send Byte Protocol with PEC

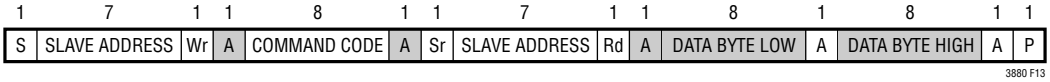

Figure 13. Read Word Protocol

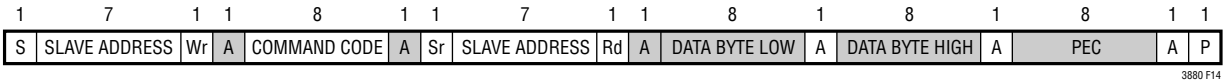

Figure 14. Read Word Protocol with PEC

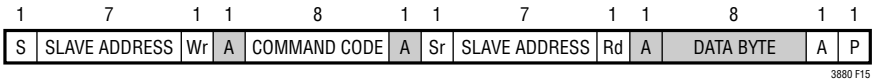

Figure 15. Read Byte Protocol

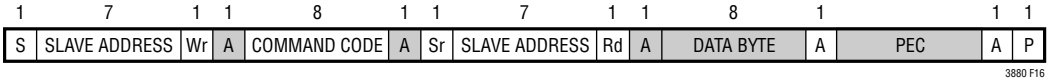

Figure 16. Read Byte Protocol with PEC

Refer to Figure 6 for a legend.

Handshaking features are included to ensure robust system communication. Please refer to the PMBus Communication and Command Processing subsection of the Applications Information section for further details.

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PMBus COMMAND SUMMARY

PMBUS COMMANDS

The following tables list supported PMBus commands and manufacturer specific commands. A complete description of these commands can be found in the "PMBus Power System Mgt Protocol Specification – Part II – Revision 1.1". Users are encouraged to reference this specification. Exceptions or manufacturer specific implementations are listed below in Table 2. Floating point values listed in the "DEFAULT VALUE" column are either Linear 16-bit Signed (PMBus Section 8.3.1) or Linear_5s_11s (PMBus Section 7.1) format, whichever is appropriate for the command. All commands from 0xD0 through 0xFF not listed in this table are implicitly reserved by the manufacturer. Users should avoid blind writes within this range of commands to avoid undesired operation of the part. All commands from 0x00 through 0xCF not listed in this table are implicitly not supported by the manufacturer. Attempting to access non-supported or reserved commands may result in a CML command fault event. All output voltage settings and measurements are based on the VOUT_MODE setting of 0x14. This translates to an exponent of 2^{-12}.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these circumstances the part follows the protocols defined in the PMBus Specification v1.1, Part II, Section 10.8.7, to communicate that it is busy. The part includes handshaking features to eliminate busy errors and simplify error handling software while ensuring robust communication and system behavior. Please refer to the subsection titled PMBus Communication and Command Processing in the Applications Information section for further details.

Table 2. Summary (Note: The Data Format abbreviations are detailed at the end of this table.)

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	63
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80	67
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E	66
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA	91
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	63
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA	101
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA	101
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	90
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14	71
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000	72
VOUT_MAX	0x24	Upper limit on the commanded output voltage including VOUT_MARGIN_HIGH.	R/W Word	Y	L16	V	Y	4.096 ch0 0x4189 5.5 ch1 0x5800	71
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD	72
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33	72
VOUT_TRANSITION_RATE	0X27	Rate the output changes when VOUT commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 AA00	78

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PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	350 0xFABC	69
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	6.5 0xCB40	70
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	6.0 0xCB00	70
IOUT_CAL_GAIN	0x38	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R/W Word	Y	L11	mΩ	Y	1.8 0xBB9A	74
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A	71
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	81
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133	72
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD	73
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66	73
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	82
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	29.75 0xDBB8	75
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	84
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	20.0 0xDA80	76
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	100.0 0xEB20	77
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8	86
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	85.0 0xEAA8	77
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	–40.0 0xE580	77
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8	86
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	15.5 0xD3E0	70
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	80
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	6.3 0xCB26	70
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280	75
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	0.93 0x0EE1	73

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PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted.	R/W Word	Y	L16	V	Y	0.92 0x0EB8	73
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000	78
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	L11	ms	Y	8.0 0xD200	78
TON_MAX_FAULT_LIMIT	0x62	Maximum time from V_{OUT_EN} on for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	10.00 0xD280	78
TON_MAX_FAULT_ RESPONSE	0x63	Action to be taken by the device when a TON_ MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	83
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000	79
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	8.00 0xD200	79
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	150 0xF258	79
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA	92
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA	92
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA	93
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA	93
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA	94
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA	94
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA	95
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA	95
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA	98
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA	99
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA	99
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA	99
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA	99
READ_TEMPERATURE_2	0x8E	Internal junction temperature. Does not affect any other registers.	R Word	N	L11	C		NA	99
READ_DUTY_CYCLE	0x94	Duty cycle of the top gate control signal.	R Word	Y	L11	%		NA	100
READ_POUT	0x96	Measured output power.	R Word	Y	L11	W		NA	100
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	90
MFR_ID	0x99	The manufacturer ID of the LTC3880 in ASCII.	R String	N	ASC			LTC	90
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTC3880	90
MFR_SERIAL	0x9E	Serial number of this specific unit.	R Block	N	CF			NA	90
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage.	R Word	Y	L16	V		4.096 CH0 5.5 CH1	73
USER_DATA_00	0xB0	OEM RESERVED. Typically used for part serialization.	R/W Word	N	Reg		Y	NA	89

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PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	89
USER_DATA_02	0xB2	OEM RESERVED. Typically used for part serialization.	R/W Word	N	Reg		Y	NA	89
USER_DATA_03	0xB3	A NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000	89
USER_DATA_04	0xB4	A NVM word available for the user.	R/W Word	N	Reg		Y	0x0000	89
MFR_INFO	0xB6	Manufacturing specific information.	R Word	N	Reg			NA	100
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA	108
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA	108
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA	108
MFR_CHAN_CONFIG_ LTC3880	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x1F	65
MFR_CONFIG_ALL_ LTC3880	0xD1	Configuration bits that are common to all pages.	R/W Byte	N	Reg		Y	0x09	65
MFR_GPIO_PROPAGATE_ LTC3880	0xD2	Configuration that determines which faults are propagated to the $\overline{\text{GPIO}}$ pins.	R/W Word	Y	Reg		Y	0x2993	87
MFR_PWM_MODE_ LTC3880	0xD4	Configuration for the PWM engine of each channel.	R/W Byte	Y	Reg		Y	0xC2	68
MFR_GPIO_RESPONSE	0xD5	Action to be taken by the device when the $\overline{\text{GPIO}}$ pin is externally asserted low.	R/W Byte	Y	Reg		Y	0xC0	89
MFR_OT_FAULT_ RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0	85
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA	100
MFR_CHANNEL_ ADDRESS	0xD8	Address to the PAGE activated channel.	R/W Byte	Y	Reg		Y	0x80	64
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	350 0xFABC	80
MFR_RESTART_DELAY	0xDC	Minimum time the RUN pin is held low by the LTC3880.	R/W Word	Y	L11	ms	Y	500 0xFBE8	80
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA	100
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA	100
MFR_TEMPERATURE_1_ PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA	100
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				NA	91
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA	97
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F	64
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTC3880	R Word	N	Reg			402x	90
MFR_IIN_OFFSET	0xE9	Coefficient used to add to the input current to account for the IQ of the part.	R/W Word	Y	L11	A	Y	0.050 0X9333	74

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PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM. This causes the part to behave as if a channel has faulted off.	Send Byte	N				NA	103
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA	107
MFR_READ_IIN	0xED	Measured input current per channel	R Word	Y	L11	A		NA	99
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	Reg		Y	NA	103
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple LTC chips.	R Byte	N	Reg			NA	97
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA	101
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA	100
MFR_PWM_CONFIG_LTC3880	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10	68
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF		Y	3900 0x0F3C	74
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	1.0 0x4000	76
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor with respect to –273.1°C	R/W Word	Y	L11	C	Y	0.0 0x8000	76
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80	64
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send Byte	N				NA	67

Note 1: Commands indicated with Y indicate that these commands are stored and restored using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

Note 2: Commands with a default value of NA indicate “not applicable”. Commands with a default value of FS indicate “factory set on a per part basis”.

Note 3: The LTC3880 contains additional commands not listed in this table. Reading these commands is harmless to the operation of the IC; however, the contents and meaning of these commands can change without notice.

Note 4: Some of the unpublished commands are read-only and will generate a CML bit 6 fault if written.

Note 5: Writing to commands not published in this table is not permitted.

Note 6: The user should not assume compatibility of commands between different parts based upon command names. Always refer to the manufacturer’s data sheet for each part for a complete definition of a command’s function.

LTC has made every reasonable attempt to keep command functionality compatible between parts; however, differences may occur to address product requirements.

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PMBus COMMAND SUMMARY

*DATA FORMAT

L11	Linear_5s_11s	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Example: For b[15:0] = 0x9807 = 'b10011_000_0000_0111 Value = $7 \cdot 2^{-13} = 854 \cdot 10^{-6}$ From "PMBus Spec Part II: Paragraph 7.1"
L16	Linear_16u	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where Y = b[15:0] is an unsigned integer and N = Vout_mode_parameter is a 5-bit two's complement exponent that is hardwired to –12 decimal Example: For b[15:0] = 0x4C00 = 'b0100_1100_0000_0000 Value = $19456 \cdot 2^{-12} = 4.75$ From "PMBus Spec Part II: Paragraph 8.2"
Reg	Register	PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in detailed PMBus Command Register Description.
I16	Integer Word	PMBus data field b[15:0] Value = Y where Y = b[15:0] is a 16 bit unsigned integer Example: For b[15:0] = 0x9807 = 'b1001_1000_0000_0111 Value = 38919 (decimal)
CF	Custom Format	Value is defined in detailed PMBus Command Register Description. This is often an unsigned or two's complement integer scaled by an MFR specific constant.
ASC	ASCII Format	A variable length string of text characters conforming to ISO/IEC 8859-1 standard.

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APPLICATIONS INFORMATION

The Typical Application on the back page is a basic LTC3880 application circuit. The LTC3880 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. The LTC3880 can nominally account for the temperature dependency of the DCR sensing element. The accuracy of the current reading and current limit are typically limited by the accuracy of the DCR resistor (accounted for in the IOUT_CAL_GAIN parameter of the LTC3880). Thus current sensing resistors provide the most accurate current sense and limiting for the application. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Then the input and output capacitors are selected. Finally the current limit is selected. All of these components and ranges are required to be determined prior to calculating the external compensation components. The current limit range is required because the two ranges (25mV to 50mV vs 37.5mV to 70mV) have different EA gains set with bit 7 of the MFR_PWM_MODE_LTC3880 command. The voltage RANGE bit also modifies the loop gain and impacts the compensation network set with bits 5, 6 of MFR_PWM_CONFIG_LTC3880. All other programmable parameters do not affect the loop gain, allowing parameters to be modified without impact to the transient response to load.

CURRENT LIMIT PROGRAMMING

The LTC3880 has two ranges of current limit programming and a total of eight levels within each range. Refer to the IOUT_OC_FAULT_LIMIT section of the PMBus commands. Within each range the error amp gain is fixed, resulting in constant loop gain. The LTC3880 will account for the DCR of the inductor and automatically update the current limit as the inductor temperature changes. The temperature coefficient of the DCR is stored in the MFR_IOUT_TC register.

For the best current limit accuracy, use the 75mV setting. The 25mV setting will allow for the use of very low DCR inductors or sense resistors, but at the expense of current limit accuracy. Keep in mind this operation is on a cycle-by-cycle basis and is only a function of the peak inductor current. The average inductor current is monitored by the ADC converter and can provide a warning if too much average output current is detected. The overcurrent fault is detected when the ITH voltage hits the maximum value. The digital processor within the LTC3880 provides the ability to either ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). Refer to the overcurrent portion of the Operation section for more detail.

I_{SENSE}^+ AND I_{SENSE}^- PINS

The I_{SENSE}^+ and I_{SENSE}^- pins are the inputs to the current comparators and the A/D. The common mode input voltage range of the current comparators is 0V to 5.5V. Both the SENSE pins are high impedance inputs with small base currents typically less than 1µA. When the I_{SENSE} pins ramp up from 0V to 1.4V, the small base currents flow out of the SENSE pins. When the I_{SENSE} pins are greater than 1.4V, the base currents flow into the I_{SENSE} pins. The high impedance inputs to the current comparators allow accurate DCR sensing. Do not to float these pins during normal operation.

Filter components mutual to the I_{SENSE} lines should be placed close to the IC. The positive and negative traces should be routed differentially and Kelvin connected to the current sense element, see Figure 17. A non-Kelvin connection elsewhere can add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. In a PolyPhase system, poor placement of the sensing element will result in sub-optimal current sharing between power stages. If DCR sensing is used (Figure 18a), sense resistor R1 should be placed close to the switching node to prevent noise from

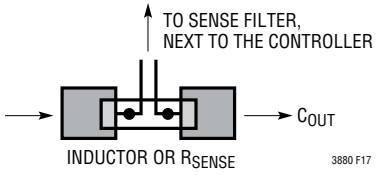

Figure 17. Optimal Sense Line Placement

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APPLICATIONS INFORMATION

coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins. This impedance difference can result in loss of accuracy in the current reading of the ADC. The current reading accuracy can be improved by matching the impedance of the two pins. To accomplish this add a series resistor between V_{OUT} and I_{SENSE}^- equal to R1. A capacitor of 1µF or greater should be placed in parallel with this resistor. If the peak voltage is <75mV at room temperature, R2 is not required.

LOW VALUE RESISTOR CURRENT SENSING

A typical sensing circuit using a discrete resistor is shown in Figure 18b. R_{SENSE} is chosen based on the required output current.

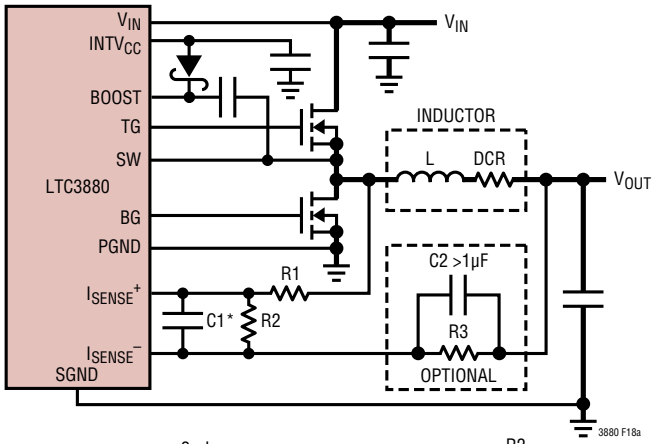

Figure 18a. Inductor DCR Current Sense Circuit

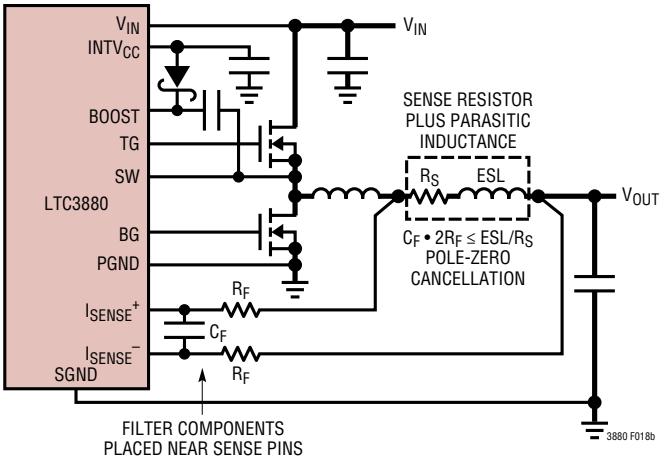

Figure 18b. Resistor Current Sense Circuit

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIMIT} setting. The input common mode range of the current comparator is 0V to 5.5V (if V_{IN} is greater than 6V). The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Due to possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 15mV minimum ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications.

For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628/LTC3728 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. In the new highest current density solutions; however, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be less than 20mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions, the voltage drop across the sense resistor's parasitic inductance is no longer negligible. A typical sensing circuit using a discrete resistor is shown in Figure 18b. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of the capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 100Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 200ns.

This same RC filter with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 19 illustrates the voltage waveform across a 2mΩ resistor with a 2010 footprint. The waveform is

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APPLICATIONS INFORMATION

the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \bullet \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}} \quad (1)$$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resultant waveform looks resistive, as shown in Figure 20. For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use Equation 1 to determine the ESL. However, do not overfilter the signal. Keep the RC time constant less than or equal to the inductor time constant to maintain a sufficient ripple voltage on V_{RSENSE} for optimal operation of the current loop controller.

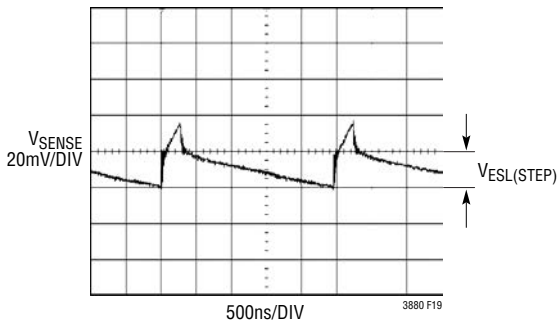

Figure 19. Voltage Measured Directly Across R_{SENSE}

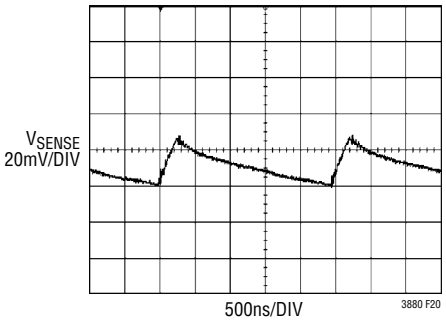

Figure 20. Voltage Measured After the R_{SENSE} Filter

INDUCTOR DCR CURRENT SENSING

For applications requiring the highest possible efficiency at high load currents, the LTC3880 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 18a. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost a few points of efficiency compared to DCR sensing.

If the external (R1+R3)||R2 • C1 time constant is chosen to be exactly equal to the 2 • L/DCR time constant, assuming R1=R3, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1+R2+R3). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. The DCR value is entered as the IOUT_CAL_GAIN in mΩ unless R2 is required. If R2 is used, IOUT_CAL_GAIN = DCR • R2/(R1+R2+R3). If there is no need to attenuate the signal, R2 can be removed. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the manufacturers' data sheets for detailed information. The LTC3880 will account for temperature variation if the correct parameter is entered into the MFR_IOUT_CAL_GAIN_TC register. Typically the resistance has a 3900ppm/°C coefficient.

C2 can be optimized for a flat frequency response, assuming R1 = R3 by the following equation

$$C2 = [2R1 \bullet R2 \bullet C1 - L/DCR \bullet (2R1+R2)]/R1^2$$

Using the inductor ripple current value from the inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, be sure to pick the optimum I_{LIMIT} value accounting for errors in the DCR versus the MFR_IOUT_CAL_GAIN parameter entered.

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APPLICATIONS INFORMATION

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for errors in the temperature sensing element of 3°C to 5°C and any additional errors associated with the proximity of the temperature sensor element to the inductor.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$RD = \frac{R_{SENSE(EQUIV)}}{DCR_{(MAXERROR)} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.047µF to 4.7µF. This forces R1||R2 to be approximately 2k. This resistance minimizes errors caused by the SENSE pin leakage currents. Adding optional elements R3 and C2 shown in Figure 18a will minimize offset errors associated with these leakage currents.

The equivalent resistance (R1+R3)||R2 is scaled to the room temperature inductance and maximum DCR:

$$(R1+R3)\,||\,R2 = \frac{2 \bullet L}{(DCR \text{ at } 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = R3;\ R1 = \frac{R1||R2}{RD};\ R2 = \frac{R1 \bullet RD}{1-RD}$$

The maximum power loss in R1 is related to the duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}R1 = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reducing conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method. Selecting Burst Mode operation or discontinuous mode will improve the converter efficiency at light loads regardless of the current sensing method.

To maintain a good signal-to-noise ratio for the current sense signal, use a minimum ΔV_{SENSE} of 10mV to 15mV. For a DCR sensing application, the actual ripple voltage will be determined by the equation:

$$\Delta V_{SENSE} = \frac{V_{IN} - V_{OUT}}{R1 \bullet C1} \bullet \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

SLOPE COMPENSATION AND INDUCTOR PEAK CURRENT

Slope compensation provides stability in constant frequency current mode architectures by preventing sub-harmonic oscillations at high duty cycles. This is accomplished internally by adding a compensation ramp to the inductor current signal at duty cycles in excess of 35%. The LTC3880 uses a patented current limit technique that counteracts the compensating ramp. This allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

INDUCTOR VALUE CALCULATION

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \bullet f_{OSC} \bullet L}$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at the lowest frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that the ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \bullet f_{OSC} \bullet I_{RIPPLE}}$$

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INDUCTOR CORE SELECTION

Once the inductor value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance. As the inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials saturate hard, which means that the inductance collapse abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

POWER MOSFET AND SCHOTTKY DIODE (OPTIONAL) SELECTION

Two external power MOSFETs must be selected for each controller in the LTC3880: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V. Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet \left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right]\bullet f_{OSC}$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{TH(MIN)}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

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The optional Schottky diodes conduct during the dead time between the conduction of the two power MOSFETs. These prevent the body diodes of the bottom MOSFETs from turning on, storing charge during the dead time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

VARIABLE DELAY TIME, SOFT-START AND OUTPUT VOLTAGE RAMPING

The LTC3880 must enter the run state prior to soft-start. The RUN pins are released after the part initializes and V_{IN} is greater than the VIN_ON threshold. If multiple LTC3880s are used in an application, they should be configured to share the same RUN pins. They all hold their respective RUN pins low until all devices initialize and V_{IN} exceeds the VIN_ON threshold for all devices. The SHARE_CLK pin assures all the devices connected to the signal use the same time base.

After the RUN pin releases, the controller waits for the user-specified turn-on delay (TON_DELAY) prior to initiating an output voltage ramp. Multiple LTC3880s and other LTC parts can be configured to start with variable delay times. To work correctly, all devices use the same timing clock (SHARE_CLK) and all devices must share the RUN pin. This allows the relative delay of all parts to be synchronized. The actual variation in the delay will be dependent on the highest clock rate of the devices connected to the SHARE_CLK pin (all Linear Technology ICs are configured to allow the fastest SHARE_CLK signal to control the timing of all devices). The SHARE_CLK signal can be ±10% in frequency, thus the actual time delays will have some variance.

Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set point. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting TON_RISE to any value less than 0.250ms. The LTC3880 will perform the necessary math internally to assure the voltage ramp is controlled to the desired slope. However, the voltage slope can not be any faster than the fundamental limits of the power stage. The shorter TON_RISE time is set, the more jagged the TON_RISE ramp will appear. The number of steps in the ramp is equal to TON_RISE/0.1ms.

The LTC3880 PWM will always use discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom gate is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a pre-biased load.

There is no tracking feature in the LTC3880; however, two outputs can be given the same TON_RISE and TON_DELAY times to effectively ramp up at the same time. Because the RUN pins are released at the same time and both units use the same time base, the outputs will track very closely. If the circuit is in a PolyPhase configuration, all timing parameters must be the same.

The described method of start-up sequencing is time based. For concatenated events it is possible to control the RUN pin based on the $\overline{GPIO}$ pin of a different controller. The $\overline{GPIO}$ pin can be configured to release when the output voltage of the converter is greater than the VOUT_UV_FAULT_LIMIT. It is recommended to use the unfiltered V_{OUT} UV fault limit because there is little appreciable time delay between the converter crossing the UV threshold and the $\overline{GPIO}$ pin releasing. The unfiltered output can be enabled using the MFR_GPIO_PROPAGATE_VOUT_UVUF (PGOOD) command. (Refer to the MFR section of the PMBus commands in this document). The unfiltered signal may have some glitching as the V_{OUT} signal transitions through the comparator threshold. A small internal digital filter of 70µs has been added to minimize this problem. To minimize the risk of $\overline{GPIO}$ pins glitching, make the TON_RISE times less than 100ms. If unwanted transitions still occur on $\overline{GPIO}$, place a capacitor to ground on the $\overline{GPIO}$ pin to filter the waveform. The RC time-constant of the filter should be set sufficiently fast to assure no appreciable delay is incurred. A value of 300µs to 500µs will provide some additional filtering without significantly delaying the trigger event.

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DIGITAL SERVO MODE

For maximum accuracy in the regulated output voltage, enable the digital servo loop by asserting bit 6 of the MFR_PWM_MODE_LTC3880 command. In digital servo mode, the LTC3880 will adjust the regulated output voltage based on the ADC voltage reading. Every 90ms the digital servo loop will step the LSB of the DAC (nominally 1.375mV or 0.6875mV depending on the voltage range bit) until the output is at the correct ADC reading. At power-up this mode engages after TON_MAX_FAULT_LIMIT unless the limit is set to 0 (infinite). If the TON_MAX_FAULT_LIMIT is set to 0 (infinite), the servo begins after TON_RISE is complete and VOUT has exceeded the VOUT_UV_FAULT_LIMIT and IOUT_OC is not present. This same point in time is when the output changes from discontinuous to the programmed mode as indicated in MFR_PWM_MODE_LTC3880 bits 0 and 1. Refer to Figure 21 for details on the VOUT waveform under time based sequencing.

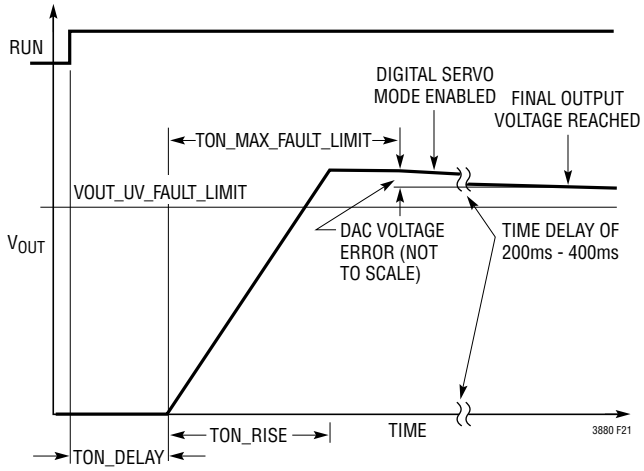

Figure 21. Timing Controlled V_{OUT} Rise

If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is set to ignore 0x00, the servo begins:

1. After the TON_RISE sequence is complete
2. After the TON_MAX_FAULT_LIMIT time is reached; and
3. After the VOUT_UV_FAULT_LIMIT has been exceed or the IOUT_OC_FAULT_LIMIT is not longer active.

If the TON_MAX_FAULT_IMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is not set to ignore 0X00, the servo begins:

1. After the TON_RISE sequence is complete;
2. After the TON_MAX_FAULT_LIMIT time has expired and both VOUT_UV_FAULT and IOUT_OC_FAULT are not present.

The maximum rise time is limited to 1.3 seconds.

In a PolyPhase configuration it is recommended only one of the control loops have the digital servo mode enabled. This will assure the various loops do not work against each other due to slight differences in the reference circuits.

SOFT OFF (SEQUENCED OFF)

In addition to a controlled start-up, the LTC3880 also supports controlled turn-off. The TOFF_DELAY and TOFF_FALL functions are shown in Figure 22. TOFF_FALL is processed when the RUN pin goes low or if the part is commanded off. If the part faults off or $\overline{GPIO}$ is pulled low externally and the part is programmed to respond to this, the output will three-state rather than exhibiting a controlled ramp. The output will decay as a function of the load.

The output voltage will operate as shown in Figure 22 so long as the part is in forced continuous mode and the TOFF_FALL time is sufficiently slow that the power stage can achieve the desired slope. The TOFF_FALL time can only be met if the power stage and controller can sink

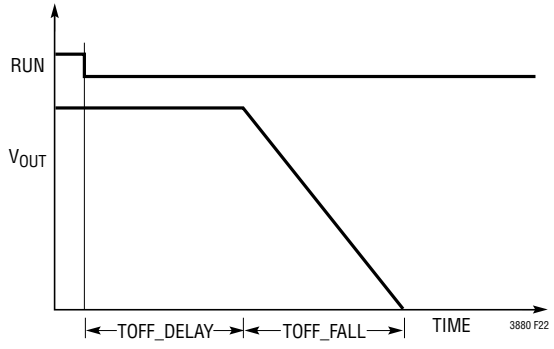

Figure 22. TOFF_DELAY and TOFF_FALL

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sufficient current to assure the output is a zero volts by the end of the fall time interval. If the TOFF_FALL time is set shorter than the time required to discharge the load capacitance, the output will not reach the desired zero volt state. At the end of TOFF_FALL, the controller will cease to sink current and V_{OUT} will decay at the natural rate determined by the load impedance. If the controller is in discontinuous mode, the controller will not pull negative current and the output will be pulled low by the load, not the power stage. The maximum fail time is limited to 1.3 seconds. The shorter TOFF_FALL time is set, the more jagged the TOFF_FALL ramp will appear. The number of steps in the ramp is equal to TOFF_FALL/0.1ms.

$INTV_{CC}$ REGULATOR

The LTC3880 features an NPN linear regulator that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers, V_{DD33} and much of the LTC3880 internal circuitry. The linear regulator produces the voltage at the $INTV_{CC}$ pin to nominally 5V when V_{IN} is greater than 6.5V. The regulator can supply a peak current of 100mA and must be bypassed to ground with a minimum of 1µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels. The NPN linear regulator on the LTC3880-1 is not present and an external 5V supply is needed.

High input voltage application in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3880 to be exceeded. The $INTV_{CC}$ current, of which a large percentage is due to the gate charge current, may be supplied by either the internal 5V linear regulator or from an external 5V regulator on the LTC3880-1. If the LTC3880 is used with the internal regulator activated, the power through the IC is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations in Note 2 of the Electrical Characteristics. For example, the LTC3880 $INTV_{CC}$ current is limited to less than 69mA from a 24V supply:

$$T_J = 70°C + 69mA \bullet 24V \bullet 33°C/W = 125°C$$

To prevent the maximum junction temperature from being exceeded, a LTC3880-1 can be used. In the LTC3880-1, the $INTV_{CC}$ linear regulator is disabled and approximately 2mA of current is supplied internally from V_{IN}. Significant system efficiency and thermal gains can be realized by powering the $EXTV_{CC}$ pin from a switching 5V regulator. The V_{IN} current resulting from the gate driver and control circuitry will be scaled by a factor of:

$$\left(\frac{V_{EXTVCC}}{V_{IN}}\right)\left(\frac{1}{Efficiency}\right)$$

Tying the $EXTV_{CC}$ pin to a 5V supply (LTC3880-1 only) reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + 69mA \bullet 5V \bullet 33°C/W + 2mA \bullet 24V \bullet 33°C/W = 83°C$$

Do not tie $INTV_{CC}$ on the LTC3880 to an external supply because $INTV_{CC}$ will attempt to pull the external supply high and hit current limit, significantly increasing the die temperature.

For applications where V_{IN} is 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 23. To minimize the voltage drop caused by the gate charge current a low ESR capacitor must be connected to the $V_{IN}/INTV_{CC}$ ($EXTV_{CC}$) pins. This configuration will override the $INTV_{CC}$ ($EXTV_{CC}$) linear regulator and will prevent $INTV_{CC}$ ($EXTV_{CC}$) from dropping too low. Make sure the $INTV_{CC}$ ($EXTV_{CC}$)

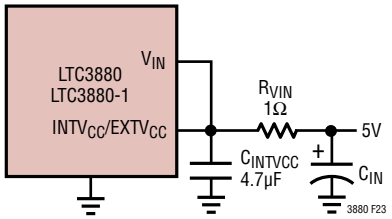

Figure 23. Setup for a 5V Input

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voltage exceeds the $R_{DS(ON)}$ test voltage for the MOSFETs which is typically 4.5V for logic level devices. The UVLO on $INTV_{CC}$ ($EXTV_{CC}$) is set to approximately 4V. Both a LTC3880 and LTC3880-1 are valid for this configuration.

TOPSIDE MOSFET DRIVER SUPPLY (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Block Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

PWM jitter has been observed in some designs operating at higher V_{IN}/V_{OUT} ratios. This jitter does not substantially affect the circuit accuracy. Referring to Figure 24, PWM jitter can be removed by inserting a series resistor with a value of 1Ω to 5Ω between the cathode of the diode and the BOOST*n* pin. A resistor case size of 0603 or larger is recommended to reduce ESL and achieve the best results.

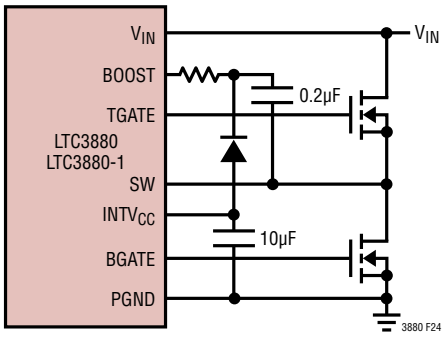

Figure 24. Boost Circuit to Minimize PWM Jitter

UNDERVOLTAGE LOCKOUT

The LTC3880 is initialized by an internal threshold-based UVLO where V_{IN} must be approximately 4V and $INTV_{CC}$/$EXTV_{CC}$, V_{DD33}, V_{DD25} must be within approximately 20% of the regulated values. In addition, V_{DD33} must be within approximately 7% of the targeted value before the RUN and SHARE_CLK pins are released. After the part has initialized, an additional comparator monitors V_{IN}. The VIN_ON threshold must be exceeded before the power sequencing can begin. When V_{IN} drops below the VIN_OFF threshold, the SHARE_CLK pin will be pulled low and V_{IN} must increase above the VIN_ON threshold before the controller will restart. The normal start-up sequence will be allowed after the VIN_ON threshold is crossed.

It is possible to program the contents of the NVM in the application if the V_{DD33} supply is externally driven. This will activate the digital portion of the LTC3880 without engaging the high voltage sections. PMBus communications are valid in this supply configuration. If V_{IN} has not been applied to the LTC3880, bit 3 (NVM Not Initialized) in MFR_COMMON will be asserted low. If this condition is detected, the part will only respond to addresses 5A and 5B. To initialize the part issue the following set of commands: global address 0x5B command 0xBD data 0x2B followed by global address 5B command 0xBD and data 0xC4. The part will now respond to the correct address. Configure the part as desired then issue a STORE_USER_ALL. When V_{IN} is applied a MFR_RESET command must be issued to allow the PWM to be enabled and valid ADC conversions to be read.

C_{IN} AND C_{OUT} SELECTION

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input

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capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3880, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC3880 2-phase operation can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The sources of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the sources and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC3880, is also suggested. A 2.2Ω – 10Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two channels.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

FAULT CONDITIONS

The LTC3880 $\overline{\text{GPIO}}n$ pins are configurable to indicate a variety of faults including OV/UV, OC, OT, timing faults, peak overcurrent faults. In addition the $\overline{\text{GPIO}}n$ pins can be pulled low by external sources indicating a fault in some other portion of the system. The fault response is configurable and allow the following options:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Refer to the PMBus section of the data sheet and the PMBus specification for more details.

The OV response is automatic and virtually immediate. If an OV is detected, TG goes low and BG is asserted.

Fault logging is available on the LTC3880. The fault logging is configurable to automatically store data when a fault occurs that causes the unit to fault off. The header portion of the fault logging table contains peak values. It is possible to read these values at any time. This data will be useful while troubleshooting the fault.

If the LTC3880 internal temperature is in excess of 85°C, the write into the NVM is not recommended. The data will still be held in RAM, unless the 3.3V supply UVLO threshold is reached. If the die temperature exceeds 130°C all

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NVM communication is disabled until the die temperature drops below 120°C.

OPEN-DRAIN PINS

The LTC3880 has the following open-drain pins:

3.3V Pins

1. $\overline{\text{GPIO}n}$
2. SYNC
3. SHARE_CLK

5V Pins (5V pins operate correctly when pulled to 3.3V.)

1. RUN*n*
2. $\overline{\text{ALERT}}$
3. SCL
4. SDA

All the above pins have on-chip pull-down transistors that can sink 3mA at 0.4V. The low threshold on the pins is 1.4V; thus, plenty of margin on the digital signals with 3mA of current. For 3.3V pins, 3mA of current is a 1.1k resistor. Unless there are transient speed issues associated with the RC time constant of the resistor pull-up and parasitic capacitance to ground, a 10k resistor or larger is generally recommended.

For high speed signals such as the SDA, SCL and SYNC, a lower value resistor may be required. The RC time constant should be set to 1/3 to 1/5 the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the rise time must be less than 300ns. The resistor pull-up on the SDA and SCL pins with the time constant set to 1/3 the rise time:

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k$$

The closest 1% resistor value is 1k. Be careful to minimize parasitic capacitance on the SDA and SCL pins to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is one time constant.

The SYNC pin has an on-chip pull-down transistor with the output held low for nominally 500ns. If the internal oscillator is set for 500kHz and the load is 100pF and a 3x time constant is required, the resistor calculation is as follows:

$$R_{PULLUP} = \frac{2\mu s - 500ns}{3 \bullet 100pF} = 5k$$

The closest 1% resistor is 4.99k.

If timing errors are occurring or if the SYNC frequency is not as fast as desired, monitor the waveform and determine if the RC time constant is too long for the application. If possible reduce the parasitic capacitance. If not reduce the pull up resistor sufficiently to assure proper timing. The SHARE_CLK pull-up resistor has a similar equation with a period of 10µs and a pull-down time of 1µs. The RC time constant should be approximately 3µs or faster.

PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LTC3880 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. The PLL is locked to the falling edge of the SYNC pin. The phase relationship between channel 0, channel 1 and the falling edge of SYNC is controlled by the lower 3 bits of the MFR_PWM_CONFIG_LTC3880 command. For PolyPhase applications, it is recommended all the phases be spaced evenly. Thus for a 2-phase system the signals should be 180° out of phase and a 4-phase system should be spaced 90°.

The phase detector is an edge-sensitive digital type that provides a known phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. The PLL lock range is guaranteed between 250kHz and 1MHz. Nominal parts will have a range beyond this; however, operation to a wider frequency range is not guaranteed.

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The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted and the $\overline{\text{ALERT}}$ pin is pulled low. The fault can be cleared by writing a 1 to the bit. If the user does not wish to see the PLL_FAULT, even if a synchronization clock is not available at power up, bit 3 of the MFR_CONFIG_ALL_LTC3880 command must be asserted.

If the SYNC signal is not clocking in the application, the PLL will run at the lowest free running frequency of the VCO. This will be well below the intended PWM frequency of the application and may cause undesirable operation of the converter.

If the PWM signal appears to be running at too high a frequency, monitor the SYNC pin. Extra transitions on the falling edge will result in the PLL trying to lock on to noise versus the intended signal. Review routing of digital control signals and minimize crosstalk to the SYNC signal to avoid this problem. Multiple LTC3880s are required to share the SYNC pin in PolyPhase configurations, for other configurations it is optional. If the SYNC pin is shared between LTC3880s, only one LTC3880 can be programmed with a frequency output. All the other LTC3880s must be programmed to external clock.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3880 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3880 is approximately 90ns, with reasonably good PCB layout, minimum 30% inductor current ripple and at least 10mV – 15mV ripple on the current sense signal. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak current sense voltage decreases, the minimum on-time gradually increases to 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

RCONFIG (EXTERNAL RESISTOR CONFIGURATION PINS)

The LTC3880 default NVM is programmed to respect the RCONFIG pins. If a user wishes the output voltage, PWM frequency and phasing and the address to be set without programming the part or purchasing specially programmed parts, the RCONFIG pins can be used to establish these parameters. The RCONFIG pins all require a resistor divider between the VDD25 and SGND of the LTC3880. The RCONFIG pins are only monitored at initial power up and during a reset so modifying their values perhaps using an A/D after the part is powered will have no effect. 1% resistors or better must be used to assure proper operation. Noisy clock signals should not be routed near these pins.

Voltage Selection

When an output voltage is set using the RCONFIG pins on VOUT*n*_CFG and VTRIM*n*_CFG, the following parameters are set as a percentage of the output voltage:

- VOUT_OV_FAULT_LIMIT +10%
- VOUT_OV_WARN +7.5%
- VOUT_MAX +7.5%
- VOUT_MARGIN_HI +5%
- POWER_GOOD_ON –7%
- POWER_GOOD_OFF –8%
- VOUT_MARGIN_LO –5%
- VOUT_UV_WARN –6.5%
- VOUT_UV_FAULT_LIMIT –7%

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Refer to Tables 12 and 13 to set the output voltage using RCONFIG pins VOUT*n*_CFG and VTRIM*n*_CFG. RTOP is connected between VDD25 and the pin and RBOTTOM is connected between the pin and SGND. 1% resistors must be used to assure proper operation.

The output voltage set point is equal to:

$V_{SETPOINT}$ = VOUT*n*_CFG + VTRIMn_CFG

For example, if the VOUTn_CFG pin has R_{TOP} equal to 24.9k and R_{BOTTOM} equal to 4.32k, and VTRIM*n*_CFG is set with R_{TOP} not inserted and R_{BOTTOM} equal to 0Ω:

$V_{SETPOINT}$ = 1.1V – 0.099V or 1.001V

If odd values of output voltage are required from 0.5V to 3.3V, use only the VOUT*n*_CFG resistor divider, the V_{TRIM} pin can be open or shorted to V_{DD25}. If the output set point is 5V, the VOUT*n*_CFG must have R_{TOP} equal to 10k and R_{BOTTOM} equal to 23.2k and VTRIM*n*_CFG must have R_{TOP} equal to 20k and R_{BOTTOM} equal to 11k. If VOUT is 2.5 volts or lower, low range is used. The maximum voltage command on channel 0 is 4.096 volts including VOUT_OV_FAULT, VOUT_OV_WARN, VOUT_MARGIN_HI and VOUT.

Table 12. VOUT*n*_CFG

R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	V_{OUT} (V)
0 or Open	Open	NVM
10	23.2	See VTRIM
10	15.8	3.3
16.2	20.5	3.1
16.2	17.4	2.9
20	17.8	2.7
20	15	2.5
20	12.7	2.3
20	11	2.1
24.9	11.3	1.9
24.9	9.09	1.7
24.9	7.32	1.5
24.9	5.76	1.3
24.9	4.32	1.1
30.1	3.57	0.9
30.1	1.96	0.7
Open	0	0.5

Table 13. VTRIM*n*_CFG

R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	V_{TRIM} (mV) CHANGE TO V_{SET} VOLTAGE	V_{OUT} (V) IF V_{OUT} HAS 10kΩ/23.3kΩ
0 or Open	Open	0	
10	23.2	99	
10	15.8	86.625	
16.2	20.5	74.25	
16.2	17.4	61.875	
20	17.8	49.5	
20	15	37.125	5.5
20	12.7	24.75	5.25
20	11	12.375	5
24.9	11.3	–12.375	4.75
24.9	9.09	–24.75	4.5
24.9	7.32	–37.125	4.25
24.9	5.76	–49.5	4
24.9	4.32	–61.875	3.75
30.1	3.57	–74.25	3.63
30.1	1.96	–86.625	3.5
Open	0	–99	3.46

Frequency and Phase Selection Using RCONFIG

The frequency and phase commands are linked if they are set using the RCONFIG pins. If PMBus commands are used the two parameters are independent. The SYNC pins must be shared in PolyPhase configurations where multiple LTC3880s are used to produce the output. If the configuration is not PolyPhase the SYNC pins do not have to be shared. If the SYNC pins are shared between LTC3880s only one SYNC pin can be set as a frequency output, all other SYNC pins must be set to External Clock.

For example in a 4-phase configuration clocked at 425kHz, one of the LTC3880s must be set to the desired frequency and phase and the other LTC3880 must be set to External Clock. All phasing is with respect to the falling edge of SYNC.

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Table 14. FREQ_CFG (Phase Based on Falling Edge of SYNC)

R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	FREQUENCY (kHz)	θ_{SYNC} TO θ_0	θ_{SYNC} TO θ_1	DESCRIPTION
0 or Open	Open	NVM	NVM	NVM	NVM
10	23.2	250	0	180	2-Phase
10	15.8	250	120	240	3-Phase
16.2	20.5	250	90	270	4-Phase
16.2	17.4	425	0	180	2-Phase
20	17.8	425	120	240	3-Phase
20	15	425	90	270	4-Phase
20	12.7	500	0	180	2-Phase
20	11	500	120	240	3-Phase
24.9	11.3	500	90	270	4-Phase
24.9	9.09	575	0	180	2-Phase
24.9	7.32	575	120	240	3-Phase
24.9	5.76	575	90	270	4-Phase
24.9	4.32	650	0	180	2-Phase
30.1	3.57	650	120	240	3-Phase
30.1	1.96	650	90	270	4-Phase
Open	0	External Clock	0	180	2-Phase

LTC3880 Chip 1 set the frequency to 425kHz with 90° and 270° phase shift:

R_{TOP} = 20kΩ and R_{BOTTOM} = 15kΩ

LTC3880 Chip 2 set the frequency to External Clock with 0° and 180° phase shift:

R_{TOP} = open and R_{BOTTOM} = 0Ω

Frequencies of 350kHz, 750kHz and 1000kHz can only be set using NVM programming. If a 6-phase configuration is desired, NVM programming will give optimal phasing. All other configurations in frequency and phasing can be achieved using the FREQ_CFG pin.

Address Selection Using RCONFIG

The LTC3880 address is selected using a combination of the address stored in NVM and the ASEL pin. The MSB of ASEL is the MSB in the NVM and the LSB is the ASEL value. This allows 16 different LTC3880s on a single board with one programmed address in NVM.

If the address stored in NVM is 0x4F, then the part address can be set from 0x40 to 0x4F using ASEL. (The standard default address is 0x4F). Do not set any part address to 0x5A or 0x5B because these are global addresses and all parts will respond to them.

To choose address 0x40 R_{TOP} is open and R_{BOTTOM} = 0Ω

To choose address 0x45 R_{TOP} = 24.9k and R_{BOTTOM} = 7.32k

To choose address 0x4E R_{TOP} = 10.0k and R_{BOTTOM} = 15.8k

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Table 15. ASEL

R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	SLAVE ADDRESS	LSB HEX
0 or Open	Open	NVM	
10	23.2	xyz_1111	F
10	15.8	xyz_1110	E
16.2	20.5	xyz_1101	D
16.2	17.4	xyz_1100	C
20	17.8	xyz_1011	B
20	15	xyz_1010	A
20	12.7	xyz_1001	9
20	11	xyz_1000	8
24.9	11.3	xyz_0111	7
24.9	9.09	xyz_0110	6
24.9	7.32	xyz_0101	5
24.9	5.76	xyz_0100	4
24.9	4.32	xyz_0011	3
30.1	3.57	xyz_0010	2
30.1	1.96	xyz_0001	1
Open	0	xyz_0000	0

Table 15A[1]. LTC3880 MFR_ADDRESS Command Examples Expressing Both 7- or 8-Bit Addressing

DESCRIPTION	HEX DEVICE ADDRESS 7 BIT	8 BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W
Rail[4]	0x5A	0xB4	0	1	0	1	1	0	1	0	0
Global[4]	0x5B	0xB6	0	1	0	1	1	0	1	1	0
Default	0x4F	0x9E	0	1	0	0	1	1	1	1	0
Example 1	0x60	0xC0	0	1	1	0	0	0	0	0	0
Example 2	0x61	0xC2	0	1	1	0	0	0	0	1	0
Disabled[2,3,5]			1	0	0	0	0	0	0	0	0

Note 1: This table can be applied to the MFR_CHANNEL_ADDRESS, and MFR_RAIL_ADDRESS commands as well as the MFR_ADDRESS command.

Note 2: A disabled value in one command does not disable the device, nor does it disable the Global address.

Note 3: A disabled value in one command does not inhibit the device from responding to device addresses specified in other commands.

Note 4: It is not recommended to write the value 0x00, 0x0C (7 bit), or 0x5A or 0x5B(7 bit) to the MFR_ADDRESS, MFR_CHANNEL_ ADDRESS or the MFR_RAIL_ADDRESS commands.

Note 5: To disable the address enter 0x80 in the MFR_ADDRESS command. The 0x80 is greater than the 7-bit address field, disabling the address.

EFFICIENCY CONSIDERATIONS

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3880 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

   On the LTC3880-1, supplying $EXTV_{CC}$ from an output-derived source will scale the V_{IN} current required for the driver and control circuits by a factor of:

$$\left(\frac{V_{EXTVCC}}{V_{IN}}\right)\left(\frac{1}{\text{Efficiency}}\right)$$

   For example, in a 20V to 5V application, 10mA of $INTV_{CC}$ current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

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3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 10mΩ, R_L = 10mΩ, R_{SENSE} = 5mΩ, then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A for a 5V output, or a 3% to 12% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   Transition Loss = $(1.7)\ V_{IN}^2\ I_{O(MAX)}\ C_{RSS}\ f$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. The LTC3880 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

CHECKING TRANSIENT RESPONSE

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Typical Application circuit will provide an adequate starting point for most applications. The only two programmable parameters that affect loop gain are the voltage range, bits 5 and 6 of the MFR_PWM_CONFIG_LTC3880 command and the current range, bit 7 of the MFR_PWM_MODE_LTC3880 command. Be sure to establish these settings prior to compensation calculation.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without

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breaking the feedback loop. Placing a power MOSFET with a resistor to ground directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce to a load step. The MOSFET + R_{SERIES} will produce output currents approximately equal to V_{OUT}/R_{SERIES}. R_{SERIES} values from 0.1Ω to 2Ω are valid depending on the current limit settings and the programmed output voltage. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC BOARD LAYOUT CHECKLIST

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 25. Figure 26 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs M1 and M2 located within 1 cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The I_{TH} traces should be as short as possible. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
3. Does the LTC3880 V_{SENSE} lines equal V_{OUT}? V_{OUT0} is differential. V_{OUT1} should reference the SGND (Pin 41) to the Load 1 ground.
4. Are the I_{SENSE}^+ and I_{SENSE}^- leads routed together with minimum PC trace spacing? The filter capacitor between I_{SENSE}^+ and I_{SENSE}^- should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor or inductor, whichever is used for current sensing.

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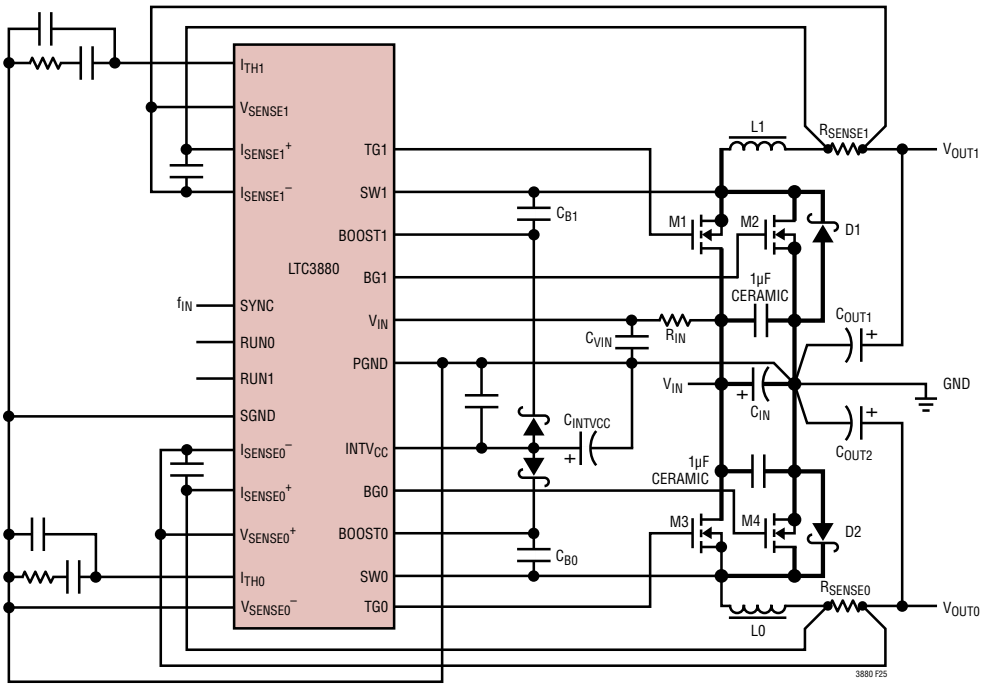

Figure 25. Recommended Printed Circuit Layout Diagram

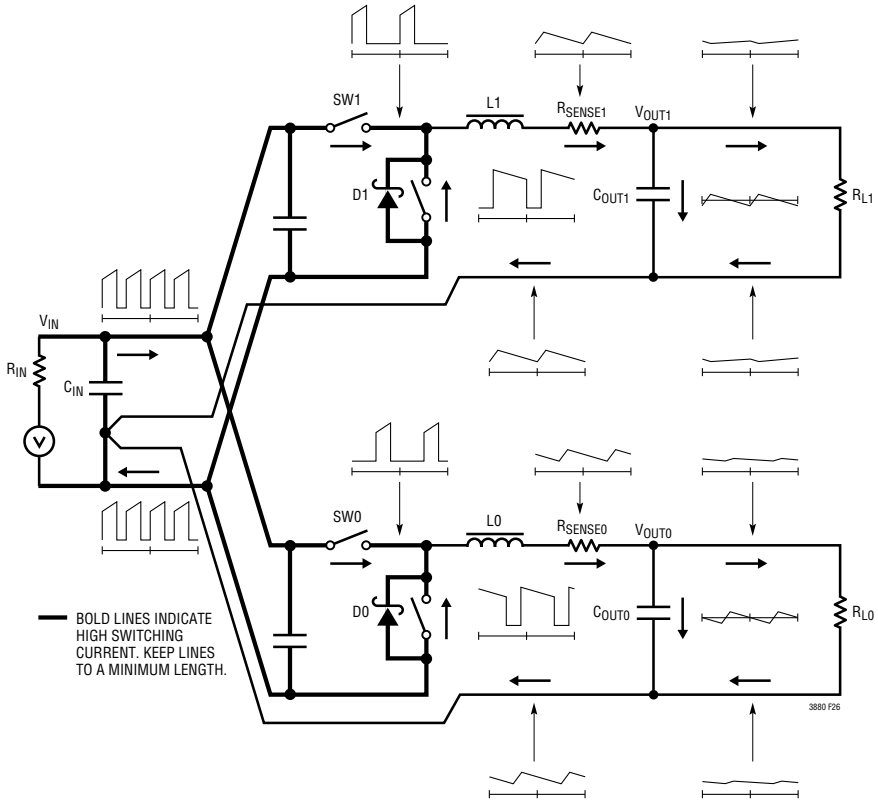

Figure 26. Branch Current Waveforms

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5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
6. Keep the switching nodes (SW1, SW0), top gate nodes (TG1, TG0), and boost nodes (BOOST1, BOOST0) away from sensitive small-signal nodes, especially from the opposite channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3880 and occupy minimum PC trace area. If DCR sensing is used, place the top resistor (Figure 18a, R1) close to the switching node.
7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

PC BOARD LAYOUT DEBUGGING

Start with one controller at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

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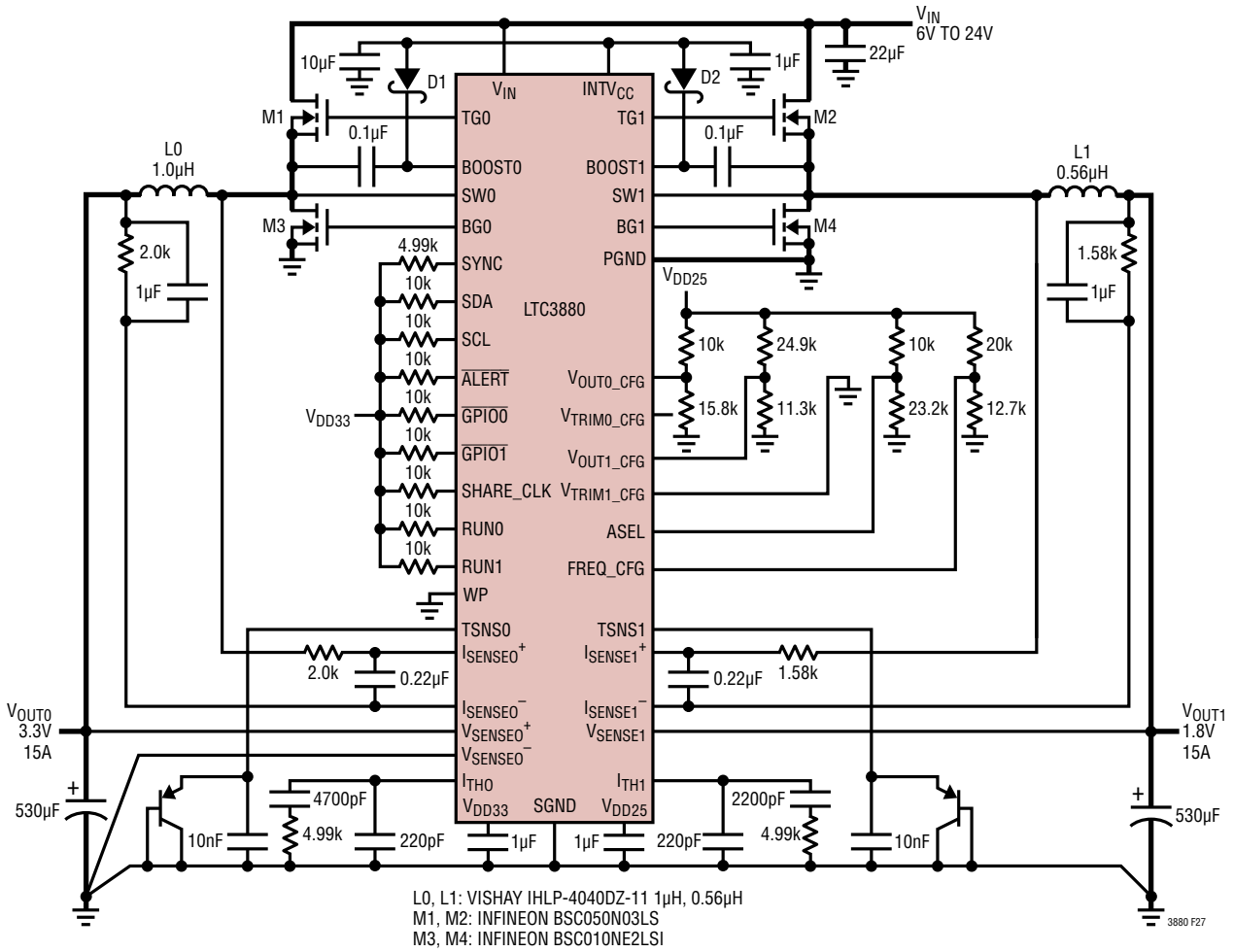

Figure 27. High Efficiency Dual 500kHz 3.3V/1.8V Step-Down Converter

DESIGN EXAMPLE

As a design example for a two channel medium current regulator, assume V_{IN} = 12V nominal, V_{IN} = 20V maximum, V_{OUT0} = 3.3V, V_{OUT1} = 1.8V, $I_{MAX0,1}$ = 15A and f = 500kHz (see Figure 27).

The regulated output is established by the VOUT_ COMMAND stored in NVM or placing the following resistor divider between VDD25 the RCONFIG pin and SGND:

1. VOUT0_CFG, R_{TOP} = 10k, R_{BOTTOM} = 15.8k
2. VTRIM0_CFG, Open
3. VOUT1_CFG, R_{TOP} = 24.9k, R_{BOTTOM} = 11.3k
4. VTRIM1_CFG, R_{TOP} = Open, R_{BOTTOM} = 0Ω

The frequency and phase are set by NVM or by setting the resistor divider between VDD25 FREQ_CFG and SGND with R_{TOP} = 20k and R_{BOTTOM} = 12.7k. The address is set to XF where X is the MSB stored in NVM.

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The following parameters are set as a percentage of the output voltage if the resistor configuration pins are used to determined output voltage:

- VOUT_OV_FAULT_LIMIT ..... +10%
- VOUT_OV_WARN ..... +7.5%
- VOUT_MAX ..... +7.5%
- VOUT_MARGIN_HI ..... +5%
- POWER_GOOD_ON ..... –7%
- POWER_GOOD_OFF ..... –8%
- VOUT_MARGIN_LO ..... –5%
- VOUT_UV_WARN ..... –6.5%
- VOUT_UV_FAULT_LIMIT ..... –7%

All other user defined parameters must be programmed into the NVM. The GUI can be utilized to quickly set up the part with the desired operating parameters.

The inductance values are based on a 35% maximum ripple current assumption (5.25A for each channel). The highest value of ripple current occurs at the maximum input voltage:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Channel 0 will require 1.05µH and channel 1 will require 0.624µH. The nearest standard values are 1µH and 0.68µH respectively. At the nominal input the ripple will be:

$$\Delta I_{L(NOM)} = \frac{V_{OUT}}{f \bullet L}\left[1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right]$$

Channel 0 will have 4.79A (32%) ripple, and channel 1 will have 5.5A (30%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current or 17.39A for channel 0 and 17.75A for channel 1. The minimum on time occurs on channel 1 at the maximum V_{IN}, and should not be less than 90ns:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f} = \frac{1.8V}{20V(500kHz)} = 180ns$$

The Vishay IHLP4040DZ-11 1µH (2.3mΩ DCR_{TYP} at 25°C) channel 0 and the VishayIHLP4040DZ-11 0.56µH (1.61mΩ DCR_{TYP} at 25°C) channel 1 are chosen.

Assuming the temperature measurement of the inductor temperature is accurate and C1 is set to 0.2µF, R_D is infinite and removed from the equations.

$$R0 = \frac{L}{(DCR \text{ at } 25°C) \bullet C1} = \frac{1\mu H}{2.3m\Omega \bullet 0.22\mu F} = 2k$$

The maximum power loss in R0 is related to the duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}R0 = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1}$$

$$= \frac{(20 - 3.3) \bullet 3.3}{2k} = 27.55mW$$

The respective values for channel 1 are R1 = 2k, R2 is open and $P_{LOSS}R1$ = 20.73mW.

The current limit will be set 20% higher than the peak value to assure variation in components and noise in the system do not limit the average current.

$$V_{ILIMIT} = I_{PEAK} \bullet R_{DCR(MAX)} = 17.39A \bullet 2.5m\Omega = 43mV$$

The closest V_{ILIMIT} setting is 42.9mV or 46.4mV. The values are entered with the IOUT_OC_FAULT_LIMIT command. Based on expected variation and measurement in the lab across the sense capacitor the user can determine the optimal setting. For channel 1 the V_{ILIMT} value is 28.6mV. The closest value is 28.6mV.

The power dissipation on the top side MOSFET can be easily estimated. Choose a RENESAS RJK0305DPB topside MOSFET. $R_{DS(ON)}$ = 10mΩ, C_{MILLER} = 75pF. At maximum input voltage with T estimated = 50°C and a bottom side MOSFET a RENESAS RJK0330DPB, $R_{DS(ON)}$ = 3mΩ:

$$P_{MAIN} = \frac{3.3V}{20V} \bullet (17.39)^2 \bullet \left[1 + (0.005)(50°C - 25°C)\right]$$

$$\bullet\ 0.006\Omega + (20V)^2 (8.695A) \bullet \left(\frac{1}{5 - 2.3} + \frac{1}{2.3}\right)$$

$$(75pF)(500kHz) = 0.386W$$

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The loss in the bottom side MOSFET is:

$$P_{SYNC} = \frac{(20V - 3.3V)}{20V} \bullet (17.39A)^2 \bullet \left[1 + (0.005)(50°C - 25°C)\right] \bullet 0.001\Omega$$
$$= 0.312W$$

Both MOSFETS have I^2R losses while the P_{MAIN} equation includes an additional term for transition losses, which are highest at high input voltages.

C_{IN} is chosen for an RMS current rating of:

$$C_{IN}\ \text{Required}\ I_{RMS} = \frac{17.39}{20}\left[(3.3) \bullet (20 - 3.3)\right]^{1/2}$$
$$= 6.5A$$

at temperature assuming only channel 0 or 1 is on. C_{OUT} is chosen with an ESR of 0.006Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is

$V_{ORIPPLE} = R(\Delta I_L) = 0.006\Omega \bullet 5.5A = 33mV.$

CONNECTING THE USB TO THE I²C/SMBus/PMBus CONTROLLER TO THE LTC3880 IN SYSTEM

The LTC USB to I²C/SMBus/PMBus controller can be interfaced to the LTC3880 on the user's board for programming, telemetry and system debug. The controller, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, fault status registers and the fault log. The final configuration can be quickly developed and stored to the LTC3880 EEPROM.

Figure 28 illustrates the application schematic for powering, programming and communication with one or more LTC3880s via the LTC I²C/SMBus/PMBus controller regardless of whether or not system power is present. If system power is not present the dongle will power the LTC3880 through the V_{DD33} supply pin. To initialize the part when V_{IN} is not applied and the V_{DD33} pin is powered use global address 5B command 0xBD data 0x2B followed by address 5B command 0xBD data 0xC4. The part can now be communicated with, and the project file updated. To write the updated project file to the NVM issue a STORE_USER_ALL command. When VIN is

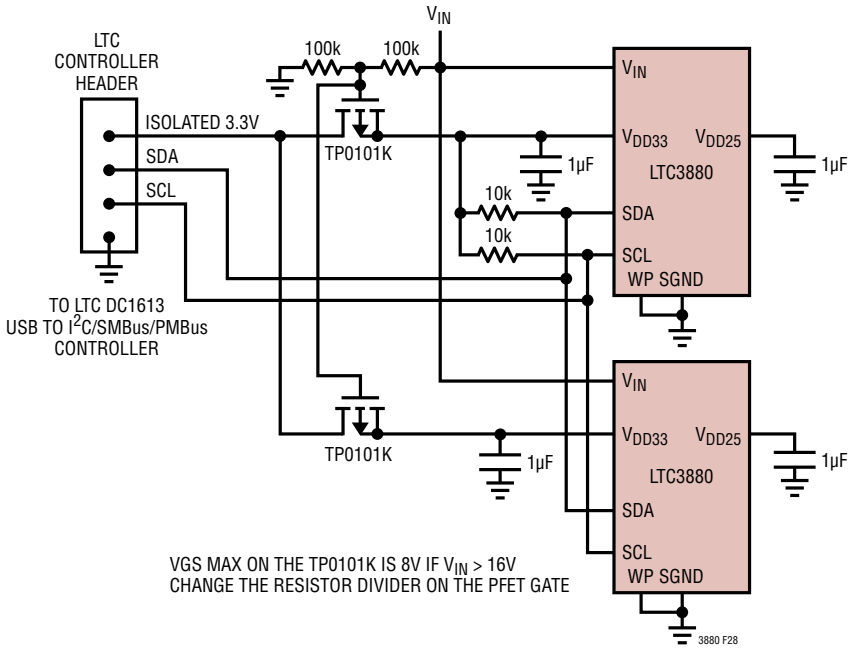

Figure 28. LTC Controller Connection

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APPLICATIONS INFORMATION

applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

Because of the controllers limited current sourcing capability, only the LTC3880s, their associated pull-up resistors and the I^2C pull-up resistors should be powered from the ORed 3.3V supply. In addition any device sharing the I^2C bus connections with the LTC3880 should not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication in the absence of system power. If VIN is applied the dongle will not supply the LTC3880s on the board. It is recommended the RUN pins be held low to avoid providing power to the load until the part is fully configured.

The LTC controller I^2C connections are optoisolated from the PC USB. The 3.3V from the controller and the LTC3880 V_{DD33} pin must be driven to each LTC3880 with a separate PFET. If V_{IN} is not applied, the V_{DD33} pins can be in parallel because the on-chip LDO is off. The controller 3.3V current limit is 100mA but typical V_{DD33} currents are under 15mA. The V_{DD33} does back drive the $INTV_{CC}/EXTV_{CC}$ pin. Normally this is not an issue if V_{IN} is open.

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER

LTpowerPlay is a powerful Windows-based development environment that supports Linear Technology digital power ICs including the LTC3880. The software supports a variety of different tasks. LTpowerPlay can be used to evaluate Linear Technology ICs by connecting to a demo board or the user application. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build multiple IC configuration files that can be

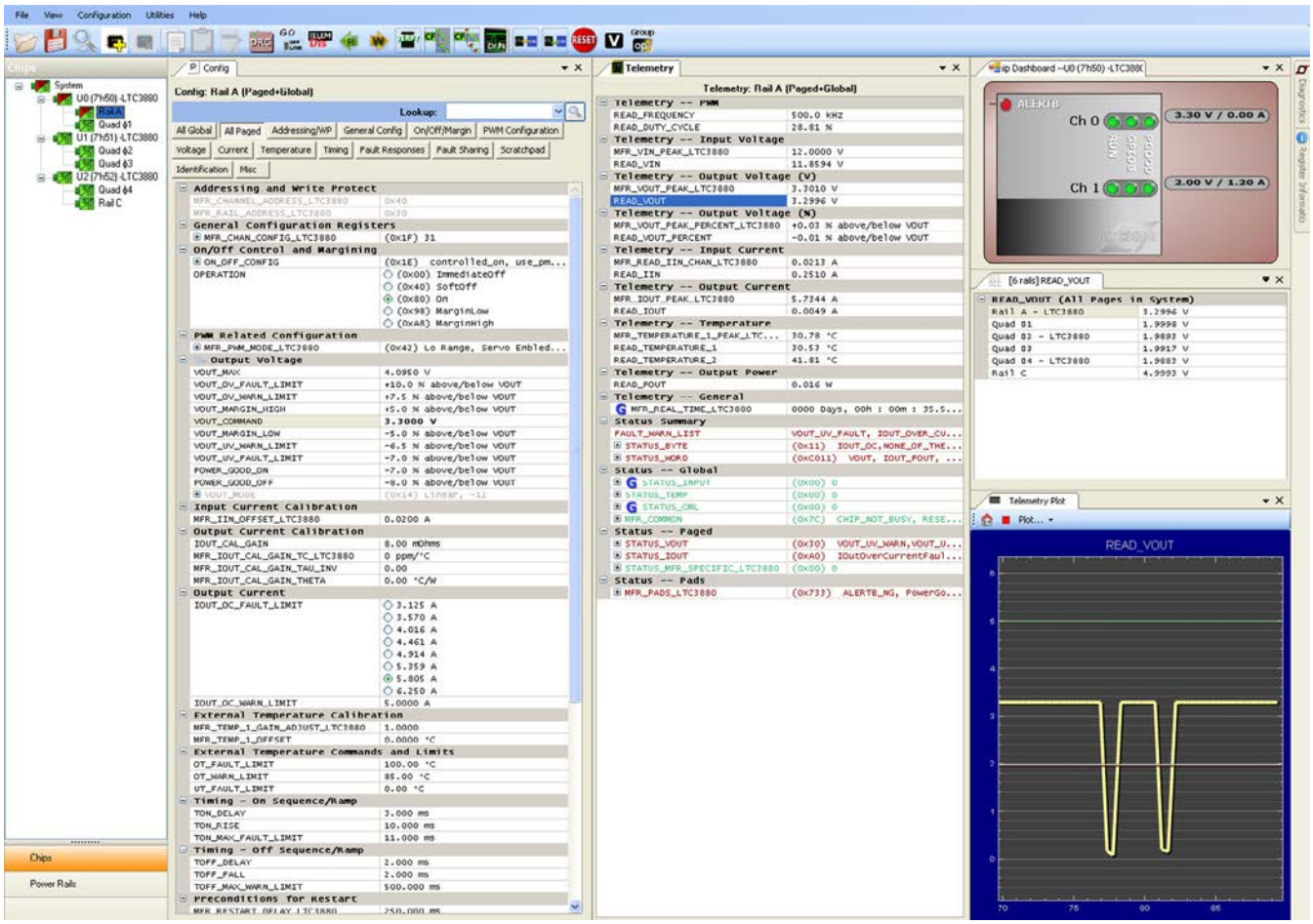

Figure 29.

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saved and re-loaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bring up rails. LTpowerPlay utilizes Linear Technology's USB-to-I^{2}C/SMBus/PMBus controller to communication with one of the many potential targets including the DC1590B-A/B demo board, the DC1709A socketed programming board, or a customer target system. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation. A great deal of context sensitive help is available with LTpowerPlay along with several tutorial demos. Complete information is available at http://www.linear.com/ltpowerplay.

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTC3880/LTC3880-1 have a one deep buffer to hold the last data written for each supported command prior to processing as shown in Figure 30; Write Command Data Processing. When the part receives a new command from the bus, it copies the data into the Write Command Data Buffer, indicates to the internal processor that this command data needs to be fetched, and converts the command to its internal format so that it can be executed.

Two distinct parallel blocks manage command buffering and command processing (fetch, convert, and execute) to ensure the last data written to any command is never lost. Command data buffering handles incoming PMBus writes by storing the command data to the Write Command Data Buffer and marking these commands for future processing. The internal processor runs in parallel and handles the sometimes slower task of fetching, converting and executing commands marked for processing.

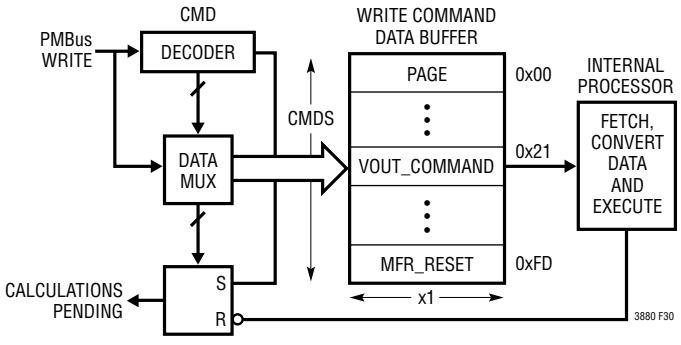

Figure 30. Write Command Data Processing

Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long relative to PMBus timing. If the part is busy processing a command, and new command(s) arrive, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in process via bit 5 of MFR_COMMON ('calculations not pending'). When the part is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 30 which ensures that commands are processed in order while simplifying error handling routines.

When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on part configuration it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and $\overline{\text{ALERT}}$ notification, or stretch the SCL clock low. For more information refer to PMBus Specification v1.1, Part II, Section 10.8.7 and SMBus v2.0 section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ALL_LTC3880. Clock stretching will only occur if enabled and the bus communication speed exceeds 100kHz.

PMBus busy protocols are well accepted standards, but can make writing system level software somewhat complex. The part provides three 'hand shaking' status bits which reduce complexity while enabling robust system level communication.

The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON ('chip not busy'). When the part is busy specifically because it is in a transitional VOUT state (margining hi/lo, power off/on, moving to a new output voltage set point, etc.) it will clear bit 4 of MFR_COMMON ('output not in transition'). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON ('calculations not pending'). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all

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three bits are set. A command immediately following the status bits being set will be accepted without NACKing or generating a BUSY fault/$\overline{\text{ALERT}}$ notification. The part can NACK commands for other reasons, however, as required by the PMBus spec (for instance, an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND register is provided in Figure 31.

```
// wait until bits 6, 5, and 4 of MFR_COMMON are all set
do
{
        mfrCommonValue = PMBUS_READ_BYTE(0xEF);
        partReady = (mfrCommonValue & 0x68) == 0x68;
}while(!partReady)

// now the part is ready to receive the next command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_COMMAND to 2V
```

Figure 31. Example of a Command Write of VOUT_COMMAND

It is recommended that all command writes (write byte, write word, etc.) be preceded with a polling loop to avoid the extra complexity of dealing with busy behavior and unwanted ALERTB notification. A simple way to achieve this is to create a SAFE_WRITE_BYTE() and SAFE_WRITE_WORD() subroutine. The above polling mechanism allows your software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases please refer to the application note section located at www.linear.com/designtools/app_notes.

When communicating using bus speeds at or below 100kHz, the polling mechanism shown here provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be configured to enable clock stretching. This requires a PMBus master that supports clock stretching. System software that detects and properly recovers from the standard PMBus NACK/BUSY faults as described in the PMBus Specification v1.1, Part II, Section 10.8.7 is required to communicate above 100kHz without clock stretching.

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PMBus COMMAND DETAILS

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F
MFR_CHANNEL_ADDRESS	0xD8	Address to the PAGE activated channel	R/W Byte	Y	Reg		Y	0x80
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80

PAGE

The page command provides the ability to configure, control and monitor both outputs through only one physical address. Each PAGE contains the Operating Memory for each output.

Pages 0x00 and 0x01 correspond to channel 0 and channel 1, respectively, in this device.

Setting the page to 0xFF means that the commands are to applied to both outputs. Performing READ commands with PAGE set to 0xFF will return the same value as PAGE 0. When PAGE is set to 0xFF there are no restrictions on R/W commands.

This command has one data byte.

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the LTC3880 device. This command does not indicate the status of the WP pin which is defined in the MFR_COMMON command. The WP pin takes precedence over the value of this command unless the WRITE_PROTECT command is more stringent.

BYTE	MEANING
0x80	Disable all writes except to the WRITE_PROTECT, PAGE_MFR_EE_UNLOCK and STORE_USER_ALL command
0x40	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, STORE_USER_ALL, OPERATION and CLEAR_FAULTS command. ndividual fault bits can be cleared by writing a 1 to the respective bits in the STATUS registers.
0x20	Disable all writes except to the WRITE_PROTECT, OPERATION, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, CLEAR_FAULTS, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and STORE_USER_ALL. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS registers.
0x10	Reserved, must be 0
0x08	Reserved, must be 0
0x04	Reserved, must be 0
0x02	Reserved, must be 0
0x01	Reserved, must be 0

Enable writes to all commands when WRITE_PROTECT is set to 0x00.

This command has one data byte.

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PMBus COMMAND DETAILS

If WP pin is high, PAGE, OPERATION, MFR_CLEAR_PEAKS, MFR_EE_UNLOCK and CLEAR_FAULTS commands are supported. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS registers.

MFR_ADDRESS

The MFR_ADDRESS command byte sets the 7 bits of the PMBus slave address for this device.

Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If RCONFIG is set to ignore, the ASEL pin is still used to determine the LSB of the channel address. If the ASEL pin is open, the LTC3880 will use the address value stored in NVM.

This command has one data byte.

MFR_CHANNEL_ADDRESS

The MFR_CHANNEL_ADDRESS command enables direct device address access to the PAGE activated channel. The value of this command should be unique on the PMBus and should not be the same as another channel or device.

If this command is not set to 0x80, a status condition specific to this channel will result in the Alert Response Address (ARA) value to be equal to the value of the MFR_CHANNEL_ADDRESS command.

Setting this command to a value of 0x80 disables channel device addressing for the channel.

This command has one data byte.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE activated channel. The value of this command should be common to all devices attached to a single power supply rail.

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTC3880 will detect bus contention and set a CML communications fault.

Setting this command to a value of 0x80 disables rail device addressing for the channel.

This command has one data byte.

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PMBus COMMAND DETAILS

GENERAL CONFIGURATION REGISTERS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_CHAN_CONFIG_LTC3880	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x1F
MFR_CONFIG_ALL_LTC3880	0xD1	Configuration bits that are common to all pages.	R/W Byte	N	Reg		Y	0x09

MFR_CHAN_CONFIG_LTC3880

General purpose configuration command common to multiple LTC products.

BIT	MEANING
7	Reserved
6	Reserved
5	Reserved
4	Disable RUN Low. When asserted the RUN pin is not pulsed low if commanded OFF
3	Short Cycle. When asserted the output will immediate off if commanded ON while waiting for TOFF_DELAY or TOFF_FALL. TOFF_MIN of 120mS is honored then the part will command ON.
2	SHARE_CLOCK control, if SHARE_CLOCK is held low, the output is disabled
1	No $\overline{\text{GPIO}}$ $\overline{\text{ALERT}}$, $\overline{\text{ALERT}}$ is not pulled low if $\overline{\text{GPIO}}$ is pulled low externally. Assert this bit if either POWER_GOOD or VOUT_UVUF (PGOOD) is propagated on $\overline{\text{GPIO}}$
0	Disables the VOUT decay value requirement for MFR_RETRY_TIME processing. When this bit is set to a 0, the output must decay to less than 12.5% of the programmed value for any action that turns off the rail including a fault, an OFF/ON command, or a toggle of RUN from high to low to high.

This command has one data byte.

MFR_CONFIG_ALL_LTC3880

General purpose configuration command common to multiple LTC products

BIT	MEANING
7	Enable Fault Logging
6	Ignore Resistor Configuration Pins
5	Reserved, set to 1
4	Reserved
3	Mask PLL Unlock Fault
2	PMBus command writes require a valid Packet Error Checking, PEC, byte to be accepted.*
1	Enable the use of PMBus clock stretching
0	Enables a low to high transition on either RUN pin to issue a CLEAR_FAULTS command

*PMBus command writes that have a valid PEC byte are always processed. PMBus command writes that have an invalid PEC byte are not processed and set a CML status fault.

This command has one data byte.

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PMBus COMMAND DETAILS

ON/OFF/MARGIN

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80
MFR_RESET	0xFD	Commanded reset without requiring a power-down.	Send Byte	N				NA

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of RUN*n* pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied.

Table 3. Supported Values:

VALUE	MEANING
0x1F	OPERATION value and RUN*n* pin must both command the device to start/run. Device executes immediate off when commanded off.
0x1E	OPERATION value and RUN*n* pin must both command the device to start/run. Device uses TOFF_command values when commanded off.
0x17	RUN*n* pin control with immediate off when commanded off. OPERATION on/off control ignored.
0x19	RUN*n* pin control using TOFF_command values when commanded off. OPERATION on/off control ignored.

Note: A high on the RUN pin is always required to start power conversion. Power conversion will always stop with a low on RUN.

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault and the command will be ignored.

This command has one data byte.

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PMBus COMMAND DETAILS

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the RUN*n* pins. It is also used to cause the unit to set the output voltage to the upper or lower MARGIN VOLTAGEs. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the RUN*n* pin instructs the device to change to another mode. If the part is stored in the MARGIN_LOW/HIGH state, the next RESET or POWER_ON cycle will ramp to that state. If the OPERATION command is modified, for example ON is changed to MARGIN_LOW, the output will move at a fixed slope set by the VOUT_TRANSITION_RATE.

Margin High (Ignore Faults) and Margin Low (Ignore Faults) operations are not supported by the LTC3880.

The part defaults to the ON state.

This command has one data byte.

Table 4. OPERATION Command Detail Register OPERATION Data Contents When On_Off_Config_Use_PMBus Enables Operation_Control

SYMBOL	Action	Value
BITS		
FUNCTION	Turn off immediately	0x00
	Turn on	0x80
	Margin Low	0x98
	Margin High	0xA8
	Sequence off	0x40

OPERATION Data Contents When On_Off_Config is Configured Such That OPERATION Command Is Not Used to Command Channel On or Off

SYMBOL	Action	Value
BITS		
FUNCTION	Output at Nominal	0x80
	Margin Low	0x98
	Margin High	0xA8

Note: Attempts to write a reserved value will cause a CML fault.

MFR_RESET

This command provides a means by which the user can perform a reset of the LTC3880.

This write-only command has no data bytes.

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PMBus COMMAND DETAILS

PWM CONFIG

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_PWM_MODE_LTC3880	0xD4	Configuration for the PWM engine of each channel	R/W Byte	Y	Reg		Y	0xC2
MFR_PWM_CONFIG_LTC3880	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10
FREQUENCY_SWITCH	0x33	Switching frequency of the controller	R/W Word	N	L11	kHz	Y	350 0xFABC

MFR_PWM_MODE_LTC3880

The MFR_PWM_MODE_LTC3880 command allows the user to program the PWM controller to use Burst Mode operation, discontinuous (pulse-skipping mode), or forced continuous conduction mode.

BIT	MEANING
7	Use High Range of I_{LIMIT} 0 – Low Current Range 1 – High Current Range
6	Enable Servo Mode
5	Reserved
4	Reserved
3	Reserved
2	Reserved
Bit[1:0]	Mode
00b	Discontinuous
01b	Burst Mode Operation
10b	Forced Continuous

Whenever the channel is ramping on, the PWM mode will be discontinuous, regardless of the value of this command.

Bit [7] of this command determines if the part is in high range or low range of the IOUT_OC_FAULT_LIMIT command. Changing this bit value changes the PWM loop gain and compensation. Changing this bit value whenever an output is active may have detrimental system results.

Bit [6] The LTC3880 will not servo while the part is OFF, ramping on or ramping off. When set to a one, the output servo is enabled. The output set point DAC will be slowly adjusted to minimize the difference between the READ_VOUT_ADC and the VOUT_COMMAND (or the appropriate margined value).

This command has one data byte.

MFR_PWM_CONFIG_LTC3880

The MFR_PWM_CONFIG_LTC3880 command sets the switching frequency phase offset with respect to the falling edge of the SYNC signal. The part must be in the OFF state to process this command. Either the RUN pins must be low or the part must be commanded off. If the part is in the RUN state and this command is written, the command will be ignored and a BUSY fault will be asserted. Bits 5 and 6 of this command affect the loop gain of the respective channels which may require modifications to the external compensation network.

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PMBus COMMAND DETAILS

BIT	MEANING	
7	Reserved, set to 0.	
6	If V_{OUT0} RANGE = 1, the maximum output voltage for V0 is 2.75V. If RANGE = 0, the maximum output voltage for V0 is 4.096V.	
5	If V_{OUT1} RANGE = 1, the maximum output voltage for V1 is 2.75V. If RANGE = 0, the maximum output voltage for V1 is 5.5V.	
4	Share Clock Enable : If this bit is 1, the SHARE_CLK pin will not be released until V_{IN} > VIN_ON. The SHARE_CLK pin will be pulled low when V_{IN} < VIN_OFF. If this bit is 0, the SHARE_CLK pin will not be pulled low when VIN < VIN_OFF except for the initial application of VIN.	
3	Reserved	
BIT [2:0]	**CHANNEL 0 (DEGREES)**	**CHANNEL 1 (DEGREES)**
000b	0	180
001b	90	270
010b	0	240
011b	0	120
100b	120	240
101b	60	240
110b	120	300

This command has one data byte.

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets the switching frequency, in kHz, of a PMBus device.

Supported Frequencies:

VALUE [15:0]	RESULTING FREQUENCY (TYP)
0x0000	External Oscillator
0xF3E8	250kHz
0xFABC	350kHz
0xFB52	425kHz
0xFBE8	500kHz
0x023F	575kHz
0x028A	650kHz
0x02EE	750kHz
0x03E8	1000kHz

The part must be in the OFF state to process this command. Either the RUN pins must be low or the part must be commanded off. If the part is in the RUN state and this command is written, the command will be ignored and a BUSY fault will be asserted. When the part is commanded off and the frequency is changed, a PLL_UNLOCK status may be detected as the PLL locks onto the new frequency.

This command has two data bytes and is formatted in Linear_5s_11s format.

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PMBus COMMAND DETAILS

VOLTAGE

Input Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_ LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	15.5 0xD3E0
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	6.3 0xCB26
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	6.5 0xCB40
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	6.0 0xCB00

VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the measured input voltage, in volts, that causes an input overvoltage fault. The fault is detected with the A/D converter resulting in latency up to 90ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of the input voltage that causes an input undervoltage warning. The warning is detected with the A/D converter resulting in latency up to 90ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_ON

The VIN_ON command sets the input voltage, in volts, at which the unit should start power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

VIN_OFF

The VIN_OFF command sets the input voltage, in volts, at which the unit should stop power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

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PMBus COMMAND DETAILS

Output Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-2} 0x14
VOUT_MAX	0x24	Upper limit on the commanded output voltage including VOUT_MARGIN_HIGH.	R/W Word	Y	L16	V	Y	4.096 Ch0 0x4189 5.5 Ch1 0x5800
VOUT_OV_FAULT_ LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A
VOUT_OV_WARN_ LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33
VOUT_UV_WARN_ LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD
VOUT_UV_FAULT_ LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	0.93 0x0EE1
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted.	R/W Word	Y	L16	V	Y	0.92 0x0EB8
MFR_VOUT_MAX	0xA5	Maximum allowed voltage command including VOUT_OV_FAULT_LIMIT.	R Word	Y	L16	V		4.096 Ch0 5.5 Ch1

VOUT_MODE

The data byte for VOUT_MODE command, used for commanding and reading output voltage, consists of a 3-bit mode (only linear format is supported) and a 5-bit parameter representing the exponent used in output voltage Read/Write commands.

This read-only command has one data byte

VOUT_MAX

The VOUT_MAX command sets an upper limit on the output voltage, including VOUT_MARGIN_HIGH, the unit can command regardless of any other commands or combinations.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured at the sense pins, in volts, which causes an output overvoltage fault.

If the VOUT_OV_FAULT_LIMIT is modified and the switcher is active, allow 10ms after the command is modified to assure the new value is being honored. The part indicates if it is busy making a calculation. Monitor bits 5 and 6 of

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MFR_COMMON. Either bit is low if the part is busy. If this wait time is not met, and the VOUT_COMMAND is modified above the old overvoltage limit, an OV condition might temporarily be detected resulting in undesirable behavior and possible damage to the switcher.

If VOUT_OV_FAULT_RESPONSE is set to OV_PULLDOWN, the $\overline{\text{GPIO}}$ pin will not assert if VOUT_OV_FAULT is propagated. The LTC3880 will pull the TG low and assert the BG bit as soon as the overvoltage condition is detected.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured at the sense pins, in volts, which causes an output voltage high warning. The READ_VOUT value will be used to determine if this limit has been exceeded.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Overvoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This condition is detected by the ADC so the response time may be up to 90ms.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to “Margin High”. The value must be greater than VOUT_COMMAND.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_COMMAND

The VOUT_COMMAND consists of two bytes and is used to set the output voltage, in volts.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to “Margin Low”. The value must be less than VOUT_COMMAND.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

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PMBus COMMAND DETAILS

VOUT_UV_WARN_LIMIT

The VOUT_UV_ WARN_LIMIT command reads the value of the output voltage measured at the sense pins, in volts, which causes an output voltage low warning.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Undervoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This condition is detected by the ADC so the response time may be up to 90ms.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command reads the value of the output voltage measured at the sense pins, in volts, which causes an output undervoltage fault.

This command has two data bytes and is formatted in Linear_16u format.

POWER_GOOD_ON

The POWER_GOOD_ON command sets the output voltage at which the POWER_GOOD signal should be asserted. POWER_GOOD_ON is detected with an A/D read resulting in latency of up to 90ms.

This command has two data bytes and is formatted in Linear_16u format.

POWER_GOOD_OFF

The POWER_GOOD_OFF command sets the output voltage at which the POWER_GOOD signal should be negated. POWER_GOOD_OFF is detected with an A/D read resulting in latency of up to 90ms. At initial power up the output of this pin will be high even though the state should be low. If the proper state at power-up is required, place a Schottky diode between RUN and $\overline{\text{GPIO}}$. The Anode must be tied to $\overline{\text{GPIO}}$ and the Cathode to RUN.

The POWER_GOOD_ON status is masked from initiating an $\overline{\text{ALERT}}$. The POWER_GOOD status bit in the STATUS_WORD command is always reflective of VOUT wrt. the POWER_GOOD threshold.

This command has two data bytes and is formatted in Linear_16u format.

MFR_VOUT_MAX

The MFR_VOUT_MAX command is the maximum output voltage in volts for each channel including VOUT_OV_FAULT_LIMIT. If the output voltages are set to high range (Bits 5 and 6 of MFR_PWM_CONFIG_LTC3880 set to a 0) MFR_VOUT_MAX for channel 0 is 4.096V and MFR_VOUT_MAX for channel 1 is 5.5V. If the output voltages are set to low range (Bits 5 and 6 of MFR_PWM_CONFIG_LTC3880 set to a 1) the MFR_VOUT_MAX for both channels is 2.75V. Entering VOUT_COMMAND values greater than this will result in a CML fault and the output voltage setting will be clamped to the maximum level.

This read-only command has 2 data bytes and is formatted in Linear_16u format.

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PMBus COMMAND DETAILS

CURRENT

Input Current Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_IIN_OFFSET	0xE9	Coefficient used to add to the input current to account for the IQ of the part.	R/W Word	Y	L11	A	Y	0.050 0x9333

MFR_IIN_OFFSET

The MFR_IIN_OFFSET command allows the user to set an input current representing the quiescent current of each channel. For accurate results at low output current, the part should be in continuous conduction mode.

This command has 2 data bytes and is formatted in Linear_5s_11s format.

Output Current Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_CAL_GAIN	0x38	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R/W Word	Y	L11	mΩ	Y	1.8 0xBB9A
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF		Y	3900 0x0F3C

IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the resistance value of the current sense resistor in milliohms. (see also MFR_IOUT_CAL_GAIN_TC).

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC command allows the user to program the temperature coefficient of the IOUT_CAL_GAIN sense resistor or inductor DCR in ppm/°C.

This command has two data bytes and is formatted in 16-bit 2's complement integer ppm. N = –32768 to 32767 • 10^{-6}. Nominal temperature is 27°C. The IOUT_CAL_GAIN is multiplied by:

[1.0 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERATURE_1-27)]. DCR sensing will have a typical value of 3900.

The IOUT_CAL_GAIN and MFR_IOUT_CAL_GAIN_TC impact all current parameters including: READ_IOUT, READ_IIN, IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT.

Input Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IIN_OC_WARN_LIMIT	0x5D	Input overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280

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PMBus COMMAND DETAILS

IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current, in amperes, that causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded.

In response to the IIN_OC_WARN_LIMIT being exceeded, the device:

- Sets the OTHER bit in the STATUS_BYTE
- Sets the INPUT bit in the upper byte of the STATUS_WORD
- Sets the IIN Overcurrent Warning bit in the STATUS_INPUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This condition is detected by the ADC so the response time may be up to 90ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

Output Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	29.75 0xDBB8
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	20.0 0xDA80

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the peak output current limit, in amperes. When the controller is in current limit, the overcurrent detector will indicate an overcurrent fault condition. The programmed overcurrent fault limit value is rounded up to the nearest one of the following set of discrete values:

25mV/IOUT_CAL_GAIN	Low Range (1.5x Nominal Loop Gain)
28.6mV/IOUT_CAL_GAIN	MFR_PWM_MODE_LTC3880 [7]=0
32.1mV/IOUT_CAL_GAIN	
35.7mV/IOUT_CAL_GAIN	
39.3mV/IOUT_CAL_GAIN	
42.9mV/IOUT_CAL_GAIN	
46.4mV/IOUT_CAL_GAIN	
50mV/IOUT_CAL_GAIN	
37.5mV/IOUT_CAL_GAIN	High Range (Nominal Loop Gain)
42.9mV/IOUT_CAL_GAIN	MFR_PWM_MODE_LTC3880 [7]=1
48.2mV/IOUT_CAL_GAIN	
53.6mV/IOUT_CAL_GAIN	
58.9mV/IOUT_CAL_GAIN	
64.3mV/IOUT_CAL_GAIN	
69.6mV/IOUT_CAL_GAIN	
75mV/IOUT_CAL_GAIN	

Note: This is the peak of the current waveform. The READ_IOUT command returns the average current. The peak output

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PMBus COMMAND DETAILS

current limits are adjusted with temperature based on the MFR_IOUT_CAL_GAIN_TC using the equation:

IOUT_OC_FAULT_LIMIT = IOUT_CAL_GAIN • (1 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERTURE_1-27.0)).

The LTpowerPlay GUI automatically convert the voltages to currents.

The I_{OUT} range is set with bit 7 of the MFR_PWM_MODE_LTC3880 command.

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format.

IOUT_OC_WARN_LIMIT

This command sets the value of the output current that causes an output overcurrent warning in amperes. The READ_IOUT value will be used to determine if this limit has been exceeded.

In response to the IOUT_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Warning bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This condition is detected by the ADC so the response time may be up to 90ms.

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format

TEMPERATURE

External Temperature Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	1 0x4000
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor with respect to –273.1°C.	R/W Word	Y	L11	C	Y	0 0x8000

MFR_TEMP_1_GAIN

The MFR_TEMP_1_GAIN command will modify the slope of the external temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in 16-bit 2's complement integer. N = 8192 to 32767. The effective adjustment is N • 2^{-14}. The nominal value is 1.

MFR_TEMP_1_OFFSET

The MFR_TEMP_1_OFFSET command will modify the offset of the external temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

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This command has two data bytes and is formatted in Linear_5s_11s format. The part starts the calculation with a value of –273.15 so the default adjustment value is zero.

External Temperature Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	100.0 0xEB20
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	85.0 0xEAA8
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	–40.0 0xE580

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the external sense temperature, in degrees Celsius, which causes an overtemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

This condition is detected by the ADC so the response time may be up to 90ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of the external sense temperature, in degrees Celsius, which causes an overtemperature warning. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

In response to the OT_WARN_LIMIT being exceeded, the device:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Overtemperature Warning bit in the STATUS_TEMPERATURE command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin.

This condition is detected by the ADC so the response time may be up to 90ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

UT_FAULT_LIMIT

The UT_FAULT_LIMIT command sets the value of the external sense temperature, in degrees Celsius, which causes an undertemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

Note: If the temp sensors are not installed, the UT_FAULT_LIMIT can be set to –275°C and UT_FAULT_LIMIT response set to ignore to avoid $\overline{\text{ALERT}}$ being asserted.

This condition is detected by the ADC so the response time may be up to 90ms.

Values of greater than 0.1V/ms and less than or equal to 1V/ms are recommended. If a transition rate out of this range is desired, contact the factory for more information.

This command has two data bytes and is formatted in Linear_5s_11s format.

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PMBus COMMAND DETAILS

TIMING

Timing—On Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	L11	ms	Y	8.0 0xD200
TON_MAX_FAULT_LIMIT	0x62	Maximum time from V_{OUT_EN} on for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	10.0 0xD280
VOUT_TRANSITION_RATE	0x27	Rate the output changes when VOUT commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0xAA00

TON_DELAY

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise. Values from 0ms to 83 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_RISE

The TON_RISE command sets the time, in milliseconds, from the time the output starts to rise to the time the output enters the regulation band. Values from 0 to 1.3 seconds are valid. The part will be in discontinuous mode during TON_RISE events. If TON_RISE is less than 0.25ms, the LTC3880 digital slope will be bypassed. The output voltage transition will be controlled by the analog performance of the PWM switcher. The maximum allowed slope is 4V/ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit.

A data value of 0ms means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely. The maximum limit is 83 seconds.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOUT_TRANSITION_RATE

When a PMBus device receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low) that causes the output voltage to change this command set the rate in V/ms at which the output voltage changes. This commanded rate of change does not apply when the unit is commanded on or off.

Values of greater than 0.1V/ms are recommended.

This command has two data bytes and is formatted in Linear_5s_11s format.

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PMBus COMMAND DETAILS

Timing—Off Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	8.0 0xD200
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	150 0xF258

TOFF_DELAY

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received until the output voltage starts to fall. Values from 0 to 83 seconds are valid.

This command is excluded from fault events.

This command has two data bytes and is formatted in Linear_5s_11s format.

TOFF_FALL

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the output voltage is commanded to zero. It is the ramp time of the V_{OUT} DAC. When the V_{OUT} DAC is zero, the part will three-state.

The part will maintain the mode of operation programmed. For defined TOFF_FALL times, the user should set the part to continuous conduction mode. Loading the max value indicates the part will ramp down at the slowest possible rate. The minimum supported fall time is 0.25ms. A value less than 0.25ms will result in a 0.25ms ramp. The maximum fall time is 1.3 seconds. The maximum allowed slope is 4V/ms.

In discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current.

This command has two data bytes and is formatted in Linear_5s_11s format.

TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to turn off the output until a warning is asserted. The output is considered off when the V_{OUT} voltage is less than 12.5% of the programmed VOUT_COMMAND value. The calculation begins after TOFF_FALL is complete. TOFF_MAX_WARN is not enabled in VOUT_DECAY is disabled.

A data value of 0ms means that there is no limit and that the unit can attempt to turn off the output voltage indefinitely. Other than 0, values from 120ms to 524 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

Precondition for Restart

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RESTART_ DELAY	0xDC	Delay from actual RUN active edge to virtual RUN active edge.	R/W Word	Y	L11	ms	Y	500 0xFBE8

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MFR_RESTART_DELAY

This command specifies the minimum RUN off time in milliseconds. This device will pull the RUN pin low for this length of time once a falling edge of RUN has been detected. The minimum recommended value is 136ms.

Note: The restart delay is different than the retry delay. The restart delay pulls run low for the specified time, after which a standard start-up sequence is initiated. The minimum restart delay should be equal to TOFF_DELAY + TOFF_FALL + 136ms. Valid values are from 136ms to 65.52 seconds in 16ms increments. To assure a minimum off time, set the MFR_RESTART_DELAY 16ms longer than the desired time. The output rail can be off longer than the MFR_RESTART_DELAY after the RUN pin is pulled high if the output decay bit 1 is enabled in MFR_CHAN_CONFIG_LTC3880 and the output takes a long time to decay below 12.5% of the programmed value.

This command has two data bytes and is formatted in Linear_5s_11s format.

FAULT RESPONSE

Fault Responses All Faults

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RETRY_ DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	350 0xFABC

MFR_RETRY_DELAY

This command sets the time in milliseconds between restarts if the fault response is to retry the controller at specified intervals. This command value is used for all fault responses that require retry. The retry time starts once the fault has been detected by the offending channel. Valid values are from 120ms to 83.88 seconds in 10µs increments.

Note: The retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG_LTC3880.

This command has two data bytes and is formatted in Linear_5s_11s format.

Fault Responses Input Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input supply overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The data byte is in the format given in Table 9.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD

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• Sets the VIN Overvoltage Fault bit in the STATUS_INPUT command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This command has one data byte.

Fault Responses Output Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
TON_MAX_FAULT_ RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. The data byte is in the format given in Table 5.

The device also:

• Sets the VOUT_OV bit in the STATUS_BYTE

• Sets the VOUT bit in the STATUS_WORD

• Sets the VOUT Overvoltage Fault bit in the STATUS_VOUT command

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin

The only value recognized for this command are:

0x80–The device shuts down (disables the output) and the unit does not attempt to retry. The output remains disabled until the fault is cleared (PMBus, Part II, Section 10.7).

0xB8–The device shuts down (disables the output) and device attempts retry continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.

0x4n The device shuts down and the unit does not attempt to retry. The output remains disabled until the part is commanded OFF then ON or the RUN pin is asserted low then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

0x78+n The device shuts down and the unit attempts to retry continuously until either the fault condition is cleared or the part is commanded OFF then ON or the RUN pin is asserted low then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

Any other value will result in a CML fault and the write will be ignored.

This command has one data byte.

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PMBus COMMAND DETAILS

Table 5. VOUT_OV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3880: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC3880.	00	Part performs OV pull down only (i.e., turns off the top MOSFET and turns on lower MOSFET while V_{OUT} is > VOUT_OV_FAULT)
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000-110	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. The data byte is in the format given in Table 6.

The device also:

• Sets the VOUT bit in the STATUS_WORD

• Sets the VOUT undervoltage fault bit in the STATUS_VOUT command

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin

The UV fault and warn are masked until the following criteria are achieved:

1) The TON_MAX_FAULT_LIMIT has been reached

2) The TON_DELAY sequence has completed

3) The TON_RISE sequence has completed

4) The VOUT_UV_FAULT_LIMIT threshold has been reached

5) The IOUT_OC_FAULT_LIMIT is not present

The UV fault and warn are masked whenever the channel is not active.

The UV fault and warn are masked during TON_RISE and TOFF_FALL sequencing.

This command has one data byte.

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PMBus COMMAND DETAILS

Table 6. VOUT_UV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3880: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC3880	00	The PMBus device continues operation without interruption. (Ignores the fault functionally)
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000-110	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.

TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault. The data byte is in the format given in Table 9.

The device also:

• Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE

• Sets the VOUT bit in the STATUS_WORD

• Sets the TON_MAX_FAULT bit in the STATUS_VOUT command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin

• A value of 0 disables the TON_MAX_FAULT_RESPONSE. It is not recommended to use 0.

This command has one data byte.

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PMBus COMMAND DETAILS

Fault Responses Output Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault. The data byte is in the format given in Table 7.

The device also:

- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Fault bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This command has one data byte.

Table 7. IOUT_OC_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3880: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC3880.	00	The LTC3880 continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage (known as constant-current or brick-wall limiting).
		01	Not supported.
		10	The LTC3880 continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage, for the delay time set by bits [2:0]. If the device is still operating in current limit at the end of the delay time, the device responds as programmed by the Retry Setting in bits [5:3].
		11	The LTC3880 shuts down immediately and responds as programmed by the Retry Setting in bits [5:3].
5:3	Retry Setting	000-110	The unit does not attempt to restart. The output remains disabled until the fault is cleared by cycling the RUN*n* pin or removing bias power.
		111	The device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	The number of delay time units in 16ms increments. This delay time is used to determine the amount of time a unit is to continue operating after a fault is detected before shutting down. Only valid for deglitched off state.

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PMBus COMMAND DETAILS

Fault Responses IC Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected	R Byte	N	Reg			0xC0

MFR_OT_FAULT_RESPONSE

The MFR_OT_FAULT_RESPONSE command byte instructs the device on what action to take in response to an internal overtemperature fault. The data byte is in the format given in Table 8.

The LTC3880 also:

- Sets the MFR bit in the STATUS_WORD, and
- Sets the Overtemperature Fault bit in the STATUS_MFR_SPECIFIC command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This command has one data byte.

Table 8. Data Byte Contents MFR_OT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC3880: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC3880	00	Not supported. Writing this value will generate a CML fault.
		01	Not supported. Writing this value will generate a CML fault
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared.
		001-111	Not supported. Writing this value will generate CML fault.
2:0	Delay Time	XXX	Not supported. Value ignored

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PMBus COMMAND DETAILS

Fault Responses External Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_ RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8
UT_FAULT_ RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an external overtemperature fault on the external temp sensors. The data byte is in the format given in Table 9.

The device also:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Overtemperature Fault bit in the STATUS_TEMPERATURE command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This condition is detected by the ADC so the response time may be up to 90ms.

This command has one data byte.

UT_FAULT_RESPONSE

The UT_FAULT_RESPONSE command instructs the device on what action to take in response to an external undertemperature fault on the external temp sensors. The data byte is in the format given in Table 9.

The device also:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Undertemperature Fault bit in the STATUS_TEMPERATURE command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This condition is detected by the ADC so the response time may be up to 90ms.

This command has one data byte.

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PMBus COMMAND DETAILS

Table 9. Data Byte Contents: TON_MAX_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, OT_FAULT_RESPONSE, UT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response	00	The PMBus device continues operation without interruption.
	For all values of bits [7:6], the LTC3880: • Sets the corresponding fault bit in the status commands, and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin	01	Not supported. Writing this value will generate a CML fault.
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
	The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command • The output is commanded through the RUN*n* pin, the OPERATION command, or the combined action of the RUN*n* pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC3880	11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000-110	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	Not supported. Values ignored

FAULT SHARING

Fault Sharing Propagation

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_GPIO_ PROPAGATE_LTC3880	0xD2	Configuration that determines which faults are propagated to the $\overline{\text{GPIO}}$ pins.	R/W Word	Y	Reg		Y	0x2993

MFR_GPIO_PROPAGATE_LTC3880

The MFR_GPIO_PROPAGATE_LTC3880 command enables the faults that can cause the $\overline{\text{GPIO}}$*n* pin to assert low. The command is formatted as shown in Table 10. Faults can only be propagated to the $\overline{\text{GPIO}}$ if they are programmed to respond to faults.

This command has two data bytes.

Table 10: $\overline{\text{GPIO}}$*n* Propagate Fault Configuration

The $\overline{\text{GPIO0}}$ and $\overline{\text{GPIO1}}$ pins are designed to provide electrical notification of selected events to the user. Some of these events are common to both output channels. Others are specific to an output channel. They can also be used to share faults between channels.

BIT(S)	SYMBOL	OPERATION
B[15]	VOUT disabled while not decayed.	This is used in a PolyPhase configuration when bit 0 of the MFR_CHAN_CONFIG_LTC3880 is a zero. If the channel is turned off, by toggling the RUN pin or commanding the part OFF, and then the RUN is reasserted or the part is commanded back on before the output has decayed, VOUT will not restart until the 12.5% decay is honored. The $\overline{\text{GPIO}}$ pin is asserted during this condition if bit 15 is asserted.

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PMBus COMMAND DETAILS

BIT(S)	SYMBOL	OPERATION
B[14]	Mfr_gpio_propagate_short_CMD_cycle	0: No action 1: Asserts low if commanded off then on before the output has sequenced off. Re-asserts high 120ms after sequence off.
b[13]	Mfr_gpio_propagate_ton_max_fault	0: No action if a TON_MAX_FAULT fault is asserted 1: Associated output will be asserted low if a TON_MAX_FAULT fault is asserted $\overline{\text{GPIO0}}$ is associated with page 0 TON_MAX_FAULT faults $\overline{\text{GPIO1}}$ is associated with page 1 TON_MAX_FAULT faults
b[12]	Mfr_gpio0_propagate_vout_uvuf, Mfr_gpio1_propagate_vout_uvuf	Unfiltered VOUT_UV_FAULT_LIMIT (PGOOD) comparator output $\overline{\text{GPIO0}}$ is associated with channel 0 $\overline{\text{GPIO1}}$ is associated with channel 1
b[11]	Mfr_gpio0_propagate_int_ot, Mfr_gpio1_propagate_int_ot	0: No action if the MFR_OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the MFR_OT_FAULT_LIMIT fault is asserted
b[10]	Reserved	Always set to 0
b[9]	Reserved	Always set to 0
b[8]	Mfr_gpio0_propagate_ut, Mfr_gpio1_propagate_ut	0: No action if the UT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the UT_FAULT_LIMIT fault is asserted $\overline{\text{GPIO0}}$ is associated with page 0 UT faults $\overline{\text{GPIO1}}$ is associated with page 1 UT faults
b[7]	Mfr_gpio0_propagate_ot, Mfr_gpio1_propagate_ot	0: No action if the OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the OT_FAULT_LIMIT fault is asserted $\overline{\text{GPIO0}}$ is associated with page 0 OT faults $\overline{\text{GPIO1}}$ is associated with page 1 OT faults
b[6]	Reserved	
b[5]	Reserved	
b[4]	Mfr_gpio0_propagate_input_ov, Mfr_gpio1_propagate_input_ov	0: No action if the VIN_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VIN_OV_FAULT_LIMIT fault is asserted
b[3]	Reserved	
b[2]	Mfr_gpio0_propagate_iout_oc, Mfr_gpio1_propagate_iout_oc	0: No action if the IOUT_OC_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the IOUT_OC_FAULT_LIMIT fault is asserted $\overline{\text{GPIO0}}$ is associated with page 0 OC faults $\overline{\text{GPIO1}}$ is associated with page 1 OC faults
b[1]	Mfr_gpio0_propagate_vout_uv, Mfr_gpio1_propagate_vout_uv	0: No action if the VOUT_UV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_UV_FAULT_LIMIT fault is asserted $\overline{\text{GPIO0}}$ is associated with page 0 UV faults $\overline{\text{GPIO1}}$ is associated with page 1 UV faults
b[0]	Mfr_gpio0_propagate_vout_ov, Mfr_gpio1_propagate_vout_ov	0: No action if the VOUT_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_OV_FAULT_LIMIT fault is asserted $\overline{\text{GPIO0}}$ is associated with page 0 OV faults $\overline{\text{GPIO1}}$ is associated with page 1 OV faults

Note 1: The PWRGD status is designed as an indicator and not to be used for power supply sequencing.

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PMBus COMMAND DETAILS

Fault Sharing Response

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_GPIO_RESPONSE	0xD5	Action to be taken by the device when the $\overline{\text{GPIO}}$ pin is asserted low.	R/W Byte	Y	Reg		Y	0xC0

MFR_GPIO_RESPONSE

This command determines the controller's response to the $\overline{\text{GPIO}}$*n* pin being pulled low by an external source.

VALUE	MEANING
0xC0	GPIO_INHIBIT The LTC3880 will three-state the output in response to the $\overline{\text{GPIO}}$ pin pulled low.
0x00	GPIO_IGNORE The LTC3880 continues operation without interruption.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the MFR bit in the STATUS_WORD
- Sets the GPIOB bit in the STATUS_MFR_SPECIFIC command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin. The $\overline{\text{ALERT}}$ pin pulled low can be disabled by setting bit[1] of MFR_CHAN_CFG_LTC3880.

This command has one data byte.

SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
USER_DATA_00	0xB0	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA
USER_DATA_02	0xB2	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_03	0xB3	A NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000
USER_DATA_04	0xB4	A NVM word available for the user.	R/W Word	N	Reg		Y	0x0000

USER_DATA_00 through *USER_DATA_04*

These commands are non-volatile memory locations for customer storage. The customer has the option to write any value to the USER_DATA_nn at any time. However, the LTpowerPlay software and contract manufacturers use some of these commands for inventory control. Modifying the reserved USER_DATA_nn commands may lead to undesirable inventory control and incompatibility with these products.

These commands have 2 data bytes and are in register format.

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PMBus COMMAND DETAILS

IDENTIFICATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0
MFR_ID	0x99	The manufacturer ID of the LTC3880 in ASCII.	R String	N	ASC			LTC
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTC3880
MFR_SERIAL	0x9E	Serial number of this specific unit in ASCII.	R Block	N	CF			NA
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTC3880.	R Word	N	Reg			402x

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTC3880 is PMBus Version 1.1 compliant in both Part I and Part II.

This read-only command has one data byte.

CAPABILITY

This command provides a way for a host system to determine some key capabilities of a PMBus device.

The LTC3880 supports packet error checking, 400kHz bus speeds, and $\overline{\text{ALERT}}$ pin.

This read-only command has one data byte.

MFR_ID

The MFR_ID command indicates the manufacturer ID of the LTC3880 using ASCII characters.

This read-only command is in block format.

MFR_MODEL

The MFR_MODEL command indicates the manufacturer's part number of the LTC3880 using ASCII characters.

This read-only command is in block format.

MFR_SERIAL

The MFR_SERIAL command contains up to 9 bytes of custom formatted data used to uniquely identify the LTC3880 configuration.

This read-only command is in block format.

MFR_SPECIAL_ID

The 16-bit word representing the part name. 0x402 denotes the part is an LTC3880, X is adjustable by the manufacturer.

This read-only command has 2 data bytes.

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PMBus COMMAND DETAILS

FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA
MFR_CLEAR_PEAKS	0xE3	Clears all peaks values.	Send Byte	N				NA
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA
STATUS_ TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMERATURE_1.	R/W Byte	Y	Reg			NA
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA
STATUS_MFR_ SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple LTC chips.	R Byte	N	Reg			NA
MFR_INFO	0xB6	Manufacturing specific information	R Byte	N	Reg			NA

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{ALERT}}$ pin signal output if the device is asserting the $\overline{\text{ALERT}}$ pin signal.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted when:

- The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or
- MFR_RESET command is issued.
- Bias power is removed and reapplied to the integrated circuit

If the fault is still present when the bit is cleared, the fault bit will remain set and the host notified by asserting the $\overline{\text{ALERT}}$ pin pin low. CLEAR_FAULTS can take up to 10µs to process. If a fault occurs within that time frame it may be cleared before the status register is set.

This write-only command has no data bytes.

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values. A reset will initiate this command.

This write-only command has no data bytes.

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PMBus COMMAND DETAILS

STATUS_BYTE

The STATUS_BYTE command returns a one-byte summary of the most critical faults.

STATUS_BYTE Message Contents:

BIT	STATUS BIT NAME	MEANING
7*	BUSY	A fault was declared because the LTC3880 was unable to respond.
6	OFF	This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled.
5	VOUT_OV	An output overvoltage fault has occurred.
4	IOUT_OC	An output overcurrent fault has occurred.
3	VIN_UV	Not supported (LTC3880 returns 0).
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0*	NONE OF THE ABOVE	A fault Not listed in bits[7:1] has occurred.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is typically the same as the STATUS_BYTE command: However, if a fault occurs at the exact right time, the read value can have a bit set in the lower byte with no corresponding bits set in the upper byte. An immediate second read of STATUS_WORD will have the corresponding bits in the upper byte set.

STATUS_WORD High Byte Message Contents:

BIT	STATUS BIT NAME	MEANING
15	V_{OUT}	An output voltage fault or warning has occurred.
14	I_{OUT}	An output current fault or warning has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A fault or warning specific to the LTC3880 has occurred.
11	POWER_GOOD#	The POWER_GOOD state is false if this bit is set.
10	FANS	Not supported (LTC3880 returns 0).
9	OTHER	Not supported (LTC3880 returns 0).
8	UNKNOWN	Not supported (LTC3880 returns 0).

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has two data bytes.

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PMBus COMMAND DETAILS

STATUS_VOUT

The STATUS_VOUT commands returns one byte of V_{OUT} status information.

STATUS_VOUT Message Contents:

BIT	MEANING
7	V_{OUT} overvoltage fault.
6	V_{OUT} overvoltage warning.
5	V_{OUT} undervoltage warning.
4	V_{OUT} undervoltage fault.
3	VOUT_MAX warning.
2	TON_MAX fault.
1	TOFF_MAX warning.
0	Not supported by the LTC3880 (returns 0).

$\overline{\text{ALERT}}$ can be asserted if any of bits[7:1] are set. These may be cleared by writing a 1 to their bit position in STATUS_VOUT, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_IOUT

The STATUS_IOUT commands returns one byte of I_{OUT} status information.

STATUS_IOUT Message Contents:

BIT	MEANING
7	I_{OUT} overcurrent fault.
6	Not supported (LTC3880 returns 0).
5	I_{OUT} overcurrent warning.
4:0	Not supported (LTC3880 returns 0).

$\overline{\text{ALERT}}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_IOUT, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

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PMBus COMMAND DETAILS

STATUS_INPUT

The STATUS_INPUT commands returns one byte of V_{IN} (VINSNS) status information.

STATUS_INPUT Message Contents:

BIT	MEANING
7	V_{IN} overvoltage fault.
6	Not supported (LTC3880 returns 0).
5	V_{IN} undervoltage warning.
4	Not supported (LTC3880 returns 0).
3	Unit off for insufficient V_{IN}.
2	Not supported (LTC3880 returns 0).
1	Input over current warning.
0	Not supported (LTC3880 returns 0)

$\overline{\text{ALERT}}$ can be asserted if bit 7 is set. Bit 7 may be cleared by writing it to a 1, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE commands returns one byte of sensed external temperature status information.

STATUS_TEMPERATURE Message Contents:

BIT	MEANING
7	External overtemperature fault.
6	External overtemperature warning.
5	Not supported (LTC3880 returns 0).
4	External undertemperature fault.
3:0	Not supported (LTC3880 returns 0).

$\overline{\text{ALERT}}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_TEMPERATURE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

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PMBus COMMAND DETAILS

STATUS_CML

The STATUS_CML commands returns one byte of status information on received commands, internal memory and logic.

STATUS_CML Message Contents:

BIT	MEANING
7	Invalid or unsupported command received.
6	Invalid or unsupported data received.
5	Packet error check failed.
4	Memory fault detected.
3	Processor fault detected.
2	Reserved (LTC3880 returns 0).
1	Other communication fault.
0	Other memory or logic fault.

$\overline{\text{ALERT}}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_CML, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC commands returns one byte with the manufacturer specific status information.

Each channel has a copy of the same information. Only bit 0 is page specific.

The format for this byte is:

BIT	MEANING
7	Internal Temperature Fault Limit Exceeded.
6	Internal Temperature Warn Limit Exceeded.
5	NVM CRC Fault.
4	PLL is Unlocked
3	Fault Log Present
2	V_{DD33} UV or OV Fault
0	$\overline{\text{GPIO}}$ Pin Asserted Low by External Device (paged)

If any of these bits are set, the MFR bit in the STATUS_WORD will be set.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command. Exception: The fault log present bit can only be cleared by issuing the MFR_FAULT_LOG_CLEAR command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

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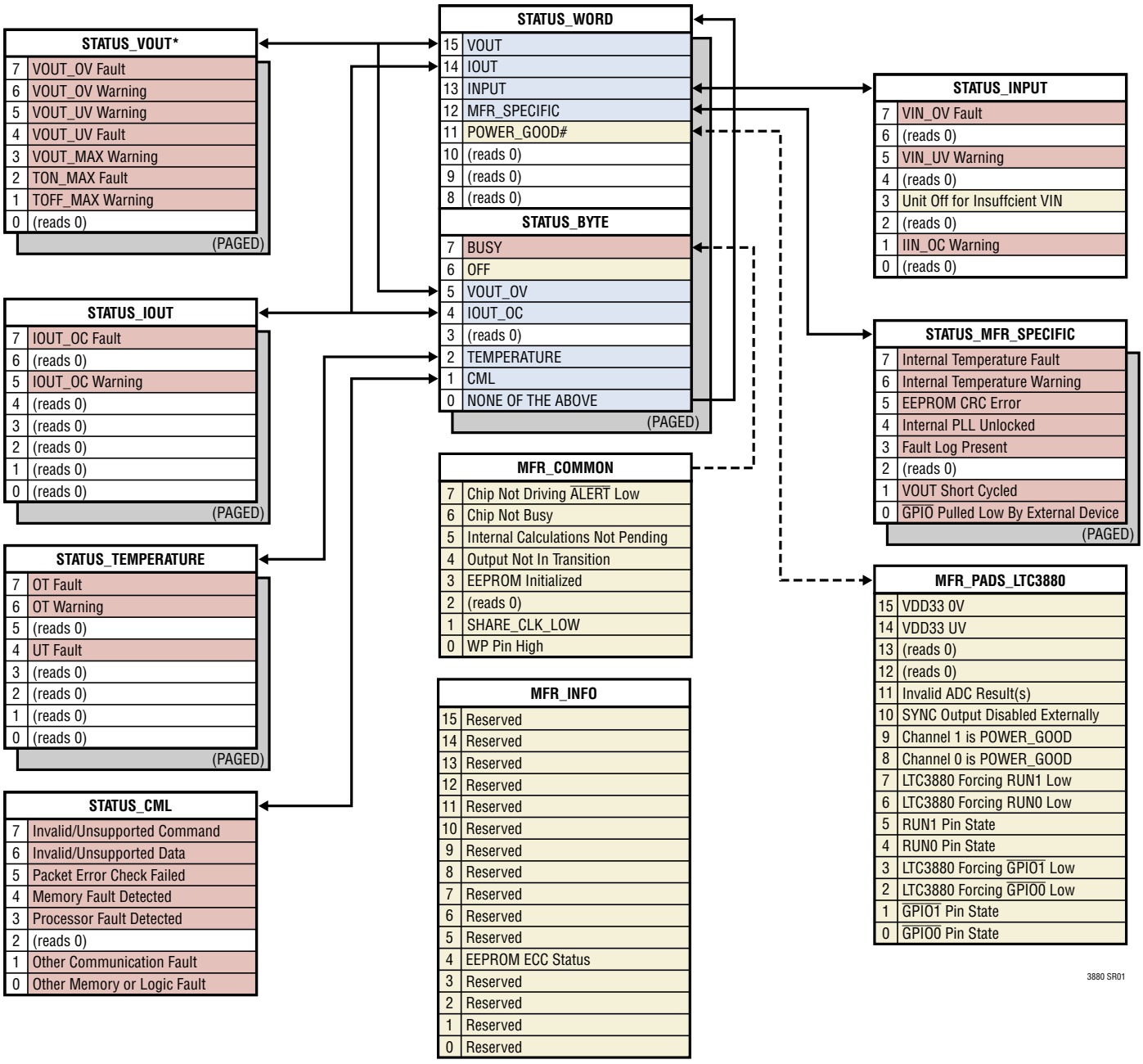
PMBus COMMAND DETAILS

Summary of the Status Registers



DESCRIPTION	MASKABLE	GENERATES ALERT	BIT CLEARABLE
General Fault or Warning Event	Yes	Yes	Yes
Dynamic	No	No	No
Status Derived from Other Bits	No	Not Directly	No

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PMBus COMMAND DETAILS

MFR_PADS

This command provides the user a means of directly reading the digital status of the I/O pins of the device. The bit assignments of this command are as follows:

BIT	ASSIGNED DIGITAL PIN
15	V_{DD33} OV Fault
14	V_{DD33} UV Fault
13	Reserved
12	Reserved
11	ADC Values Invalid, Occurs During Start-Up
10	Device Driving $\overline{\text{ALERT}}$ Low
9	PowerGood1
8	PowerGood0
7	Device Driving RUN1 Low
6	Device Driving RUN0 Low
5	RUN1
4	RUN0
3	Device Driving $\overline{\text{GPIO1}}$ Low
2	Device Driving $\overline{\text{GPIO0}}$ Low
1	$\overline{\text{GPIO1}}$
0	$\overline{\text{GPIO0}}$

A 1 indicates the condition is true.

This read-only command has two data bytes.

MFR_COMMON

The MFR_COMMON command contains bits that are common to all LTC digital power and telemetry products.

BIT	MEANING
7	CHIP NOT DRIVING ALERT LOW
6	CHIP NOT BUSY
5	CALCULATIONS NOT PENDING
4	OUTPUT NOT IN TRANSITION
3	NVM Initialized
2	Reserved
1	SHARE_CLK Timeout
0	WP Pin Status

This read-only command has one data byte.

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PMBus COMMAND DETAILS

MFR_INFO

The MFR_INFO command contains additional status bits that are LTC3880-specific and may be common to multiple LTC PSM products.

MFR_INFO Data Contents:

BIT	MEANING
15:6	Reserved.
5	EEPROM ECC status. 0: Corrections made in the EEPROM user space. 1: No corrections made in the EEPROM user space.
4:0	Reserved

EEPROM ECC status is updated after each RESTORE_USER_ALL or RESET command, a power-on reset or an EEPROM bulk read operation. This read-only command has two data bytes.

TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA
READ_IIN	0x89	Calculated input supply current.	R Word	N	L11	A		NA
MFR_READ_IIN	0xED	Calculated input current per channel.	R Word	Y	L11	A		NA
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA
READ_TEMPERATURE_2	0x8E	Internal junction temperature. Does not affect any other registers.	R Word	N	L11	C		NA
READ_DUTY_CYCLE	0x94	Duty cycle of the top gate control signal.	R Word	Y	L11	%		NA
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W		NA
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA
MFR_TEMPERATURE_2_PEAK	0xF4	Maximum measured value of external Temperature (READ_TEMPERATURE_2) since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA

READ_VIN

The READ_VIN command returns the measured input voltage, in volts.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

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PMBus COMMAND DETAILS

READ_VOUT

The READ_VOUT command returns the measured output voltage in the same format as set by the VOUT_MODE command.

This read-only command has two data bytes and is formatted in Linear_16u format.

READ_IIN

The READ_IIN command returns the input current in Amperes. Note: Input current is calculated from READ_IOUT current and the READ_DUTY_CYCLE value from both outputs plus the MFR_IIN_OFFSET. For accurate values at low currents the part must be in continuous conduction mode. The greatest source of error if DCR sensing is used, is the accuracy of the inductor parasitic DC resistance (DCR) at room temperature IOUT_CAL_GAIN.

READ_IIN = $MFR_READ_IIN_{_PAGE0}$ + $MFR_READ_IIN_{_PAGE1}$

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_IIN

The MFR_READ_IIN command is a paged reading of the input current that applies the paged MFR_IIN_OFFSET parameter. This calculation is similar to READ_IIN except the paged values are used.

MFR_READ_IIN = MFR_IIN_OFFSET + (IOUT • DUTYCYCLE)

This command has 2 data bytes and is formatted in Linear_5s_11s format.

READ_IOUT

The READ_IOUT command returns the average output current in amperes. The IOUT value is a function of:

a) the differential voltage measured across the I_{SENSE} pins

b) the IOUT_CAL_GAIN value

c) the MFR_IOUT_CAL_GAIN_TC value, and

d) READ_TEMPERATURE_1 value

e) The MFR_TEMP_1_GAIN and the MFR_TEMP_1_OFFSET

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of the external sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_2

The READ_TEMPERATURE_2 command returns the temperature, in degrees Celsius, of the internal sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

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PMBus COMMAND DETAILS

READ_DUTY_CYCLE

The READ_DUTY_CYCLE command returns the duty cycle of controller, in percent.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_POUT

The READ_POUT command is a paged reading of the DC/DC converter output power in Watts. The POUT is calculated based on the most recent correlated output voltage and current readings.

This command has 2 data bytes and is formatted in Linear_5s_11s format.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_16u format.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_2_PEAK

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

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PMBus COMMAND DETAILS

NVM MEMORY COMMANDS

Store/Restore

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the non-volatile user contents of the Operating Memory to the matching locations in the non-volatile User NVM memory.

Executing this command if the die temperature exceeds 85°C is not recommended and the data retention of 10 years cannot be guaranteed. If the die temperature exceeds 130°C, the STORE_USER_ALL command is disabled. The command is re-enabled when the IC temperature drops below 125°C.

Communication with the LTC3880 and programming of the NVM can be initiated when VDD33 is available and VIN is not applied. To enable the part in this state, using global address 0x5B write 0x2B followed by 0xC4. The part can now be communicated with, and the project file updated. To write the updated project file to the NVM issue a STORE_USER_ALL command. When VIN is applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

This write-only command has no data bytes.

RESTORE_USER_ALL

The RESTORE_USER_ALL command instructs the PMBus device to copy the contents of the non-volatile User memory to the matching locations in the Operating Memory. The values in the Operating Memory are overwritten by the value retrieved from the User commands. When a RESTORE_USER_ALL command is issued, the RUN pins and SHARE_CLK pin are asserted low until the restore is complete. The RUN pins and SHARE_CLK pin are then released. The run pins are held low for the MFR_RESTART_DELAY. The RESTORE_USER_ALL command will place the value of all commands stored in NVM into the RAM ignoring the pin-strapped resistor configuration pins including ASEL. The MFR_RESET command is recommended to be used instead of RESTORE_USER_ALL because the MFR_RESET command always honors the ASEL pins and will honor the pin-strapped RCONFIG pins if the part is programmed to respect them.

RESTORE_USER_ALL. RESTORE_USER_ALL commands are disabled if the die exceeds 130°C and are not re-enabled until the die temperature drops below 125°C.

This write-only command has no data bytes.

MFR_COMPARE_USER_ALL

The MFR_COMPARE_USER_ALL command instructs the PMBus device to compare current command contents with what is stored in non-volatile memory. If the compare operation detects differences, a CML bit 0 fault will be generated.

This write-only command has no data bytes.

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PMBus COMMAND DETAILS

Fault Log Operation

A conceptual diagram of the fault log is shown in Figure 32. The fault log provides telemetry recording capability to the LTC3880. During normal operation, the contents of the status registers, the output voltage readings, temperature readings as well as peak values of these quantities are stored in a continuously updated buffer in RAM. You can think of the operation as being similar to a strip chart recorder. When a fault occurs, the contents are written into EEPROM for nonvolatile storage. The EEPROM fault log is then locked. The part can be powered down with the fault log available for reading at a later time. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced. When reading the fault log from RAM, all 6 events of cyclical data remain. However, when the fault log is read from EEPROM (after a reset), the last 2 events are lost. The read length of 147 bytes remains the same, but the fifth and sixth events are a repeat of the fourth event.

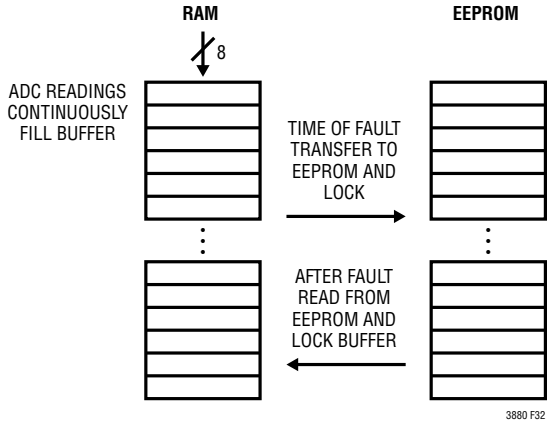

Figure 32. Fault Log Conceptual Diagram

Fault Logging

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_LOG	0xEE	Fault log data bytes. This sequentially retrieved data is used to assemble a complete fault log.	R Block	N	CF		Y	NA
MFR_FAULT_LOG_ STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM. This causes the part to behave as if a channel has faulted off.	Send Byte	N				NA
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	Send Byte	N				NA

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PMBus COMMAND DETAILS

MFR_FAULT_LOG

The MFR_FAULT_LOG command allows the user to read the contents of the FAULT_LOG after the first fault occurrence since the last MFR_FAULT_LOG_CLEAR command was last written. The contents of this command are stored in non-volatile memory, and are cleared by the MFR_FAULT_LOG_CLEAR command. The length and content of this command are listed in Table 11. If the user accesses the MFR_FAULT_LOG command and no fault log is present, the command will return a data length of 0. If a fault log is present, the MFR_FAUTL_LOG will always return a block of data 147 bytes long. If a fault occurs within the first second of applying power, some of the earlier pages in the fault log may not contain valid data.

NOTE: The approximate transfer time for this command is 3.4ms using a 400kHz clock.

This read-only command is in block format.

MFR_FAULT_LOG_STORE

The MFR_FAULT_LOG_STORE command forces the fault log operation to be written to NVM just as if a fault event occurred. This command will generate a MFR_SPECIFIC fault if the “Enable Fault Logging” bit is set in the MFR_CONFIG_ALL_LTC3880 command.

If the die temperature exceeds 130°C, the MFR_FAULT_LOG_STORE command is disabled until the IC temperature drops below 125°C.

Up-Time Counter is in the Fault Log header. The counter is the time since the last reset in 200µs increments. This is a 48-bit binary counter.

This write-only command has no data bytes.

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PMBus COMMAND DETAILS

Table 11. Fault Logging

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

Data Format Definitions				LIN 11 = PMBus = Rev 1.1, Part 2, section 7.1
				LIN 16 = PMBus Rev 1.1, Part 2, section 8. Mantissa portion only
				BYTE = 8 bits interpreted per definition of this command
DATA	**BITS**	**DATA FORMAT**	**BYTE NUM**	**BLOCK READ COMMAND**
Block Length		BYTE	147	The MFR_FAULT_LOG command is a fixed length of 147 bytes The block length will be zero if a data log event has not been captured
HEADER INFORMATION				
Position_Fault		BYTE	0	Indicates the fault that caused the fault log to be activated.
MFR_REAL_TIME	[7:0}	BYTE	1	48-bit binary counter. The value is the time since the last reset in 200µs increments.
	[15:8}	BYTE	2	
	[23:16]	BYTE	3	
	[31:24]	BYTE	4	
	[39:32]	BYTE	5	
	[47:40]	BYTE	6	
MFR_VOUT_PEAK (PAGE 0)	[15:8]	LIN 16	7	Peak READ_VOUT page 0 since last MFR_CLEAR_PEAKS.
	[7:0]	LIN 16	8	
MFR_VOUT_PEAK (PAGE 1)	[15:8]	LIN 16	9	Peak READ_VOUT page 1 since last MFR_CLEAR_PEAKS.
	[7:0]	LIN 16	10	
MFR_IOUT_PEAK (PAGE 0)	[15:8]	LIN 11	11	Peak READ_IOUT page 0 since last MFR_CLEAR_PEAKS.
	[7:0]	LIN 11	12	
MFR_IOUT_PEAK (PAGE 1)	[15:8]	LIN 11	13	Peak READ_IOUT page 1 since last MFR_CLEAR_PEAKS.
	[7:0]	LIN 11	14	
MFR_VIN_PEAK	[15:8]	LIN 11	15	Peak READ_VIN since last MFR_CLEAR_PEAKS.
	[7:0]	LIN 11	16	
READ_TEMPERATURE_1 (PAGE 0)	[15:8]	LIN 11	17	External temperature sensor 0 during last event
	[7:0]	LIN 11	18	
READ_TEMPERATURE_1 (PAGE 1)	[15:8]	LIN 11	19	External temperature sensor 1 during last event
	[7:0]	LIN 11	20	
READ_TEMPERATURE_2	[15:8]	LIN 11	21	Internal temperature sensor during last event
	[7:0]	LIN 11	22	
MFR_TEMPERATURE1_PEAK (PAGE 0)	[15:8]	LIN 11	23	Peak READ_TEMPERATURE_1 page 0 since MFR_CLEAR_PEAKS.
	[7:0]	LIN 11	24	
MFR_TEMPERATURE1_PEAK (PAGE 1)	[15:8]	LIN 11	25	Peak READ_TEMPERATURE_1 page 1 since MFR_CLEAR_PEAKS.
	[7:0]	LIN 11	26	

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PMBus COMMAND DETAILS

CYCLICAL DATA				
EVENT n **(Data at Which Fault Occurred; Most Recent Data)**				Event "n" represents one complete cycle of ADC reads through the MUX at time of fault. Example: If the fault occurs when the ADC is processing step 15, it will continue to take readings through step 25 and then store the header and all 6 event pages to EEPROM
READ_VOUT (PAGE 0)	[15:8]	LIN 16	27	
	[7:0]	LIN 16	28	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	29	
	[7:0]	LIN 16	30	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	31	
	[7:0]	LIN 11	32	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	33	
	[7:0]	LIN 11	34	
READ_VIN	[15:8]	LIN 11	35	
	[7:0]	LIN 11	36	
READ_IIN	[15:8]	LIN 11	37	
	[7:0]	LIN 11	38	
STATUS_VOUT (PAGE 0)		BYTE	39	
STATUS_VOUT (PAGE 1)		BYTE	40	
STATUS_WORD (PAGE 0)	[15:8]	WORD	41	
	[7:0]	WORD	42	
STATUS_WORD (PAGE 1)	[15:8]	WORD	43	
	[7:0]	WORD	44	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	45	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	46	
EVENT n-1 **(Data Measured Before Fault Was Detected)**				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	47	
	[7:0]	LIN 16	48	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	49	
	[7:0]	LIN 16	50	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	51	
	[7:0]	LIN 11	52	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	53	
	[7:0]	LIN 11	54	
READ_VIN	[15:8]	LIN 11	55	
	[7:0]	LIN 11	56	
READ_IIN	[15:8]	LIN 11	57	
	[7:0]	LIN 11	58	
STATUS_VOUT (PAGE 0)		BYTE	59	
STATUS_VOUT (PAGE 1)		BYTE	60	
STATUS_WORD (PAGE 0)	[15:8]	WORD	61	
	[7:0]	WORD	62	
STATUS_WORD (PAGE 1)	[15:8]	WORD	63	
	[7:0]	WORD	64	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	65	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	66	
*				
*				
*				

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PMBus COMMAND DETAILS

EVENT n-5 (Oldest Recorded Data)				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	127	
	[7:0]	LIN 16	128	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	129	
	[7:0]	LIN 16	130	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	131	
	[7:0]	LIN 11	132	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	133	
	[7:0]	LIN 11	134	
READ_VIN	[15:8]	LIN 11	135	
	[7:0]	LIN 11	136	
READ_IIN	[15:8]	LIN 11	137	
	[7:0]	LIN 11	138	
STATUS_VOUT (PAGE 0)		BYTE	139	
STATUS_VOUT (PAGE 1)		BYTE	140	
STATUS_WORD (PAGE 0)	[15:8]	WORD	141	
	[7:0]	WORD	142	
STATUS_WORD (PAGE 1)	[15:8]	WORD	143	
	[7:0]	WORD	144	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	145	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	146	

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PMBus COMMAND DETAILS

Table 11a: Explanation of Position_Fault Values

POSITION_FAULT VALUE	SOURCE OF FAULT LOG
0xFF	MFR_FAULT_LOG_STORE
0x00	TON_MAX_FAULT Channel 0
0x01	VOUT_OV_FAULT Channel 0
0x02	VOUT_UV_FAULT Channel 0
0x03	IOUT_OC_FAULT Channel 0
0x05	OT_FAULT Channel 0
0x06	UT_FAULT Channel 0
0x07	VIN_OV_FAULT Channel 0
0x0A	MFR_OT_FAULT Channel 0
0x10	TON_MAX_FAULT Channel 1
0x11	VOUT_OV_FAULT Channel 1
0x12	VOUT_UV_FAULT Channel 1
0x13	IOUT_OC_FAULT Channel 1
0x15	OT_FAULT Channel 1
0x16	UT_FAULT Channel 1
0x17	VIN_OV_FAULT Channel 1
0x1A	MFR_OT_FAULT Channel 1

MFR_FAULT_LOG_CLEAR

The MFR_FAULT_LOG_CLEAR command will erase the fault log file stored values. It will also clear bit 3 in the STATUS_MFR_SPECIFIC command. After a clear is issued, the status can take up to 8ms to clear.

This write-only command is send bytes.

Block Memory Write/Read

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA

All the NVM commands are disabled if the die temperature exceeds 130°C. NVM commands are re-enabled when the die temperature drops below 125°C.

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PMBus COMMAND DETAILS

MFR_EE_UNLOCK

Multiple writes to MFR_EE_UNLOCK with the appropriate unlock keys are used to enable MFR_EE_ERASE and MFR_EE_DATA access and configure PEC.

Communication with the LTC3880 and programming of the NVM can be initiated when VDD33 is applied and VIN is not. To enable the part in this state, use global address 0x5B command 0xBD data 0x2B followed by address 0x5B command 0xBD data 0xC4. When VIN is applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

Writing 0x2B followed by 0xD4 clears PEC, resets the EEPROM address pointer and unlocks the part for EEPROM erase and data command writes.

Writing 0x2B followed by 0xD5 sets the PEC, resets the EEPROM address pointer and unlocks the part for EEPROM erase and data command writes.

Writing 0x2B followed by 0x91 and 0xE4 clears PEC, resets the EEPROM address pointer and unlocks the part for EEPROM data reads of all locations.

Writing 0x2B followed by 0x91 and 0xE5 sets PEC, resets the EEPROM address pointer and unlocks the part for EEPROM data reads of all locations.

MFR_EE_ERASE

A single write after the appropriate unlock key erases the EEPROM allowing subsequent data writes. This register may be read to indicate if an EEPROM access is in progress.

A value of 0x2B will erase the EEPROM. If the part is busy writing or erasing the EEPROM a non-zero value will be returned.

MFR_EE_DATA

Sequential writes or reads perform block loads or restores from the EEPROM. Successive MFR_EE_DATA word writes will enter the EEPROM until it is full. Extra writes will lock the part. The first write is to the lowest address. The first read returns the 16 bit EEPROM packing revision ID. The second read returns the number of 16 bit words available. Subsequent reads return EEPROM data starting with the lowest address.

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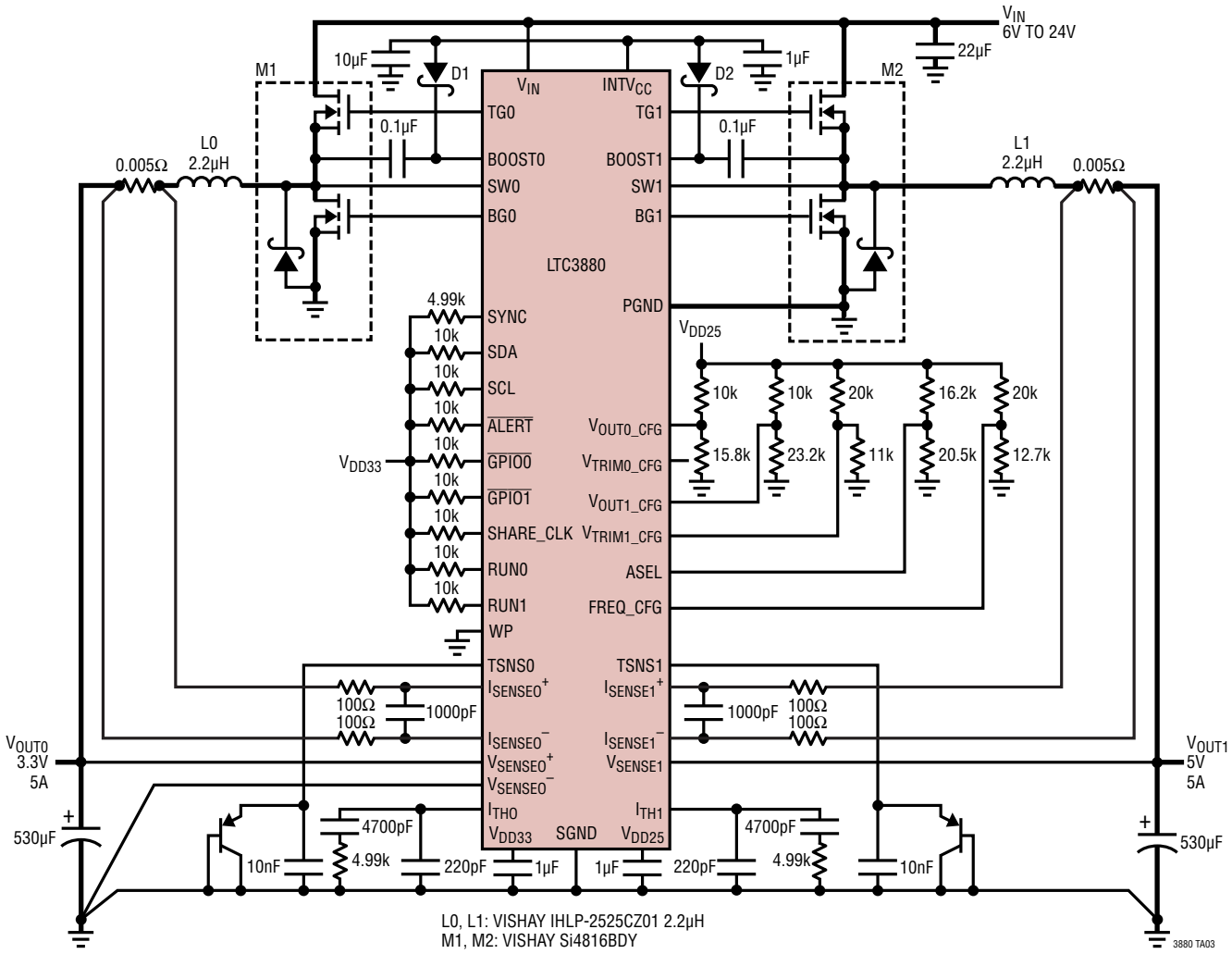
TYPICAL APPLICATIONS

High Efficiency Dual 500kHz 5V/3.3V Step-Down Converter with Sense Resistors



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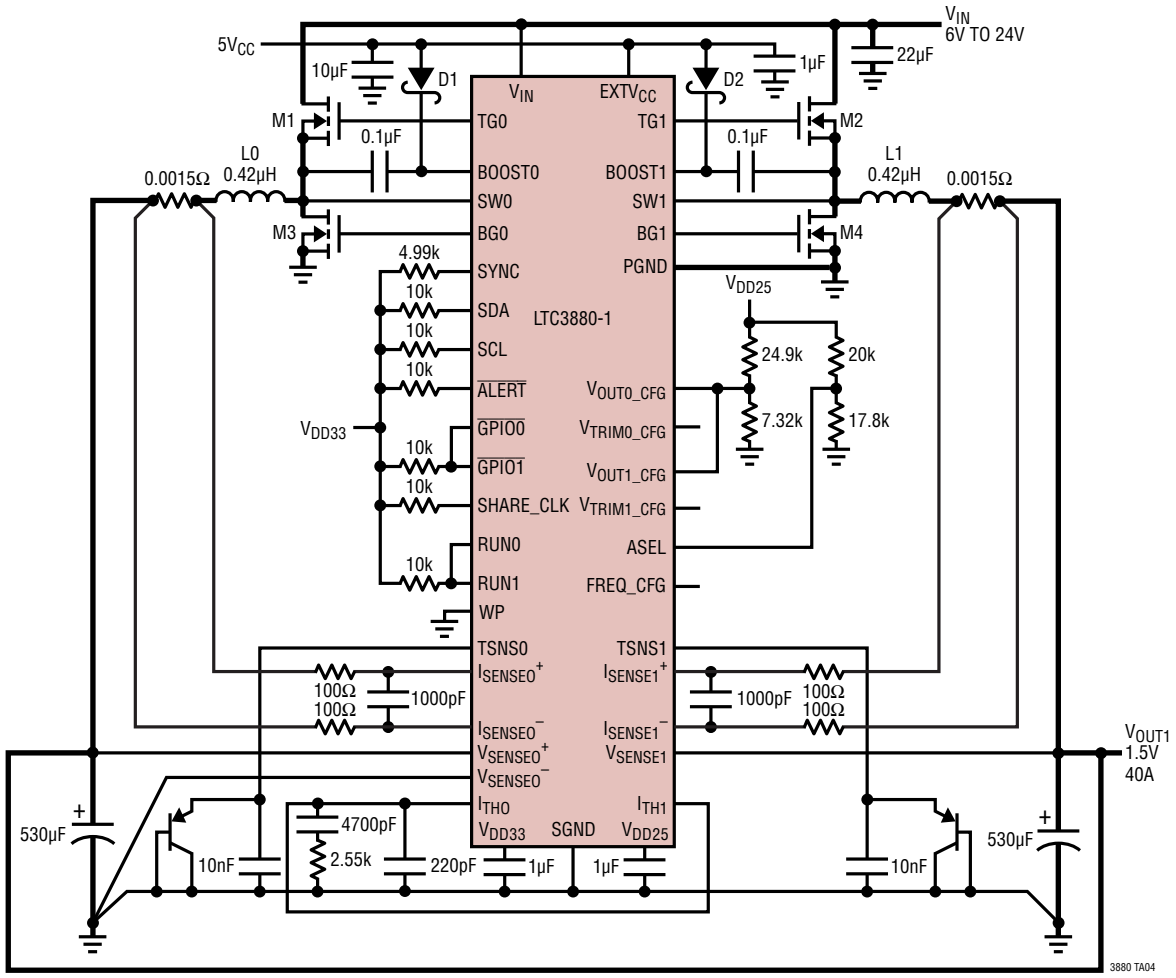
TYPICAL APPLICATIONS

High Efficiency 350kHz 2-Phase 1.5V Dual Step-Down Converter with External V_{CC} and Sense Resistors



L0, L1: VITEC 59PR9875 0.42µH
M1, M2: INFINEON BSC050N03LS
M3, M4: INFINEON BSC010NE2LSI

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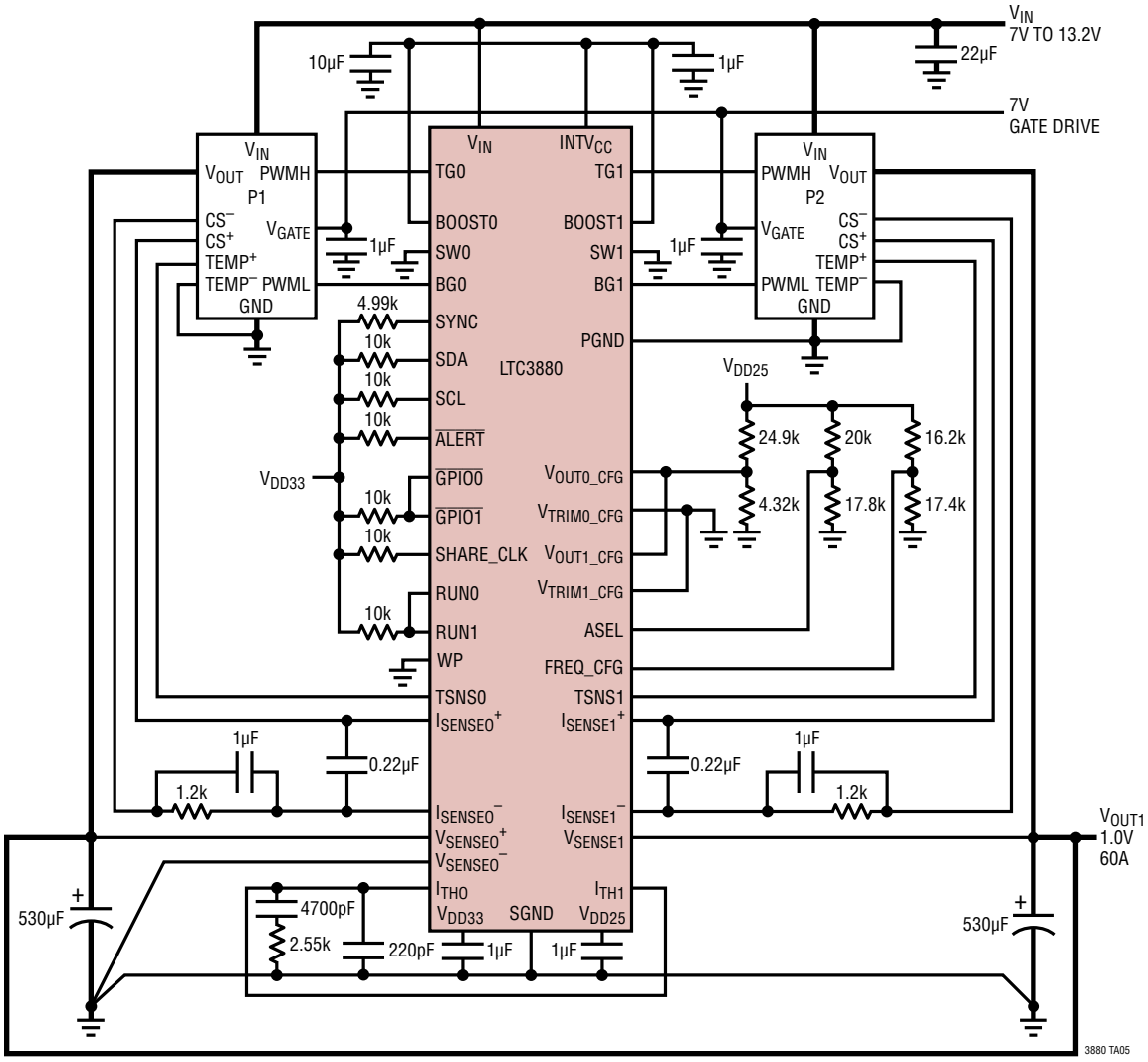
TYPICAL APPLICATIONS

High Efficiency 425kHz 1V Step-Down Dual Phase Converter with Power Blocks



P1, P2: VRA001-4C3G ACBEL POWER BLOCK

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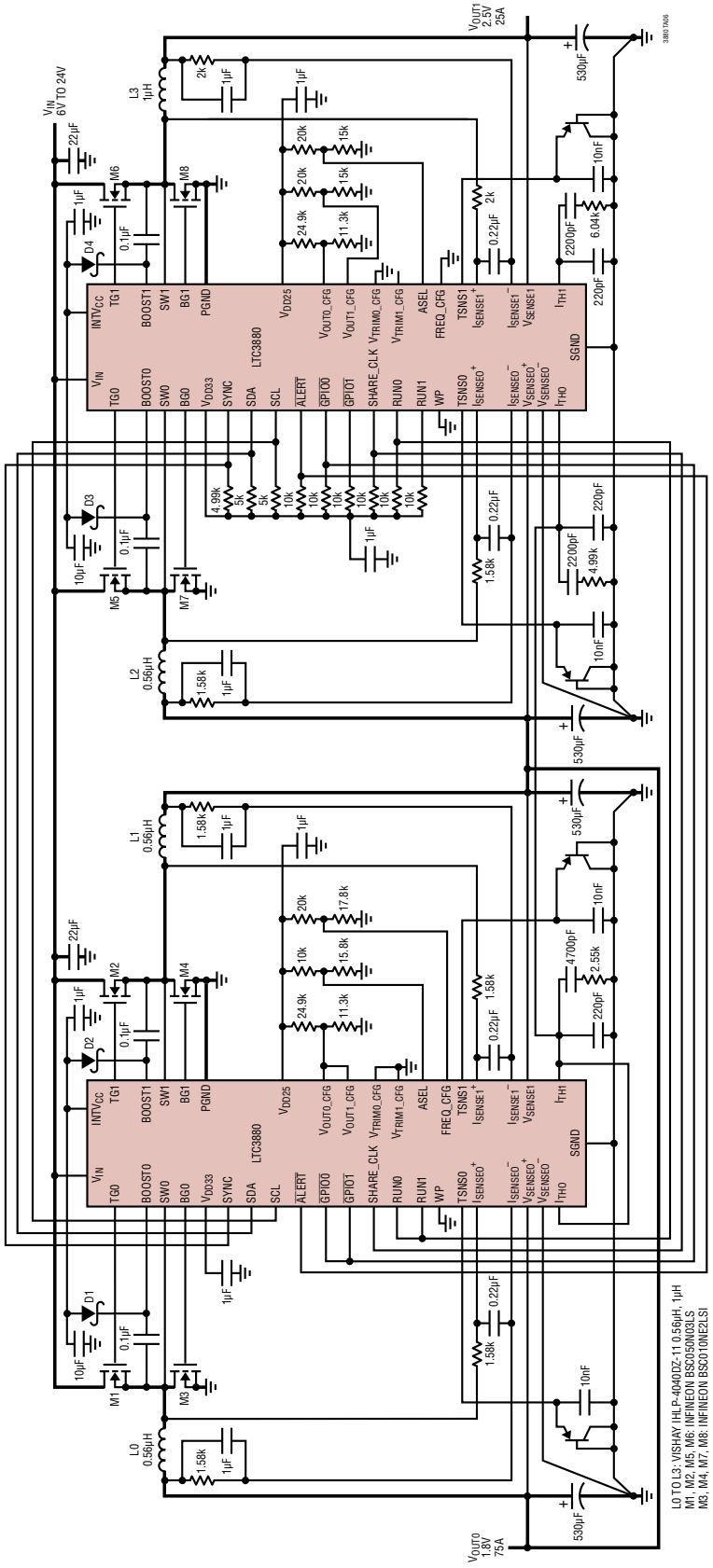
TYPICAL APPLICATIONS

High Efficiency 425kHz 3-Phase 1.8V and 1-Phase 2.5V Step-Down Converter



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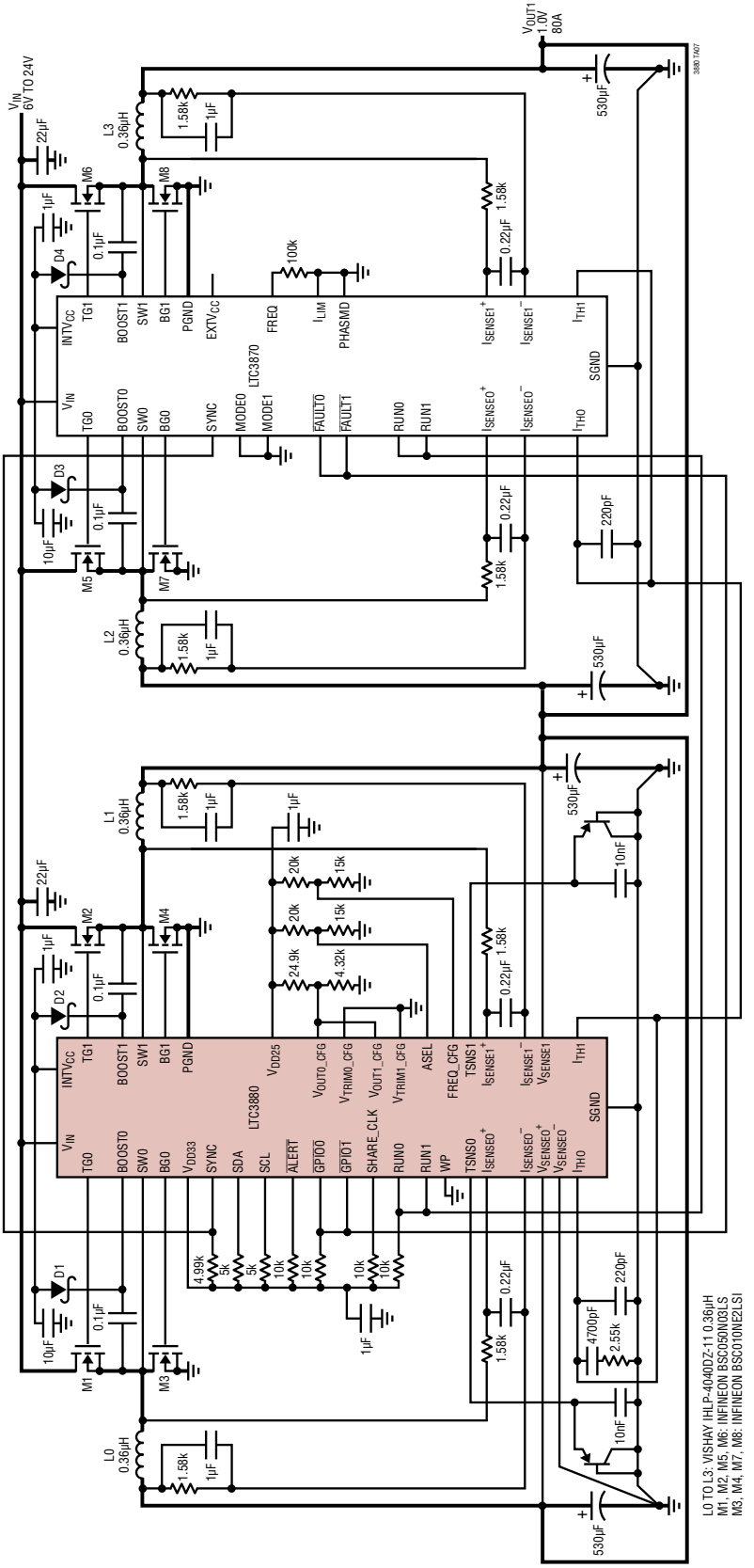
TYPICAL APPLICATIONS

High Efficiency 425kHz 4-Phase 1.0V Step-Down 1V Converter with an LTC3880 and LTC3870 PSM Slave



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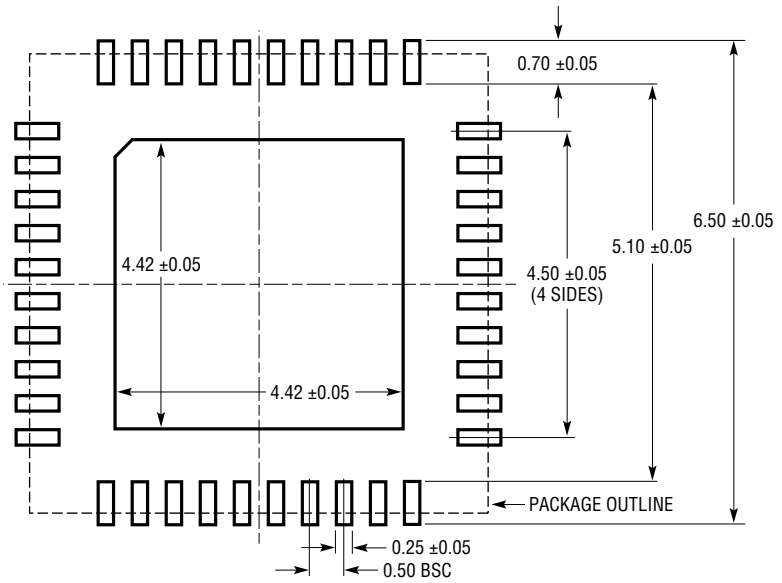
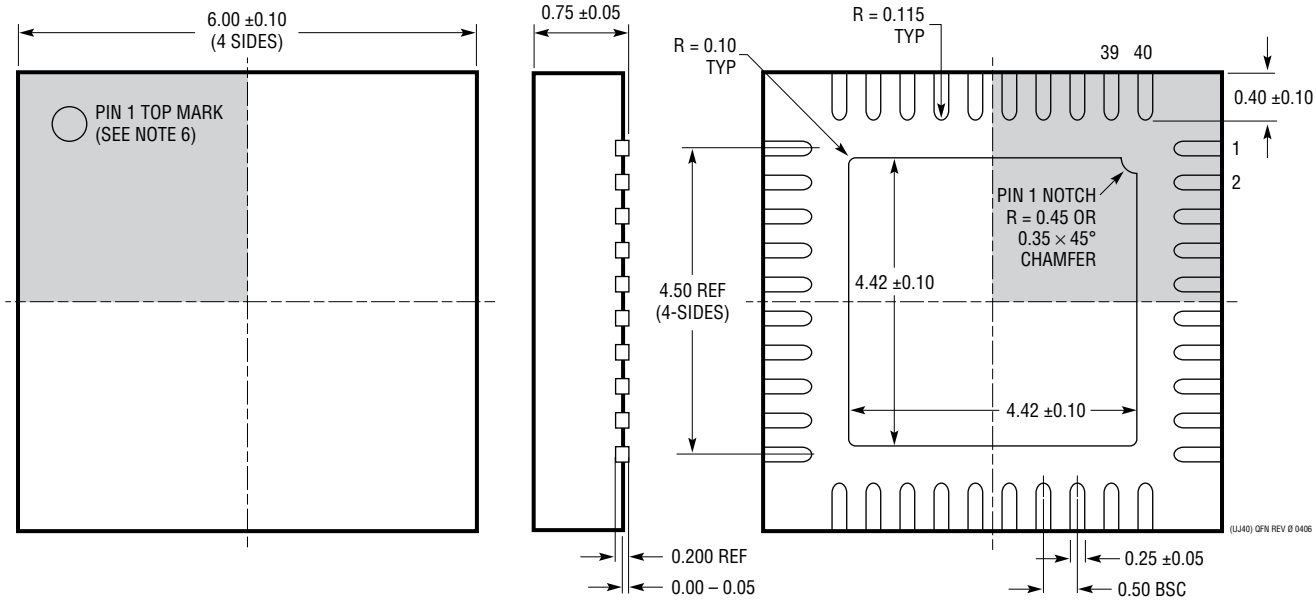
PACKAGE DESCRIPTION

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/11	Added I-grade, all sections updated	1-112
B	11/13	Amended upper limit of $I_{SENSE0/1}$	5
		Amended parametric errors and typical values	6
		Amended Pin Function errors	13
		Amended 2nd left paragraph under Operation	17
		Amended 3rd left paragraph under Operation	23
		Amended commands on Table 2	31
		Amended formula on Figure 18a	38
		Amended component on Figure 27	56
		Amended Scratchpad table	88
		Amended Identification table	89
		Amended PMBus Command Details table	100
		Amended components on Typical Application page	106
C	05/14	Added Initialization Time	5
		Reduced readback time	Throughout
		Edit equations	40, 57, 58
		Changed schematic MOSFET part numbers	56, 106, 108, 109
		Edit VOUT_MAX description	31
		Edit MFR_VOUT_MAX description	33
		Added STATUS Message content	90, 91, 92, 93
D	12/14	Added (PGOOD) after VOUT_UVUF	19, 24, 43, 65, 88
E	7/16	Added LTC3880-1 to V_{IN} pin description	14
		Added LTC3887/LTC3887-1 comparison table	1
F	9/16	Widened storage temperature range	4
G	04/17	Added ECC	1, 16, 17, 24
		Reduced initialization	5
		Reduced conversion time	6
H	09/19	Added AEC-Q100 Qualified for Automotive Applications and orderable part numbers	1, 5

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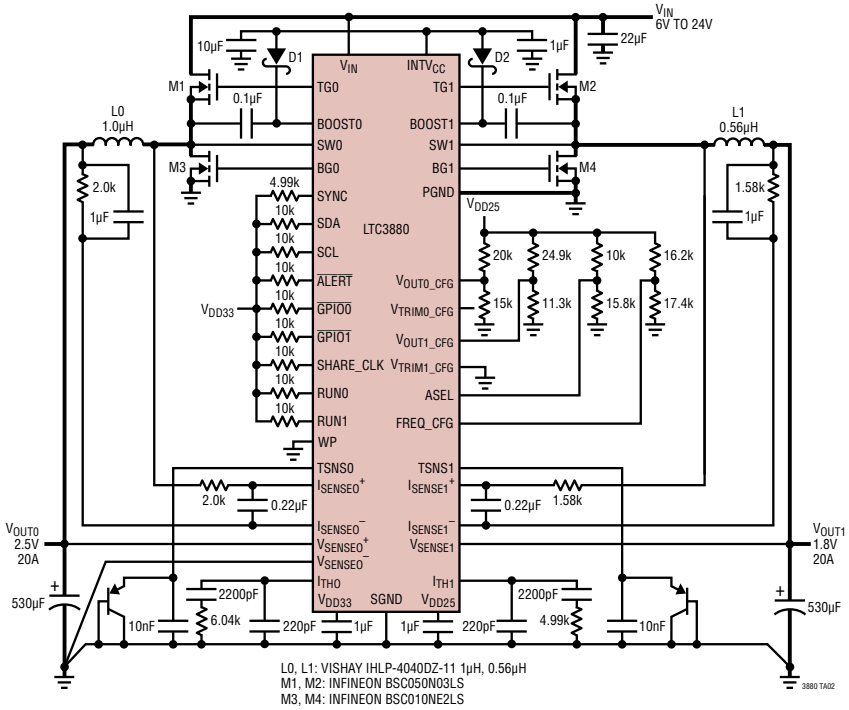
TYPICAL APPLICATION

High Efficiency Dual 425kHz 2.5V/1.8V Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4676A	Dual 13A or Single 26A Step-Down DC/DC µModule Regulator with Digital Power System Management	V_{IN} Up to 26.5V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.4V, ±2% I_{OUT} ADC Accuracy, Fault Logging, I^2C/PMBus Interface, 16mm × 16mm × 5mm, BGA Package
LTM4675	Dual 9A or Single 18A Step-Down DC/DC µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤17V; 0.5V ≤ V_{OUT} ≤ 5.5V, ±0.5% V_{OUT} Accuracy I^2C/PMBus Interface, 11.9mm × 16mm × 3.5mm, BGA Package
LTM4677	Dual 18A or Single 36A µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤16V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 1.8V, I^2C/PMBus Interface, 16mm × 16mm × 5mm, BGA Package
LTC3870/ LTC3870-1	Dual Output Multiphase Step-Down Slave Controller	V_{IN} Up to 60V, 0.5V ≤ V_{OUT} ≤ 14V, Very High Output Current, Accurate Current Sharing, Current Mode Applications
LTC3884	Dual Output MultiPhase Step-Down Controller with Sub MilliOhm DCR Sensing Current Mode Control and Digital Power System Management	4.5V ≤ V_{IN} ≤ 38V, 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, I^2C/PMBus Interface, Programmable Analog Loop Compensation, Input Current Sense
LTC3887	Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ $V_{OUT0,1}$ ≤ 5.5V, 70mS Start-Up, Analog Control Loop, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3886	60V Dual Output Step-Down Controller with Digital Power System Management	4.5V ≤ V_{IN} ≤ 60V, 0.5V ≤ $V_{OUT0,1}$ (±0.5%) ≤ 13.8V, I^2C/PMBus Interface, Input Current Sense
LTC3883/ LTC3883-1	Single Phase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, Input Current Sense Amplifier, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3882/ LTC3882-1	Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management	V_{IN} Up to 38V, 0.5V ≤ $V_{OUT1,2}$ ≤ 5.25V, ±0.5%, V_{OUT} Accuracy I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3815	6A Monolithic Synchronous DC/DC Step-Down Converter with Digital Power System Management	2.25V ≤ V_{IN} ≤ 5.5V, 0.4V ≤ V_{OUT} ≤ 0.72 V_{IN}, Programmable V_{OUT} Range ±25% with 0.1% Resolution, Up to 3MHz Operation with 13-Bit ADC
LTC3874	Multiphase Step-Down Synchronous Slave Controller for Sub-MilliOhm DCR Sensing	4.5V ≤ V_{IN} ≤ 38V, V_{OUT} up to 5.5V, Very High Output Current, Accurate Current Sharing, Current Mode Applications

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