ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages
- HV_{CC} ..... –0.3V to 18V
- V_{CC} ..... –0.3V to 6.5V

Input Voltages
- V1, V2, V3, V4 ..... –0.3V to 12V
- MS1, MS2, RDIS ..... –0.3V to 6.5V
- SQT1, SQT2, VSEL ..... –0.3V to 6.5V
- RT1, RT2, RT3, RT4 ..... –0.3V to 6.5V
- ON, OVA ..... –0.3 to V_{CC} + 0.3V
- STMR, PTMR, RTMR ..... –0.3 to V_{CC} + 0.3V

Output Voltages
- EN1, EN2, EN3, EN4 (Note 3) ..... –0.3V to 12V
- CMP1, CMP2, CMP3, CMP4 ..... –0.3V to 6.5V
- $\overline{FLT}$, $\overline{RST}$, $\overline{OV}$, CAS ..... –0.3V to 6.5V
- $\overline{DONE}$, REF ..... –0.3V to V_{CC} + 0.3V

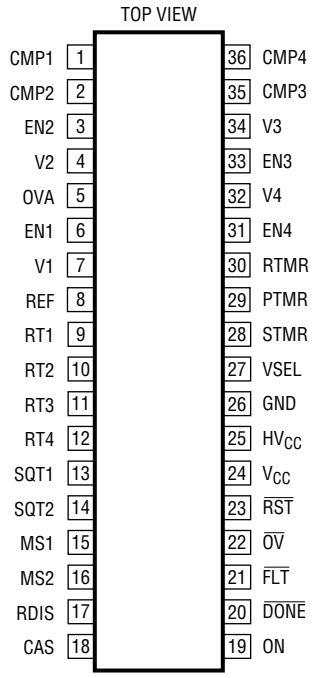
RMS Currents
- IV_{CC} ..... ±10mA
- IHV_{CC} ..... ±20mA
- I_{REF} ..... ±10mA

Operating Ambient Temperature Range
- LTC2928C ..... 0°C to 70°C
- LTC2928I ..... –40°C to 85°C

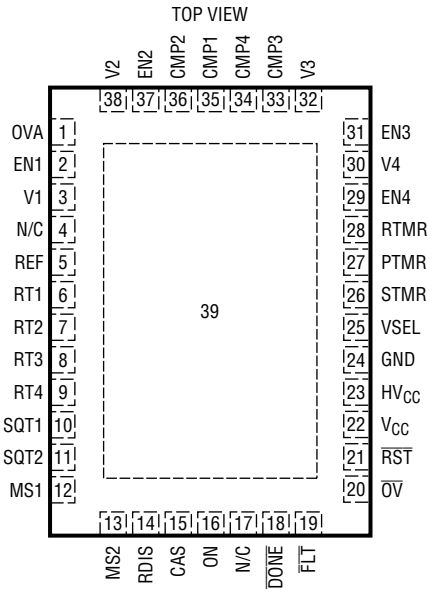
Storage Temperature Range
- SSOP Package ..... –65°C to 150°C
- QFN Package ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- SSOP Package ..... 300°C

PIN CONFIGURATION



G PACKAGE
36-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) PCB GND CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2928CG#PBF	LTC2928CG#TRPBF	LTC2928CG	36-Lead Plastic SSOP (5.3mm)	0°C to 70°C
LTC2928IG#PBF	LTC2928IG#TRPBF	LTC2928IG	36-Lead Plastic SSOP (5.3mm)	0°C to 70°C
LTC2928CUHF#PBF	LTC2928CUHF#TRPBF	2928	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 85°C
LTC2928IUHF#PBF	LTC2928IUHF#TRPBF	2928	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 85°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Pins: V_{CC}, HV_{CC}							
V_{VCC}	V_{CC} Input Supply Range		●	2.9		6	V
I_{VCC}	V_{CC} Input Supply Current	HV_{CC} = GND	●		1	2.5	mA
V_{UVL}	V_{CC} Input Supply Undervoltage Lockout	V_{CC} Rising	●	2.75	2.8	2.85	V
$V_{UVL(HYST)}$	Undervoltage Lockout Hysteresis		●	50	100	150	mV
V_{HVCC}	High Voltage Input Supply Range		●	7.2	12	16.5	V
$V_{CC(REG)}$	Regulated V_{CC} from HV_{CC}	V_{HVCC} = 12V	●	3.2	3.3	3.4	V
I_{REG}	Regulated V_{CC} Output Current to External Load (Note 2)		●			–10	mA
I_{HVCC}	HV_{CC} Input Supply Current	I_{REG} = 0mA, V_{HVCC} = 12V	●		1	2	mA
Sequence Up/Down Pin: ON							
V_{ON}	ON Threshold Voltage	V_{ON} Rising	●	0.985	1.00	1.015	V
$V_{ON(HYST)}$	ON Hysteresis		●	20	30	40	mV
$I_{ON(LKG)}$	ON Leakage Current	V_{ON} = 1V	●			±50	nA
Voltage Monitor Pins: V1, V2, V3, V4							
$V_{MON(TH)}$	Reset Threshold Voltage V1 Negative Threshold Voltage	VSEL = V_{CC}	● ●	0.4925	0.500	0.5075 ±18	V mV
$V_{SEQ(TH)}$	Sequencing Thresholds 0.67 $V_{MON(TH)}$ 0.33 $V_{MON(TH)}$ 0.10 $V_{MON(TH)}$	See Table 4	 ● ● ●	 0.315 0.149 0.032	 0.333 0.167 0.05	 0.351 0.185 0.068	 V V V
$I_{MON(LKG)}$	Monitor Pin Leakage Current	V_{MON} = 0.55V	●			±15	nA
$t_{MON(UV)}$	Undervoltage Pulse Width Required to Trip Comparators	V_{MON} below $V_{MON(TH)}$ by 1%			225		µs
$t_{MON(OV)}$	Overvoltage Pulse Width Required to Trip $\overline{OV}$	V_{MON} above Overvoltage Threshold by 1%			225		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Enable Pins: EN1, EN2, EN3, EN4							
V_{EN}	Enable Pin Voltage Output in On State	I_{EN} = –1µA	●	V_{CC} + 4.5	V_{CC} + 5.5	V_{CC} + 6	V
$I_{EN(UP)}$	Enable Pin Pull-Up Current	Enable Pin On, $V_{EN} \le (V_{CC} + 4V)$	●	–7.5	–10	–12.5	µA
$V_{EN(OL)}$	Enable Pin Voltage Output Low	I_{EN} = 2.5mA	●		0.25	0.4	V
Comparator Outputs: CMP1, CMP2, CMP3, CMP4							
$V_{CMP(OL)}$	Comparator Voltage Output Low	I_{CMP} = 2.5mA	●		0.15	0.3	V
$V_{CMP(OH)}$	Comparator Voltage Output High (Note 4)	I_{CMP} = –1µA	●	V_{CC} – 1			V
Three-State Selection Inputs: SQT1, SQT2, MS1, MS2, RDIS							
V_{IL}	Voltage Input Low Threshold		●			0.4	V
V_{IH}	Voltage Input High Threshold		●	1.4			V
I_{HZ}	High Z Pin Current	V_{HZ} = 0.7V V_{HZ} = 1.1V	● ●	–10 10			µA µA
Positive/Negative Selection Input: VSEL							
V_{IL}	Voltage Input Low Threshold		●			0.4	V
V_{IH}	Voltage Input High Threshold		●	1.4			V
Sequence Time Position Control Inputs: RT1, RT2, RT3, RT4 (See Resistor Selection Table 3)							
$V_{RT(LO)}$	Voltage Required to Force Enable Pin Low While Sequencing		●			0.045 • V_{CC}	V
$V_{RT(HI)}$	Voltage Required to Force Enable Pin High Outside of Sequencing		●	0.955 • V_{CC}			V
R_{RT}	R_T Pin Input Resistance		●	11.2	12	12.8	kΩ
Cascade Pin: CAS							
$V_{CAS(OL)}$	CAS Voltage Output Low	I_{CAS} = 2.5mA	●		0.15	0.3	V
$I_{CAS(UP)}$	CAS Pull-Up Current	Master Pulling CAS High, V_{CAS} = GND	●	–45	–60	–75	µA
$t_{CAS(HI)}$	Fixed Time Delay between Sequence Time Positions (Note 5)	CAS High, C_{STMR} = 1500pF	●	11	13	15	ms
$t_{CAS(MIN)}$	Minimum CAS Low Time During Sequencing		●	15	22.5	30	µs
Fault Status Pin: $\overline{FLT}$							
$V_{FLT(OL)}$	$\overline{FLT}$ Voltage Output Low	I_{FLT} = 2.5mA	●		0.15	0.3	V
$I_{FLT(UP)}$	$\overline{FLT}$ Pull-Up Current	$V_{FLT} = V_{CC}$ –1V	●	–12	–17	–22	µA
$V_{FLT(TH)}$	External Fault Input Threshold	V_{FLT} Falling	●	1.0	1.1	1.2	V
$V_{FLT(HYST)}$	External Fault Input Hysteresis		●	25	100	150	mV
t_{FLT}	Minimum Detectable External Fault Pulse Width					2	µs
$I_{FLT(LKG)}$	Fault Pin Leakage Current	$V_{FLT} = V_{CC}$	●			± 1	µA
Done Status Pin: $\overline{DONE}$							
$V_{DONE(OL)}$	$\overline{DONE}$ Voltage Output Low	I_{DONE} = 2.5mA	●		0.15	0.3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 3.3V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{DONE(DN)}$	$\overline{DONE}$ Pull-Down Current	V_{DONE} = 3.3V (Note 6)	●		20	40	µA
R_{DONE}	Required Pull-Up Resistance on "Last" LTC2928	5% Tolerance or Better	●	2.4		5.1	kΩ
$V_{DONE(LAST)}$	Voltage Output High when Configured as "Last"		●	0.8 • V_{CC}			V
Reset Pin: $\overline{RST}$							
$V_{RST(OL)}$	$\overline{RST}$ Voltage Output Low	V_{CC} = 0.2V, I_{RST} = 0.1µA	●		5	60	mV
		V_{CC} = 0.5V, I_{RST} = 5µA	●		10	150	mV
		V_{CC} = 1V, I_{RST} = 200µA	●		25	300	mV
		V_{CC} = 3V, I_{RST} = 2500µA	●		150	300	mV
$V_{RST(OH)}$	$\overline{RST}$ Voltage Output High	I_{RST} = –1µA (Note 7)	●	V_{CC} – 1			V
Timer Pins: RTMR, PTMR, STMR							
$I_{TMR(UP)}$	Timer Pull-Up Current	V_{TMR} = GND	●	–1.7	–2	–2.3	µA
$I_{TMR(DN)}$	Timer Pull-Down Current	V_{TMR} = 1.3V	●	15	20	25	µA
t_{RTMR}	Timer Period, RTMR (Note 8)	C_{RTMR} = 1500pF	●	5	6	7	ms
t_{PTMR}	Timer Period, PTMR	C_{PTMR} = 1500pF	●	5	6	7	ms
t_{STMR}	Timer Period, STMR	C_{STMR} = 1500pF	●	11	13	15	ms
External Voltage Reference Pin: REF							
V_{REF}	Reference Voltage Output	I_{REF} = 0.2mA, –1mA, C_{REF} = ≤ 1000pF	●	1.172	1.189	1.205	V
	100% Sequence Threshold	VSEL = V_{CC}	●	1.172	1.189	1.205	V
	67% Sequence Threshold	VSEL = V_{CC}	●	0.780	0.793	0.806	V
	33% Sequence Threshold	VSEL = V_{CC}	●	0.386	0.396	0.406	V
	10% Sequence Threshold	VSEL = V_{CC}	●	0.109	0.119	0.129	V
Over Voltage Indication Pin: $\overline{OV}$							
$V_{OV(OL)}$	$\overline{OV}$ Voltage Output Low	I_{OV} = 2.5mA	●		0.15	0.3	V
$V_{OV(OH)}$	$\overline{OV}$ Voltage Output High (Note 7)	I_{OV} = –1µA	●	V_{CC} – 1			V
t_{OV}	$\overline{OV}$ Indication Time (Note 8)	$\overline{OV}$ Low Time Upon Cleared OV Event, C_{RTMR} = 1500pF	●	5	6	7	ms
Over Voltage Adjust Pin: OVA							
$V_{OVA(TH)}$	Over Voltage Threshold at Comparator Inputs (Note 9)	V_{OVA} = GND	●	0.546	0.556	0.566	V
		V_{OVA} Floating	●	0.650	0.660	0.670	V
		V_{OVA} = V_{CC} = 3.3V	●	1.042	1.072	1.102	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

Note 3: Internal circuits regulate the EN output voltage to V_{EN}. Driving this pin to voltages beyond V_{EN} may damage the part.

Note 4: The comparator outputs have internal pull-ups to V_{CC} of typically –10µA. However, external pull-up resistors may be used when faster rise times are required or for V_{OH} voltages greater than V_{CC}.

Note 5: The CAS high time after an ON edge is stretched by the ON pin propagation delay (20µs typical).

Note 6: The $\overline{DONE}$ pull-down current is present when $\overline{DONE}$ is high to facilitate cascading multiple LTC2928s.

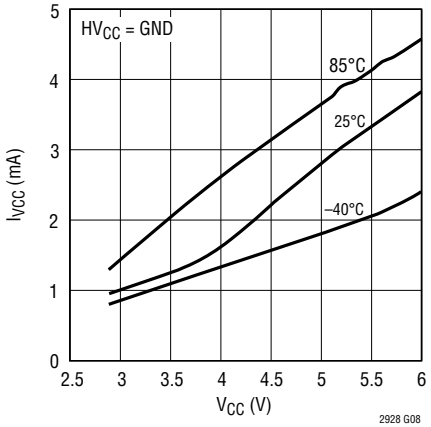
Note 7: The $\overline{RST}$ and $\overline{OV}$ outputs have an internal pull-up to V_{CC} of typically –10µA. However, external pull-up resistors may be used when faster rise times are required or for V_{OH} voltages greater than V_{CC}.

Note 8: If the termination of under and overvoltage events occur within one nominal t_{RTMR} period, the variation in t_{RTMR} and/or t_{OV} may be ±15%.

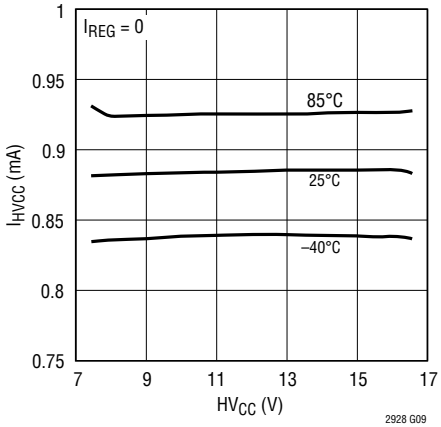
Note 9: Use a resistor from OVA to ground or V_{CC} to configure overvoltage thresholds within the max/min ranges shown. See Applications Information for details.

TYPICAL PERFORMANCE CHARACTERISTICS

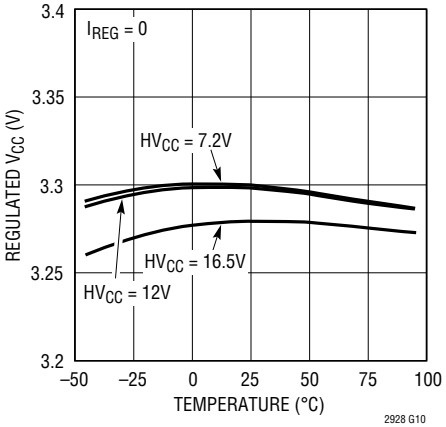
I_{VCC} vs V_{CC}



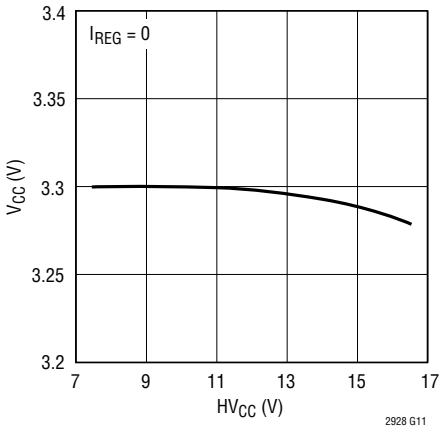
I_{HVCC} vs HV_{CC}



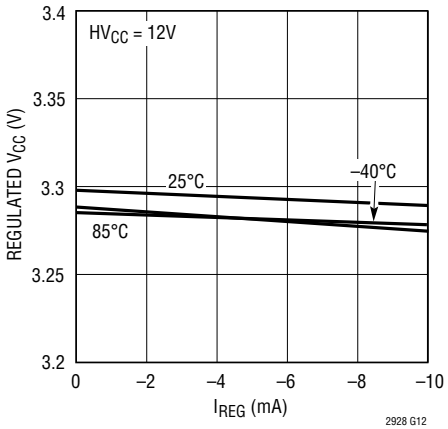
Regulated V_{CC} vs Temperature



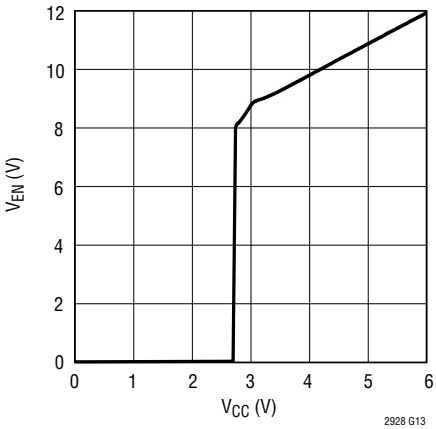
Regulated V_{CC} vs HV_{CC}



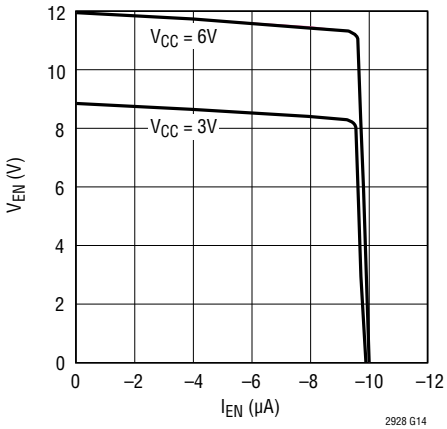
Regulated V_{CC} vs I_{REG}



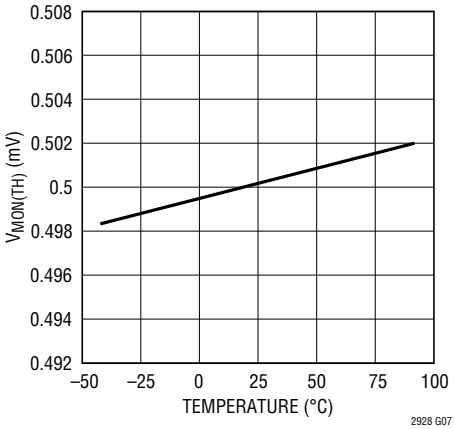
Enable Output Voltage in On State vs V_{CC}



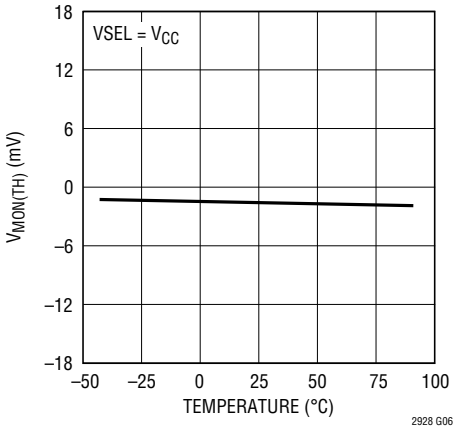
Enable Output Voltage vs Enable Output Current and V_{CC}



Under Voltage Monitor Threshold (100%) vs Temperature

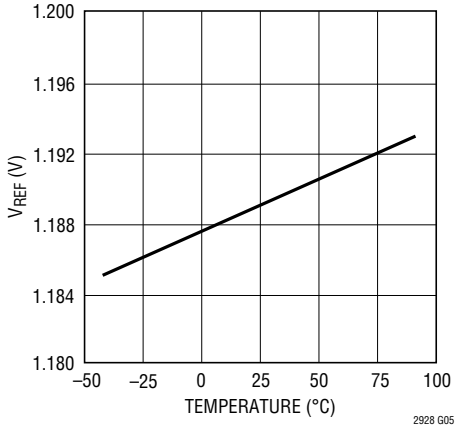


V1 Negative Threshold vs Temperature

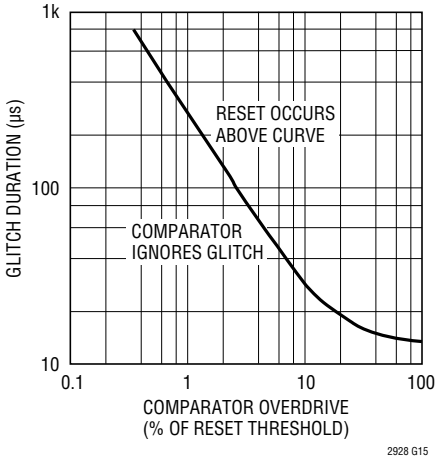


TYPICAL PERFORMANCE CHARACTERISTICS

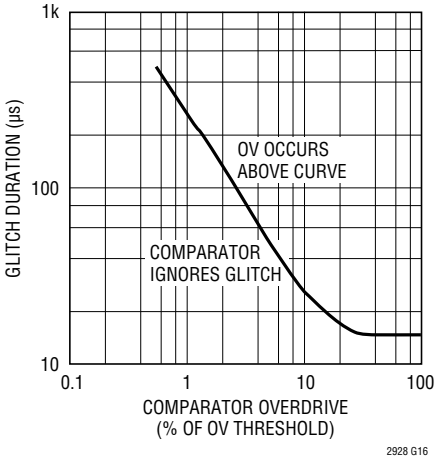
Reference Output Voltage vs Temperature



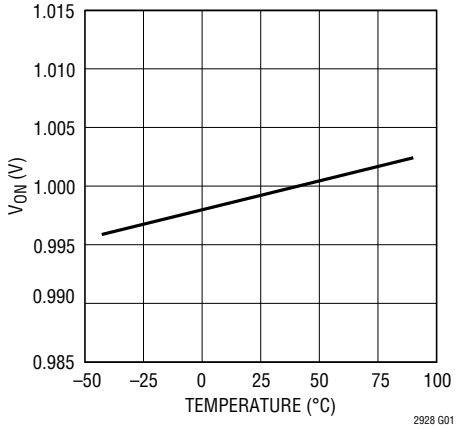
Comparator Under-Voltage Glitch Immunity



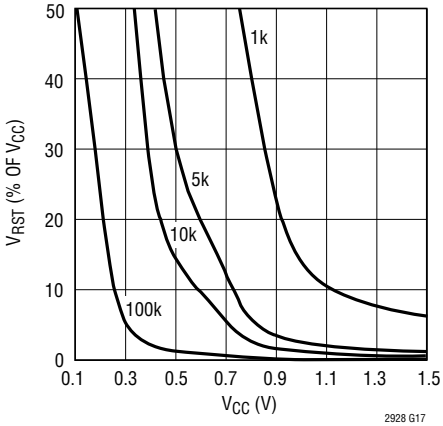
Comparator Over-Voltage Glitch Immunity



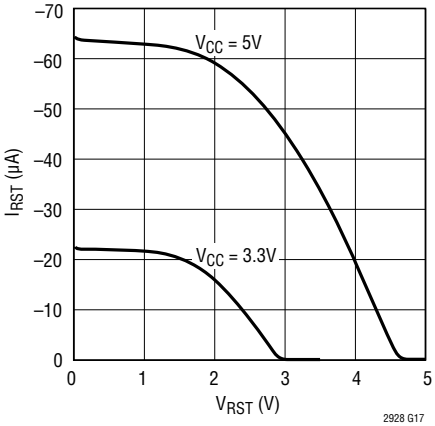
ON Threshold Voltage (Rising) vs Temperature



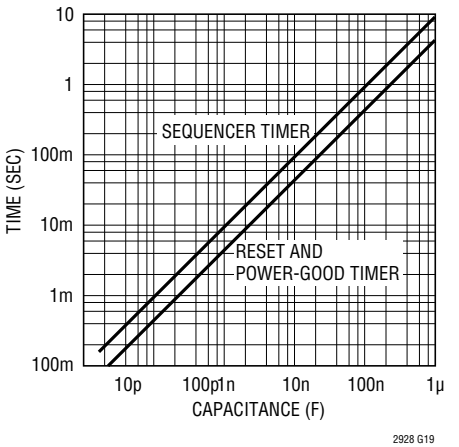
Relative Reset Output Voltage vs V_{CC} (with Reset Pull-Up Resistor to V_{CC})



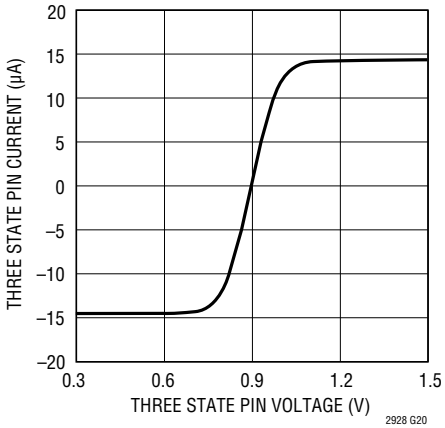
$\overline{RST}$ Pull-Up Current vs External Voltage on $\overline{RST}$



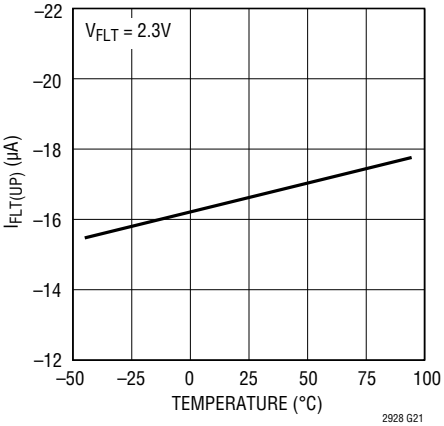
Sequence, Reset and Power-Good Timing vs Capacitance



Three State Selection Pin Current vs Pin Voltage (SQT1, SQT2, MS1, MS2, RDIS)

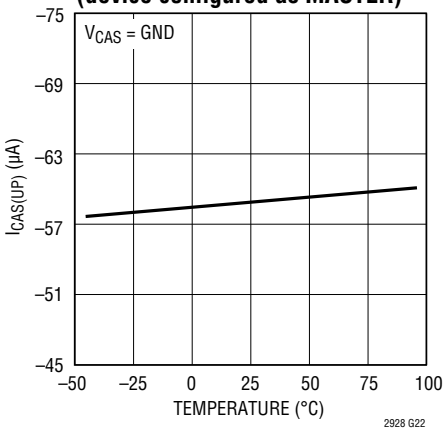


$I_{FLT(UP)}$ vs Temperature

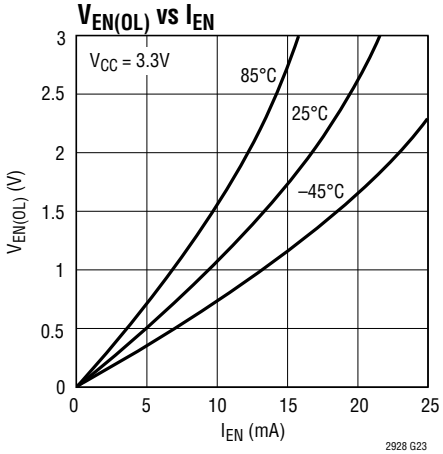


TYPICAL PERFORMANCE CHARACTERISTICS

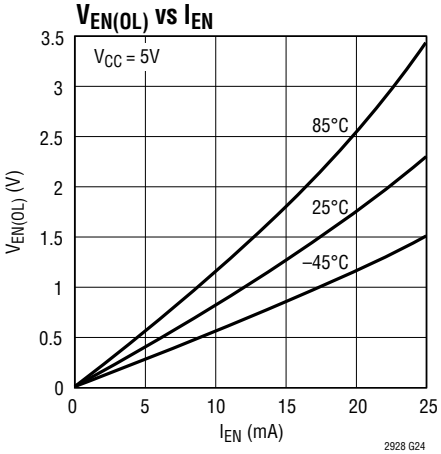
$I_{CAS(UP)}$ vs Temperature (device configured as MASTER)



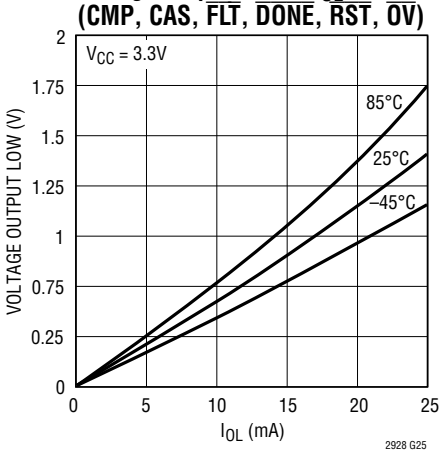
$V_{EN(OL)}$ vs I_{EN}



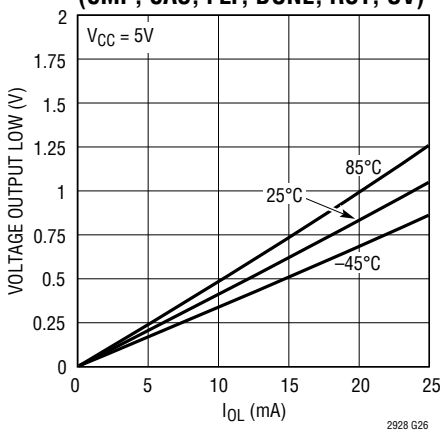
$V_{EN(OL)}$ vs I_{EN}



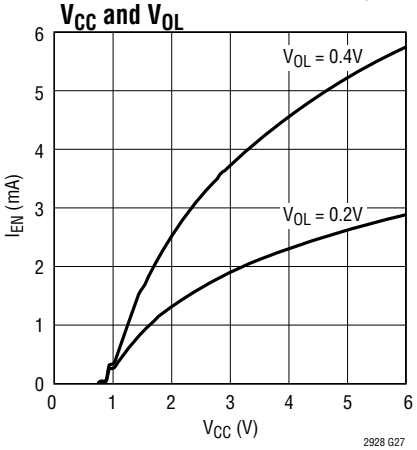
Voltage Output Low vs I_{OL} (CMP, CAS, $\overline{FLT}$, $\overline{DONE}$, $\overline{RST}$, $\overline{OV}$)



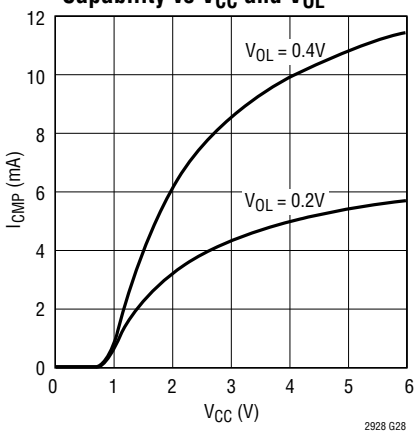
Voltage Output Low vs I_{OL} (CMP, CAS, $\overline{FLT}$, $\overline{DONE}$, $\overline{RST}$, $\overline{OV}$)



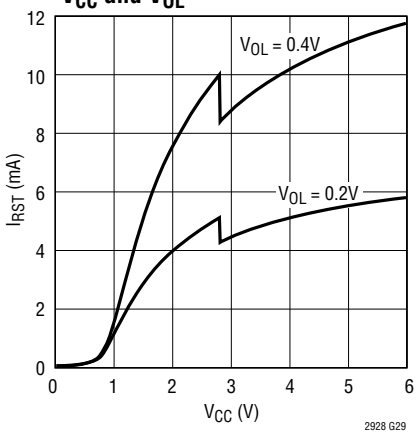
Enable Current Sink Capability vs V_{CC} and V_{OL}



Comparator Output Current Sink Capability vs V_{CC} and V_{OL}



Reset Current Sink Capability vs V_{CC} and V_{OL}



PIN FUNCTIONS

CAS: Cascade Input/Output. Connect the cascade pin between a master and one or more slave devices to increase the number of supplies that can be sequenced per time position. See Applications Information for details. Do not add capacitance to the cascade pin. Leave open if unused.

CMP1-CMP4: Comparator and/or Fault Status Outputs. The CMP outputs have a weak internal pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. During sequence-up or sequence-down operation, all comparator outputs are low. After sequencing-up, during supply monitoring, comparator outputs pull low if their monitor input drops below its undervoltage threshold. In the event of a system fault, the CMP outputs latch and may be read to diagnose the type and source of fault. See Applications Information for the fault reporting details. Leave the CMP outputs open if unused.

$\overline{\text{DONE}}$: Sequence Done Output. The last (or only) LTC2928 must have $\overline{\text{DONE}}$ pulled high with an external resistor to V_{CC} (3.3k 5% recommended). The LTC2928 floats $\overline{\text{DONE}}$ until the completion of a sequence-up operation when it is pulled down. At the end of a sequence-down operation, the LTC2928 returns $\overline{\text{DONE}}$ to a high-impedance state. If subsequent time positions are required for additional supplies, use the $\overline{\text{DONE}}$—ON handshake connection. See Applications Information regarding the $\overline{\text{DONE}}$—ON protocol.

EN1-EN4: Enable Outputs. Connect these outputs to a power supply shutdown input or an external N-channel MOSFET gate for the supply to be sequenced. When enabled, each output is connected to an internal charge pumped supply (nominally V_{CC} + 5.5V) via an internal 10µA current source. When disabled, each output is pulled to ground. EN outputs operate with their respective RT inputs. Leave enable outputs open when unused.

Exposed Pad: Exposed pad may be left floating or connected to device ground.

$\overline{\text{FLT}}$: Fault Input/Output. Pull $\overline{\text{FLT}}$ high with an external resistor (10k recommended). The LTC2928 will pull $\overline{\text{FLT}}$ low if an internal fault condition is detected (see Applications Information for details). An external signal such as $\overline{\text{OV}}$ may also pull down the $\overline{\text{FLT}}$ pin to cause an external fault. Any internal or external fault condition forces all enable outputs low. In order to clear a fault condition, a "return-to-zero" state must be reached with all monitored supplies falling below their configured sequence-down thresholds, while the ON input is below 0.97V. Debugging modes are available (use the MS1, MS2 inputs) to leave supplies enabled upon system faults. See Applications Information for configuration tables.

GND: Device ground.

HV_{CC}: High Voltage (7.2V to 16.5V) Power Supply Input. Bypass HV_{CC} with at least 0.1µF to ground in close proximity to this pin. The internal HV_{CC} regulator provides a regulated 3.3V to V_{CC}. V_{CC} may be used to power external circuits (limited to 10 mA external load). Tie HV_{CC} to ground when unused.

MS1, MS2: Master/Slave Three State Configuration Inputs. Depending on the application, select each LTC2928 as a master or slave part and whether or not the part is designated as the first part in a cascade application. The $\overline{\text{RST}}$—$\overline{\text{FLT}}$ relationship (after $\overline{\text{RST}}$ pulls high for the first time) is also configured with these inputs. Select whether or not $\overline{\text{RST}}$ pulling low should cause $\overline{\text{FLT}}$ to pull low and shutdown the system. Select debugging modes to leave supplies enabled upon system faults. See Applications Information for configuration table.

N/C: No Connect. Unconnected pins.

ON: Sequence Up/Down Input. A voltage transition above 1V starts the sequence-up phase. A voltage transition below 0.97V starts the sequence-down phase. An ON transition applied during a sequence-up (or down) phase is treated as a command fault. See Applications Information for using the $\overline{\text{DONE}}$—ON handshake protocol when cascading multiple LTC2928s to append additional time positions.

PIN FUNCTIONS

$\overline{OV}$: Overvoltage Output. Pulls low when any positive supply exceeds its configured overvoltage threshold. $\overline{OV}$ remains low until all positive supplies have remained below the overvoltage threshold for a time equal to the configured $\overline{RST}$ delay time. To generate an overvoltage fault, connect $\overline{OV}$ to $\overline{FLT}$. The $\overline{OV}$ output has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. $\overline{OV}$ may be left unconnected if unused. See Applications Information for details.

OVA: Over Voltage Adjust Input. After configuring the undervoltage thresholds, bias this input to set the overvoltage threshold for all positive supplies. Leave the pin floating to set an overvoltage threshold approximately 32% above the undervoltage threshold. Tie OVA to V_{CC} to move the overvoltage threshold above 1V. Consult the Applications Information for details on OVA biasing.

PTMR: Power Good Timer. Attach an external capacitor to ground to set the maximum time allowed for all supplies to reach their configured undervoltage threshold during sequence-up phase (or all supplies below their sequence-down threshold during sequence-down phase). The timer is started when the first enable (EN) is raised (or lowered). The power good timing scale factor is 4000ms/µF. A 0.1µF capacitor generates a 400ms delay time. If any supply is late, a sequence fault is generated. $\overline{FLT}$ pulls low and all supply enable outputs are pulled low. Disable the power good timer by grounding PTMR. Consult Applications Information for more details.

RDIS: Reset Disable Three State Input. Typically used for supply margining applications. Pull RDIS high or low to force $\overline{RST}$ high. Leave the RDIS input open to allow $\overline{RST}$ to operate normally.

REF: Reference Output. REF is used to offset negative supplies connected through resistance to V1. The reference will move during sequence-up and sequence-down operation to effect the selected thresholds. The buffered reference sources 1mA and sinks up to 200µA of current. The reference drives a bypass capacitor of up to 1000pF without oscillation.

$\overline{RST}$: Reset Output. If any supply is below its undervoltage threshold, $\overline{RST}$ pulls low. $\overline{RST}$ pulls high after all supplies are above their undervoltage threshold for the configured delay time (configure delay time using the RTMR pin). The $\overline{RST}$ output has a weak pull-up to V_{CC} and may be pulled above V_{CC} using an external pull-up. $\overline{RST}$ is guaranteed low with V_{CC} down to 0.5V. Configure the $\overline{RST}$ to $\overline{FLT}$ relationship using the MS1, MS2 inputs. See Applications Information for details. Leave the $\overline{RST}$ output open if unused.

RTMR: Reset Timer. Attach an external capacitor to ground to set a reset delay time of 4000ms/µF. Floating RTMR generates a minimum delay of approximately 50µs. A 0.047µF capacitor will generate a 190ms delay time.

RT1-RT4: Resistive Time Position Configuration Inputs. Place a single resistor from V_{CC} to each input to select one of eight time positions in which to turn-on or turn-off each enable output (see Applications Information for RT table). Each RT input numerically corresponds to a respective EN output and monitor input. During sequencing-up, an enable output (EN) pulls high at the start of its chosen time position. During sequencing-down, an enable output (EN) pulls low at the start of its chosen time position (sequence-down position is the reverse of sequence-up). To remove a monitor channel from participation, command any enable off by pulling its corresponding RT input to ground. Prior to sequencing, any enable may be commanded on by pulling its corresponding RT input to V_{CC}. Maximum capacitive load is 150pF.

SQT1, SQT2: Sequencing Threshold Three State Configuration Inputs. Select sequencing thresholds as a percentage of the 0.5V supply monitor threshold for positive supplies and as a percentage of REF for negative supplies. For sequencing-up choose from 33%, 67% or 100%. For sequencing-down choose from 100%, 67%, 33% or 10%. See Applications Information for configuration table.

PIN FUNCTIONS

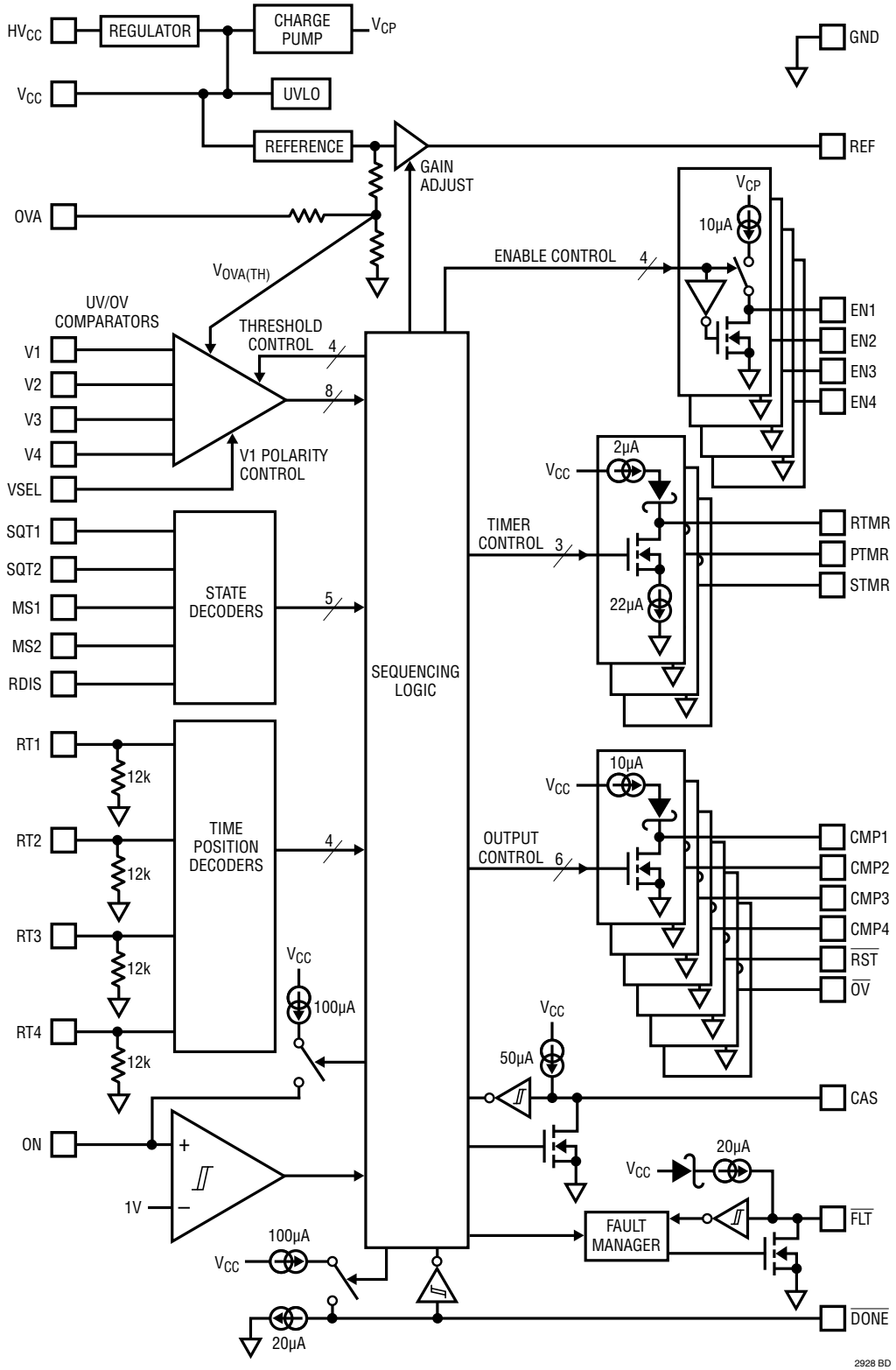
STMR: Sequence Timer. Attach an external capacitor to ground to set the adjacent time-position delay between sequenced supplies. For supplies in adjacent time positions, this delay resides between the previous supply crossing its sequence-up (down) threshold and the next enable (EN) pulling high (low). For a supply in time position 1, the sequence delay is the time from ON going high to its enable pulling high. The sequence timing scale factor is 8670ms/µF. Floating STMR generates a minimum sequencing time delay of approximately 100µs. A 3300pF capacitor will generate a 29ms delay time. Referring to the timing diagrams, the sequence delay time is equivalent to the cascade (CAS) pin high time. Consult Applications Information for details.

V_{CC}: Power Supply Input/Output. All internal circuits are powered from V_{CC}. Bypass V_{CC} with at least 0.1µF to ground in close proximity to this pin (1µF minimum when using HV_{CC}).

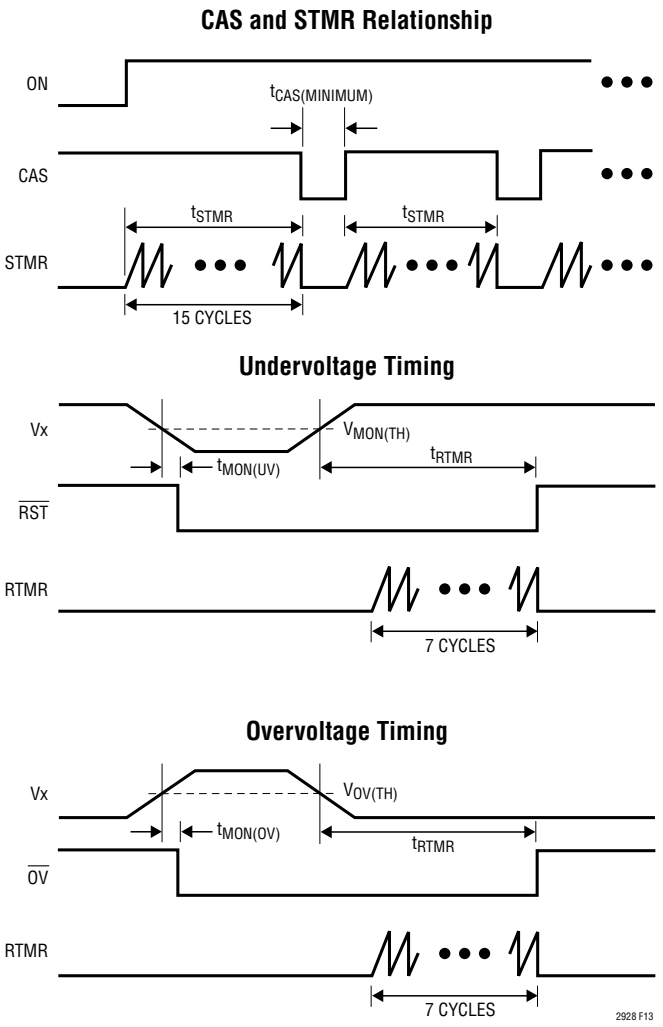
VSEL: Voltage Monitor Select Input. Tie to ground to select four positive inputs. Tie to V_{CC} for three positive and one negative adjustable input. Negative supplies are monitored on the V1 input. See Applications Information for configuration table.

V1-V4: Voltage Monitor Inputs. Connect these high impedance inputs to external resistive dividers between each monitored power supply and ground (or REF for negative supplies monitored on V1). See Applications Information for selecting resistors to configure the monitor thresholds. Voltage monitor inputs operate with their respective RT inputs and EN outputs. OV comparators are always active. Tie unused monitor inputs to GND.

FUNCTIONAL DIAGRAM



TIMING DIAGRAMS



OPERATION

The LTC2928 is a four channel, cascadable power supply sequencer and supervisor for use with external N-channel MOSFETs or power supplies with shutdown/enable inputs. An unlimited number of power supplies may be fully sequenced at configurable points in time using multiple LTC2928s. A single LTC2928 controls up to four supplies (four positives or three positives and one negative) and one external resistor per supply configures each supply enable (disable) time position. Device power is applied through either V_{CC} (2.9V to 6V) or HV_{CC} (7.2V to 16.5V). When applying power through HV_{CC}, a regulated 3.3V is output on V_{CC}. An internal charge pump provides (V_{CC} + 5.5V) gate drive voltages at the enable outputs EN1 to EN4 for driving external pass FETs.

The LTC2928 monitors four supply thresholds per supply (sequence-up, sequence-down, undervoltage, overvoltage) during a full system cycle. A full cycle comprises a sequence-up phase, monitor phase and sequence-down phase. A sequence timer sets the time delay between supply enables during both the sequence-up and sequence-down phases. The power-good timer is a watchdog for stalled supplies during the sequence-up and sequence-down phases. A microprocessor reset signal is issued once all supplies are above their undervoltage threshold for the chosen reset time. During the monitor phase, all enabled supply voltages are continuously compared with their undervoltage threshold. If any supply falls below its undervoltage threshold, the reset output pulls low. The reset output pulls high once all enabled supplies have been in compliance for the chosen reset time. During any phase, all positive supplies are continuously monitored for overvoltage conditions.

Implementing complex power-on and power-off schemes is simple using the LTC2928. System errors are easily diagnosed with the LTC2928 fault event reporting feature. Basic LTC2928 operation is discussed below. Configuration tables are given in the Applications Information section. The Applications Information also includes many of the unique and advantageous extensions to the basic operation, such as Master/Slave configurations.

Sequence-Up Phase

While V_{CC} is ramping up, the LTC2928 enters a power-on mode and pulls down its CAS pin. When V_{CC} is stabilized, the LTC2928 is configured for operation and releases its CAS pin. Multiple LTC2928s with common CAS connections will therefore synchronize with each other. The ON input is used to start the sequence-up and sequence-down process. The state of ON is ignored until CAS is released. When the voltage at the ON input exceeds 1V, the sequence-up phase is enabled after a small propagation delay (20µs typical). If the ON signal prematurely pulls below 0.97V during the sequence-up phase, a command fault is generated, causing enable (EN) outputs to pull low. For more details refer to the discussion on system faults later in this document.

At the beginning of the sequence-up phase, a current source begins to charge the STMR capacitance. When

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the sequence timer has expired the CAS pin pulls low. At this time, any enable (EN) scheduled (using the RT inputs) for "time position 1" pulls high, allowing a supply (or supplies) to be turned on. The CAS pin is held low until all monitored inputs in the current time position exceed their selected sequencing-up threshold (25µs minimum).

Once all supply monitor inputs cross their sequencing-up threshold, or if no enable was selected for the current time position, the CAS pin is allowed to pull high. The STMR capacitor begins to charge again, moving the system to "time position 2". This process repeats until the system is clocked through "time position 8".

During the sequence-up phase, supply monitor inputs are expected to cross their sequence-up threshold (which may be different from their undervoltage threshold). Any supply monitor input failing to cross its sequence-up threshold will stall the process and a sequence-up fault is generated (if the power-good timer is active). The power-good timer starts with the first enable output to go high and is cleared when the last supply monitor input reaches its undervoltage threshold. Any supply monitor input failing to cross its sequence-up threshold before the power-good timer expires also generates a sequence-up fault. A sequence-up fault pulls $\overline{FLT}$ and all supply enable outputs (EN) low. Use a single capacitor from PTMR to ground to select the power good time. To disable the power good timer, simply tie PTMR to ground.

Each comparator switches to its undervoltage threshold when the respective supply monitor input crosses its sequence-up threshold. The comparator outputs are allowed to pull high after the LTC2928 clocks through time position 8.

After a system fault, fault information is latched to the CMP outputs. Read the CMP outputs to obtain the fault type (internally generated sequence-fault, reset-fault, command-fault or an externally generated fault) and the fault channel (if any). For more details refer to the discussion on system faults later in this document.

After the system has clocked through "time position 8", the last LTC2928 (defined by a 2.4k to 5.1k pull-up resistor on $\overline{DONE}$) pulls down on $\overline{DONE}$.

Supply Monitor Phase

Once all supply monitor inputs have crossed their sequence-up thresholds, the LTC2928 enters its supply monitor phase. As referred to earlier, the comparators switch to their highly accurate undervoltage thresholds after crossing their sequence-up threshold. The monitor thresholds maintain 1.5% accuracy over temperature.

$\overline{RST}$ pulls high after all supply monitor inputs (V1 to V4) have been above their undervoltage threshold for the selected reset delay time. The reset delay is set with a capacitor attached between RTMR and ground.

The supply monitor comparators will filter out minor glitches coupled to their inputs. If any supply falls below threshold with sufficient magnitude and duration, the $\overline{RST}$ line pulls low. The reset timer starts once all inputs return above threshold.

The LTC2928 can be configured to issue a fault if $\overline{RST}$ pulls low due to an undervoltage event (see master/slave configuration table in Applications Information). Upon a $\overline{RST}$ fault, $\overline{FLT}$ and the enable outputs pull low. Use the fault report capability to determine which input was below threshold. For more details refer to the discussion on system faults later in this document.

The reset disable input (RDIS) may be pulled high or low to force $\overline{RST}$ high regardless of voltage monitor level. This feature is useful during voltage margining tests.

Sequence-Down Phase

The sequence-down phase is initiated by pulling the ON input below 0.97V. This action pulls $\overline{RST}$ low immediately. The comparator thresholds (and REF for negative supplies) are moved to their selected sequence-down thresholds. Beginning with any supplies in "time position 8", the enable outputs are sequenced-down by pulling enable low in the reverse order of sequence-up (last on, first off).

During the sequence-down phase, supply monitor inputs are expected to cross their sequence-down threshold (which may be different from their undervoltage threshold) within the selected power good time. Any supply monitor input failing to cross its sequence-down threshold will stall the process and a sequence-down fault is generated (if the power-good timer is active).The power-

OPERATION

good timer starts with the first enable output pulling low and is cleared when the last supply monitor input crosses its sequence-down threshold. A sequence-down fault pulls $\overline{FLT}$ and all enable outputs low. Use a single capacitor from PTMR to ground to select the power good time. To disable the power good timer, tie PTMR to ground.

All comparator outputs pull low at the start of the sequence-down phase (ON low). If a sequence-down fault occurs, use the fault report capability to determine which supply failed to meet threshold (or other source of fault). Force all supplies down in an un-sequenced manner by pulling $\overline{FLT}$ low (external fault). For more details refer to the Applications Information and discussion on system faults later in this document.

After the system has clocked through "time position 1", the last LTC2928 (defined by a 2.4k to 5.1k pull-up resistor on $\overline{DONE}$) releases the pull down on $\overline{DONE}$ and $\overline{DONE}$ pulls high.

Table 1. Input Polarity Selection

V1	V2	V3	V4	VSEL
+ ADJ (0.5V)	+ ADJ (0.5V)	+ ADJ (0.5V)	+ ADJ (0.5V)	GND
– ADJ (0V)	+ ADJ (0.5V)	+ ADJ (0.5V)	+ ADJ (0.5V)	V_{CC}

Table 2. Master/Slave Configuration Pins

MASTER	SLAVE	FIRST CASCADE POSITION	NOT FIRST CASCADE POSITION	$\overline{RST}$ PULLS $\overline{FLT}$	$\overline{RST}$ DOES NOT PULL $\overline{FLT}$	NO SHUTDOWN DEBUG MODE*	MS1	MS2
●		●		●			GND	GND
●		●			●		GND	Open
●			●	●			GND	V_{CC}
●			●		●		Open	GND
	●	●		●			Open	Open
	●	●			●		Open	V_{CC}
●		●		●		●	V_{CC}	GND
●			●	●		●	V_{CC}	Open
	●	●		●		●	V_{CC}	V_{CC}

* No shutdown debug mode. In this mode, any internal or external fault will halt the system with full fault reporting but all enabled supplies remain enabled.

Table 3. Sequence Time Position Resistors (1%)

POSITION NUMBER	R_T (kΩ)
1	95.3
2	42.2
3	24.3
4	15.0
5	9.53
6	6.04
7	3.40
8	1.50

Table 4. Sequencing Threshold Selection (% of 0.5V for ADJ, % of REF for –ADJ)

SEQUENCE-UP (%)	SEQUENCE-DOWN (%)	SQT1	SQT2
100	100	V_{CC}	V_{CC}
100	67	Open	V_{CC}
100	33	Open	Open
100	10	Open	GND
67	100	V_{CC}	Open
67	67	GND	V_{CC}
67	33	GND	Open
67	10	GND	GND
33	100	V_{CC}	GND

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Fault Detection

The LTC2928 has sophisticated fault detection circuitry which can detect:

- Stalled supplies (with power good timer enabled) during sequencing
- Under or overvoltage supplies
- System controller command errors
- Externally commanded faults

If any of the above faults are detected, the LTC2928 immediately pulls the EN1 through EN4 outputs low, turning off all enabled supplies.

In order to clear the fault condition within the LTC2928, the following conditions must exist:

- All sequenced supplies must be below their sequence-down thresholds
- The ON input must be below 0.97V
- The $\overline{FLT}$ pin must be externally released

Sequencing Faults

The LTC2928 keeps track of power supplies that need to exceed their sequencing thresholds within the configured power good time during the sequence-up and sequence-down phases. Should any supply fail this test a sequence fault is generated. All enable outputs and $\overline{FLT}$ are pulled low.

System Controller Command Faults

After the sequence-up phase has begun (ON input high), the ON input must remain above 1V until $\overline{DONE}$ pulls low (sequence-up complete). Pulling ON low before the sequence-up process is complete is considered a command fault. All enable outputs and $\overline{FLT}$ are pulled low.

Similarly, after the sequence-down phase has begun (ON input low), the ON input must remain below 0.97V until $\overline{DONE}$ pulls high (sequence-down complete). Pulling ON high before the sequence-down process is complete is considered a command fault. All enable outputs and $\overline{FLT}$ are pulled low.

Reset Faults

Use the MS1 and MS2 configuration pins to select whether or not the system should fault if any monitored input falls below its undervoltage threshold. A reset fault may only occur after the LTC2928 comes out of reset for the first time after sequencing. All enable outputs and $\overline{FLT}$ are pulled low.

External Faults

An external fault is generated by pulling the $\overline{FLT}$ pin low. Tie the $\overline{OV}$ pin to $\overline{FLT}$ to generate overvoltage faults. In applications using multiple LTC2928s, tie all the $\overline{FLT}$ pins together to ensure proper re-sequencing. Upon detecting an external fault, all enable outputs are pulled low.

Fault Reporting Map

For diagnostic purposes, fault information is latched to the comparator outputs after a fault. The table below provides a map to the available fault information. The fault information remains latched until the LTC2928 completes the next sequence-up operation.

Table 5. Fault Reporting

FAULT CODES		
FAULT TYPE	**CMP1**	**CMP2**
Sequence Fault	Low	Low
Reset Fault	Low	High
Command Fault	High	Low
External Fault	High	High
FAULT CHANNEL	**CMP3**	**CMP4**
1	Low	Low
2	Low	High
3	High	Low
4	High	High

Should multiple faults occur simultaneously, the reported fault is given priority according to the following order:

1) Sequence Fault
2) External Fault
3) Reset Fault
4) Command Fault (channel code is meaningless)

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Should multiple channels fault simultaneously, the reported channel is given priority according to the channel number (1,2,3,4).

In the event of an external fault, the LTC2928 fault manager reports overvoltage channels to the fault channel outputs (CMP3, CMP4). If no channel is overvoltage, the default report is channel 4 (High, High). As such, in certain applications, a potential reporting ambiguity exists.

Operating without Pass Transistors

The LTC2928 enable outputs may directly drive the shutdown/enable, run/soft-start or control inputs on DC/DC converters. However, since the LTC2928 enable outputs may drive to a relatively high voltage with low current (10μA), care must be taken not to exceed the maximum voltage rating on the DC/DC converter enable input. The gate voltage available from the LTC2928 enable output ranges between V_{CC} + 4.5V to V_{CC} + 6V. Use a resistor to limit an enable output to an external supply voltage. A resistor between 4.7k and 27k is recommended.

Cascading Multiple LTC2928s

LTC2928s can be cascaded in two ways, simultaneously. The first method, time extension, allows an unlimited number of supplies to be sequenced in additional time positions. The second method, supply extension, allows additional supplies to be sequenced in the same time position. The examples below demonstrate how to achieve time and supply extension.

Central to configuring a cascade application is the assignment of LTC2928 properties such as master/slave and first/not-first/last status. Master/Slave and first/not-first designation is made with the MS1 and MS2 three-state configuration inputs (see Table 2). An LTC2928 is configured as "LAST" by pulling $\overline{DONE}$ to V_{CC} with a 2.4k to 5.1k resistor.

Next, the appropriate connection of one or both bidirectional communication lines must be made. To achieve supply extension, the CAS pins between master and slave devices are tied together (Figure 1). To achieve time extension, the $\overline{DONE}$ pin of the preceding LTC2928 is connected to the ON pin of the subsequent LTC2928 (Figure 2). Both connections are allowed to exist within one system (Figure 4). It is important not to corrupt these communication lines with added passive or active loads.

CAS Connection: Supply Extension

When more than four supplies need to be synchronized in time, use the CAS connection. Consider the application in Figure 1. This application allows for 8 supplies in 8 distinct time positions, or all at once depending upon the choice of RT resistors. The upper device is designated as master and the lower device is the slave. Both LTC2928s are configured as "FIRST" and "LAST" and the CAS pins are tied together.

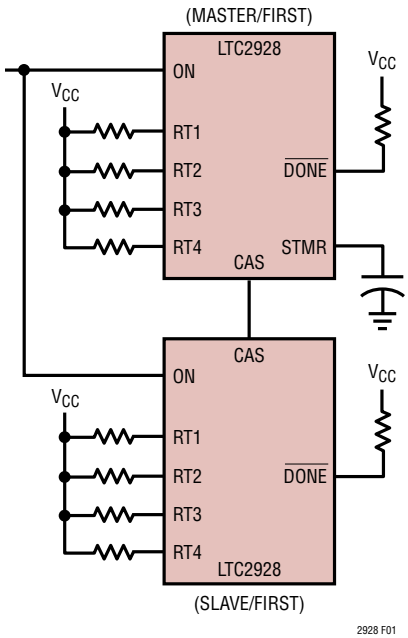

Figure 1. Using the CAS Pin to Synchronize Additional Power Supplies (Slave STMR is Not Used)

The master controls the sequencing. The time delay between adjacent positions is configured with a capacitor on the master's STMR pin and the slave STMR is ignored. After application of the ON signal to start the sequence-up phase, the CAS pin pulls low, enabling any supply configured for time position 1. After supplies in time position 1 cross their sequence-up threshold, CAS is released and pulled high. If no supplies are configured for a particular time position, CAS pulls high after 25μs. CAS remains high for one STMR period (100μs minimum) and then pulls low again to enable supplies in time position 2. The

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process repeats until CAS clocks through time position 8 and $\overline{DONE}$ pulls low.

To sequence down, the ON input is pulled low. Supplies in time position 8 are disabled. After supplies in time position 8 fall below their sequence-down threshold, CAS is released and pulled high. CAS remains high for one STMR period and then pulls low again to disable supplies in time position 7. The process repeats until CAS clocks through time position 1 and $\overline{DONE}$ pulls high.

$\overline{DONE}$-ON Connection: Time Extension

When additional time positions and/or additional supplies require control, use the $\overline{DONE}$—ON connection. Consider the application in Figure 2. This application allows for 8 supplies in 16 distinct time positions (4 supplies within the first 8 time positions, and 4 more within the second 8 time positions). Both LTC2928s are designated as master. Each has its own STMR capacitor allowing for different sequence timing. The left most device is designated as "FIRST", and the right most device is "NOT FIRST" and "LAST".

It is critical to note here that the $\overline{DONE}$ pin of the first device is connected to the ON pin of the second device, and that this connection forms a bidirectional communication line for the purposes of sequence control. $\overline{DONE}$ and ON do not function as typical $\overline{DONE}$ and ON pins. The handshaking that occurs between these pins is described below.

To start the sequence-up process, the first ON input is pulled high. The first device sequences the first 4 supplies as usual. The first $\overline{DONE}$ pin has recognized that the first device is not the last because it has not been pulled up to V_{CC} with a resistor. Knowing this information, the first $\overline{DONE}$ pin pulls up the second ON input. The second device now sequences its 4 supplies normally. When the second device is finished, the second $\overline{DONE}$ pin pulls low as expected.

To start the sequence-down process, the first ON input is pulled low. The first device has recognized that the first $\overline{DONE}$ pin was high and already knows that it is not the last device. The first $\overline{DONE}$ pin therefore pulls the second ON pin low. The second $\overline{DONE}$ pin was low and is the last device. Therefore, the second device starts its sequence-down procedure. When finished, the second $\overline{DONE}$ stays low, and the second ON pin, knowing that it is not first, pulls up the first $\overline{DONE}$ pin. The first $\overline{DONE}$ pin senses the pulled up condition and triggers the sequence-down process for the first device. When the first device is finished, the $\overline{DONE}$ pin pulls down, overriding the pull-up from the second ON pin. The second device then releases its $\overline{DONE}$ pin, which pulls up to V_{CC}, and the process is complete.

Time extension can cascade to more than two devices as shown in Figure 3. It is a simple matter of adding more LTC2928s in the middle of the cascade, with a master/not-first designation.

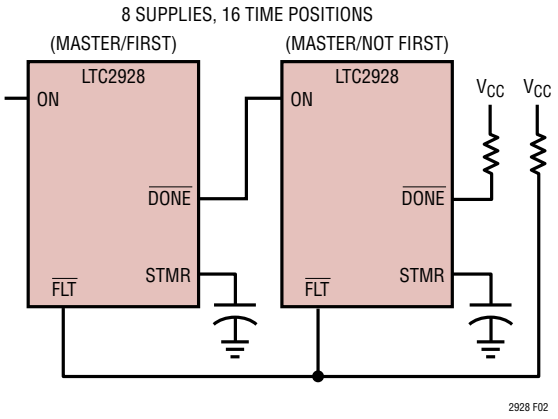


Figure 2. Using the $\overline{DONE}$—ON Interface to Extend Number of Supplies and Time Positions (STMR Capacitors May Be Different)

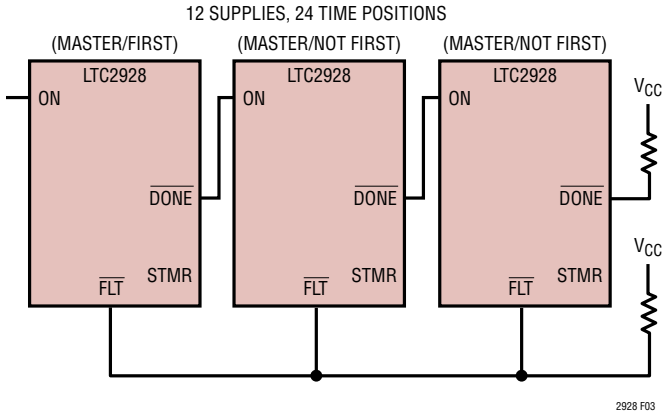


Figure 3. Additional Supply and Time Extension

APPLICATIONS INFORMATION

Another interesting application combines the usage of both the CAS pin connection and the $\overline{\text{DONE}}$—ON communications link. Figure 4 shows a two dimensional configuration of four LTC2928s that allows for 16 supplies to be sequenced in up to 16 time positions.

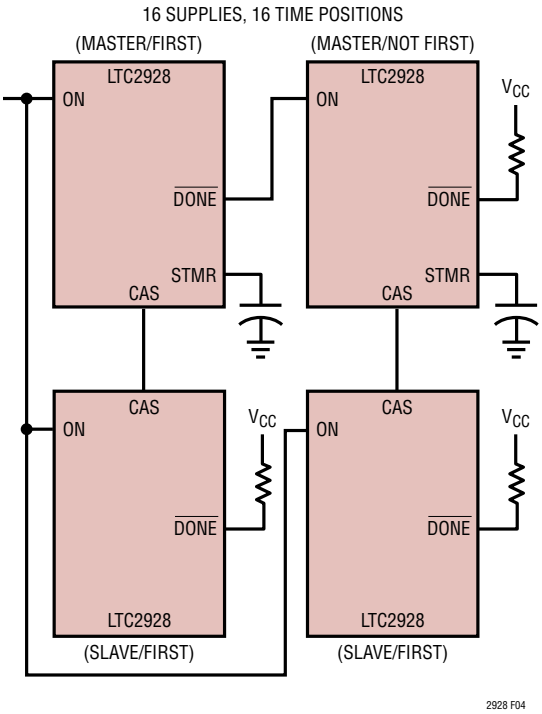


Figure 4. Two-Dimensional Application

In this application, both slave devices are clocked by the masters through their CAS pins. Again, sequencing-up begins with ON pulling high. Although the ON input is high on the device in the lower right quadrant, sequencing-up will not begin there until the first master (upper left), and its slave are finished sequencing-up. At that time the $\overline{\text{DONE}}$ pin will pull up the ON pin of the second master. The second master and slave will then start sequencing up their supplies.

Using an Enable Line to Generate a Sequencing-Up Delay

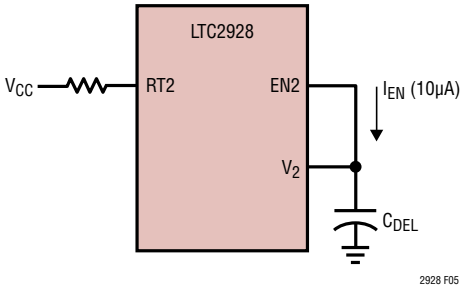


Figure 5. Adjustable Sequencing Delay

An arbitrary delay between enables may be added by using an enable pull-up current (10µA) to charge a delay capacitor (Figure 5). Position the delay using an RT resistor. Assuming 100% sequencing thresholds (0.5V) and a fully discharged delay capacitor (C_{DEL}), the added time delay (T_{DEL}) is:

$$T_{DEL}(ms) = 50 \bullet C_{DEL}(\mu F)$$

Be sure to account for the extra delay when using the power-good timer (PTMR).

Extending Sequencing Delay to Subsequent Supplies

Sequencing delays can be extended after certain events by paralleling capacitance to the STMR pin. Figure 6 shows one way to add capacitance after a particular enable output pulls high.

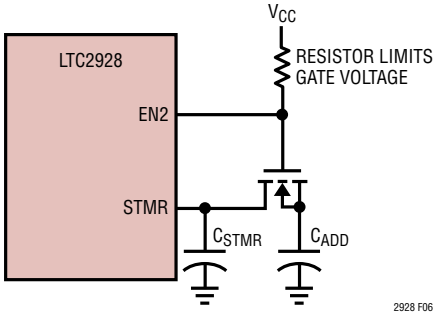


Figure 6. Adding STMR Capacitance

APPLICATIONS INFORMATION

Correcting for IR Drops

Sense feedback is common in high current applications. Parasitic resistance coupled with high currents causes voltage drops. The sense pin of a power module is designed to help regulate the voltage at a point in the distribution circuitry beyond the voltage drops. The output of the power module is raised until the desired voltage is achieved at the sense point. During startup with sense feedback, large inrush currents may cause the output of the power module to exceed its maximum output. This may cause the module to shutdown.

The LTC2928 is easily configured to enable a sense transistor after a power supply has been sequenced on and inrush currents have diminished (Figure 7). The sense transistor feeds the sequenced supply voltage back to the sense line of the power module. The power module will raise its output to compensate for voltage drops across the sequencing transistor and other parasitics.

During the sequence-down phase, the sense transistor will be disconnected before the supply sequencing transistor. If the supply transistor were to be disconnected first, the power module would sense the voltage drop and may attempt to drive higher in order to compensate.

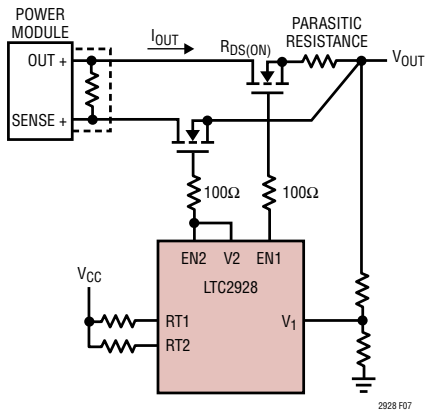


Figure 7. Correcting for IR Drops (RT1 > RT2)

Discharging Load Capacitance

It is often necessary to discharge load capacitance quickly. Use the pull-down strength of the LTC2928 enable outputs to achieve faster turn-off times. Sequence the enable outputs in the same time position (RT resistors are identical). With the connections shown in Figure 8, EN1 is used to discharge the load capacitance through its 100Ω on resistance. If shorter discharge time is required, use external inverters as shown in Figure 9.

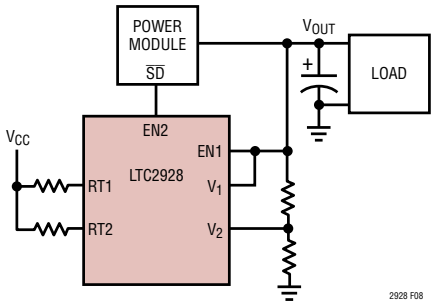


Figure 8. Load Capacitance Discharge

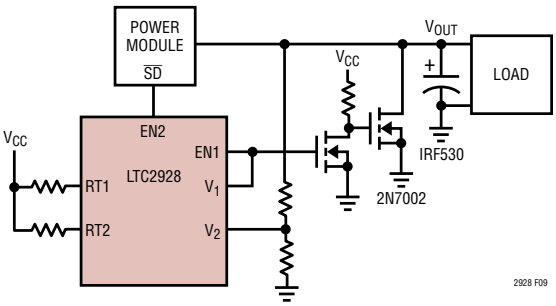


Figure 9. Fast Load Capacitance Discharge

Using the Power Module Voltages to Gate the Sequenced Supplies

The application shown in Figure 10 demonstrates how the power module outputs can be enabled and monitored for compliance, and then passed to various loads. Sequencing up and down is controlled by the level of the 12V supply. Sequencing up begins at 10.76V. If the application is disconnected from the 12V supply, an orderly shutdown will commence when the 12V supply drops to 10.43V. The blocking diode (D1) allows the 470µF capacitor (C1) to retain enough energy to complete the sequence down process.

APPLICATIONS INFORMATION

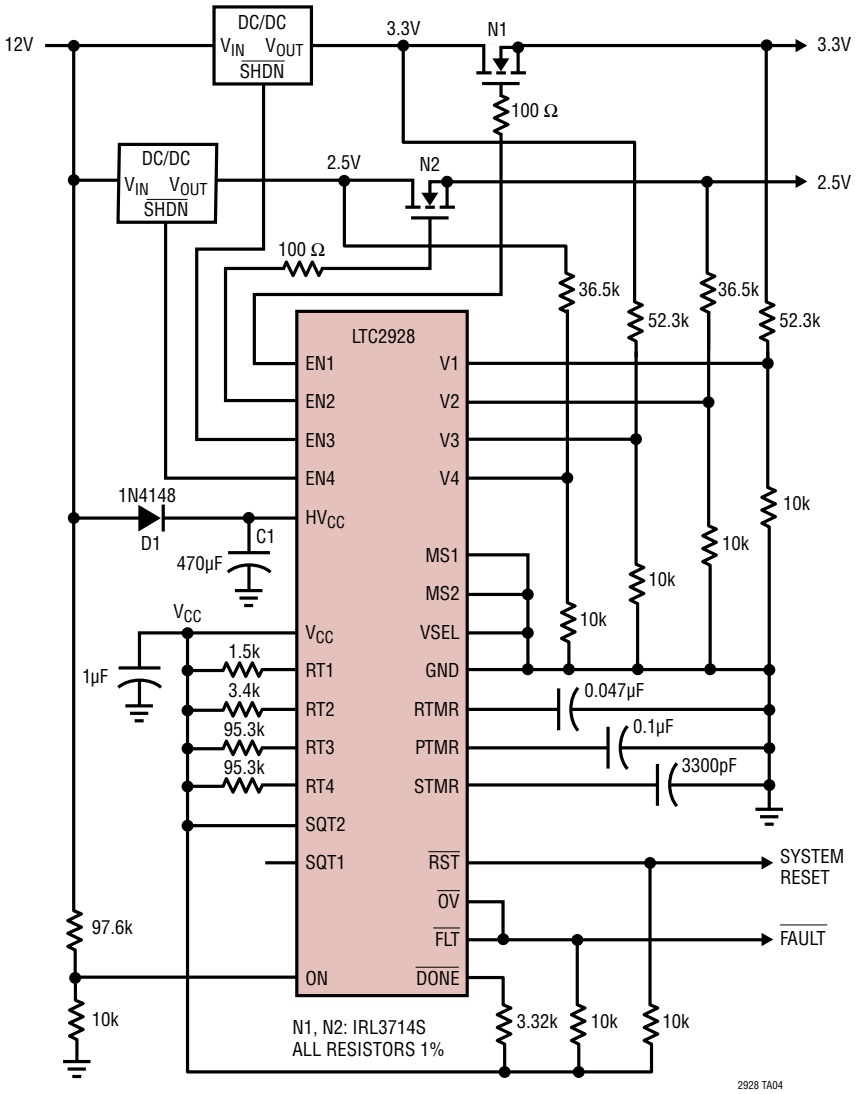


Figure 10. Supply Sequencing with Stabilized Power Module Outputs

APPLICATIONS INFORMATION

Forcing Supplies Off or Disabling Unused Channels

The most convenient way to mask an unused channel is to tie its respective RT input to ground. After sequencing begins, any enable output (EN) may be pulled low permanently by driving the respective RT input to ground (asynchronous OFF command). An asynchronously OFF channel cannot be re-enabled until a new sequence-up procedure is started. Any channel that is asynchronously OFF is removed from participation in the sequencing and supply monitoring processes, allowing the LTC2928 to operate normally on the remaining operating channels.

When experiencing a fault in the "No Shutdown Debug Mode", the asynchronous OFF feature may be used to conveniently pull down the enable outputs. Alternatively, V_{CC} may be turned off and on again. Clearing a fault condition requires the ON input to be low while the supplies are below their sequence-down thresholds.

Forcing Supplies On Prior to Sequencing

Prior to sequencing, any or all enable pins may be forced high by pulling the respective RT pin to V_{CC}. In this manner, supplies may be tested individually or together in any combination. With any RT pin at V_{CC}, the respective voltage monitor inputs and comparator outputs become active with thresholds parked at the configured sequence-up threshold. Outside of sequencing, $\overline{RST}$ (with 100% thresholds selected) and $\overline{OV}$ are always functional, regardless of RT pin state. If all four RT pins are at V_{CC}, the LTC2928 can be used as a stand-alone quad voltage monitor with under- and overvoltage indication as shown in Figure 11 (100% thresholds). With ON low in the RT forcing mode, sequence, command and reset faults do not occur. External faults however, may be detected (overvoltage, for example). Any previously logged faults remain in memory and their reporting will return upon exiting the forcing mode.

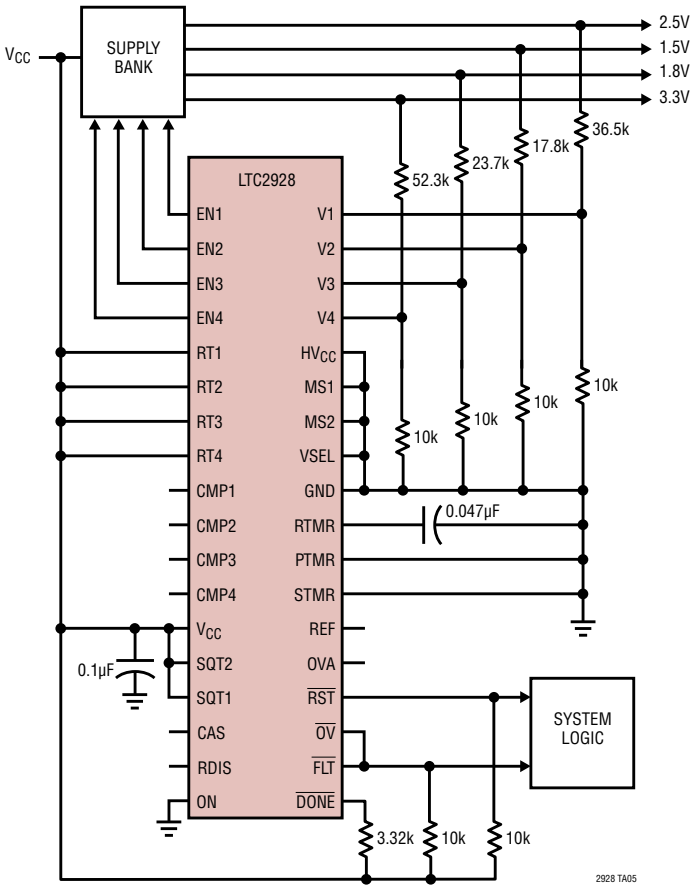


Figure 11. Quad Supervisor (No Sequencing)

APPLICATIONS INFORMATION

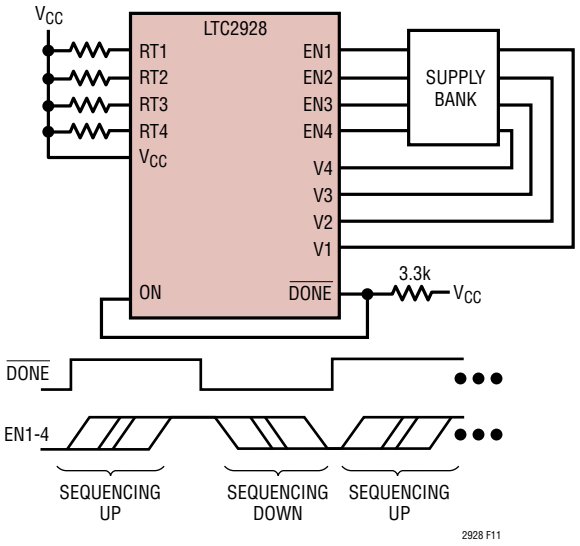


Figure 12. Cycle Supply Enables Repeatedly (Useful for System Burn-In)

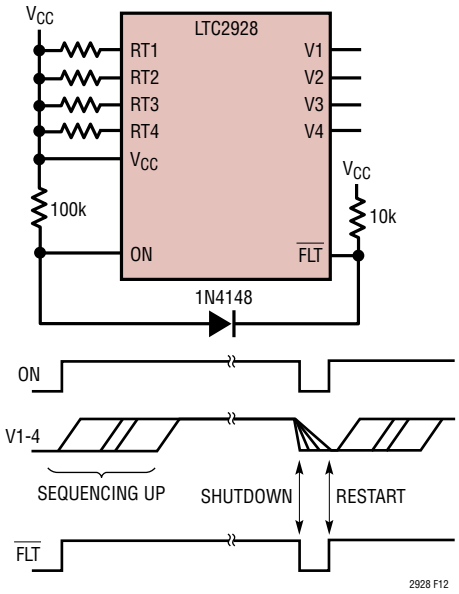


Figure 13. Automatic Restart After Fault

APPLICATIONS INFORMATION

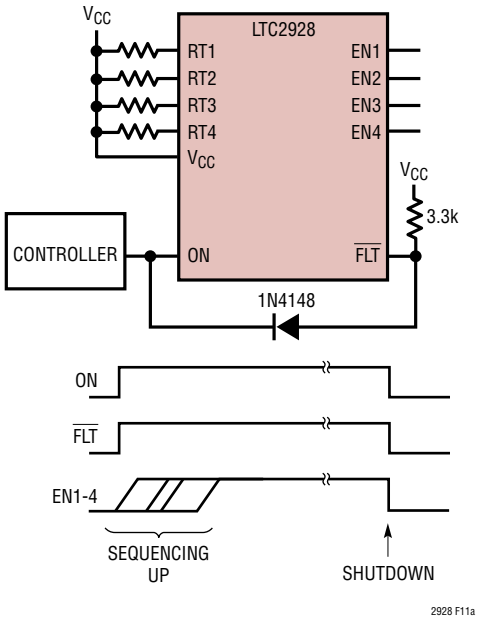


Figure 14. Turn-Off Enables Simultaneously (No Sequence-Down)

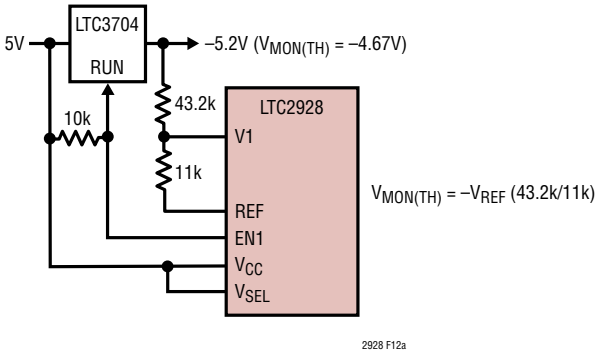


Figure 15. Negative Supply Monitoring

APPLICATIONS INFORMATION

LTC2928 Design Example

The following design example describes a power supply sequencing application using many features of the LTC2928. The example discusses a configuration procedure for the LTC2928 in a system containing a dual-supply DSP and FPGA. The design example schematic is shown in Figure 20. The three main operating phases—sequence-up, supply monitor, and sequence-down are discussed. All resistor, capacitor and configuration settings are reviewed. A timing diagram for sequencing-up is shown in Figure 18 and sequencing-down in Figure 19.

A main 3.3V supply provides application power, including V_{CC} for the LTC2928, and is sub-regulated to provide the lower voltages (2.5V, 1.8V, 1.5V). The LTC2928 controls external N-channel MOSFETs connected to two of the four supplies, used to pass power to the loads. The DSP core is powered from 1.8V and its I/O uses the 3.3V supply. The FPGA internals are powered from 1.5V and its I/O uses 2.5V.

1) Configure the LTC2928 based on application requirements

a. Apply device power.

Since the HV_{CC} input is unused, connect it to ground. Connect the main 3.3V supply to the V_{CC} pin. Bypass V_{CC} with 0.1µF to ground.

b. Monitored Supply Polarity

The application monitors four positive voltages. Connect the voltage selection input (VSEL) to ground (Table 2).

c. Device designations

The application requires only one LTC2928, and it is considered the MASTER device. By definition, it is also the FIRST and LAST device. Configure the MASTER/FIRST designation with the three-state MS1 and MS2 inputs connected to ground (Table 2). With MS1 and MS2 at ground, a reset fault is generated if $\overline{RST}$ pulls low during the supply monitor phase. Configure LAST device status with a 3.32k resistor from $\overline{DONE}$ to V_{CC}.

d. Sequence threshold selection

During the sequencing-up or sequencing-down phase, time positions terminate (CAS is released) when a supply (or supplies) reaches it sequence threshold. This design example requires sequence thresholds at 67% of their under-voltage threshold. Therefore, connect SQT1 to GND and SQT2 to V_{CC} (Table 4).

e. Choose minimum power supply enable spacing

The shortest time between successive power supply enables ($t_{CAS(HI)}$) is controlled by a capacitor connected to the STMR pin and ground (also referenced as the sequence timer period, t_{STMR}). The sequence timer period for this application is 29ms. Calculate the sequence timer capacitor from

$$C_{STMR(F)} = \frac{t_{STMR}(s)}{8.67M\Omega}$$

For this application,

$$C_{STMR} = \frac{29ms}{8.67M\Omega} = 3300pF$$

f. Supply order (time position)

The application requires the 1.8V DSP core supply to start first, about 100ms after the ON signal is received. The 1.8V supply is monitored on the V3 input and implies selection of the RT3 resistor, since monitor inputs correspond numerically with the RT and EN inputs. The 100ms required delay is approximately three sequence timer periods, so configure the first supply for time position 3 (select RT3 = 24.3k). Table 3 shows the recommended RT resistor values as a function of time position.

The 3.3V DSP I/O supply (monitored on V4) needs to turn on just after the core supply is alive, in order to minimize electrical stress and the possibility of bus contention. Turn on pass transistor N4 approximately 29ms after the core supply reaches its sequence threshold by selecting time position 4 (RT4 = 15k).

The FPGA needs to be powered about 100ms after the DSP, with its core and I/O supplies enabled simultaneously. The 2.5V I/O supply is monitored on V1, and the 1.5V core supply is monitored on V2. Since the required turn on delay is about three sequence timer periods after the DSP, select RT1 = RT2 = 3.4k (time position 7).

APPLICATIONS INFORMATION

g. Undervoltage thresholds

The positive supply monitor undervoltage threshold at all of the monitor inputs is 0.5V. Connect a resistive divider from the sensed voltage to ground. Connect the tap point to the respective high impedance monitor input. Specify the required undervoltage threshold (UV_{TH}) and calculate the divider ratio using

$$\frac{RnB}{RnA} = \frac{UV_{TH}(V)}{0.5V} - 1$$

This application requires –6.5% undervoltage thresholds for all supplies. For the 1.8V supply monitored on V3, the undervoltage threshold is 1.683V (1.8V x 0.935). The necessary divider ratio is

$$\frac{R3B}{R3A} = \frac{1.683}{0.5V} - 1 \approx 2.37$$

A good choice for R3B is 23.7k and R3A is 10k. All sequence thresholds are a percentage of the configured undervoltage threshold. The remaining ratios are:

$$\frac{R1B}{R1A} = \frac{2.338}{0.5V} - 1 \approx 3.68$$

$$\frac{R2B}{R2A} = \frac{1.403}{0.5V} - 1 \approx 1.81$$

$$\frac{R4B}{R4A} = \frac{3.086}{0.5V} - 1 \approx 5.17$$

h. Power-good timing

The "power-good" time defines the maximum time allowed for all monitored voltages to reach their undervoltage threshold when sequencing-up, or the sequence-down threshold (when sequencing-down) with respect to the time of the first enabled (disabled) supply. If the "power-good" timer expires, a sequence fault occurs. The "power-good" time (t_{PTMR}) is set with a capacitor from the PTMR pin to ground. Calculate the "power-good" capacitance from

$$C_{PTMR}(F) = \frac{t_{PTMR}(s)}{4.0M\Omega}$$

For this application, the "power-good" time is 400ms, yielding

$$C_{PTMR} = \frac{400ms}{4.0M\Omega} = 0.1\mu F$$

i. Reset delay time

The reset delay time is the additional time that $\overline{RST}$ is held low after all monitor inputs are above their undervoltage threshold. It is also the additional time that $\overline{OV}$ is held low (after an overvoltage event) after all monitor inputs are below their overvoltage threshold. When the reset timer expires, $\overline{RST}$ and/or $\overline{OV}$ is allowed to pull high. The reset delay time (t_{RTMR}) is set with a capacitor from the RTMR pin to ground. Calculate the reset capacitance from

$$C_{RTMR}(F) = \frac{t_{RTMR}(s)}{4.0M\Omega}$$

For this application, the reset delay time is 190ms, yielding

$$C_{RTMR}(F) = \frac{190ms}{4.0M\Omega} = 0.047\mu F$$

j. Overvoltage thresholds

Configure the OVA pin to set the global overvoltage thresholds. The application requires overvoltage thresholds at approximately 25% above the nominal supply voltage. For the 1.8V supply, the overvoltage threshold (OV_{TH}) equals 2.25V (1.8V x 1.25). Compute the required value for V_{OVA} from:

$$V_{OVA}(V) = \frac{RnA}{RnA + RnB} \bullet OV_{TH}(V)$$

For this application,

$$V_{OVA}(V) = \frac{10k}{10k + 23.7k} \bullet 2.25 = 0.667V$$

From the curves in Figures 16 and 17, the approximate value for V_{OVA} is achieved by leaving the OVA pin open. Since the other monitor inputs were configured for the same relative undervoltage level, the relative overvoltage levels for the other supplies are the same (+ 25%).

The application requires a fast shutdown upon overvoltage. To generate a fault upon an overvoltage condition, tie $\overline{OV}$ to $\overline{FLT}$. The fault condition shuts down all controlled supplies.

APPLICATIONS INFORMATION

2) Sequence-Up Phase

Start the sequence-up phase by transitioning the ON input above 1V. At this point, the LTC2928 senses the sequence position resistors on inputs RT1 through RT4. The sequence timer is operating and the CAS pin pulls low at the start of each time position. The CMP outputs are low during sequencing unless a fault has occurred.

Protect shutdown inputs on regulators that are sensitive to high voltage. In this application, the FPGA regulators have their shutdown inputs connected to the 3.3V supply through a 10k resistor, thereby limiting the pull-up voltage on the shutdown inputs (the EN outputs alone may attempt to pull-up as high as 9.3V (V_{CC} + 6V).

$\overline{DONE}$ pulls low when all time positions are clocked through (CAS has completed pulling low 8 times). The comparator outputs become active and are allowed to pull high if the supply monitor inputs are above their under-voltage threshold.

The $\overline{RST}$ output pulls high after all the supplies have remained above their undervoltage threshold for approximately 190ms. After $\overline{RST}$ is allowed to pull high, the LTC2928 enters its supply-monitor phase. The LTC2928 $\overline{RST}$ pin pulls up to 3.3V. The Schottky diode SD1 and resistor RP1 limit the pull-up voltage at the FPGA reset pin.

3) Supply Monitor Phase

During the supply-monitor phase, if any of the four supplies drops below its selected threshold, $\overline{RST}$ pulls low. Since this application considers an under-voltage condition during the supply-monitor phase to be a reset fault, $\overline{FLT}$ pulls low. All enable outputs pull low and the pass transistors shut off. Because of the fault condition, the LTC2928 is prevented from re-sequencing until all supplies drop below their sequence-down threshold, and the ON input is below 0.97V.

4) Sequence-Down Phase

Begin the sequence-down phase by pulling the ON input below 0.97V. $\overline{RST}$ and all CMP outputs pull low as soon as the sequence-down command is detected. Beginning with supplies in time position 8, the supplies are sequenced-down reverse of the order in which they came up. At the end of the sequence-down phase, $\overline{DONE}$ pulls high (CAS has completed pulling low 8 times).

Overvoltage Indication

If any positive supply monitor input exceeds its overvoltage threshold at any time, $\overline{OV}$ pulls low. $\overline{OV}$ returns high once all positive supplies are below their overvoltage threshold for a period equal to the $\overline{RST}$ delay time. To shutdown all supplies upon overvoltage, tie the $\overline{OV}$ output to $\overline{FLT}$.

Overvoltage Threshold Adjustment

Use the OVA input to set the overvoltage threshold for all positive supplies. Leave the OVA input open to set the OV threshold at the supply monitor inputs to 32% above the undervoltage threshold (V_{OVA} = 0.660V). Ground the OVA input to set the OV threshold to 12% above the undervoltage threshold (V_{OVA}) = 0.556V). Tie the OVA input to V_{CC} = 3.3V to set the OV threshold to 115% above the undervoltage threshold (V_{OVA} = 1.072V). Select accurate OV thresholds between 0.556V and 0.660V by connecting and external resistor between OVA and ground (Figure 16). Configure higher OV thresholds by connecting an external resistor between OVA and V_{CC} (Figure 17). These higher thresholds are potentially less accurate due to variations in V_{CC}.

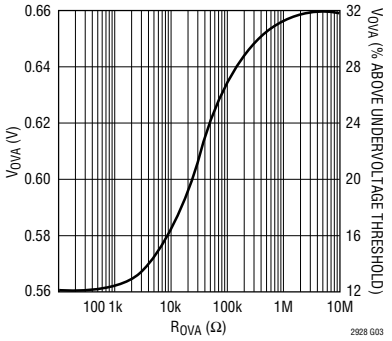


Figure 16. External Resistor from OVA to Ground

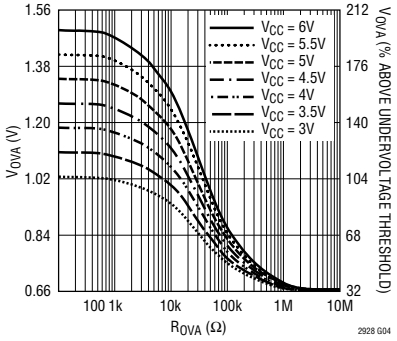


Figure 17. External Resistor from OVA to V_{CC}

APPLICATIONS INFORMATION

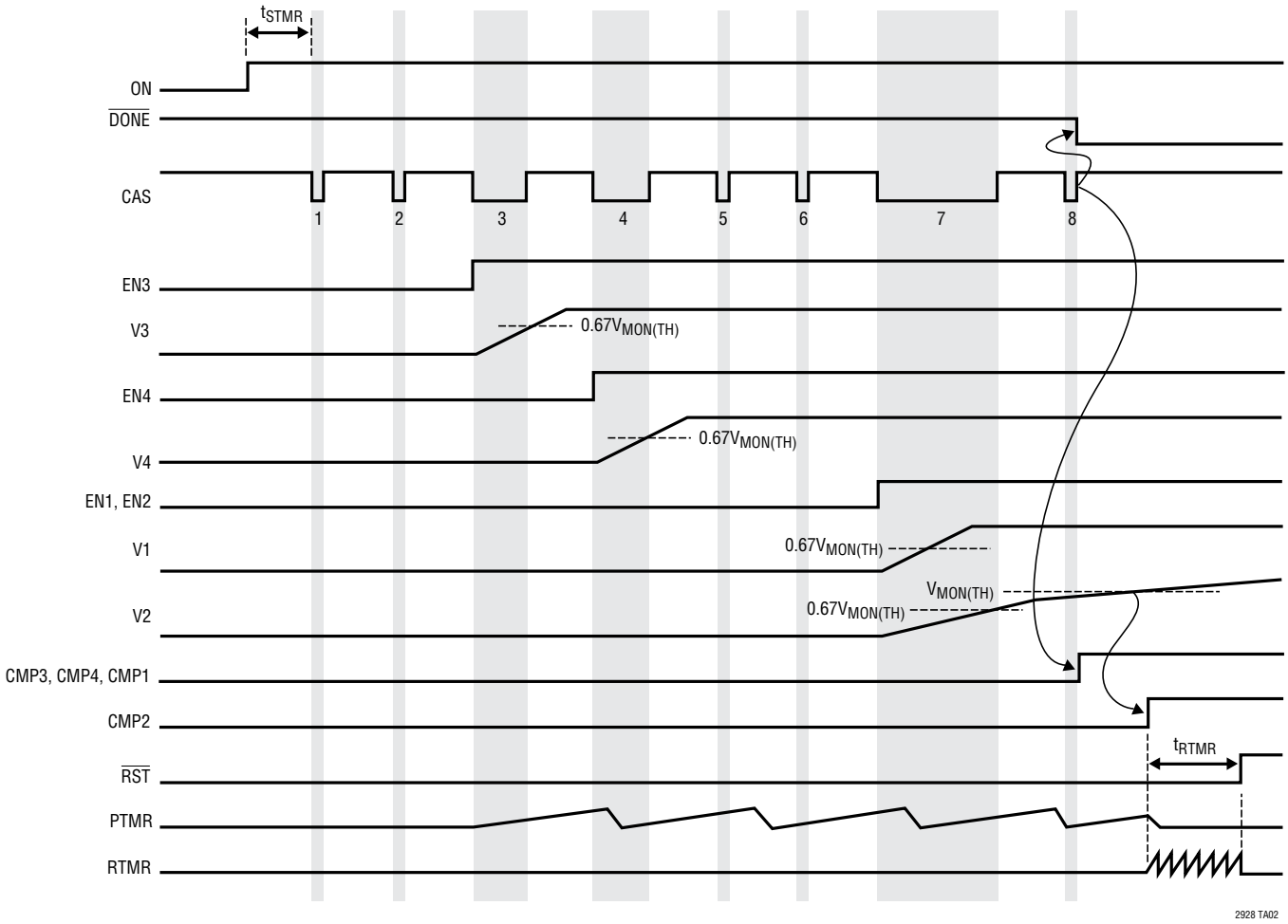


Figure 18. Design Example Timing Diagram, Sequencing-Up

APPLICATIONS INFORMATION

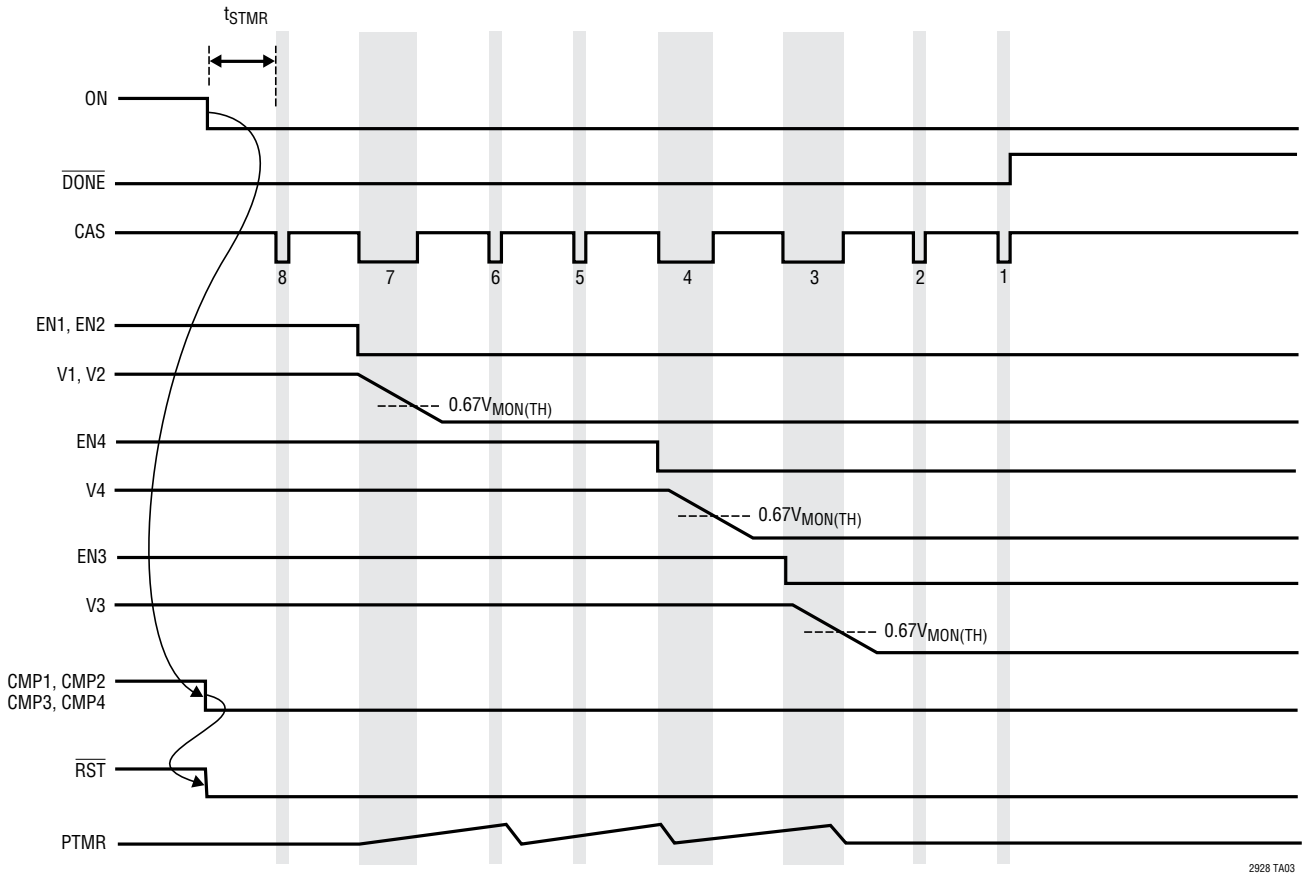


Figure 19. Design Example Timing Diagram, Sequencing-Down

APPLICATIONS INFORMATION

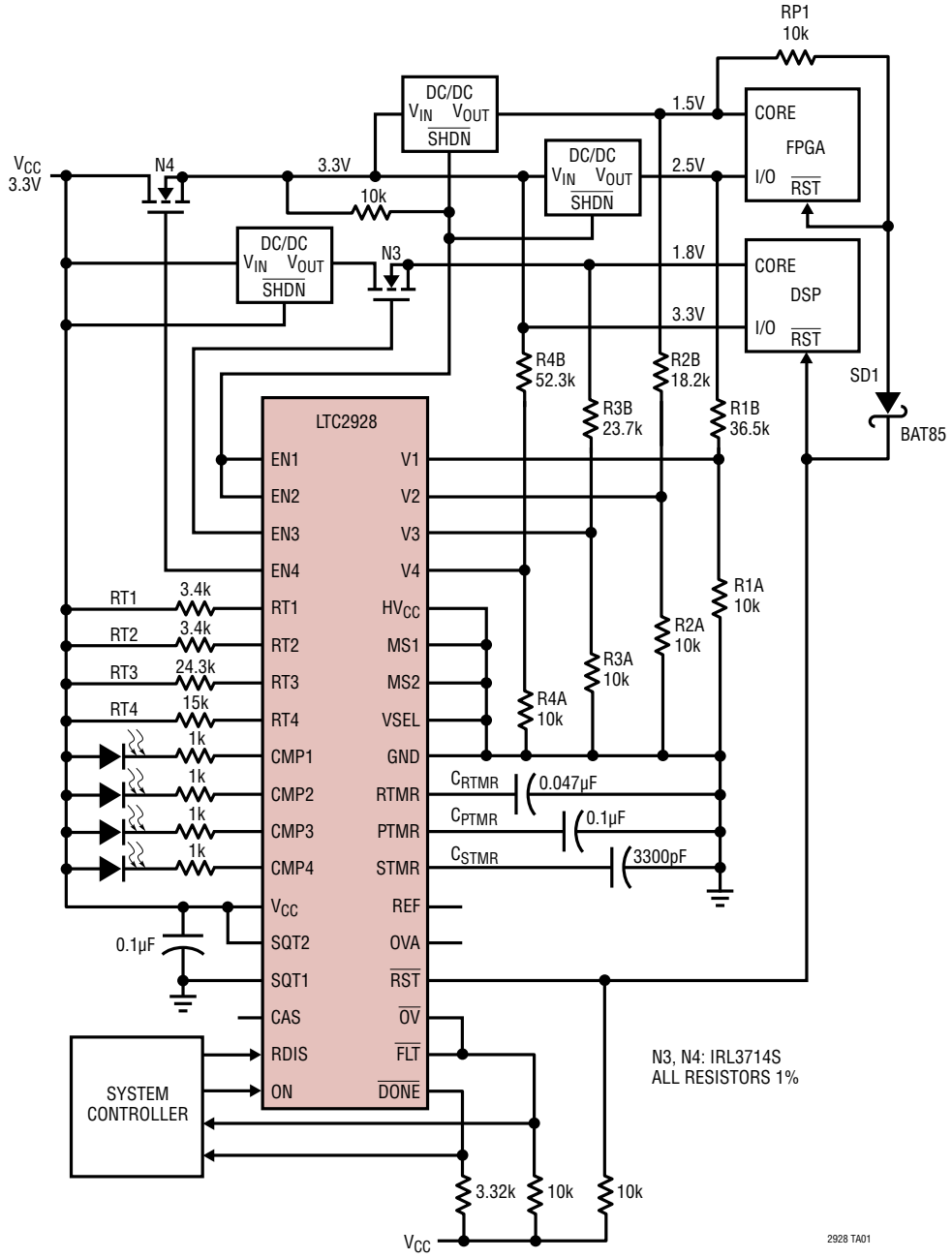
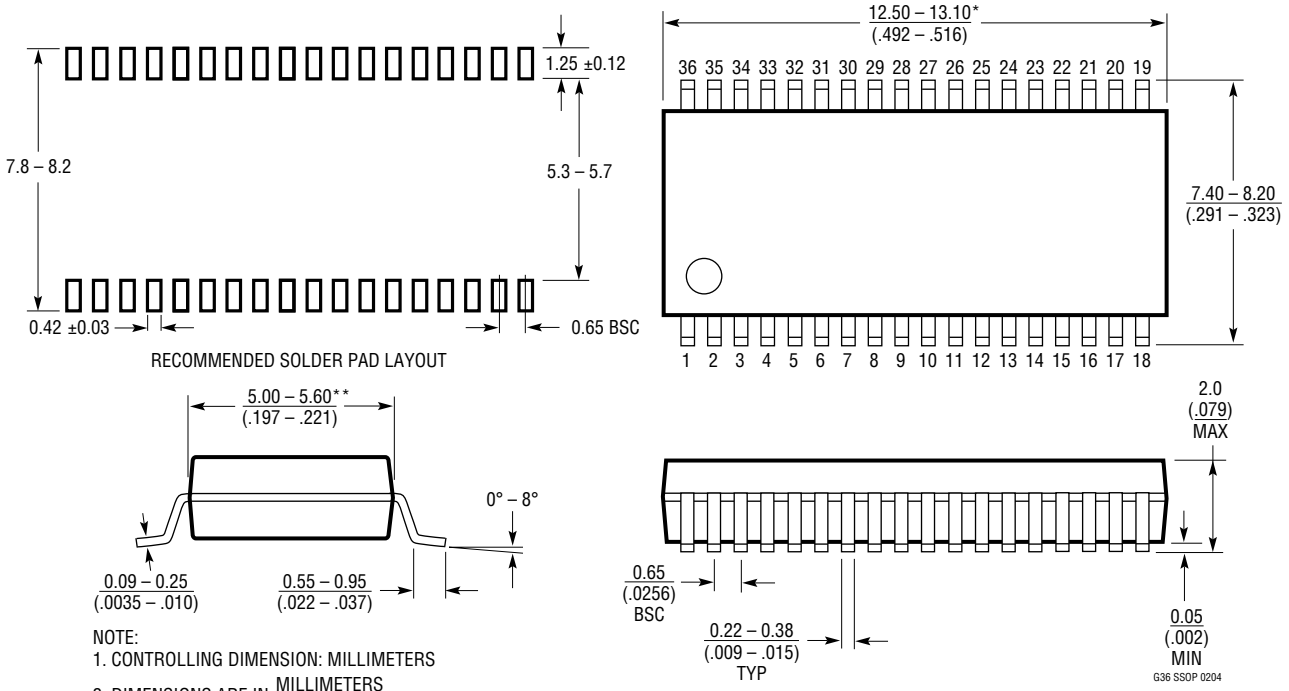


Figure 20. LTC2928 Design Example

PACKAGE DESCRIPTION

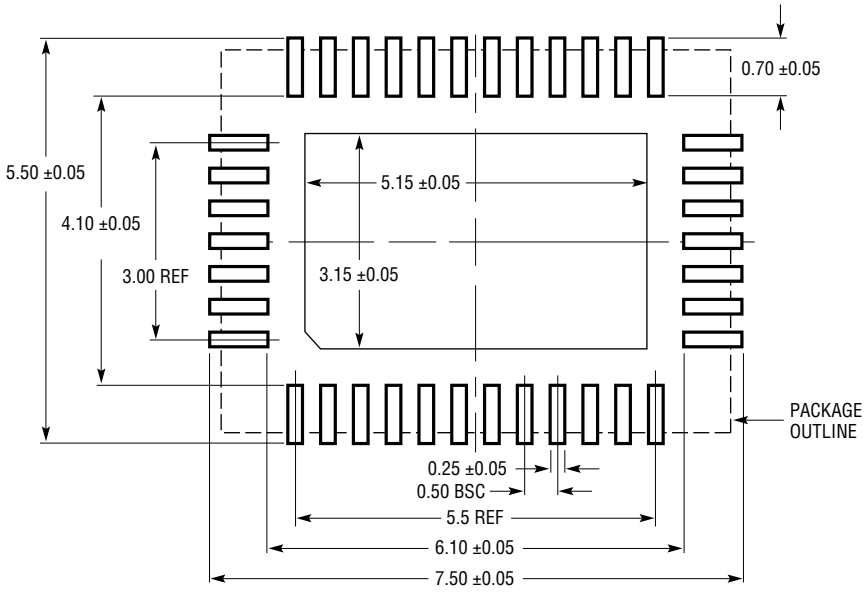
G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



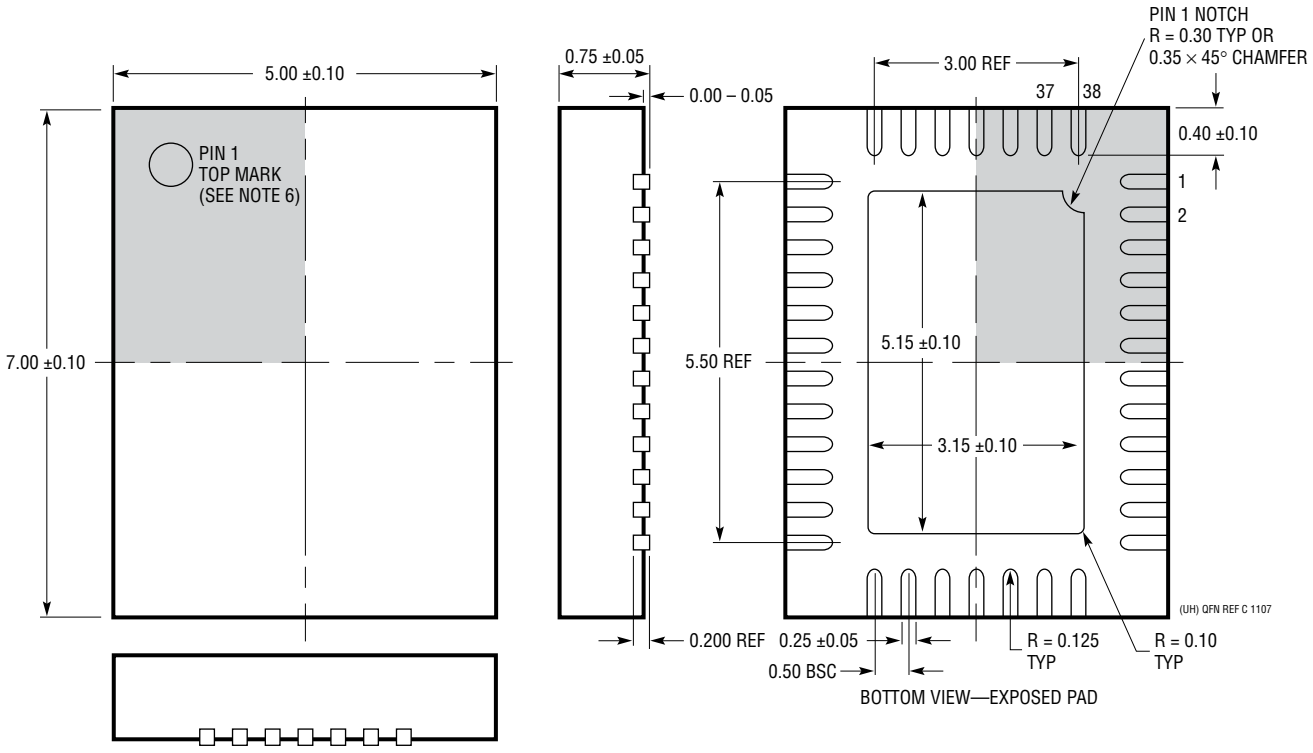
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/15	Expanded V1-V4 pin description	11
		Updated UHF package drawing	32
B	03/20	Updated UHF Part Marking	3

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2920-1 LTC2920-2	Single/Dual Power Supply Margining Controller	Symmetric/Asymmetric High and Low Voltage Margining
LTC2921/LTC2922	Power Supply Tracker with Input Monitor	Monitor up to Five Supplies, Includes Remote Sense Switches
LTC2923	Power Supply Tracking Controller	Up to 3 Supplies
LTC2924	Quad Power Supply Sequencer	Cascadable
LTC2925	Multiple Power Supply Tracking Controller with Power Good Timeout	Controls Three Supplies Without FETs, Includes Three Shutdown Control Pins
LTC2926	Power Supply Tracking Controller	Active Tracking Control with Series MOSFETs
LTC2927	Single Power Supply Tracking Controller	Controls Single Supply Without FETs, Daisy-Chain for Multiple Supplies
LTC2970	Digital Power Monitor and Margining Controller	Dual Supply Controller with 14-Bit ADC, 8-Bit DACs, Accurate Reference, Temperature Sensor and Automatic Servo Logic
LTC2974	4-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision
LTC2977	8-Channel PMBus Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Temperature Monitoring and Supervision
LTC2987	4-Channel µModule PMBuse Power System Manager	0.25% TUE 16-Bit ADC, Voltage/Current/Temperature Monitoring and Supervision