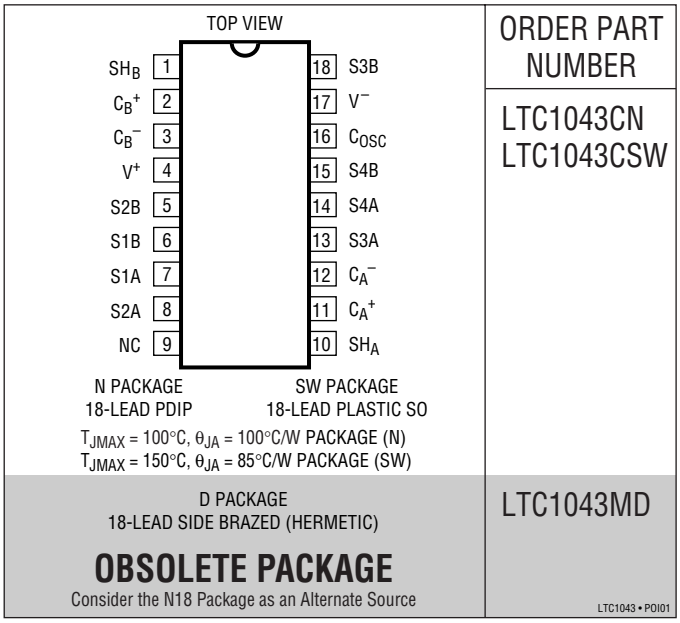
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 18V
Input Voltage at Any Pin ..... $-0.3V \le V_{IN} \le V^+ + 0.3V$
Operating Temperature Range
LTC1043C ..... $-40°C \le T_A \le 85°C$
LTC1043M **(OBSOLETE)**..... $-55°C \le T_A \le 125°C$
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1043CN LTC1043CSW
LTC1043MD

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V^+ = 10V$, $V^- = 0V$, LTC1043M operates from $-55°C \le T_A \le 125°C$; LTC1043C operates from $-40°C \le T_A \le 85°C$, unless otherwise noted.

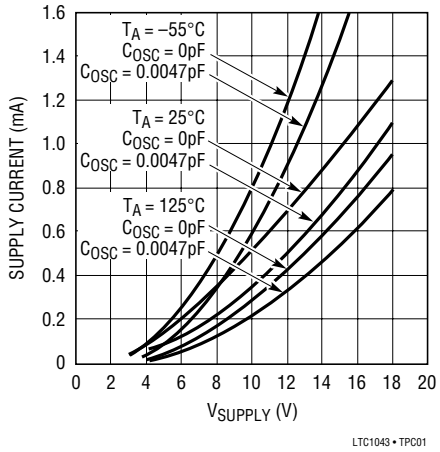
SYMBOL	PARAMETER	CONDITIONS		LTC1043M MIN	LTC1043M TYP	LTC1043M MAX	LTC1043C MIN	LTC1043C TYP	LTC1043C MAX	UNITS
I_S	Power Supply Current	Pin 16 Connected High or Low			0.25	0.4		0.25	0.4	mA
			●			0.7			0.7	mA
		C_{OSC} (Pin 16 to V^-) = 100pF			0.4	0.65		0.4	0.65	mA
			●			1			1	mA
I_I	OFF Leakage Current	Any Switch, Test Circuit 1 (Note 2)			6	100		6	100	pA
			●		6	500		6		nA
R_{ON}	ON Resistance	Test Circuit 2, V_{IN} = 7V, 1 = ±0.5mA V^+ = 10V, V^- = 0V			240	400		240	400	Ω
			●			700			700	Ω
R_{ON}	ON Resistance	Test Circuit 2, V_{IN} = 3.1V, 1 = ±0.5mA V^+ = 5V, V^- = 0V			400	700		400	700	Ω
			●			1			1	kΩ
f_{OSC}	Internal Oscillator Frequency	C_{OSC} (Pin 16 to V^-) = 0pF			185			185		kHz
		C_{OSC} (Pin 16 to V^-) = 100pF		20	34	50	20	34	50	kHz
		Test Circuit 3	●	15		75	15		75	kHz
I_{OSC}	Pin Source or Sink Current	Pin 16 at V^+ or V^-			40	70		40	70	µA
			●			100			100	µA
	Break-Before-Make Time				25			25		ns
	Clock to Switching Delay	C_{OSC} Pin Externally Driven			75			75		ns
f_M	Max External CLK Frequency	C_{OSC} Pin Externally Driven with CMOS Levels			5			5		MHz
CMRR	Common Mode Rejection Ratio	V^+ = 5V, V^- = –5V, $-5V < V_{CM} < 5V$ DC to 400Hz			120			120		dB

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

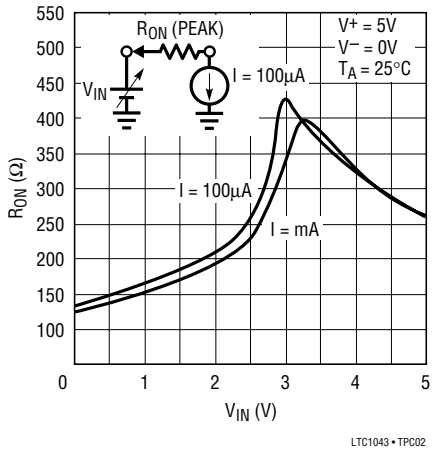
Note 2: OFF leakage current is guaranteed but not tested at 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

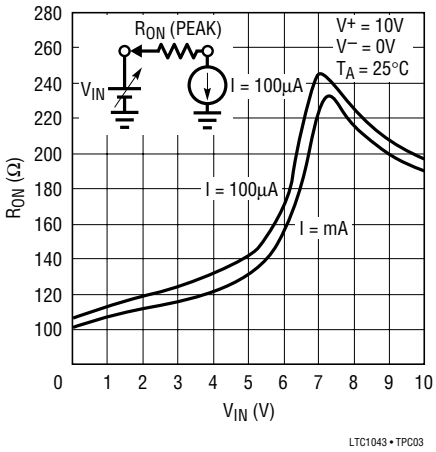
Power Supply Current vs Power Supply Voltage



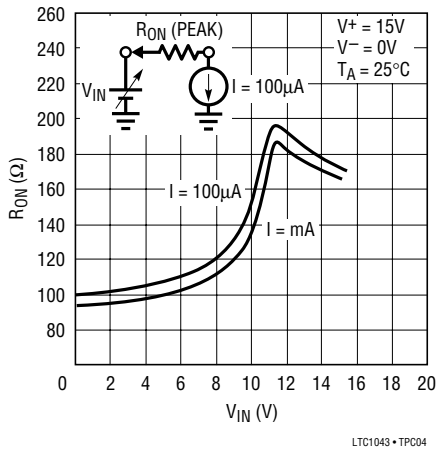
R_{ON} vs V_{IN}



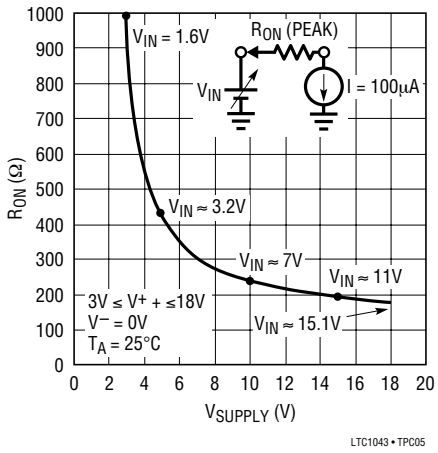
R_{ON} vs V_{IN}



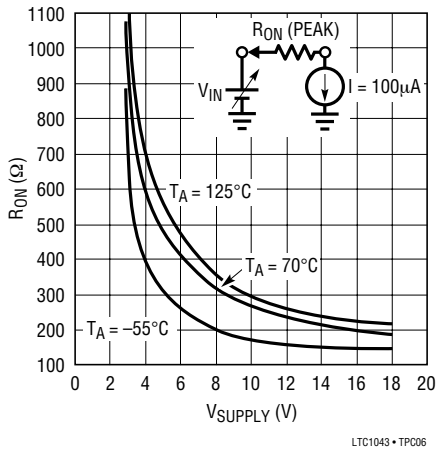
R_{ON} vs V_{IN}



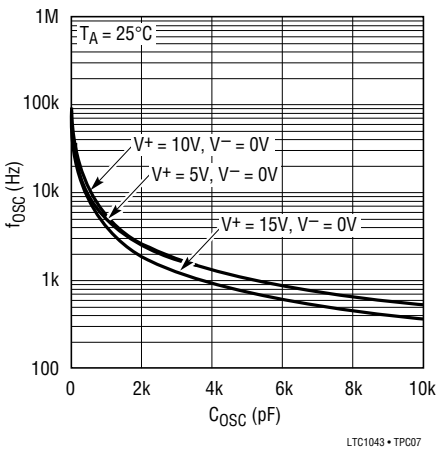
R_{ON} (Peak) vs Power Supply Voltage



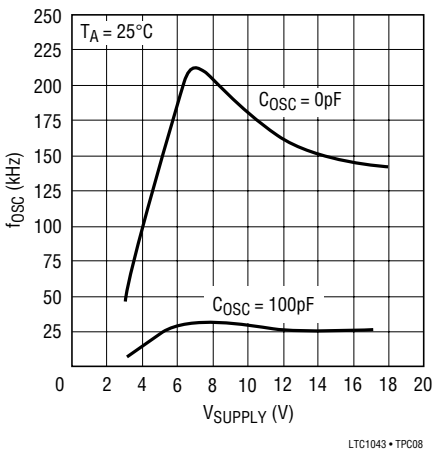
R_{ON} (Peak) vs Power Supply Voltage and Temperature



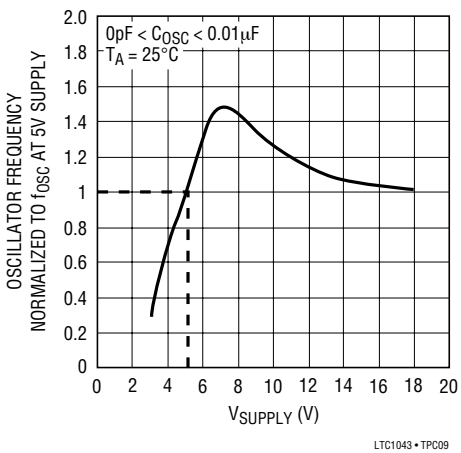
Oscillator Frequency, f_{OSC} vs C_{OSC}



Oscillator Frequency, f_{OSC} vs Supply Voltage

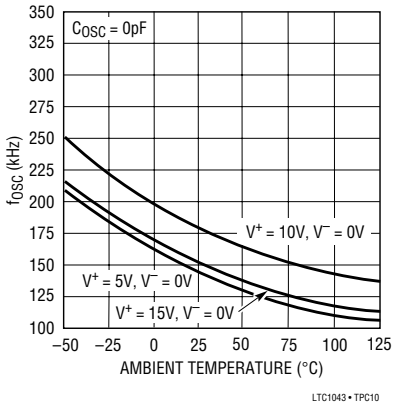


Normalized Oscillator Frequency, f_{OSC} vs Supply Voltage



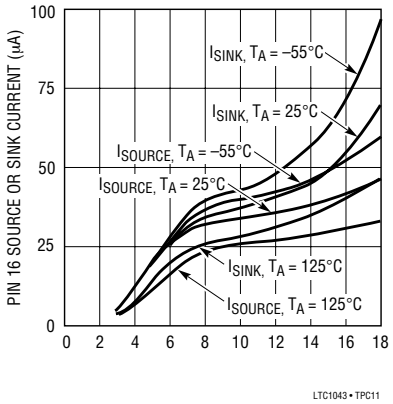
TYPICAL PERFORMANCE CHARACTERISTICS (Test Circuits 2 through 4)

Oscillator Frequency, f_{OSC} vs Ambient Temperature, T_A



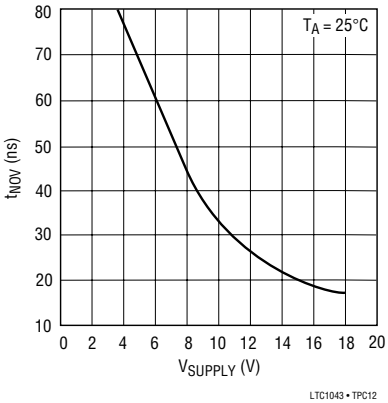
LTC1043 • TPC10

C_{OSC} Pin I_{SINK}, I_{SOURCE} vs Supply Voltage



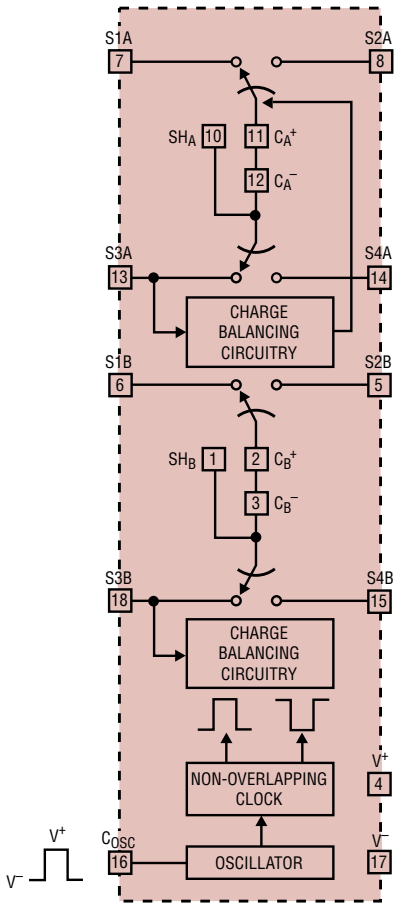
LTC1043 • TPC11

Break-Before-Make Time, t_{NOV}, vs Supply Voltage



LTC1043 • TPC12

BLOCK DIAGRAM



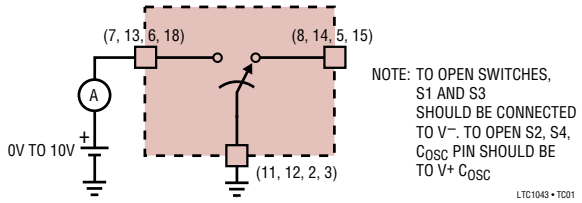
THE SWITCHES ARE TIMED AS SHOWN WITH PIN 16 HIGH

THE CHARGE BALANCING CIRCUITRY SAMPLES THE VOLTAGE AT S3 WITH RESPECT TO S4 (PIN 16 HIGH) AND INJECTS A SMALL CHARGE AT THE C^+ PIN (PIN 16 LOW). THIS BOOSTS THE CMRR WHEN THE LTC1043 IS USED AS AN INSTRUMENTATION AMPLIFIER FRONT END. FOR MINIMUM CHARGE INJECTION IN OTHER TYPES OF APPLICATIONS, S3A AND S3B SHOULD BE GROUNDED

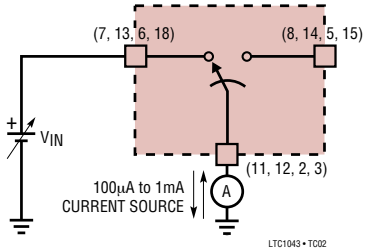
LTC1043 • BD01

TEST CIRCUITS

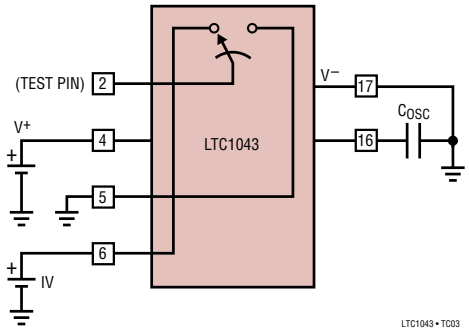
Test Circuit 1. Leakage Current Test



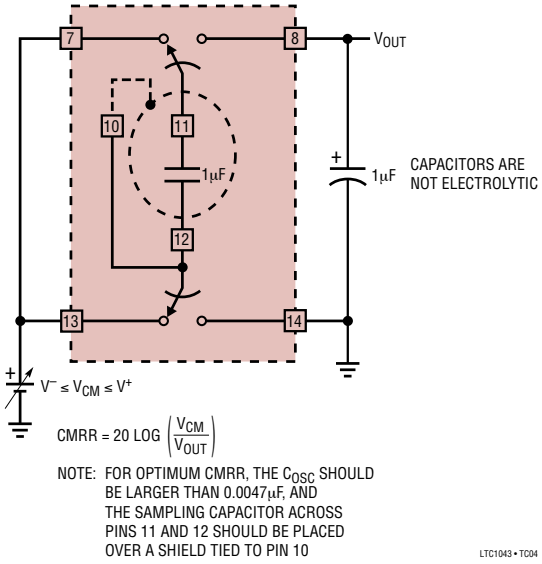
Test Circuit 2. R_{ON} Test



Test Circuit 3. Oscillator Frequency, f_{OSC}



Test Circuit 4. CMRR Test



APPLICATIONS INFORMATION

Common Mode Rejection Ratio (CMRR)

The LTC1043, when used as a differential to single-ended converter rejects common mode signals and preserves differential voltages (Figure 1). Unlike other techniques, the LTC1043's CMRR does not degrade with increasing common mode voltage frequency. During the sampling mode, the impedance of Pins 2, 3 (and 11, 12) should be reasonably balanced, otherwise, common mode signals will appear differentially. The value of the CMRR depends on the value of the sampling and holding capacitors (C_S, C_H) and on the sampling frequency. Since the common mode voltages are not sampled, the common mode signal frequency can well exceed the sampling frequency without experiencing aliasing phenomena. The CMRR of Figure 1 is measured by

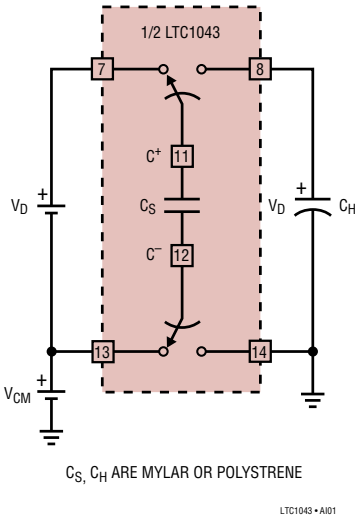


Figure 1. Differential to Single-Ended Converter

APPLICATIONS INFORMATION

shorting Pins 7 and 13 and by observing, with a precision DVM, the change of the voltage across C_H with respect to an input CM voltage variation. During the sampling and holding mode, charges are being transferred and minute voltage transients will appear across the holding capacitor. Although the R_{ON} on the switches is low enough to allow fast settling, as the sampling frequency increases, the rate of charge transfer increases and the average voltage measured with a DVM across it will increase proportionally; this causes the CMRR of the sampled data system, as seen by a "continuous" instrument (DVM), to decrease (Figure 2).

Switch Charge Injection

Figure 3 shows one out of the eight switches of the LTC1043, configured as a basic sample-and-hold circuit. When the switch opens, a "hold step" is observed and its magnitude depends on the value of the input voltage. Figure 4 shows charge injected into the hold capacitor. For instance, a 2pCb of charge injected into a 0.01μF capacitor causes a 200μV hold step. As shown in Figure 4, there is a predictable and repeatable charge injection cancellation when the input voltage is close to half the supply voltage of the LTC1043. This is a unique feature of this product, containing charge-balanced switches fabricated with a self-aligning gate CMOS process. Any switch of the LTC1043, when powered with symmetrical dual supplies, will sample-and-hold small signals around ground without any significant error.

Shielding the Sampling Capacitor for Very High CMRR

Internal or external parasitic capacitors from the C^+ pin(s) to ground affect the CMRR of the LTC1043 (Figure 1). The common mode error due to the internal junction capacitances of the C^+ Pin(s) 2 and 11 is cancelled through internal circuitry. The C^+ pin, therefore, should be used as the top plate of the sampling capacitor. The interpin capacitance between pin 2 and dummy Pin 1 (11 and 10) appears in parallel with the sampling capacitor so it does not degrade the CMRR. A shield placed underneath the sampling capacitor and connected to either Pin 1 or 3 helps to boost the CMRR in excess of 120dB (Figure 5).

Excessive external parasitic capacitance between the C^- pins and ground indirectly degrades CMRR; this becomes visible especially when the LTC1043 is used with clock frequencies above 2kHz. Because of this, if a shield is used, the parasitic capacitance between the shield and circuit ground should be minimized.

It is recommended that the outer plate of the sampling capacitor be connected to the C^- pin(s).

Input Pins, SCR Sensitivity

An internal 60Ω resistor is connected in series with the input of the switches (Pins 5, 6, 7, 8, 13, 14, 15, 18) and it is included in the R_{ON} specification. When the input voltage exceeds the power supply by a diode drop, current will flow into the input pin(s). The LTC1043 will not latch until the input current reaches 2mA–3mA. The device will

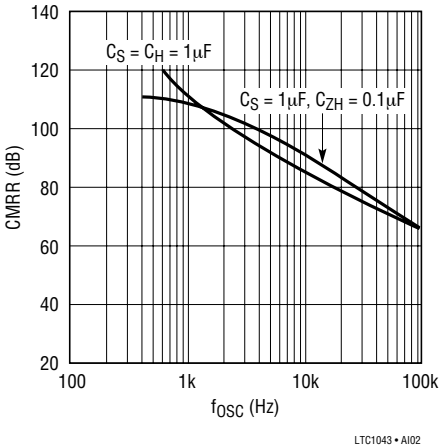


Figure 2. CMRR vs Sampling Frequency

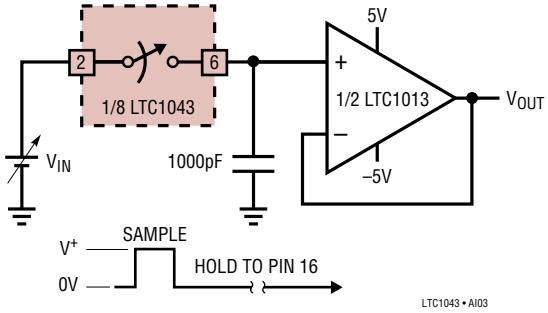


Figure 3

APPLICATIONS INFORMATION

recover from the latch mode when the input drops 3V to 4V below the voltage value which caused the latch. For instance, if an external resistor of 200Ω is connected in series with an input pin, the input can be taken 1.3V above the supply without latching the IC. The same applies for the C^+ and C^- pins.

C_{OSC} Pin (16), Figure 6

The Cosc pin can be used with an external capacitor, Cosc, connected from Pin 16 to Pin 17, to modify the internal oscillator frequency. If Pin 16 is floating, the internal 24pF capacitor, plus any external interpin capacitance, set the oscillator frequency around 190kHz with ±5V supply. The typical performance characteristics curves provide the necessary information to set the oscillator frequency for various power supply ranges. Pin 16 can also be driven with an external clock to override the internal oscillator. Although standard 7400 series CMOS gates do not guarantee CMOS levels with the current source and sink requirements of Pin 16, they will in reality drive the Cosc pin. CMOS gates conforming to standard B series output drive have the appropriate voltage levels and more than enough output current to simultaneously drive several LTC1043 C_{OSC} pins. The typical trip levels of the Schmitt trigger (Figure 6) are given below.

SUPPLY	TRIP LEVELS
$V^+ = 5V, V^- = 0V$	$V_H = 3.4V V_L = 1.35V$
$V^+ = 10V, V^- = 0V$	$V_H = 6.5V V_L = 2.8V$
$V^+ = 15V, V^- = 0V$	$V_H = 9.5V V_L = 4.1V$

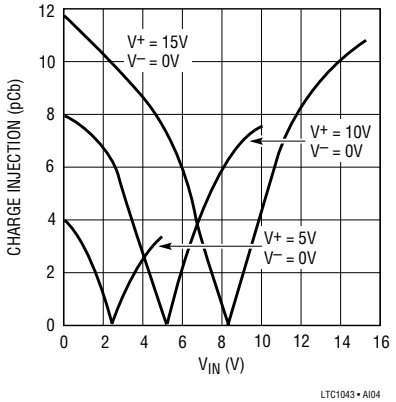


Figure 4. Individual Switch Charge Injection vs Input Voltage

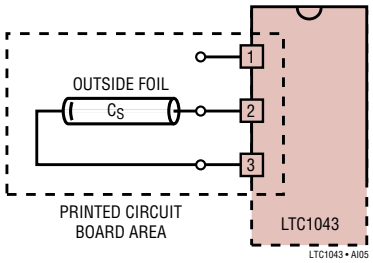


Figure 5. Printed Circuit Board Layout Showing Shielding the Sampling Capacitor

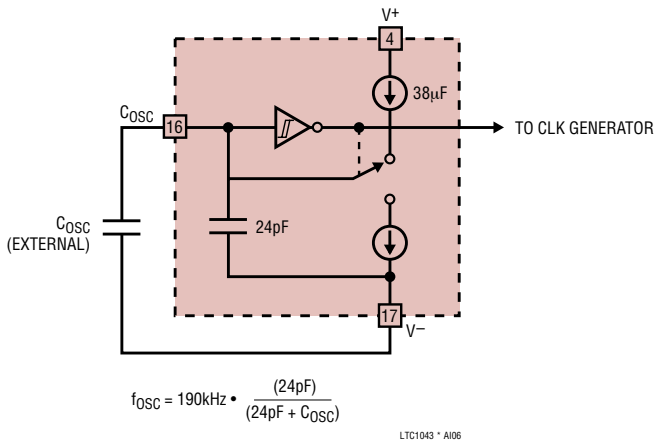
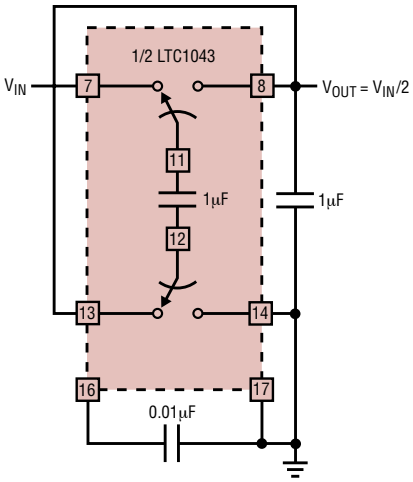


Figure 6. Internal Oscillator

TYPICAL APPLICATIONS

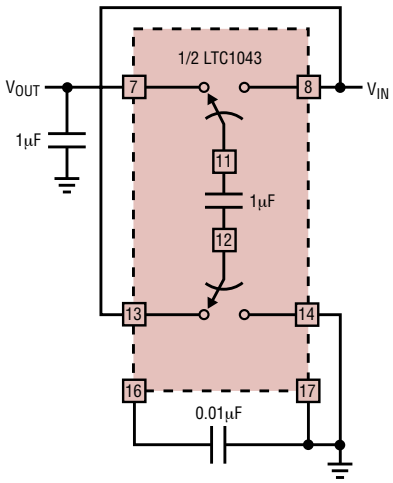
Divide by 2



$V_{OUT} = V_{IN}/2 \pm 1ppm$
$0 \le V_{IN} \le V^+$
$3 \le V^+ \le 18V$

LTC1043 • A01

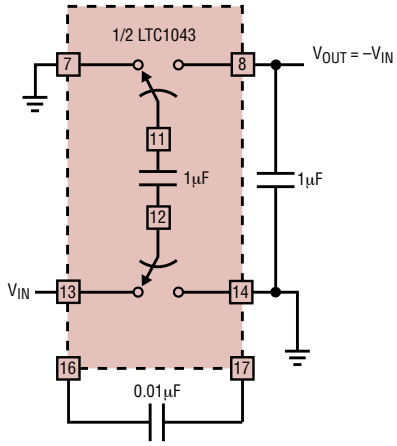
Multiply by 2



$V_{OUT} = 2V_{IN} \pm 5ppm$
$0 \le V_{IN} \le V^+/2$
$3 \le V^+ \le 18V$

LTC1043 • A02

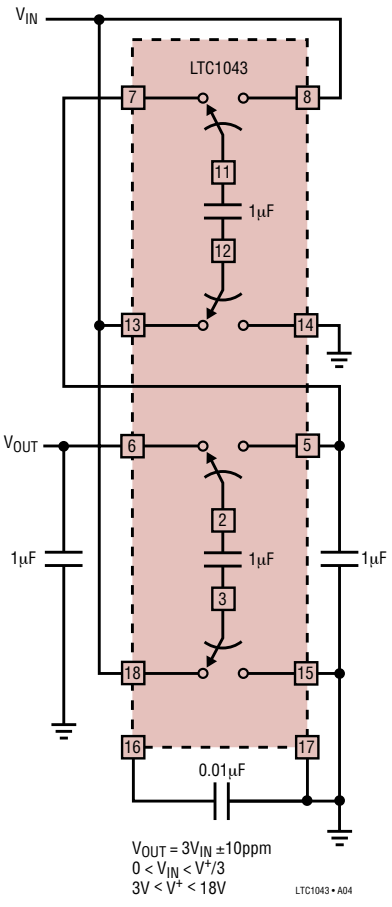
Ultra Precision Voltage Inverter



$V_{OUT} = -V_{IN} \pm 2ppm$
$V^- < V_{IN} < V^+$
$V^+ = +5V, V^- = -5V$

LTC1043 * A03

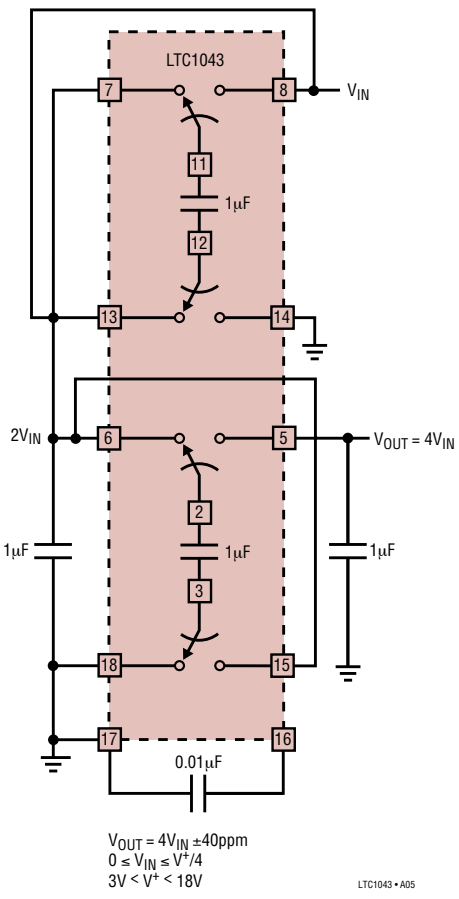
Precision Multiply by 3



$V_{OUT} = 3V_{IN} \pm 10ppm$
$0 < V_{IN} < V^+/3$
$3V < V^+ < 18V$

LTC1043 • A04

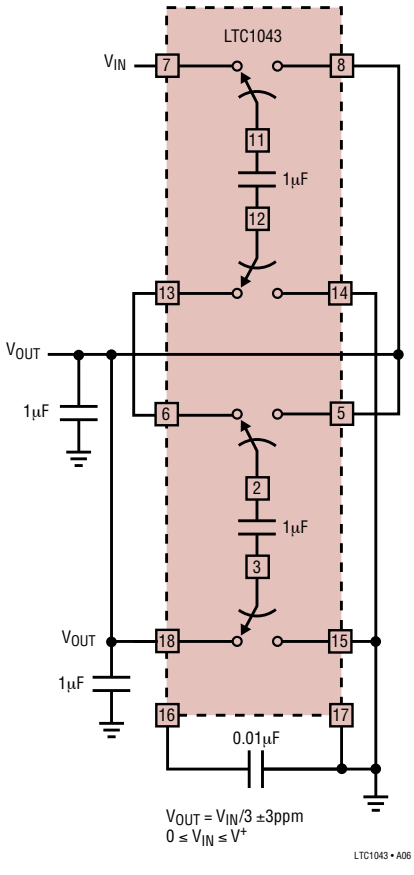
Precision Multiply by 4



$V_{OUT} = 4V_{IN} \pm 40ppm$
$0 \le V_{IN} \le V^+/4$
$3V < V^+ < 18V$

LTC1043 • A05

Divide by 3

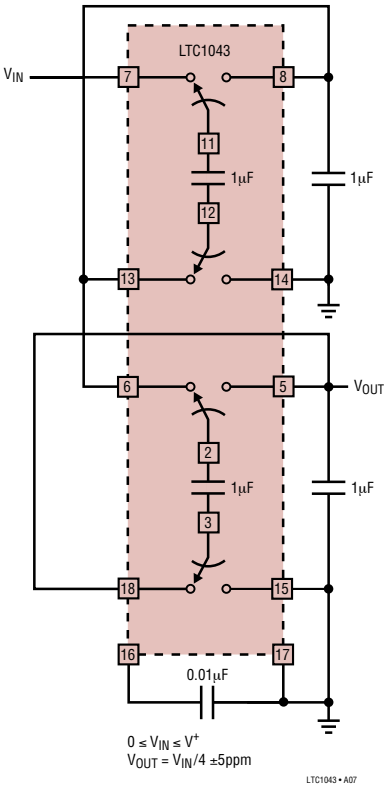


$V_{OUT} = V_{IN}/3 \pm 3ppm$
$0 \le V_{IN} \le V^+$

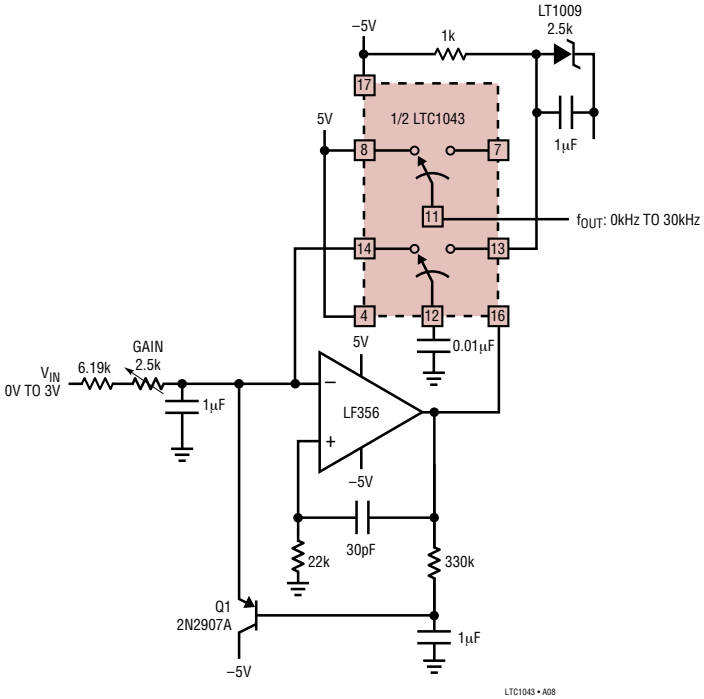
LTC1043 • A06

TYPICAL APPLICATIONS

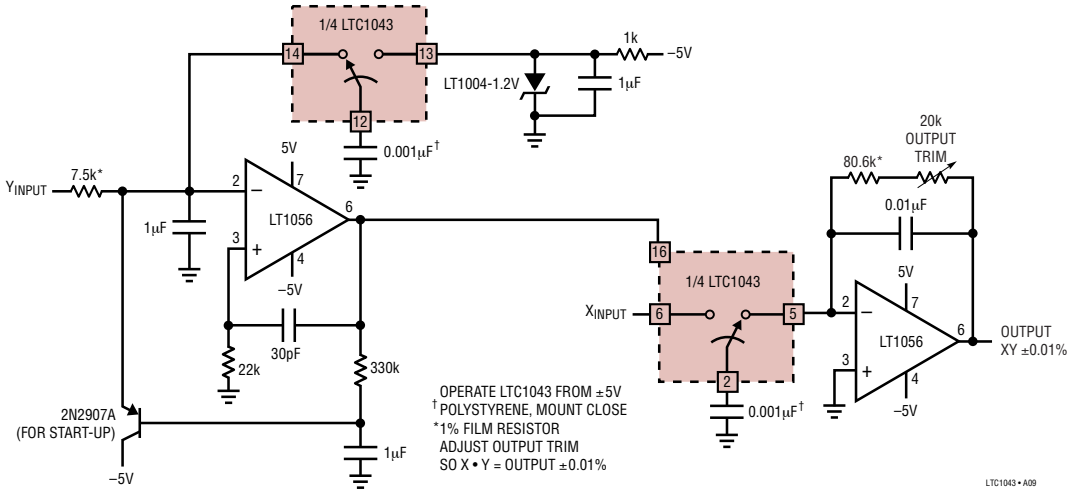
Divide by 4



0.005% V/F Converter

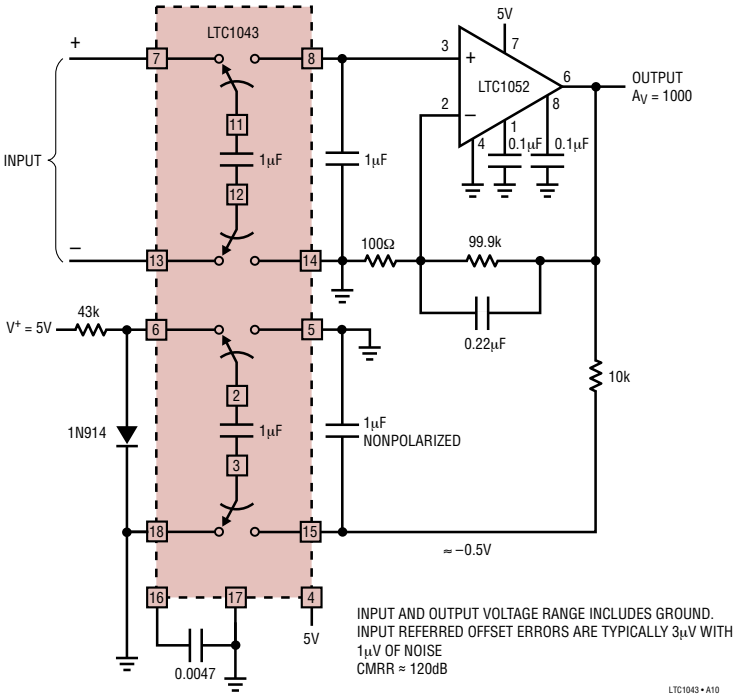


0.01% Analog Multiplier

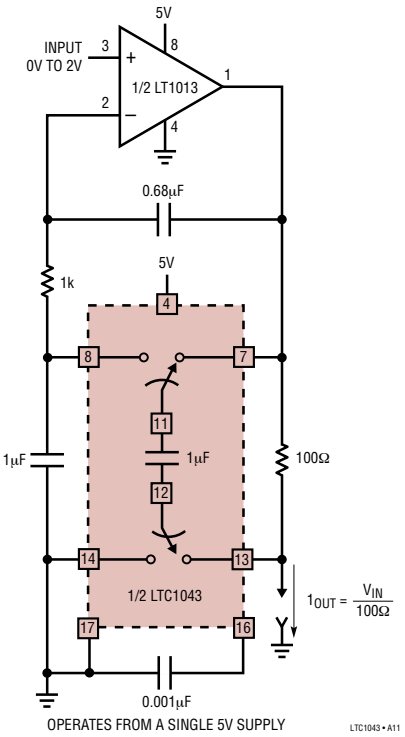


TYPICAL APPLICATIONS

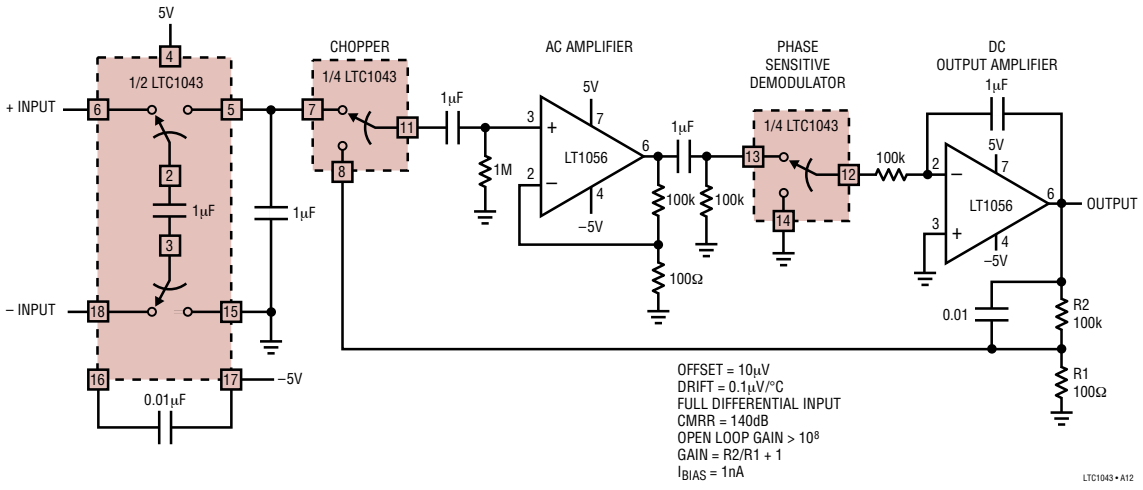
Single 5V Supply, Ultra Precision Instrumentation Amplifier



Voltage Controlled Current Source with Ground Referred Input and Output

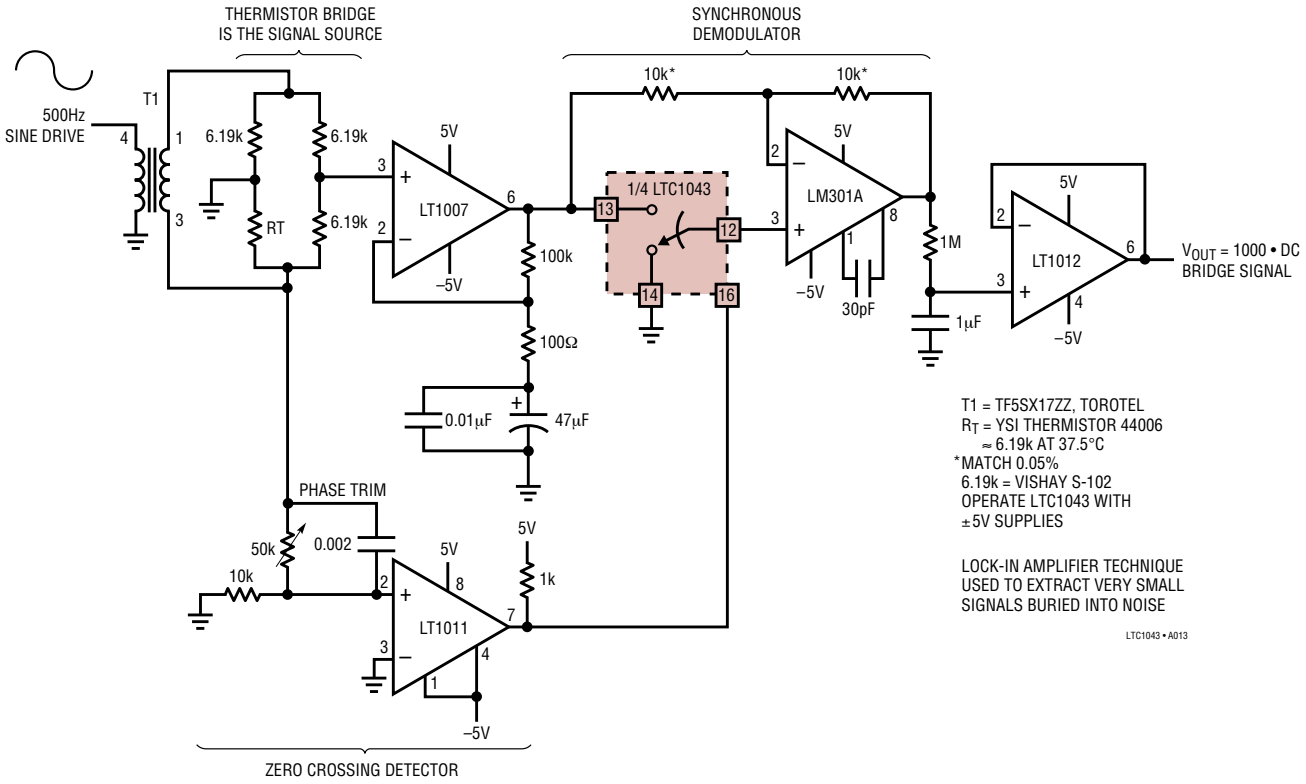


Precision Instrumentation Amplifier



TYPICAL APPLICATIONS

Lock-In Amplifier (= Extremely Narrow-Band Amplifier)

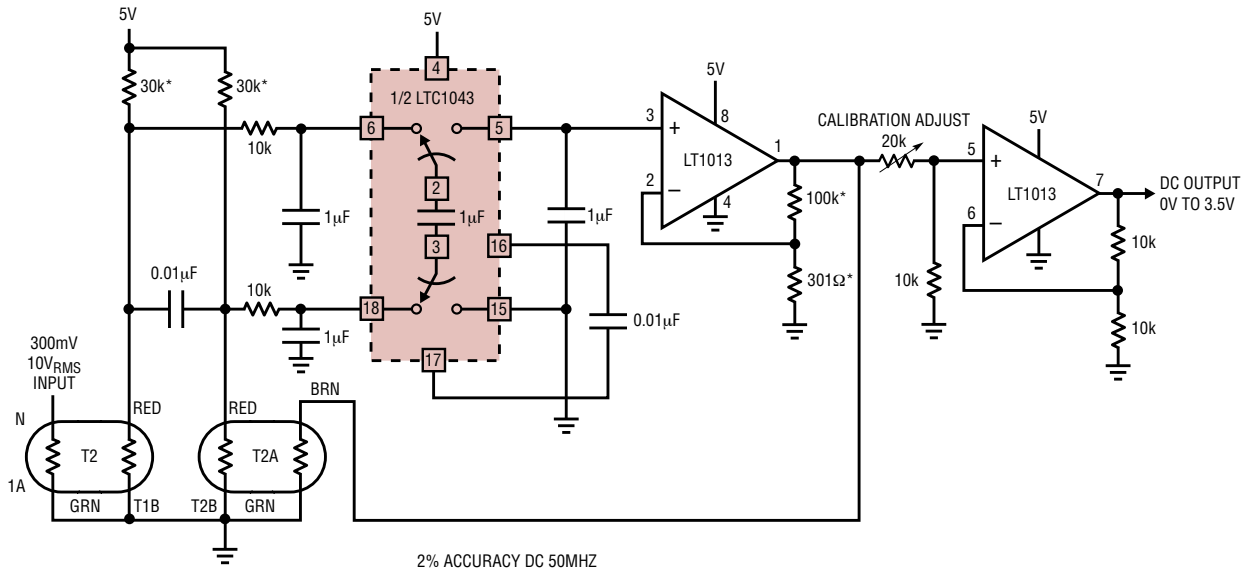


T1 = TF5SX17ZZ, TOROTEL
R_T = YSI THERMISTOR 44006
≈ 6.19k AT 37.5°C
*MATCH 0.05%
6.19k = VISHAY S-102
OPERATE LTC1043 WITH
±5V SUPPLIES

LOCK-IN AMPLIFIER TECHNIQUE
USED TO EXTRACT VERY SMALL
SIGNALS BURIED INTO NOISE

LTC1043 • A013

50MHz Termal RMS/DC Converter



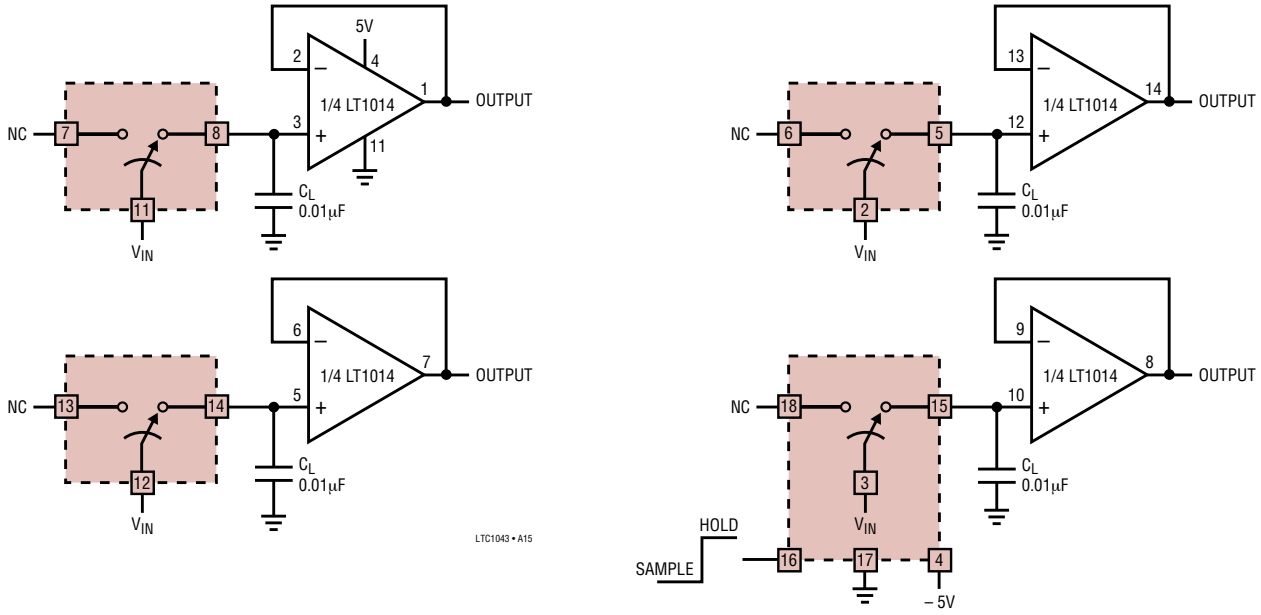
*1% RESISTOR

2% ACCURACY DC 50MHZ
100:1 CREST FACTOR CAPABILITY
T1 TO T2 = YELLOW SPRINGS INST. CO.
THERMISTOR COMPOSITE
ENCLOSE T1 AND T2 IN STYROFOAM

LTC1043 • A14

TYPICAL APPLICATIONS

Quad Single 5V Supply, Low Hold Step, Sample-and-Hold



FOR 1V ≤ V_{IN} ≤ 4V, THE HOLD STEP IS ≤ 300µV
ACQUISITION TIME ~ 8 • R_{ON} C_H FOR 10-BIT ACCURACY

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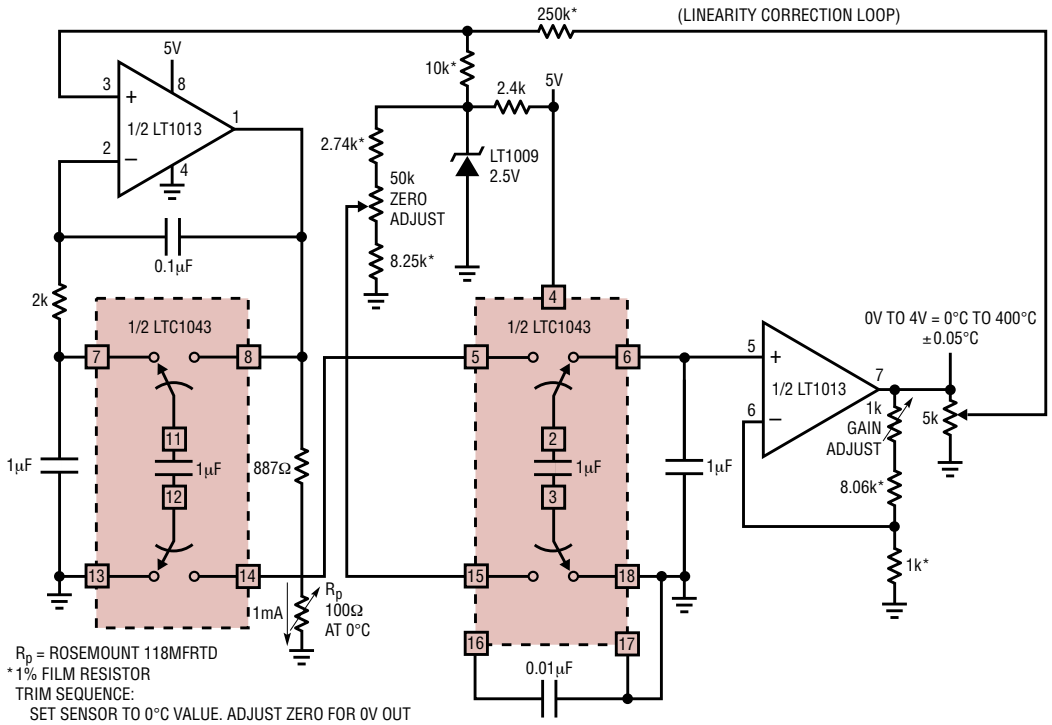
Single Supply Precision Linearized Platinum RTD Signal Conditioner

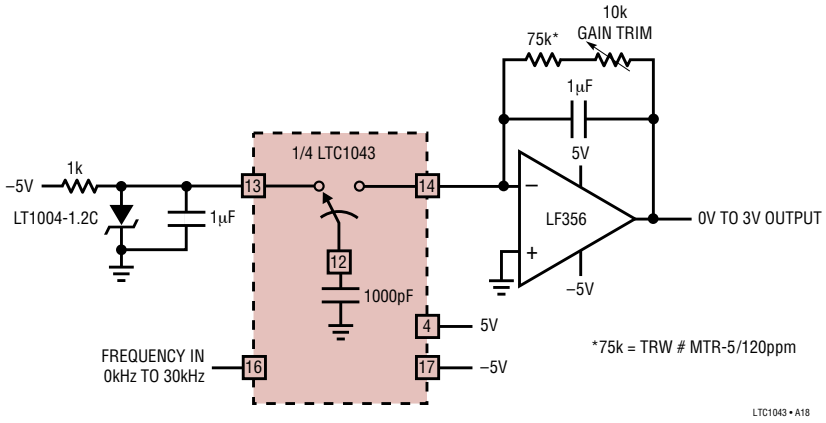


R_p = ROSEMOUNT 118MFRTD
*1% FILM RESISTOR
TRIM SEQUENCE:
SET SENSOR TO 0°C VALUE. ADJUST ZERO FOR 0V OUT
SET SENSOR TO 100°C VALUE. ADJUST GAIN FOR 1,000V OUT
SET SENSOR TO 400°C VALUE. ADJUST LINEARITY FOR 4,000V OUT
REPEAT AS REQUIRED

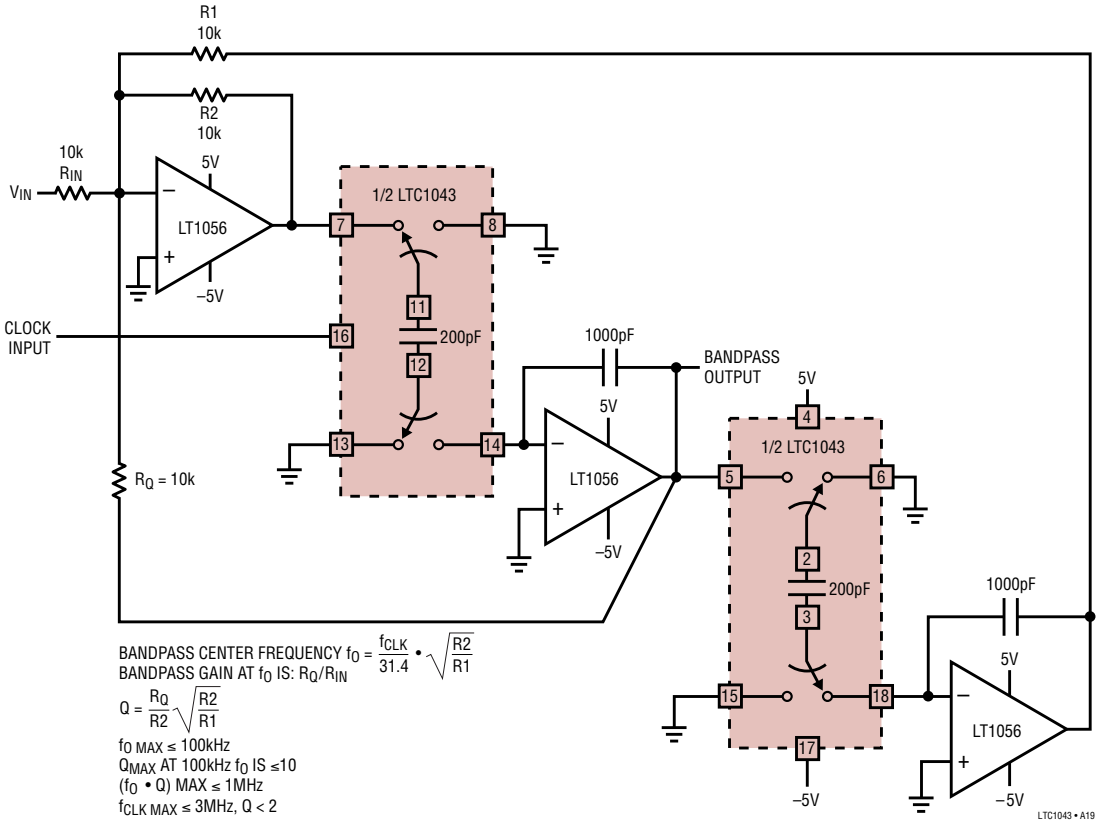
LTC1043 • A17

TYPICAL APPLICATIONS

0.005% F/V Converter

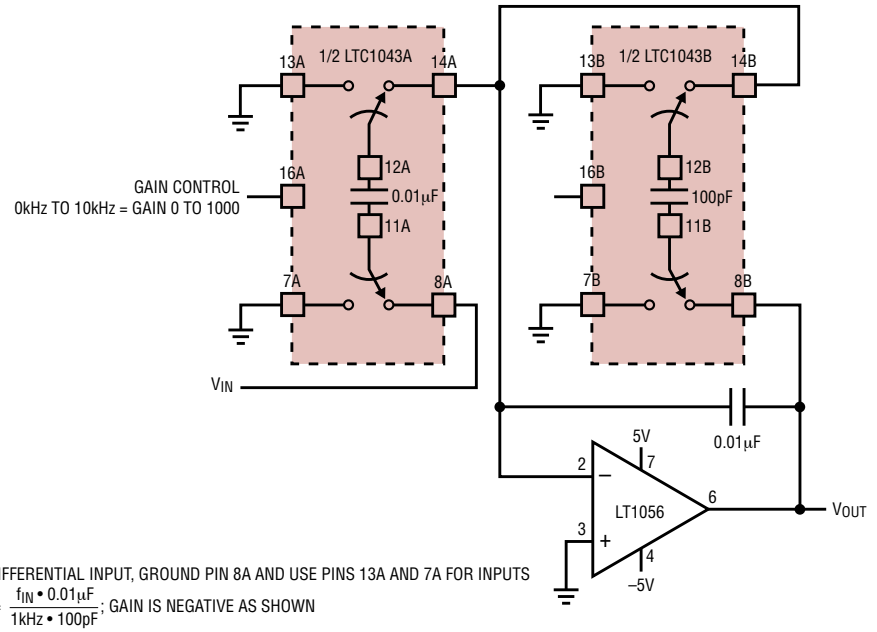


High Frequency Clock Tunable Bandpass Filter



TYPICAL APPLICATIONS

Frequency-Controlled Gain Amplifier



FOR DIFFERENTIAL INPUT, GROUND PIN 8A AND USE PINS 13A AND 7A FOR INPUTS

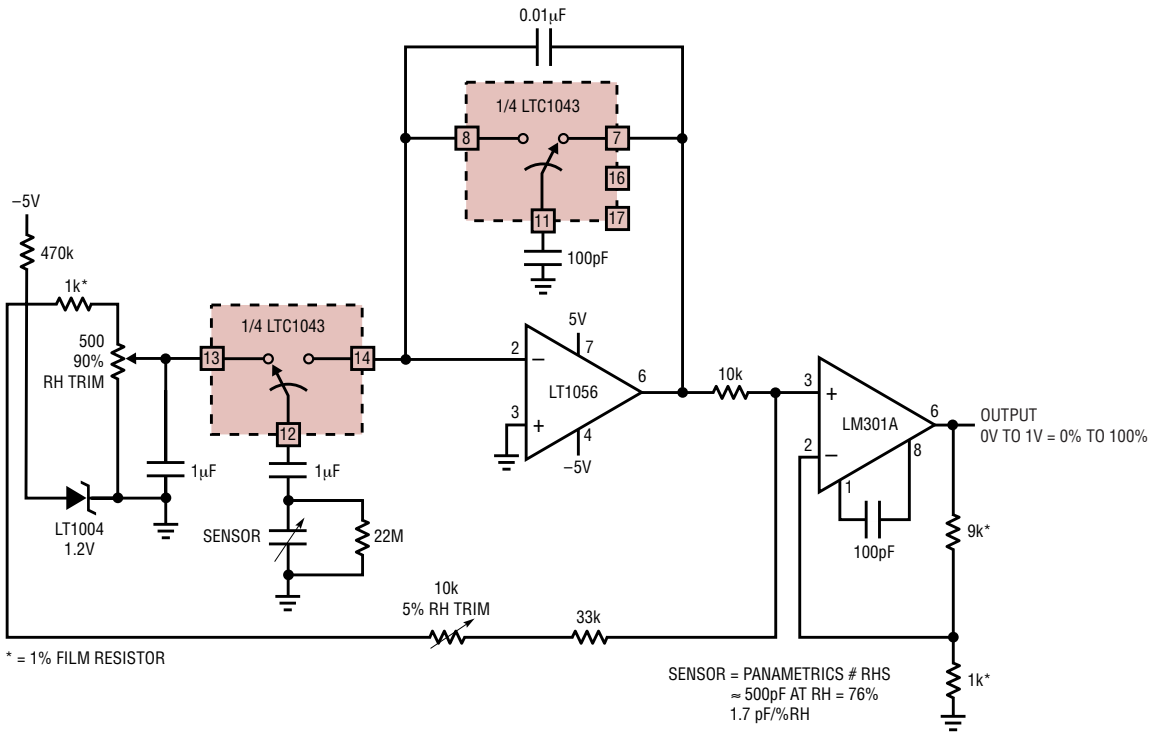
GAIN = $\frac{f_{IN} \bullet 0.01\mu F}{1kHz \bullet 100pF}$; GAIN IS NEGATIVE AS SHOWN

FOR SINGLE-ENDED INPUT AND POSITIVE GAIN, GROUND PIN 8A AND USE PIN 7A FOR INPUT

USE ±5V SUPPLIES FOR LTC1043

LTC1043 • A20

Relative Humidity Sensor Signal Conditioner



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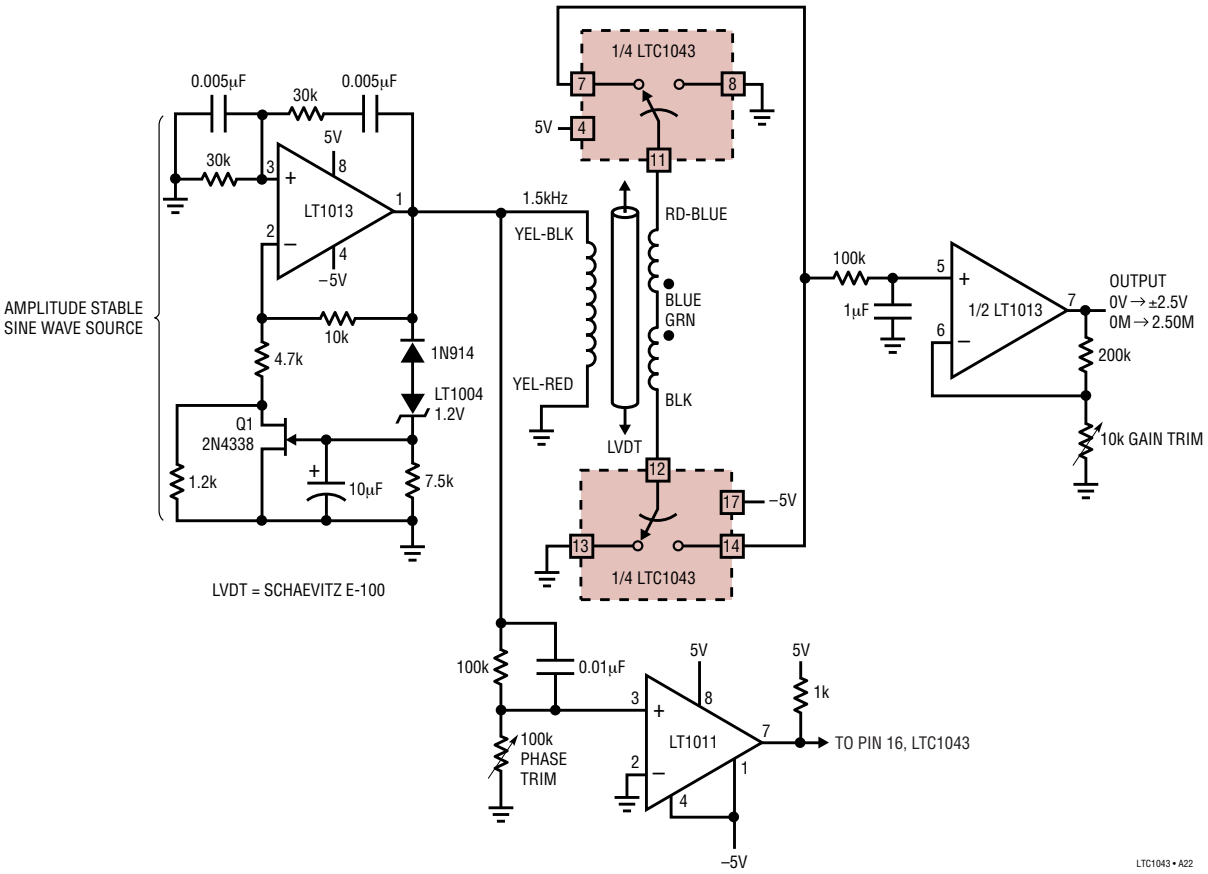
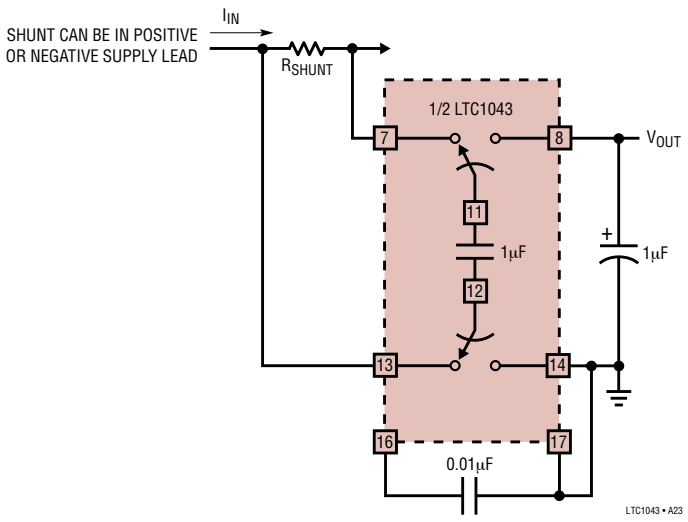
TYPICAL APPLICATIONS

Linear Variable Differential Transformer (LVDT), Signal Conditioner

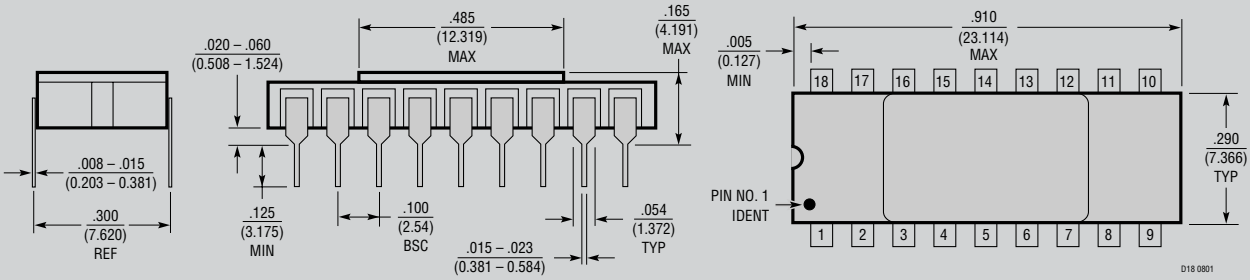


Precision Current Sensing in Supply Rails



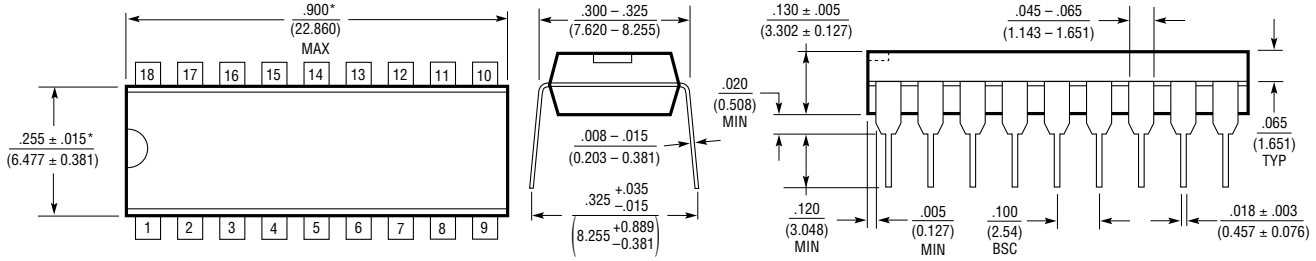
PACKAGE DESCRIPTION

D Package
18-Lead Side Brazed (Hermetic)
(Reference LTC DWG # 05-08-1210)



OBSOLETE PACKAGE

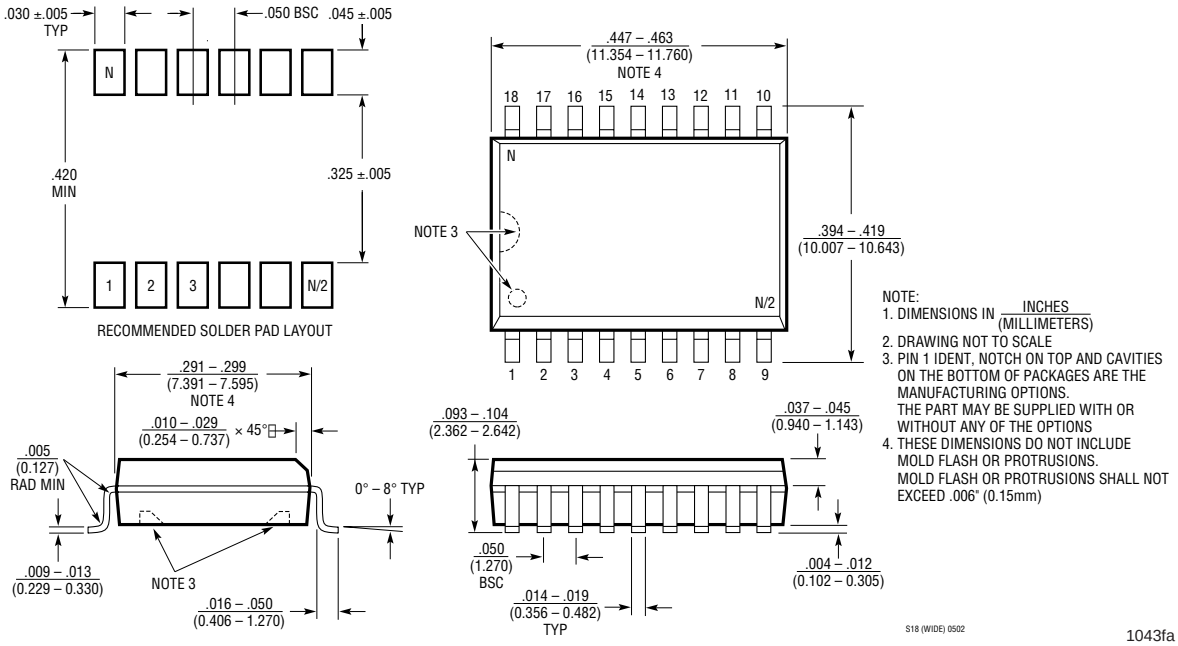
N Package
18-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

SW Package
18-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

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