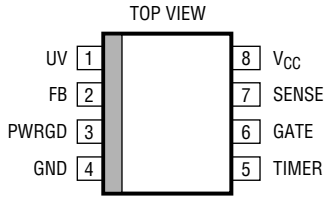
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) ..... –0.3 to 100V
SENSE, PWRGD ..... –0.3 to 100V
GATE (Note 2) ..... –0.3V to V_{CC} + 10V
Maximum Input Current (GATE) 200µA
FB, UV ..... –0.3 to 44V
TIMER ..... –0.3V to 4.3V
Maximum Input Current (TIMER) 100µA
Operating Temperature
LT4256C ..... 0°C to 70°C
LT4256I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LT4256-1CS8 LT4256-1IS8 LT4256-2CS8 LT4256-2IS8
S8 PART MARKING
42561 42561I 42562 42562I

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 48V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Operating Voltage		●	10.8		80	V
I_{CC}	Operating Current				1.8	3.9	mA
V_{UVLH}	Undervoltage Threshold	V_{CC} Low-to-High Transition	●	3.96	4	4.04	V
V_{UVHYS}	Hysteresis			0.25	0.4	0.55	V
I_{INUV}	UV Input Current	UV ≥ 1.2V UV = 0V			–0.1 –1.5	–1 –3	µA µA
V_{UVRTH}	Fault Latch Reset Threshold Voltage		●	0.4	0.85	1.2	V
$V_{SENSETRIP}$	SENSE Pin Trip Voltage (V_{CC} – V_{SENSE})	FB = 0V FB ≥ 2V	● ●	5.5 45	14 55	22 65	mV mV
I_{INSNS}	SENSE Pin Input Current	V_{SENSE} = V_{CC}			40	70	µA
I_{PU}	GATE Pull-Up Current	Charge Pump On, ΔV_{GATE} = 7V	●	–16	–32	–63	µA
I_{PD}	GATE Pull-Down Current	Any Fault, V_{GATE} = 3V		40	62	80	mA
ΔV_{GATE}	External N-Channel Gate Drive (Note 2)	V_{GATE} – V_{CC}, 10.8V ≤ V_{CC} ≤ 20V 20V ≤ V_{CC} ≤ 80V	● ●	4.5 10	8.8 11.6	12.5 12.8	V V
V_{FB}	FB Voltage Threshold	FB High-to-Low Transition FB Low-to-High Transition	● ●	3.95 4.2	3.99 4.45	4.03 4.65	V V
V_{FBHYS}	FB Hysteresis Voltage			0.3	0.45	0.6	V
V_{OLPGD}	PWRGD Output Low Voltage	I_O = 1.6mA I_O = 5mA			0.25 0.6	0.4 1	V V
I_{PWRGD}	PWRGD Pin Leakage Current	V_{PWRGD} = 80V			0.1	1	µA
I_{INFB}	FB Input Current	FB = 4.5V			–0.1	–1	µA
$I_{TIMERPU}$	TIMER Pull-Up Current	TIMER = 3V, During Fault	●	–63	–105	–147	µA
$I_{TIMERPD}$	TIMER Pull-Down Current	TIMER = 3V	●	1.5	3	5	µA
$V_{THTIMER}$	TIMER Shut-Down Threshold	C_{TIMER} = 10nF	●	4.3	4.65	5	V
D_{TIMER}	Duty Cycle (RETRY Mode)		●	1.5	3	4.5	%

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 48V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PHLUV}	UV Low to GATE Low				1.7	3	µs
t_{PLHUV}	UV High to GATE High	C_{GATE} = 0			6	9	µs
t_{PHLFB}	FB Low to PWRGD Low				0.8	2	µs
t_{PLHFB}	FB High to PWRGD High				3.2	5	µs
$t_{PHLSENSE}$	(V_{CC} – V_{SENSE}) High to GATE Low	V_{CC} – V_{SENSE} = 275mV			1	3	µs

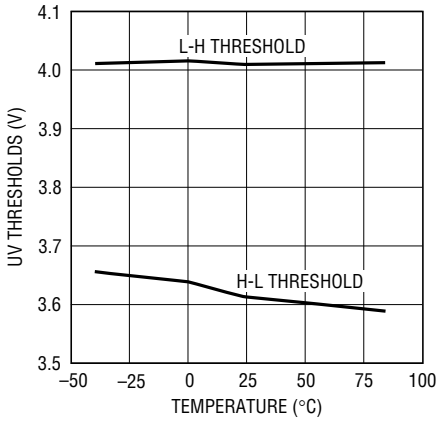
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: An internal clamp limits the GATE pin to a minimum of 10V above V_{CC}. Driving this pin to a voltage beyond the clamp voltage may damage the part.

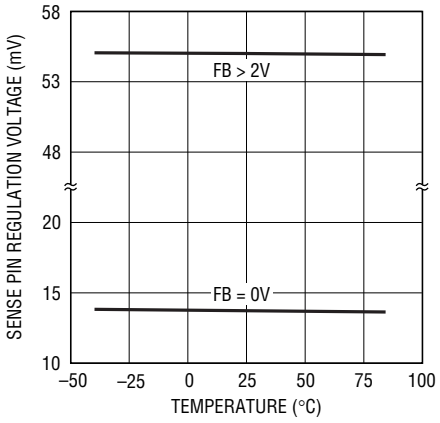
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

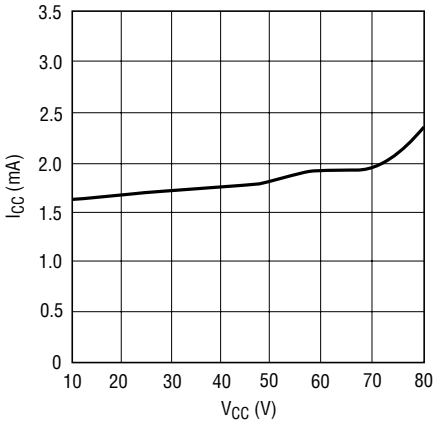
UV Thresholds vs Temperature



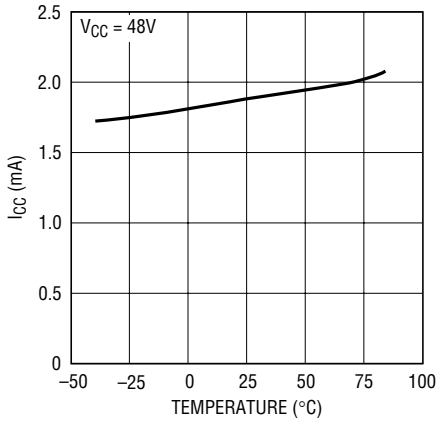
SENSE Pin Regulation Voltage vs Temperature



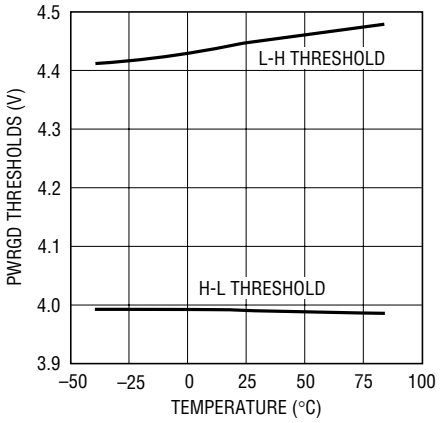
I_{CC} vs V_{CC}



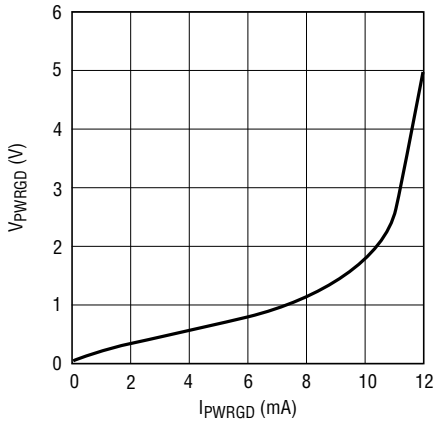
I_{CC} vs Temperature



PWRGD Thresholds vs Temperature



PWRGD Output Voltage vs I_{PWRGD}



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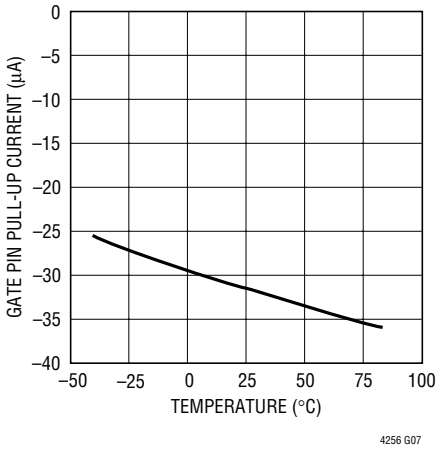
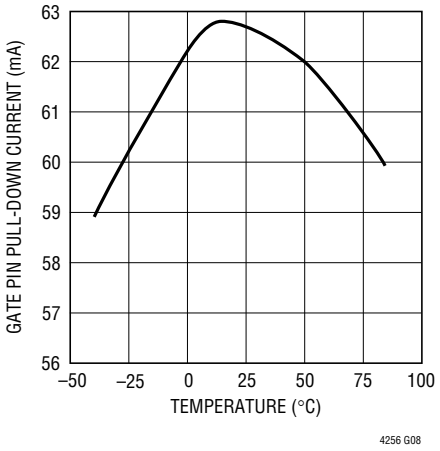
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

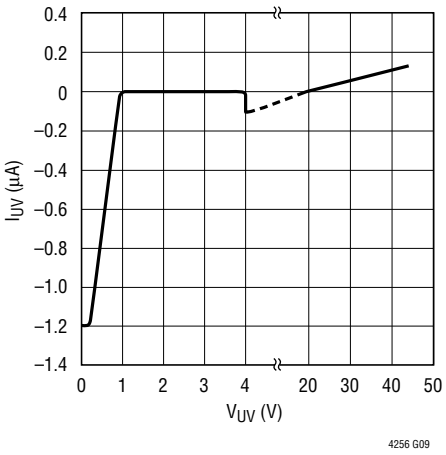
GATE Pin Pull-Up Current vs Temperature



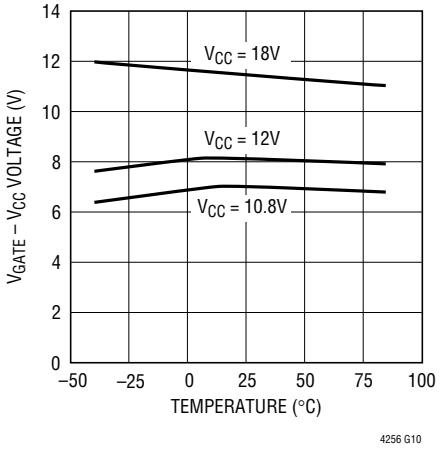
GATE Pin Pull-Down Current vs Temperature



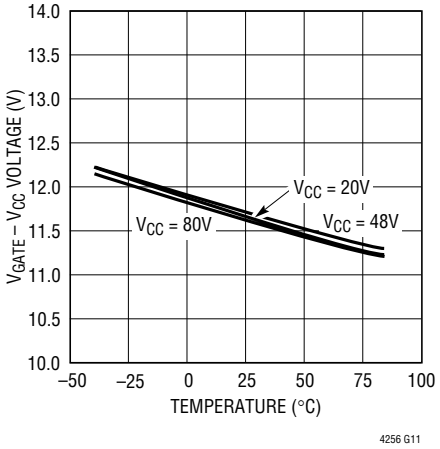
UV Pin Current vs UV Pin Voltage



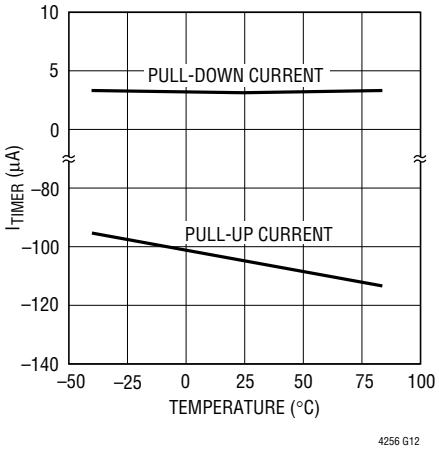
$V_{GATE} – V_{CC}$ Voltage vs Temperature



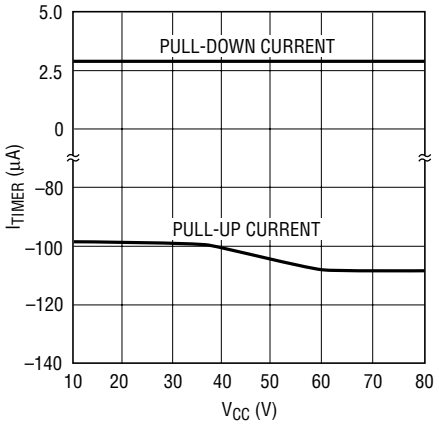
$V_{GATE} – V_{CC}$ Voltage vs Temperature



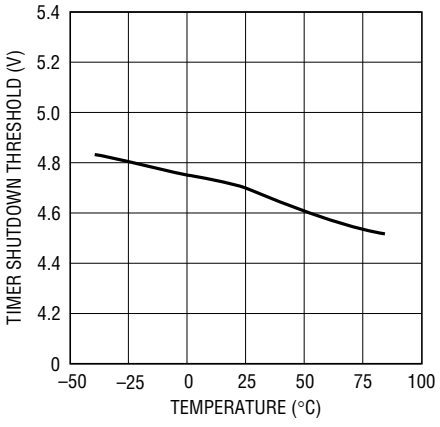
TIMER Pin Currents vs Temperature



TIMER Pin Currents vs V_{CC}



Timer Shutdown Threshold vs Temperature



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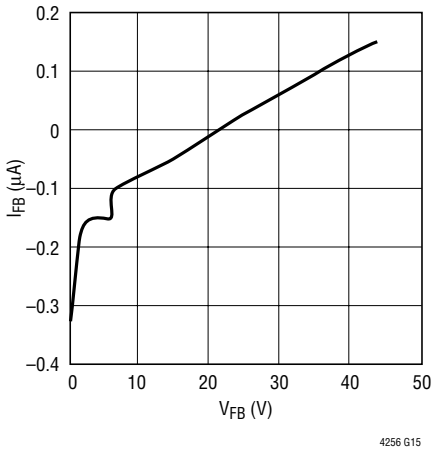
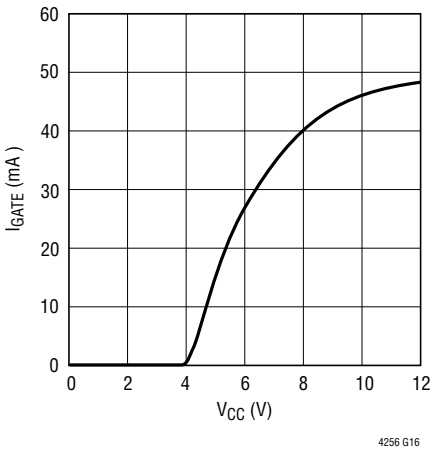
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

FB Pin Current vs FB Pin Voltage



Gate Pull-Down Capability vs V_{CC} Below Minimum Operating Voltage



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PIN FUNCTIONS

UV (Pin 1): Undervoltage Sense. UV is an input that enables the output voltage. When UV is driven above 4V, GATE will start charging and the output turns on. When UV goes below 3.6V, GATE discharges and the output shuts off.

Pulsing UV low for a minimum of 5µs after a current limit fault cycle resets the fault latch (LT4256-1) and allows the part to turn back on. This command is only accepted after TIMER has discharged below 0.65V. To disable UV sensing, connect UV to a voltage beween 5V and 44V.

FB (Pin 2): Power Good Comparator Input. FB monitors the output voltage through an external resistive divider. When the voltage on FB is lower than the high-to-low threshold of 3.99V, PWRGD is pulled low and released when FB is pulled above the 4.45V low-to-high threshold.

The voltage present on FB affects foldback current limit (see Figure 7 and related discussion).

PWRGD (Pin 3): Power Good Output. PWRGD is pulled low whenever the voltage on FB falls below the 3.99V high-to-low threshold voltage. It goes into a high impedance state when the voltage on FB exceeds the low-to-high threshold voltage. An external pull-up resistor can pull PWRGD to a voltage higher or lower than V_{CC}.

GND (Pin 4): Device Ground. This pin must be tied to a ground plane for best performance.

TIMER (Pin 5): Timing Input. An external timing capacitor from TIMER to GND programs the maximum time the part is allowed to remain in current limit. When the part goes into current limit, a 105µA pull-up current source starts to charge the timing capacitor. When the voltage on TIMER reaches 4.65V (typ), GATE pulls low; the TIMER pull-up current will be turned off and the capacitor is discharged by a 3µA pull-down current. When TIMER falls below 0.65V (typ), GATE turns on again for the LT4256-2. UV must be cycled low after TIMER has discharged below 0.65V (typ) to reset the LT4256-1. If UV is not cycled low (LT4256-1), GATE remains latched off and TIMER is discharged to near GND. Under an output short-circuit condition, the LT4256-2 cycles on and off with a 3% duty cycle.

GATE (Pin 6): High Side Gate Drive for the External N-Channel MOSFET. An internal charge pump guarantees at least 10V of gate drive for V_{CC} supply voltages above 20V and 4.5V of gate drive for V_{CC} supply voltages between 10.8V and 20V. The rising slope of the voltage on GATE is set by an external capacitor connected from GATE to GND and an internal 32µA pull-up current source from the charge pump output.

If the current limit is reached, the GATE voltage is adjusted to maintain a constant voltage across the sense resistor while the timing capacitor starts to charge. If the TIMER voltage ever exceeds 4.65V, GATE is pulled low.

GATE is also pulled to GND whenever UV is pulled low, the V_{CC} supply voltage drops below the externally programmed undervoltage threshold, or V_{CC} drops below the internal UVLO threshold (9.8V).

GATE is clamped internally to a maximum voltage of 11.6V (typ) above V_{CC} under normal operating conditions. Driving this pin beyond the clamp voltage may damage the part. A Zener diode is needed between the gate and source of the external MOSFET to protect its gate oxide under instantaneous short-circuit conditions. See Applications Information.

SENSE (Pin 7): Current Limit Sense Input. A sense resistor is placed in the supply path between V_{CC} and SENSE. The current limit circuit regulates the voltage across the sense resistor (V_{CC} – SENSE) to 55mV while in current limit when FB is 2V or higher. If FB drops below 2V, the regulated voltage across the sense resistor decreases linearly to 14mV when FB is 0V.

To defeat current limit, connect SENSE to V_{CC}.

V_{CC} (Pin 8): Input Supply Voltage. The positive supply input ranges from 10.8V to 80V for normal operation. I_{CC} is typically 1.8mA. An internal circuit disables the LT4256-1/LT4256-2 for inputs less than 9.8V (typ).

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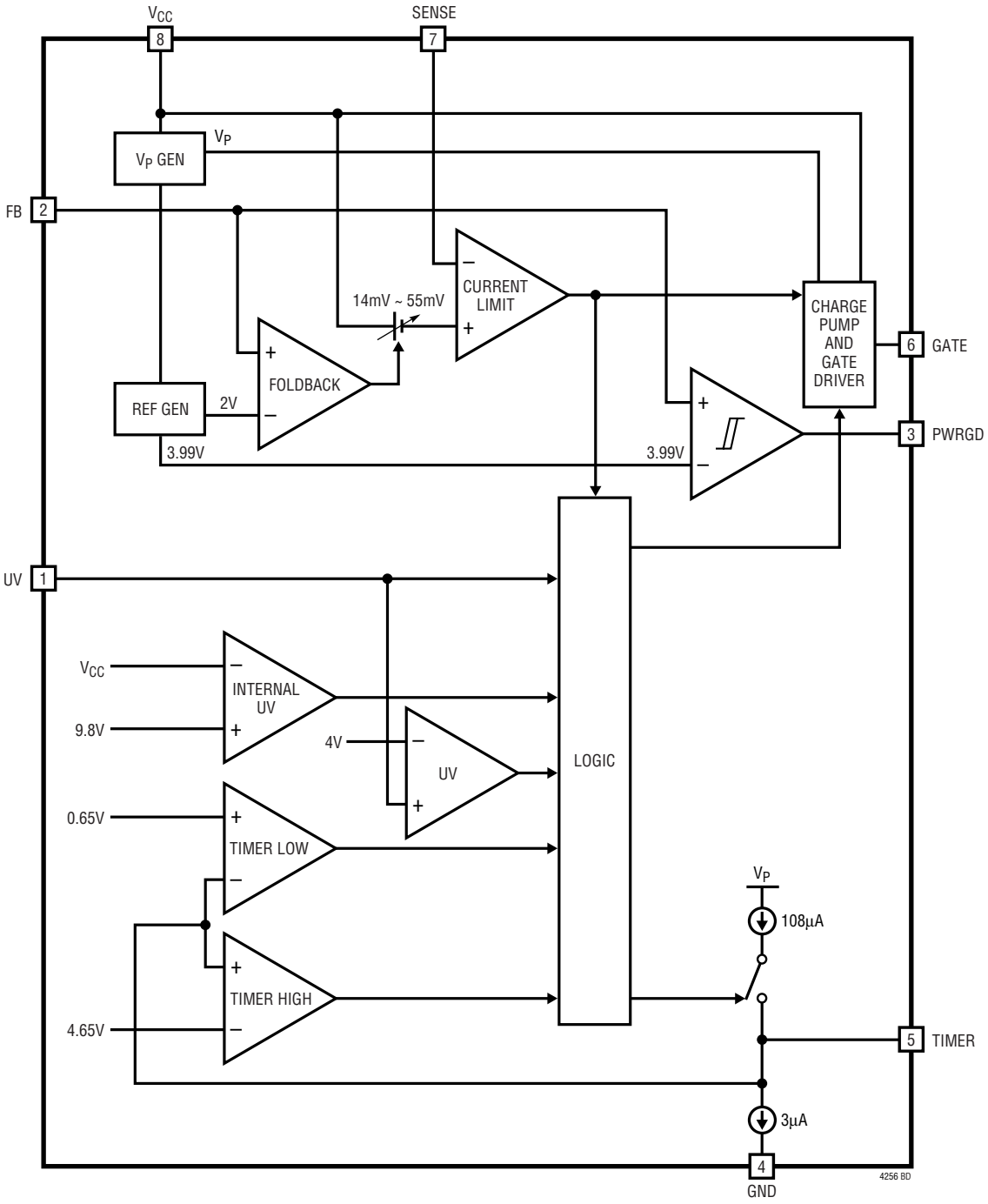
BLOCK DIAGRAM



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TEST CIRCUIT

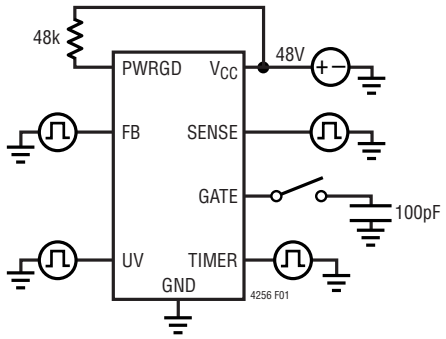

Figure 1

TIMING DIAGRAMS

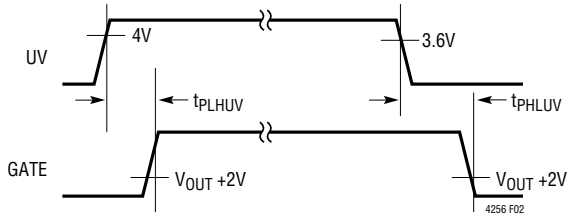

Figure 2. UV to GATE Timing

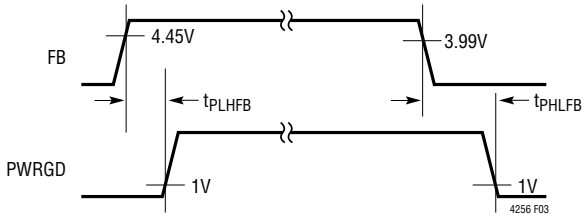

Figure 3. V_{OUT} to PWRGD Timing

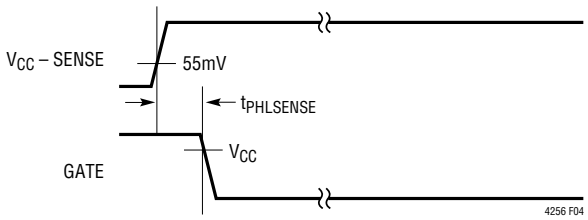

Figure 4. SENSE to GATE Timing

APPLICATIONS INFORMATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors on the boards draw high peak currents from the backplane power bus as they charge. The transient currents can permanently damage the connector pins and glitch the system supply, causing other boards in the system to reset.

The LT4256-1/LT4256-2 are designed to turn on a board's supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The device also provides undervoltage as well as overcurrent protection while a power good output signal indicates when the output supply voltage is ready with a high output.

Power-Up Sequence

An external N-channel MOSFET pass transistor (Q1) is placed in the power path to control the power up of the supply voltage (Figure 5). Resistor R5 provides current detection and capacitor C1 controls the GATE slew rate. Resistor R7 compensates the current control loop while R6 prevents high frequency oscillations in Q1.

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APPLICATIONS INFORMATION

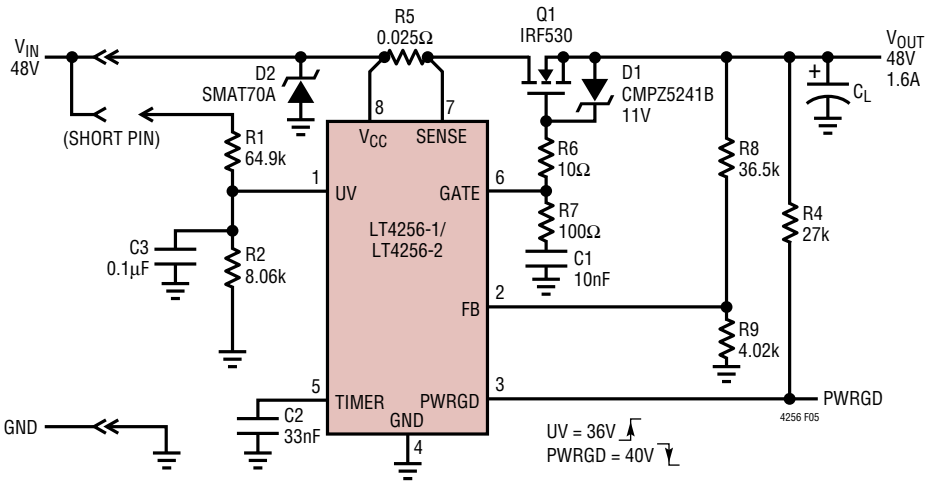

Figure 5. 1600mA, 48V Application

When the power pins first make contact, transistor Q1 is held off. If the voltage on V_{CC} is above the externally programmed undervoltage threshold, V_{CC} is above 9.8V, and the voltage on TIMER is less than 4.65V (typ), transistor Q1 will be turned on (Figure 6). The voltage on GATE rises with a slope equal to 32µA/C1 and the supply inrush current is set at:

$$I_{INRUSH} = C_L \bullet 32\mu A/C1 \quad (1)$$

where C_L is the total load capacitance.

To reduce inrush current, increase C1 or decrease load capacitance. If the voltage across the current sense resistor R5 reaches $V_{SENSETRIP}$, the inrush current will be limited by the internal current limit circuitry. The voltage on GATE is adjusted to maintain a constant voltage across the sense resistor and TIMER begins to charge.

When the FB voltage goes above the low-to-high V_{FB} threshold, PWRGD goes high.

Undervoltage Detection

The LT4256-1/LT4256-2 uses UV to monitor the V_{CC} voltage to determine when it is safe to turn on the load and allow the user the greatest flexibility for setting the threshold. Any time that UV goes below 3.6V, GATE will be pulled low until UV goes above 4V again.

The UV threshold should never be set below the internal UVLO threshold (9.8V typically) because the benefit of UV's hysteresis will be lost, making the LT4256-1/LT4256-2 more susceptible to noise (V_{CC} must be at least 9.8V when UV is at its 3.6V threshold). UV is filtered with C3 to prevent noise spikes and capacitively coupled glitches from shutting down the LT4256-1/LT4256-2 output erroneously.

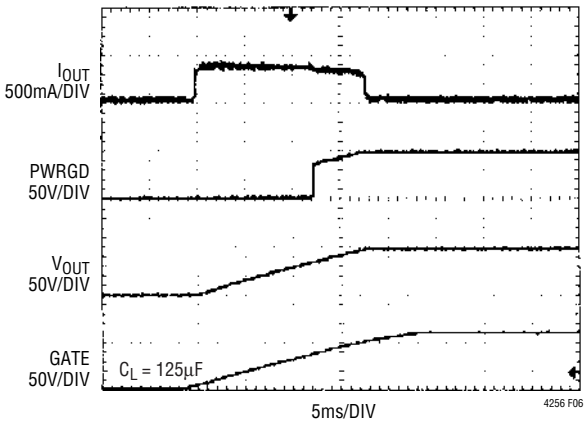

Figure 6. Start-Up Waveforms

To calculate the UV threshold, use the following equations:

$$R1 = R2\left(\frac{V_{THUVLH}}{4V} - 1\right) \quad (2)$$

$$20k\Omega \le R1 + R2 \le 200k\Omega \quad (3)$$

$$V_{THUVLH} = 3.6\left(1 + \frac{R1}{R2}\right) \quad (4)$$

where V_{THUVLH} is the desired UV threshold voltage when V_{CC} is rising (L-H), etc.

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APPLICATIONS INFORMATION

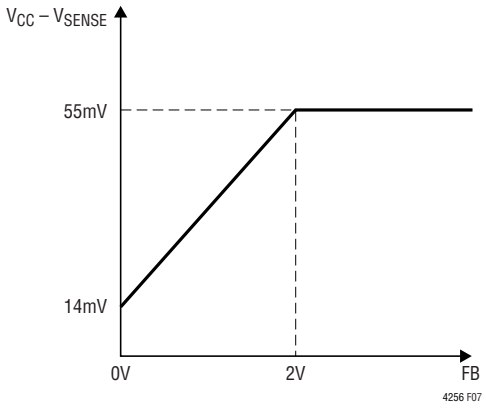

Figure 7. Current Limit Sense Voltage vs Feedback Pin Voltage

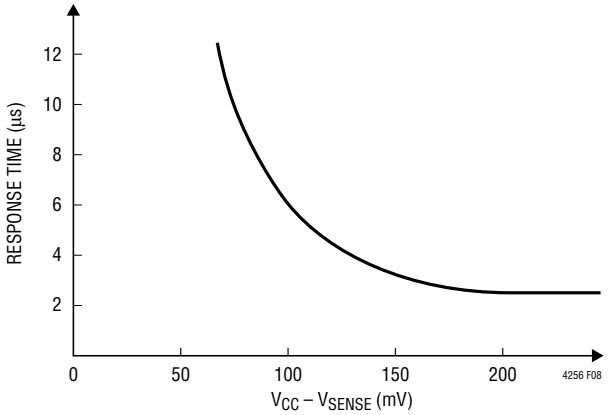

Figure 8. Response Time to Overcurrent

Figure 11 shows how the LT4256-1/LT4256-2 are commanded to shut off with a logic signal. This is accomplished by pulling the gate of the open-drain MOSFET, Q2, (tied to the UV pin) high.

Short-Circuit Protection

The LT4256-1/LT4256-2 features a programmable foldback current limit with an electronic circuit breaker that protects against short circuits or excessive load currents. The current limit is set by placing a sense resistor (R5) between V_{CC} and SENSE. The current limit threshold is calculated as:

$$I_{LIMIT} = 55mV/R5 \quad (5)$$

where R5 is the sense resistor.

To limit excessive power dissipation in the pass transistor and to reduce voltage spikes on the input supply during short-circuit conditions at the output, the current folds back as a function of the output voltage, which is sensed internally on FB.

If the LT4256-1/LT4256-2 go into current limit when the voltage on FB is 0V, the current limit circuit drives the GATE pin to force a constant 14mV drop across the sense resistor. As the output at FB increases, the voltage across the sense resistor increases until the FB pin reaches 2V, at which point the voltage across the sense resistor is held constant at 55mV (see Figure 7).

For a 0.025Ω sense resistor, the current limit is set at 2200mA and folds back to 560mA when the output is shorted to ground. Thus, MOSFET peak power dissipation under short-circuit conditions is reduced from 105.6W to 26.5W. See the Layout Considerations section for important information about board layout to minimize current limit threshold error.

The LT4256-1/LT4256-2 also features a variable overcurrent response time. The time required for the part to regulate the GATE voltage is a function of the voltage across the sense resistor connected between V_{CC} and SENSE. This helps to eliminate sensitivity to current spikes and transients that might otherwise unnecessarily trigger a current limit response and increase MOSFET dissipation. Figure 8 shows the response time as a function of the overdrive at SENSE.

TIMER

TIMER provides a method for programming the maximum time the part is allowed to operate in current limit. When the current limit circuitry is not active, the TIMER pin is pulled to GND by a 3µA current source. When the current limit circuitry becomes active, a 108µA pull-up current source is connected to TIMER and the voltage will rise with a slope equal to $105\mu A/C_{TIMER}$ as long as the circuitry stays active. Once the desired maximum current limit time is known, the capacitor value is:

$$C[nF] = 25 \bullet t[ms]; C = \frac{105\mu A}{4.65V} \bullet t \quad (6)$$

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APPLICATIONS INFORMATION

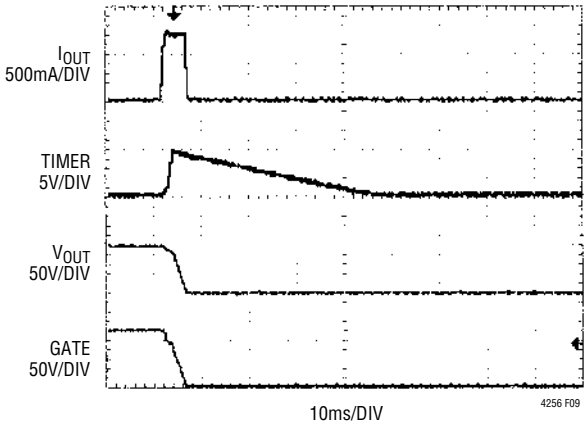

Figure 9. LT4256-1 Current Limit Waveforms

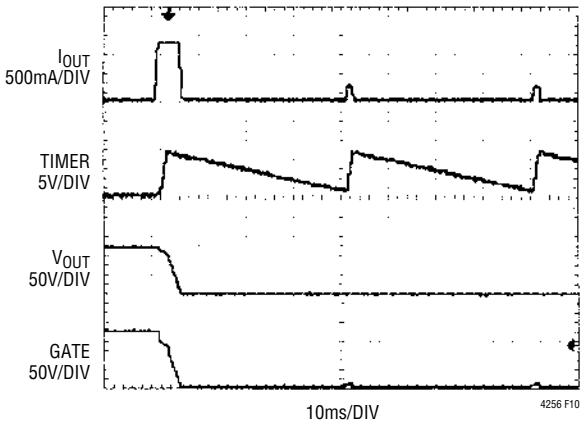

Figure 10. LT4256-2 Current Limit Waveforms

When the TIMER pin reaches 4.65V (typ), the internal fault latch is set causing GATE to be pulled low and TIMER to be discharged to GND by the 3µA current source. The part is not allowed to turn on again until the voltage on TIMER falls below 0.65V (typ).

TIMER must never be pulled high by a low impedance because whenever TIMER rises above the upper threshold (typically 4.65V) the pin characteristics change from a high impedance current source to a low impedance.

Whenever GATE is commanded off by any fault condition, it is discharged rapidly, turning off the external MOSFET. The waveform in Figure 9 shows how the output latches off following a current fault (LT4256-1). The drop across the sense resistor is held at 55mV as the timer ramps up. Once TIMER reaches its shutdown threshold (4.65V typically), the circuit latches off.

The LT4256-1 latches off after a current limit fault. After the LT4256-1 latches off, the part may be commanded to start back up. This is accomplished by cycling UV to ground and then back high (this command can only be accepted after TIMER discharges back below the 0.65V typical threshold, to prevent overheating transistor Q1).

Automatic Restart

The LT4256-2 will automatically restart after an overcurrent fault. These waveforms are shown in Figure 10.

The LT4256-2 functionality is as follows: When an overcurrent condition occurs, the GATE pin is servoed to maintain a constant voltage across the sense resistor, and the capacitor C2 at the TIMER pin will begin to charge. When the voltage at the TIMER pin reaches 4.65V (typ), the GATE pin is pulled low. When the voltage at the TIMER pin ramps back down to 0.65V (typ), the LT4256-2 turns on again. If the short-circuit condition at the output still exists, the cycle will repeat itself indefinitely. The duty cycle under short-circuit conditions is 3% which prevents Q1 from overheating.

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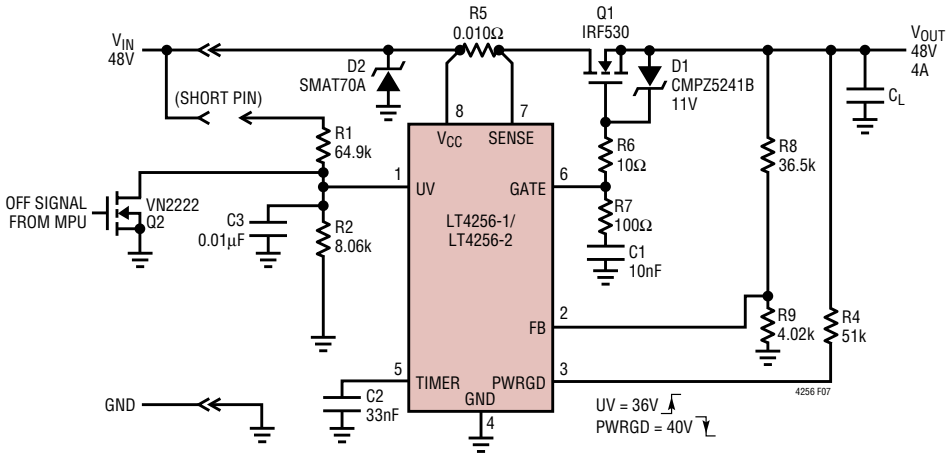

Figure 11. How to Use a Logic Signal to Control LT4256 Turn-On/-Off

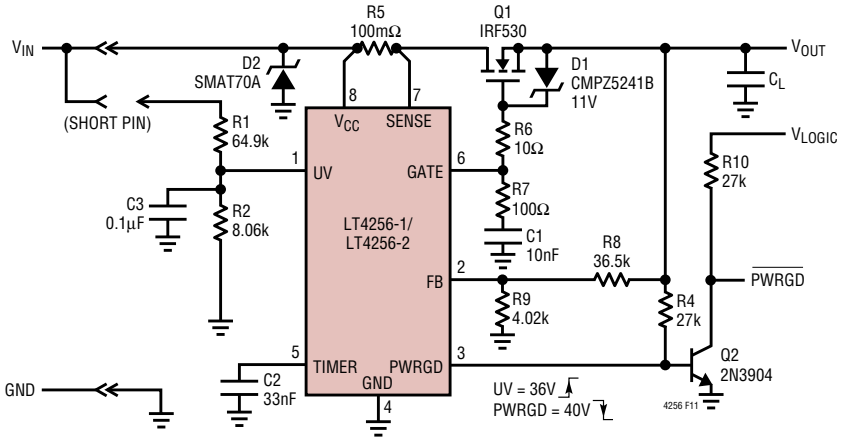

Figure 12. Active Low Enable PWRGD Application

Power Good Detection

The LT4256-1/LT4256-2 includes a comparator for monitoring the output voltage. The output voltage is sensed through the FB pin via an external resistor string. The comparator's output (PWRGD) is an open collector capable of operating from a pull-up as high as 80V.

PWRGD can be used to directly enable/disable a power module with an active high enable input. Figure 12 shows how to use PWRGD to control an active low enable input power module. Signal inversion is accomplished by transistor Q2 and R10.

The thresholds for the FB pin are 4.45V (low to high) and 3.99V (high to low). To calculate the PWRGD thresholds, use the following equations:

$$R8 = \left(\frac{V_{THPWRGD}}{3.99V} - 1\right) \bullet R9, \text{ high to low} \quad (7)$$

$$20k\Omega \le R8 + R9 \le 200k\Omega \quad (8a)$$

$$V_{THPWRGD} = 4.45V\left(1 + \frac{R8}{R9}\right), \text{ low to high} \quad (8b)$$

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APPLICATIONS INFORMATION

Supply Transient Protection

The LT4256-1/LT4256-2 is 100% tested and guaranteed to be safe from damage with supply voltages up to 80V. However, voltage transients above 100V may cause permanent damage. During a short-circuit condition, the large change in currents flowing through the power supply traces can cause inductive voltage transients which could exceed 100V. To minimize the voltage transients, the power trace parasitic inductance should be minimized by using wider traces or heavier trace plating and a 0.1µF bypass capacitor should be placed between V_{CC} and GND. A surge suppressor, as shown in the application diagrams, (Transzorb) at the input can also prevent damage from voltage transients.

GATE Pin

A curve of gate drive vs V_{CC} is shown in Figure 13. GATE is clamped to a maximum voltage of 12.8V above V_{CC}. This clamp is designed to sink the internal charge pump current. An external Zener diode must be used as shown in all applications. At a minimum input supply voltage of 12V, the minimum gate drive voltage is 4.5V. When the input supply voltage is higher than 20V, the gate drive voltage is at least 10V and a standard threshold MOSFET can be used. In applications from 12V to 15V range, a logic level MOSFET must be used.

In some applications it may be possible for the V_{OUT} pin to ring below ground (due to the parasitic trace inductance).

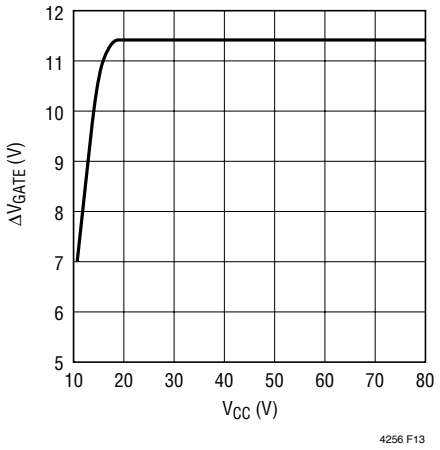

Figure 13. ΔV_{GATE} vs V_{CC}

Higher current applications, especially where the output load is physically far away from the LT4256-1/LT4256-2 will be more susceptible to these transients. This is normal and the LT4256-1/LT4256-2 have been designed to allow for some ringing below ground. However, if the application is such that V_{OUT} can ring more than 10V below ground, damage may occur to the LT4256-1 and an external diode from ground (anode) to V_{OUT} (cathode) must be added to the circuit as shown in Figure 14 (it is critical that the reverse breakdown voltage of the diode be higher than the highest expected V_{CC} voltage). A capacitor placed from ground to V_{OUT} directly at the LT4256-1/LT4256-2 can help reduce the amount of ringing on V_{OUT} but it may not be enough for some applications.

During a fault condition, the LT4256-1/LT4256-2 pulls down on GATE with a switch capable of sinking about 60mA. Once GATE drops below the output voltage by a diode forward voltage, the external Zener will forward bias and V_{OUT} will also be discharged to GND. In addition to the GATE capacitance, the output capacitance will be discharged through the LT4256-1/LT4256-2.

In applications utilizing very large external N-channel MOSFETs, the possibility exists for the MOSFET to turn on when initially inserted into a live backplane (before the LT4256-1/LT4256-2 becomes active and pulls down on GATE). This is due to the drain to gate capacitance forcing current into R7 and C1 when the drain voltage steps up from ground to V_{IN} with an extremely fast rise time. To alleviate this situation, a diode, D3, should be put across R7 with the cathode connected to C1 as shown in Figure 15.

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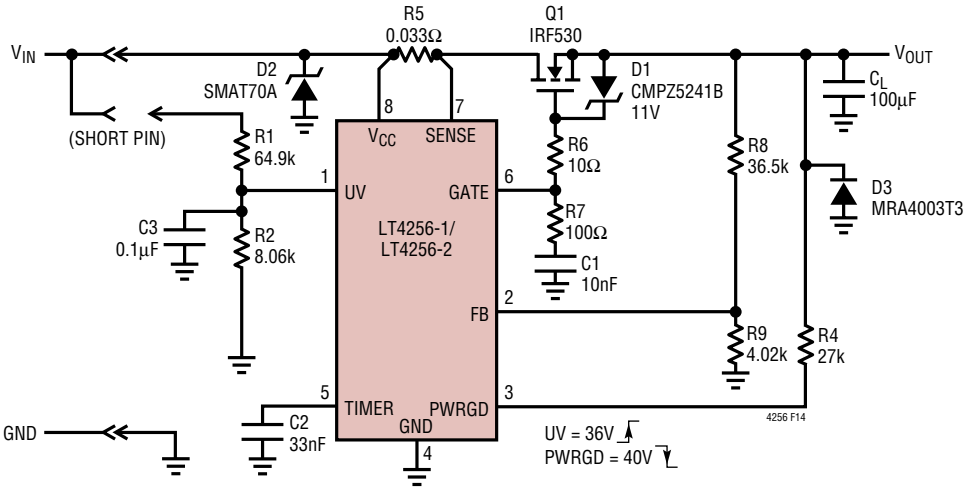

Figure 14. Negative Output Voltage Protection Diode Application

Notes on Using the LT4256 in LT1641 Applications

Even though the LT4256 and LT1641 have the same pinout, several changes were made to improve overall system accuracy and increase noise immunity. These changes are spelled out in Table 1 and must be accounted for if using the LT4256 in an LT1641 application.

Layout Considerations

To achieve accurate current sensing, a Kelvin connection to the current sense resistor (R5 in typical application circuit) is recommended. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530µΩ/❑. Small resistances can cause large errors in high current applications. Noise immunity will be improved significantly by locating resistor dividers close to the pins with short V_{CC} and GND traces. A 0.1µF decoupling capacitor from UV to GND is also required.

Table 1. Differences Between LT1641 and LT4256

SPECIFICATION	LT1641	LT4256	COMMENTS
UV Threshold	1.313V	4V	Higher 1% Reference for Better Noise Immunity and System Accuracy
FB Threshold	1.233V	3.99V	Higher 1% Reference for Better Noise Immunity and System Accuracy
TIMER Current	±70%	±40%	More Accurate TIMEOUT
TIMER Shutdown V	1.233V	4.65V	Higher Trip Voltage for Better Noise Immunity
GATE I_{PU}	10µA	30µA	Higher Current to Accommodate Higher Leakage MOSFETs or Parallel Devices
GATE Resistor	1kΩ	100Ω	Different Compensation for Current Limit Loop
Foldback I_{LIM}	12mV	14mV	Slightly Different Current Limit Trip Point
I_{LIM} Threshold	47mV	55mV	Slightly Different Current Limit Trip Point
Fault Latch Reset Threshold Voltage	1.233V	0.85V	Better Noise Immunity

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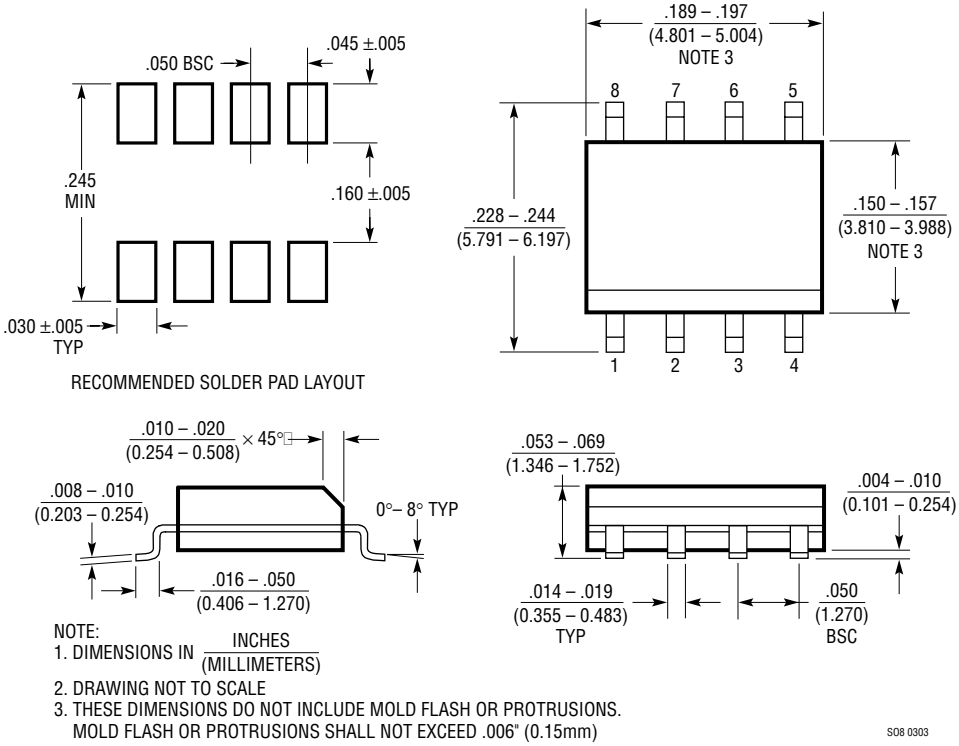
PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

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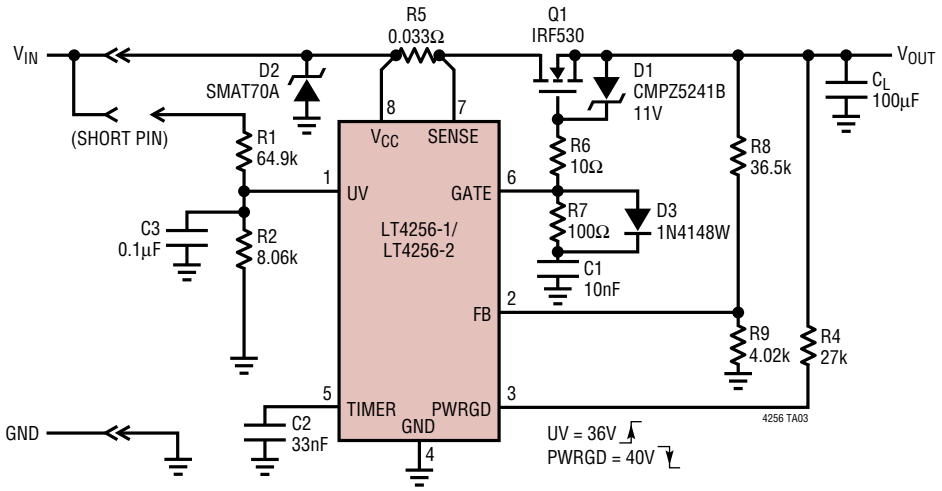

Figure 15. High dV/dT MOSFET Turn-On Protection Circuit

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1641-1/LT1641-2	Positive 48V Hot Swap Controller in SO-8	9V to 80V Operation, Active Current Limit, Autoretry/Latchoff
LTC4211	Single Hot Swap Controller with Multifunction Current Control	2.5V to 16.5V, Active Inrush Limiting, Dual Level Cicuit Breaker
LTC4251	–48V Hot Swap Controller in SOT-23	Floating Supply from –15V, Active Current Limiting, Fast Circuit Breaker
LTC4252-1/LTC4252-2	–48V Hot Swap Controller in MSOP	Floating Supply from –15V, Active Current Limiting, Power Good Output
LTC4253	–48V Hot Swap Controller and Supply Sequencer	Floating Supply from –15V, Active Current Limiting, Enables Three DC/DC Converters
LT4254	Positive High Voltage Hot Swap Controller	10.8V to 36V, Open-Circuit Detection

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