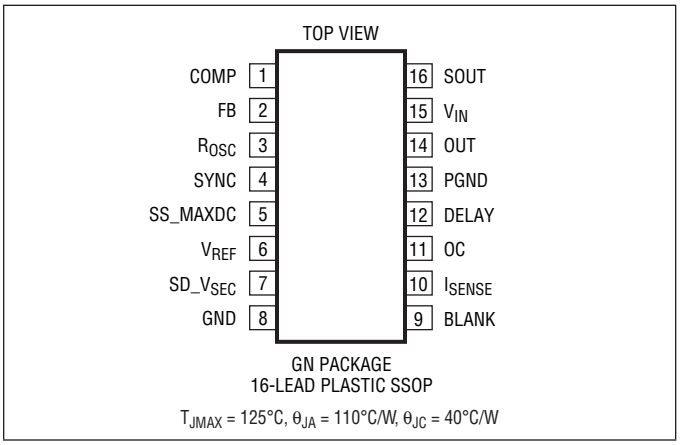
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} (Note 8) .....–0.3V to 25V
SYNC, SS_MAXDC, SD_V_{SEC}, I_{SENSE}, OC ....–0.3V to 6V
COMP, BLANK, DELAY.....–0.3V to 3.5V
FB .....–0.3V to 3V
R_{OSC}..... –50µA
V_{REF} .....–10mA
Operating Junction Temperature Range (Notes 2, 5)
E-, I-Grades .....–40°C to 125°C
MP-Grade .....–55°C to 125°C
Storage Temperature Range.....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W, θ_{JC} = 40°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1952EGN#PBF	LT1952EGN#TRPBF	1952	16-Lead Plastic SSOP	–40°C to 125°C
LT1952IGN#PBF	LT1952IGN#TRPBF	1952I	16-Lead Plastic SSOP	–40°C to 125°C
LT1952MPGN#PBF	LT1952MPGN#TRPBF	1952	16-Lead Plastic SSOP	–55°C to 125°C
LT1952EGN-1#PBF	LT1952EGN-1#TRPBF	19521	16-Lead Plastic SSOP	–40°C to 125°C
LT1952IGN-1#PBF	LT1952IGN-1#TRPBF	1952I1	16-Lead Plastic SSOP	–40°C to 125°C
LT1952MPGN-1#PBF	LT1952MPGN-1#TRPBF	19521	16-Lead Plastic SSOP	–55°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT1952EGN	LT1952EGN#TR	1952	16-Lead Plastic SSOP	–40°C to 125°C
LT1952IGN	LT1952IGN#TR	1952I	16-Lead Plastic SSOP	–40°C to 125°C
LT1952MPGN	LT1952MPGN#TR	1952	16-Lead Plastic SSOP	–55°C to 125°C
LT1952EGN-1	LT1952EGN-1#TR	19521	16-Lead Plastic SSOP	–40°C to 125°C
LT1952IGN-1	LT1952IGN-1#TR	1952I1	16-Lead Plastic SSOP	–40°C to 125°C
LT1952MPGN-1	LT1952MPGN-1#TR	19521	16-Lead Plastic SSOP	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). COMP = open, FB = 1.4V, R_{OSC} = 178k, SYNC = 0V, SS_MAXDC = V_{REF}, V_{REF} = 0.1µF, SD_V_{SEC} = 2V, BLANK = 121k, DELAY = 121k, I_{SENSE} = 0V, OC = 0V, OUT = 1nF, V_{IN} = 15V, SOUT = open, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER						
Operational Input Voltage	$I(V_{REF})$ = 0µA	●	V_{IN} OFF		25	V
V_{IN} Quiescent Current	$I(V_{REF})$ = 0µA, I_{SENSE} = OC = Open			5.2	6.5	mA
V_{IN} Start-up Current (LT1952)	FB = 0V, SS_MAXDC = 0V (Notes 4, 9)	●		460	700	µA
V_{IN} Start-up Current (LT1952-1)	FB = 0V, SS_MAXDC = 0V (Notes 4, 9)	●		400	575	µA
V_{IN} Shutdown Current	SD_V_{SEC} = 0V			240	350	µA
SD_V_{SEC} Threshold	10V < V_{IN} < 25V	●	1.261	1.32	1.379	V
SD_$V_{SEC\ (ON)}$ Current	SD_V_{SEC} = SD_V_{SEC} Threshold + 100mV			0		µA
SD_$V_{SEC\ (OFF)}$ Current	SD_V_{SEC} = SD_V_{SEC} Threshold – 100mV		8.3	10	11.7	µA
$V_{IN\ ON}$ (LT1952)		●		14.25	15.75	V
$V_{IN\ OFF}$ (LT1952)		●		8.75	9.25	V
$V_{IN\ HYSTERESIS}$ (LT1952)		●	3.75	5.5	6.75	V
$V_{IN\ ON}$ (LT1952-1)	E-, I-Grades MP-Grade	● ●		7.75 7.75	8.13 8.3	V V
$V_{IN\ OFF}$ (LT1952-1)		●		6.5	6.82	V
$V_{IN\ HYSTERESIS}$ (LT1952-1)		●	0.95	1.25		V
V_{REF}						
Output Voltage	$I(V_{REF})$ = 0µA	●	2.425	2.5	2.575	V
Line Regulation	$I(V_{REF})$ = 0µA, 10V < V_{IN} < 25V			1	10	mV
Load Regulation	0µA < $I(V_{REF})$ < 2.5mA			1	10	mV
OSCILLATOR						
Frequency: f_{OSC}	R_{OSC} = 178k, FB = 1V, SS_MAXDC = 1.84V	●	165	200	240	kHz
Minimum Programmable f_{OSC} Maximum Programmable f_{OSC}	R_{OSC} = 365k, FB = 1V R_{OSC} = 64.9k, COMP = 2.5V, SD_V_{SEC} = 2.64V		80 440	100 500	120 560	kHz kHz
SYNC Input Resistance				18		kΩ
SYNC Switching Threshold	FB = 1V			1.5	2.2	V
SYNC Frequency/f_{OSC}	FB = 1V (Note 7)			1.25	1.5	
f_{OSC} Line Reg	FB = 1V, R_{OSC} = 178k; 10V < V_{IN} < 25V, SS_MAXDC = 1.84V			0.05	0.33	%/V
V_{ROSC}	R_{OSC} Pin voltage			1		V
ERROR AMPLIFIER						
FB Reference Voltage	10V < V_{IN} < 25V, V_{OL} + 0.2V < COMP < V_{OH} – 0.2	●	1.201	1.226	1.250	V
FB Input Bias Current	FB = FB Reference Voltage			–75	–200	nA
Open Loop Voltage Gain	V_{OL} + 0.2V < COMP < V_{OH} – 0.2		65	85		dB
Unity Gain Bandwidth	(Note 6)			3		MHz
COMP Source Current	FB = 1V, COMP = 1.6V		–4	–9		mA
COMP Sink Current	COMP = 1.6V		4	10		mA
COMP Current (Disabled)	FB = V_{REF}, COMP = 1.6V		18	23	28	µA
COMP High Level: V_{OH}	FB = 1V, $I_{(COMP)}$ = –250µA		2.7	3.2		V
COMP Active Threshold	FB = 1V, SOUT Duty Cycle > 0 %		0.7	0.8		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). COMP = open, FB = 1.4V, R_{OSC} = 178k, SYNC = 0V, SS_MAXDC = V_{REF}, V_{REF} = 0.1µF, SD_V_{SEC} = 2V, BLANK = 121k, DELAY = 121k, I_{SENSE} = 0V, OC = 0V, OUT = 1nF, V_{IN} = 15V, SOUT = open, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
COMP Low Level: V_{OL}	$I_{(COMP)}$ = 250µA			0.15	0.4	V
CURRENT SENSE						
I_{SENSE} Maximum Threshold	COMP = 2.5V, FB = 1V		197	220	243	mV
I_{SENSE} Input Current (Duty Cycle = 0%) I_{SENSE} Input Current (Duty Cycle = 80%)	COMP = 2.5V, FB = 1V (Note 4) COMP = 2.5V, FB = 1V (Note 4)			–8 –35		µA µA
OC Threshold	COMP = 2.5V, FB = 1V		98	107	116	mV
OC Input Current	(OC = 100mV)			–50	–100	nA
Default Blanking Time	COMP = 2.5V, FB = 1V, R_{BLANK} = 40k (Note 10)			180		ns
Adjustable Blanking Time	COMP = 2.5V, FB = 1V, R_{BLANK} = 120k			540		ns
V_{BLANK}				1		V
SOUT DRIVER						
SOUT Clamp Voltage	$I_{(GATE)}$ = 0µA, COMP = 2.5V, FB = 1V		10.5	12	13.5	V
SOUT Low Level	$I_{(GATE)}$ = 25mA			0.5	0.75	V
SOUT High Level	$I_{(GATE)}$ = –25mA, V_{IN} = 12V, COMP = 2.5V, FB = 1V		10			V
SOUT Active Pull-Off in Shutdown	V_{IN} = 5V, SD_V_{SEC} = 0V, SOUT = 1V		1			mA
SOUT to OUT (Rise) DELAY (t_{DELAY})	COMP = 2.5V, FB = 1V (Note 10) R_{DELAY} = 120k			40 120		ns ns
V_{DELAY}				0.9		V
OUT DRIVER						
OUT Rise Time	FB = 1V, CL = 1nF (Notes 3, 6)			50		ns
OUT Fall Time	FB = 1V, CL = 1nF (Notes 3, 6)			30		ns
OUT Clamp Voltage	$I_{(GATE)}$ = 0µA, COMP = 2.5V, FB = 1V		11.5	13	14.5	V
OUT Low Level	$I_{(GATE)}$ = 20mA $I_{(GATE)}$ = 200mA			0.45 1.25	0.75 1.8	V V
OUT High Level	$I_{(GATE)}$ = –20mA, V_{IN} = 12V, COMP = 2.5V, FB = 1V $I_{(GATE)}$ = –200mA, V_{IN} = 12V, COMP = 2.5V, FB = 1V		9.9 9.75			V V
OUT Active Pull-Off in Shutdown	V_{IN} = 5V, SD_V_{SEC} = 0V, OUT = 1V		20			mA
OUT Max Duty Cycle	COMP = 2.5V, FB = 1V, R_{DELAY} = 10k (f_{OSC} = 200kHz), V_{IN} = 10V SD_V_{SEC} = 1.4V, SS_MAXDC = V_{REF}		83	90		%
OUT Max Duty Cycle Clamp	COMP = 2.5V, FB = 1V, R_{DELAY} = 10k (f_{OSC} = 200kHz), V_{IN} = 10V SD_V_{SEC} = 1.32V, SS_MAXDC = 1.84V SD_V_{SEC} = 2.64V, SS_MAXDC = 1.84V		63.5 25	72 33	80.5 41	% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). COMP = open, FB = 1.4V, R_{OSC} = 178k, SYNC = 0V, SS_MAXDC = V_{REF}, V_{REF} = 0.1µF, SD_V_{SEC} = 2V, BLANK = 121k, DELAY = 121k, I_{SENSE} = 0V, OC = 0V, OUT = 1nF, V_{IN} = 15V, SOUT = open, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SOFT-START						
SS_MAXDC Low Level: V_{OL}	$I_{(SS\_MAXDC)}$ = 150µA, OC = 1V			0.2		V
SS_MAXDC Soft-Start Reset Threshold	Measured on SS_MAXDC			0.45		V
SS_MAXDC Active Threshold	FB = 1V, DC > 0%			0.8		V
SS_MAXDC Input Current (Soft-Start Pull-Down: Idis)	SS_MAXDC = 1V, SD_V_{SEC} = 1.4V, OC = 1V			800		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT1952/LT1952-1 are tested under pulsed load conditions such that $T_J \approx T_A$. The LT1952EGN/LT1952EGN-1 are guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT1952IGN/LT1952IGN-1 are guaranteed over the –40°C to 125°C operating junction temperature range and the LT1952MPGN/LT1952MPGN-1 are tested and guaranteed over the full –55°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: Rise and Fall times are measured at 10% and 90% levels.

Note 4: Guaranteed by correlation to static test.

Note 5: Each IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: Guaranteed but not tested.

Note 7: Maximum recommended SYNC frequency = 500kHz.

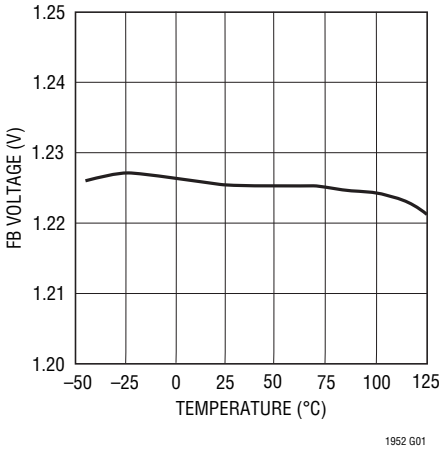
Note 8: In applications where the V_{IN} pin is supplied via an external RC network from a SYSTEM V_{IN} > 25V, an external zener with clamp voltage $V_{IN\ ON(MAX)} < V_Z < 25V$ should be connected from the V_{IN} pin to ground.

Note 9: V_{IN} start-up current is measured at $V_{IN} = V_{IN\ ON} – 0.25V$ and scaled by x 1.18 (to correlate to worst case V_{IN} start-up current at $V_{IN\ ON}$).

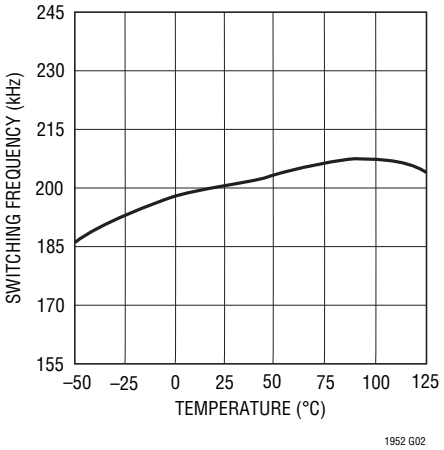
Note 10: Timing for R = 40k derived from measurement with R = 240k.

TYPICAL PERFORMANCE CHARACTERISTICS

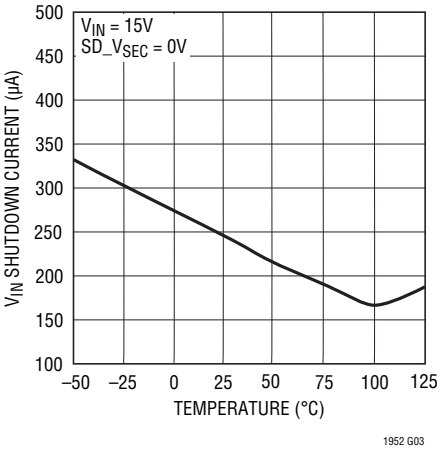
FB Voltage vs Temperature



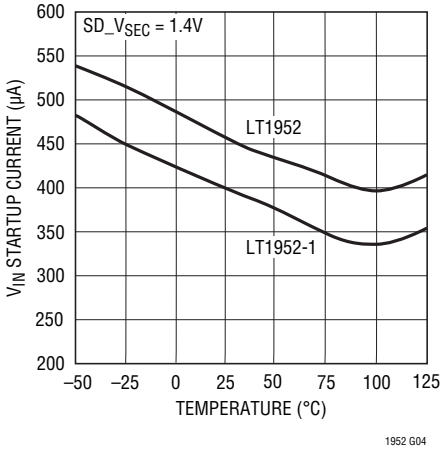
Switching Frequency vs Temperature



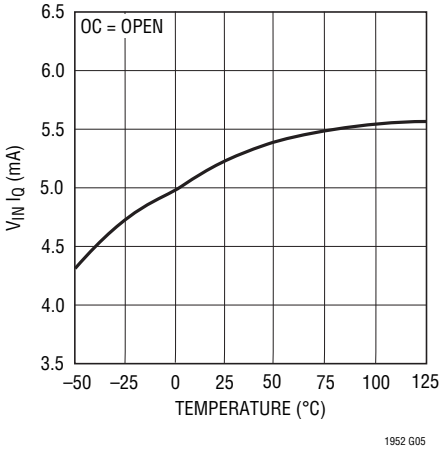
V_{IN} Shutdown Current vs Temperature



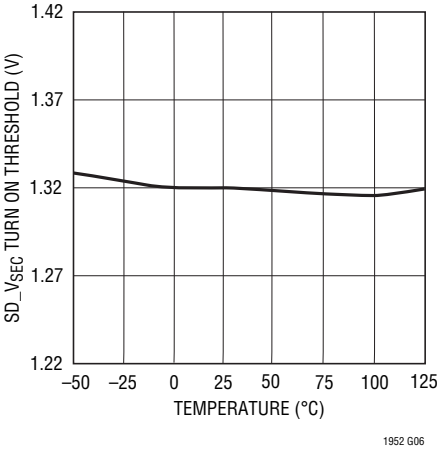
V_{IN} Start-up Current vs Temperature



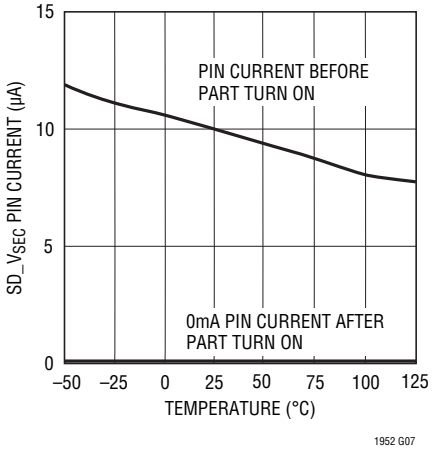
V_{IN} I_Q vs Temperature



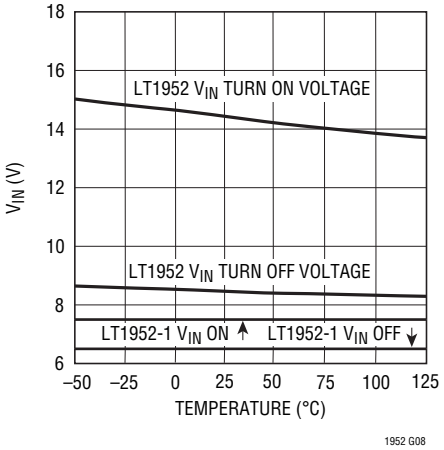
SD_V_{SEC} Turn ON Threshold vs Temperature



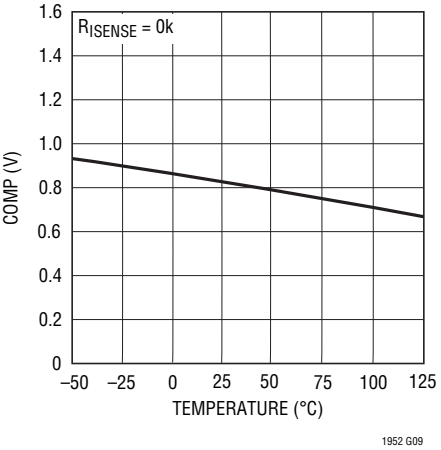
SD_V_{SEC} Pin Current vs Temperature



V_{IN} Turn ON/OFF Voltage vs Temperature

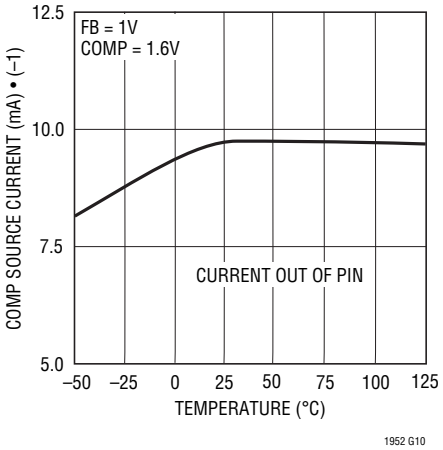


COMP Active Threshold vs Temperature

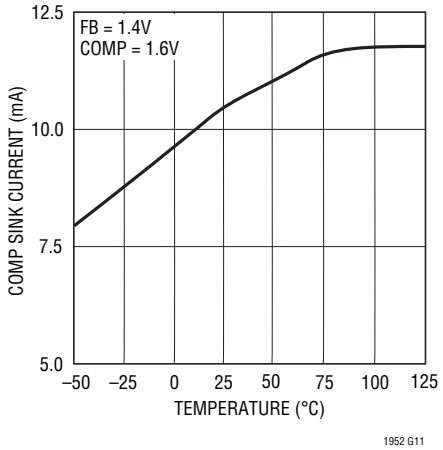


TYPICAL PERFORMANCE CHARACTERISTICS

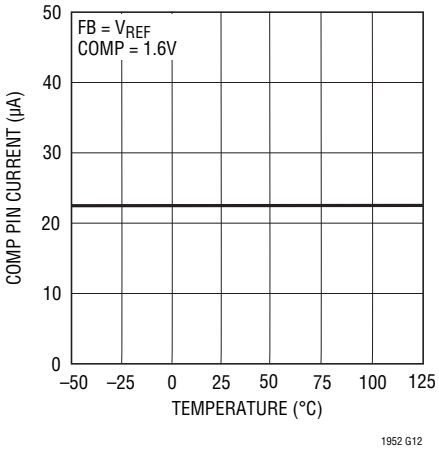
COMP Source Current vs Temperature



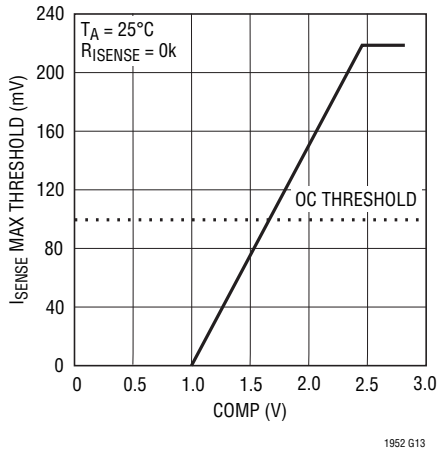
COMP Sink Current vs Temperature



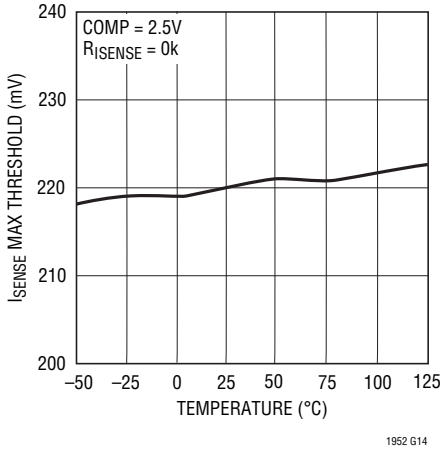
(Disabled) COMP Pin Current vs Temperature



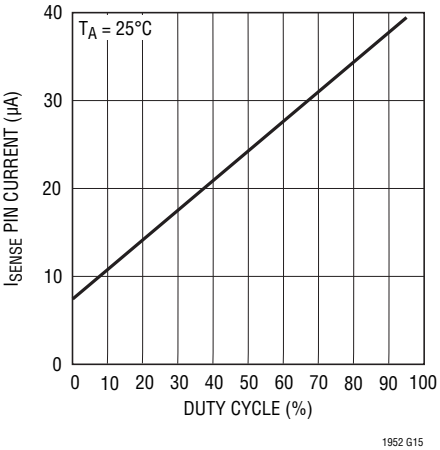
ISENSE Maximum Threshold vs COMP



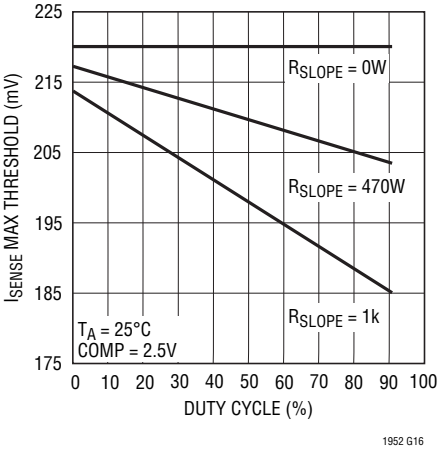
ISENSE Maximum Threshold vs Temperature



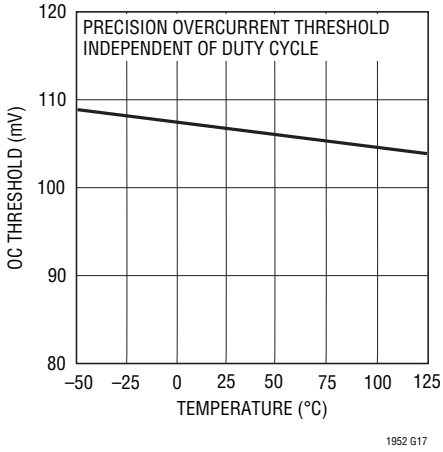
ISENSE Pin Current (Out of Pin) vs Duty Cycle



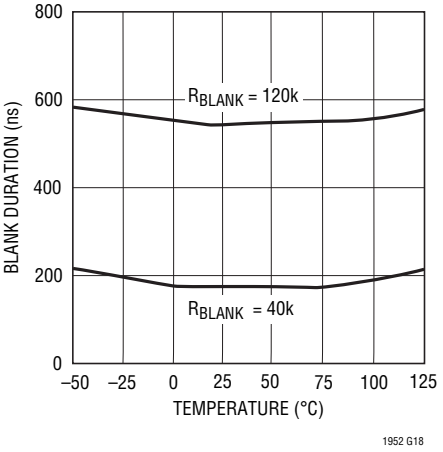
ISENSE Maximum Threshold vs Duty Cycle (Programming Slope Compensation)



OC (Overcurrent) Threshold vs Temperature

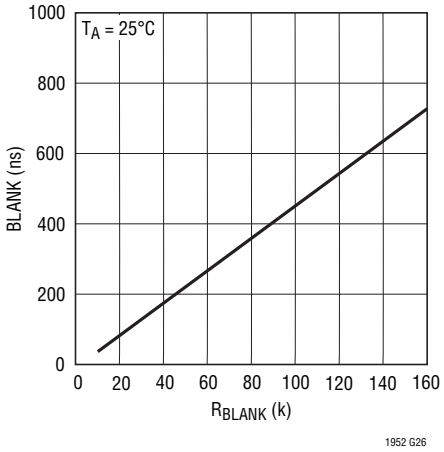


Blank Duration vs Temperature

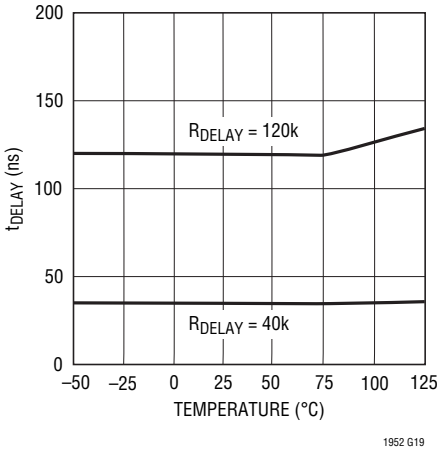


TYPICAL PERFORMANCE CHARACTERISTICS

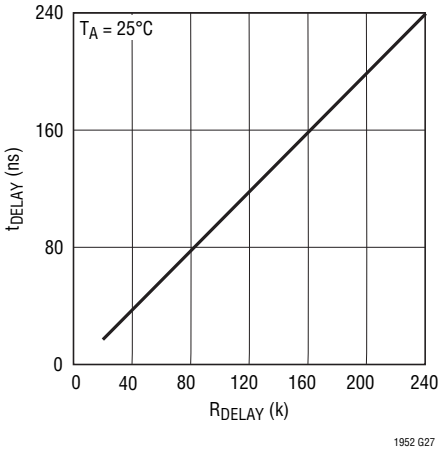
BLANK Duration vs R_{BLANK}



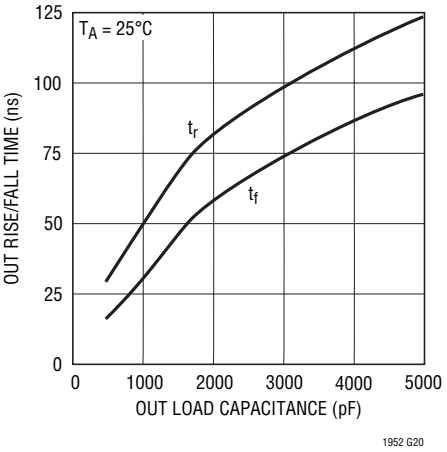
t_{DELAY}: SOUT Rise to OUT Rise vs Temperature



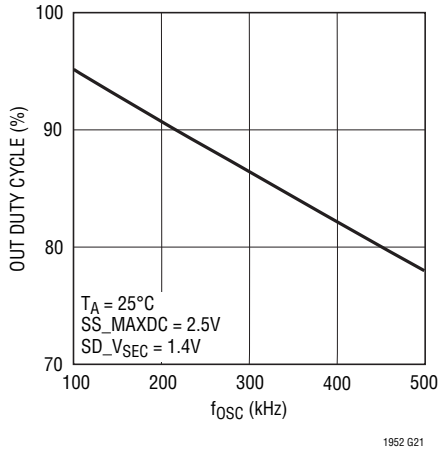
t_{DELAY}: SOUT Rise to OUT Rise vs R_{DELAY}



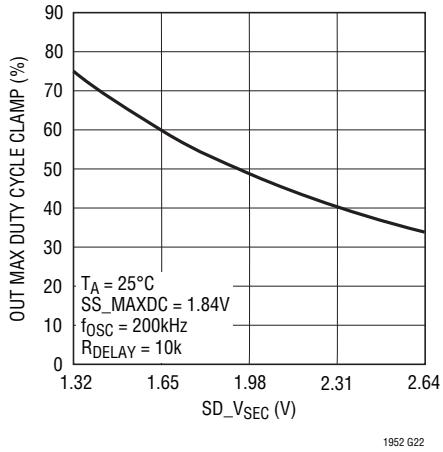
OUT Rise/Fall Time vs OUT Load Capacitance



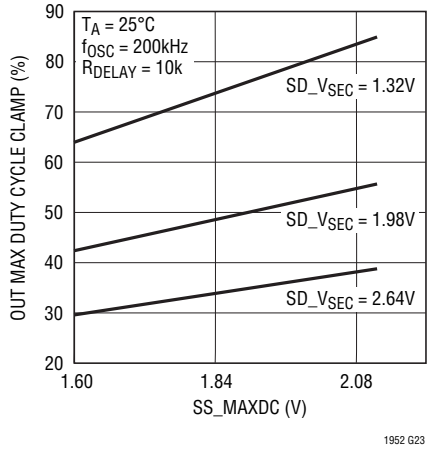
OUT: Max Duty Cycle vs f_{OSC}



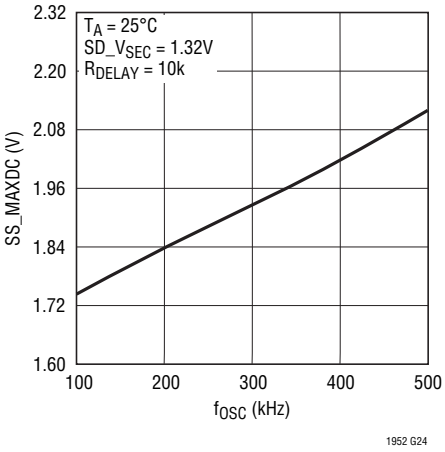
OUT: Max Duty Cycle CLAMP vs SD_V_{SEC}



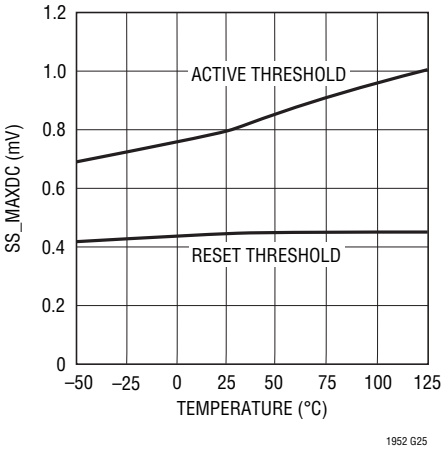
OUT: Max Duty Cycle CLAMP vs SS_MAXDC



SS_MAXDC Setting vs f_{OSC} (for OUT DC = 72%)



SS_MAXDC Reset and Active Thresholds vs Temperature



PIN FUNCTIONS

COMP (Pin 1): Output Pin of the Error Amplifier. The error amplifier is an op amp, allowing various compensation networks to be connected between the COMP pin and FB pin for optimum transient response. The voltage on this pin corresponds to the peak current of the external FET. Full operating voltage range is between 0.8V and 2.5V corresponding to 0mV to 220mV at the I_{SENSE} pin. For applications using the 100mV OC pin for overcurrent detection, typical operating range for the COMP pin is 0.8V to 1.6V. For isolated applications where COMP is controlled by an opto-coupler, the COMP pin output drive can be disabled with FB = V_{REF}, reducing the COMP pin current to (COMP – 0.7)/40k.

FB (Pin 2): Monitors the output voltage via an external resistor divider and is compared with an internal 1.23V reference by the error amplifier. FB connected to V_{REF} disables error amplifier output.

R_{OSC} (Pin 3): A resistor to ground programs the operating frequency of the IC between 100kHz and 500kHz. Nominal voltage on the R_{OSC} pin is 1.0V.

SYNC (Pin 4): Used to Synchronize the Internal Oscillator to an External Signal. It is directly logic compatible and can be driven with any signal between 10% and 90% duty cycle. If unused, the pin can be left open or connected to ground.

SS_MAXDC (Pin 5): External resistor divider from V_{REF} sets maximum duty cycle clamp (SS_MAXDC = 1.84V, SD_V_{SEC} = 1.32V gives 72% duty cycle). Capacitor on SS_MAXDC pin in combination with external resistor divider sets soft-start timing.

V_{REF} (Pin 6): The output of an internal 2.5V reference which supplies control circuitry in the IC. Capable of sourcing up to 2.5mA drive for external use. Bypass to ground with a 0.1µF ceramic capacitor.

SD_V_{SEC} (Pin 7): The SD_V_{SEC} pin, when pulled below its accurate 1.32V threshold, is used to turn off the IC and reduce current drain from V_{IN}. The SD_V_{SEC} pin is connected to system input voltage through a resistor divider to define undervoltage lockout (UVLO) and to provide a Volt-Second clamp on the OUT pin. A 10µA pin current hysteresis allows external programming of UVLO hysteresis.

GND (Pin 8): Analog Ground.

BLANK (Pin 9): A resistor to ground adjusts the extended blanking period of the overcurrent and current sense amplifier outputs during FET turn on—to prevent false current limit trip. Increasing the resistor value increases the blanking period.

I_{SENSE} (Pin 10): The Current Sense Input for the Control Loop. Connect this pin to the sense resistor in the source of the external power MOSFET. A resistor in series with the I_{SENSE} pin programs slope compensation.

OC (Pin 11): An accurate 107mV threshold, independent of duty cycle, for overcurrent detection and trigger of soft-start. Connect this pin directly to the sense resistor in the source of the external power MOSFET.

DELAY (Pin 12): A resistor to ground adjusts the delay period between SOUT rising edge and OUT rising edge. Used to maximize efficiency in forward converter applications by adjusting the control timing of secondary side synchronous rectifier MOSFETs. Increasing the resistor value increases the delay period.

PGND (Pin 13): Power Ground.

OUT (Pin 14): Drives the Gate of an N-channel MOSFET between 0V and V_{IN} with a maximum limit of 13V on OUT pin set by an internal clamp. Active pull-off exists in shutdown (see electrical specification).

V_{IN} (Pin 15): Input Supply for the Part. It must be closely decoupled to ground. An internal undervoltage lockout threshold exists for V_{IN} at approximately 14.25V on and 8.75V off for the LT1952. The LT1952-1 has lower undervoltage lockout thresholds set at 7.75V on and 6.5V off.

SOUT (Pin 16): Switched Output in Phase with OUT Pin. Provides sync signal for control of secondary side FETs in forward converter applications requiring highly efficient synchronous rectification. SOUT is actively clamped to 12V. Active pull-off exists in shutdown (see electrical specification).

TIMING DIAGRAM

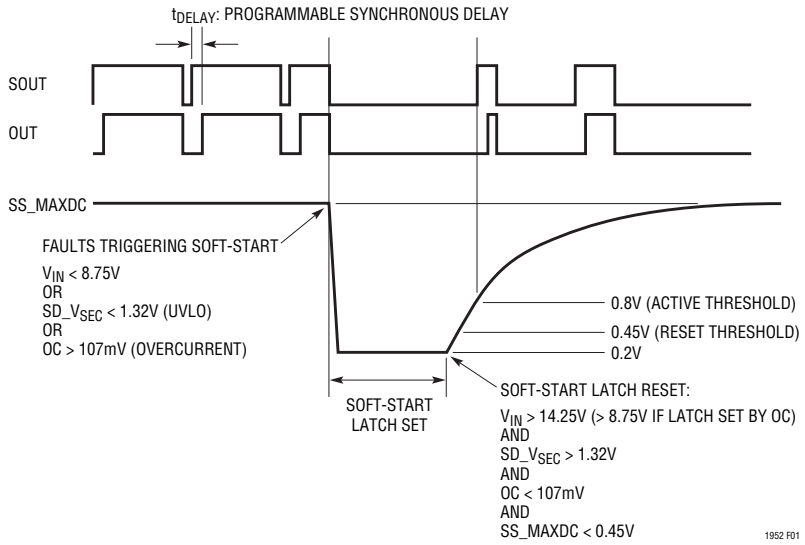


Figure 1. Timing Diagram

BLOCK DIAGRAM

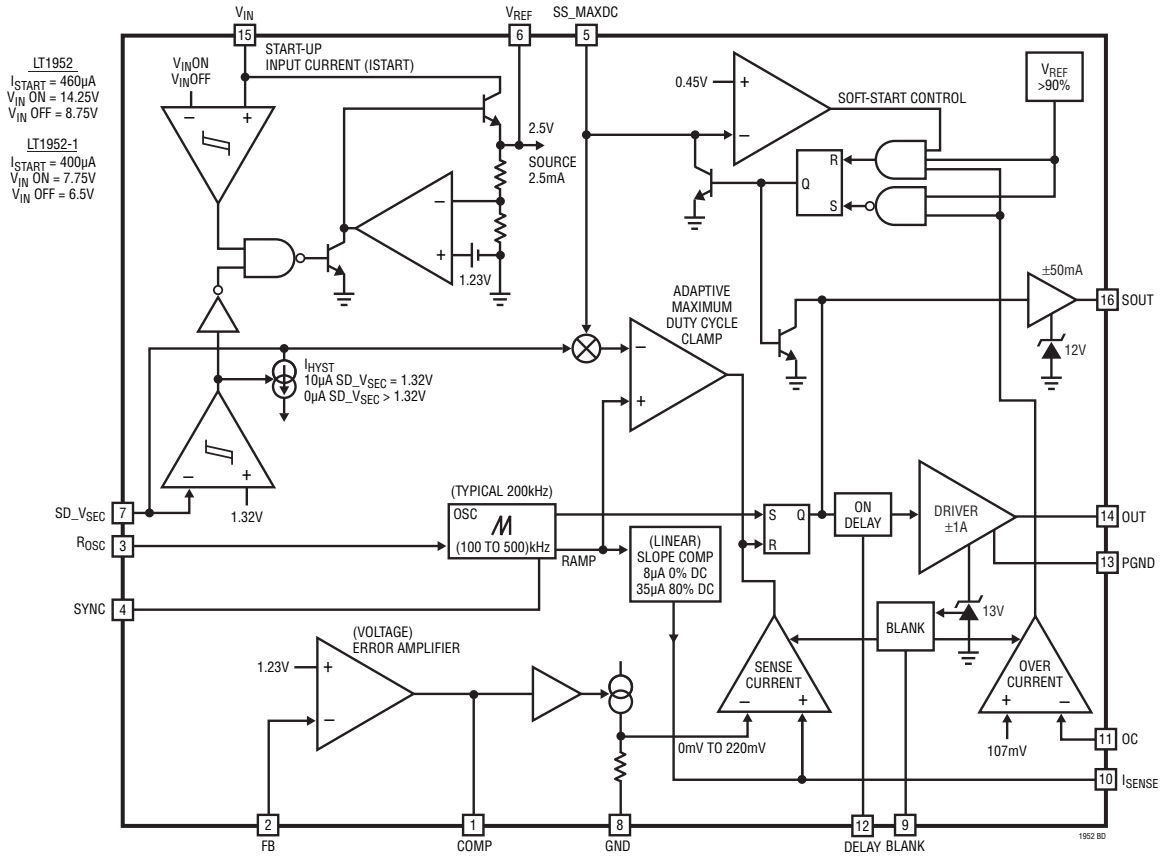


Figure 2. Block Diagram

OPERATION

Introduction

The LT1952/LT1952-1 are current mode synchronous PWM controllers optimized for control of the simplest forward converter topology—using only one primary MOSFET. The LT1952/LT1952-1 are ideal for 25W to 500W power systems where very high efficiency and reliability, low complexity and cost are required in a small space. Key features of the LT1952/LT1952-1 include an adaptive maximum duty cycle clamp for the single primary MOSFET. An additional output signal is included for synchronous rectifier control. A precision 107mV threshold senses overcurrent conditions and triggers Soft-Start for low stress short-circuit protection and control. The key functions of the LT1952/LT1952-1 are shown in the Block Diagram in Figure 2.

Part Start-up

In normal operation the SD_V_{SEC} pin must exceed 1.32V and the V_{IN} pin must exceed 14.25V (7.75V LT1952-1) to allow the part to turn on. This combination of pin voltages allows the 2.5V V_{REF} pin to become active, supplying the LT1952/LT1952-1 control circuitry and providing up to 2.5mA external drive. SD_V_{SEC} threshold can be used for externally programming an undervoltage lockout (UVLO) threshold on the system input voltage. Hysteresis on the UVLO threshold can also be programmed since the SD_V_{SEC} pin draws 11µA just before part turn on and 0µA after part turn on.

With the LT1952/LT1952-1 turned on, the V_{IN} pin can drop as low as 8.75V (6.5V LT1952-1) before part shutdown occurs. This V_{IN} pin hysteresis (5.5V LT1952; 1.25V LT1952-1) combined with low 460µA (400µA LT1952-1) start-up input current allows low power start-up using a resistor/capacitor network from system V_{IN} to supply the V_{IN} pin (Figure 3). The V_{IN} capacitor value is chosen to prevent V_{IN} falling below its turn off threshold before an auxiliary winding in the converter takes over supply to the V_{IN} pin.

Output Drivers

The LT1952/LT1952-1 have two outputs, SOUT and OUT. The OUT pin provides a ±1A peak MOSFET gate drive clamped to 13V. The SOUT pin has a ±50mA peak drive clamped to 12V and provides sync signal timing for synchronous rectification control.

For SOUT and OUT turn on, a PWM latch is set at the start of each main oscillator cycle. OUT turn on is delayed from SOUT turn on by a time t_{DELAY} (Figure 2). t_{DELAY} is programmed using a resistor from the DELAY pin to ground and is used to set the timing control of the secondary synchronous rectifiers for optimum efficiency.

SOUT and OUT turn off at the same time each cycle by one of three methods:

(1) MOSFET peak current sense at I_{SENSE} pin

(2) Adaptive maximum duty cycle clamp reached during load/line transients

(3) Maximum duty cycle reset of the PWM latch

During any of the following conditions—low V_{IN}, low SD_V_{SEC} or overcurrent detection at the OC pin—a soft-start event is latched and both SOUT and OUT turn off immediately (Figure 1).

Leading Edge Blanking

To prevent MOSFET switching noise causing premature turn off of SOUT or OUT, programmable leading edge blanking exists. This means both the current sense comparator and overcurrent comparator outputs are ignored during MOSFET turn on and for an extended period after the OUT leading edge (Figure 6). The extended blanking period is programmable by adjusting a resistor from the BLANK pin to ground.

Adaptive Maximum Duty Cycle Clamp (Volt-Second Clamp)

For forward converter applications using the simplest topology of a single MOSFET on the primary, a maximum switch duty cycle clamp which adapts to transformer input voltage is necessary for reliable control of the MOSFET. This volt-second clamp provides a safeguard for transformer reset that prevents transformer saturation. Instantaneous load changes can cause the converter loop to demand maximum duty cycle. If the maximum duty cycle of the switch is too great, the transformer reset voltage can exceed the voltage rating of the primary-side MOSFET with

OPERATION

catastrophic damage. Many converters solve this problem by limiting the operational duty cycle of the MOSFET to 50% or less—or by using a fixed (non-adaptive) maximum duty cycle clamp with very large voltage rated MOSFETs. The LT1952/LT1952-1 provide a volt-second clamp to allow MOSFET duty cycles well above 50%. This gives greater power utilization for the MOSFET, rectifiers and transformer resulting in less space for a given power output. In addition, the volt-second clamp allows a reduced voltage rating on the MOSFET resulting in lower RDS_{ON} for greater efficiency. The volt-second clamp defines a maximum duty cycle 'guard rail' which falls when system input voltage increases.

The LT1952/LT1952-1 SD_V_{SEC} and SS_MAXDC pins provide a capacitorless, programmable volt-second clamp solution. Some controllers with volt-second clamps control switch maximum duty cycle by using an external capacitor to program maximum switch ON time. Such techniques have a volt-second clamp inaccuracy directly related to the error of the external capacitor/pin capacitance and the error/drift of the internal oscillator. The LT1952/LT1952-1 use simple resistor ratios to implement a volt-second clamp without the need for an accurate external capacitor and with an order of magnitude less dependency on oscillator error.

An increase of voltage at the SD_V_{SEC} pin causes the maximum duty cycle clamp to decrease. If SD_V_{SEC} is resistively divided down from transformer input voltage, a volt-second clamp is realised. To adjust the initial maximum duty cycle clamp, the SS_MAXDC pin voltage is programmed by a resistor divider from the 2.5V V_{REF} pin to ground. An increase of programmed voltage on SS_MAXDC pin provides an increase of switch maximum duty cycle clamp.

Soft-Start

The LT1952/LT1952-1 provide true PWM soft-start by using the SS_MAXDC pin to control soft-start timing. The proportional relationship between SS_MAXDC voltage and switch maximum duty cycle clamp allows the SS_MAXDC pin to slowly ramp output voltage by ramping the maximum switch duty cycle clamp—until switch duty cycle clamp seamlessly meets the natural duty cycle of the converter.

A soft-start event is triggered whenever V_{IN} is too low, SD_V_{SEC} is too low (UVLO), or a 107mV overcurrent threshold at OC pin is exceeded. Whenever a soft-start event is triggered, switching at SOUT and OUT is stopped immediately.

The SS_MAXDC pin is discharged and only released for charging when it has fallen below it's reset threshold of 0.45V and all faults have been removed. Increasing voltage on the SS_MAXDC pin above 0.8V will increase switch maximum duty cycle. A capacitor to ground on the SS_MAXDC pin in combination with a resistor divider from V_{REF}, defines the soft-start timing.

Current Mode Topology (I_{SENSE} Pin)

The LT1952/LT1952-1 current mode topology eases frequency compensation requirements because the output inductor does not contribute to phase delay in the regulator loop. This current mode technique means that the error amplifier (nonisolated applications) or the optocoupler (isolated applications) commands current (rather than voltage) to be delivered to the output. This makes frequency compensation easier and provides faster loop response to output load transients.

A resistor divider from the application's output voltage generates a voltage at the inverting FB input of the LT1952/LT1952-1 error amplifier (or to the input of an external optocoupler) and is compared to an accurate reference (1.23V for LT1952/LT1952-1). The error amplifier output (COMP) defines the input threshold (I_{SENSE}) of the current sense comparator. COMP voltages between 0.8V (active threshold) and 2.5V define a maximum I_{SENSE} threshold from 0mV to 220mV. By connecting I_{SENSE} to a sense resistor in series with the source of an external power MOSFET, the MOSFET peak current trip point (turn off) can be controlled by COMP level and hence by the output voltage. An increase in output load current causing the output voltage to fall, will cause COMP to rise, increasing I_{SENSE} threshold, increasing the current delivered to the output. For isolated applications, the error amplifier COMP output can be disabled to allow the optocoupler to take control. Setting FB = V_{REF} disables the error amplifier COMP output, reducing pin current to (COMP – 0.7)/40k.

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Slope Compensation

The current mode architecture requires slope compensation to be added to the current sensing loop to prevent subharmonic oscillations which can occur for duty cycles above 50%. Unlike most current mode converters which have a slope compensation ramp that is fixed internally, placing a constraint on inductor value and operating frequency, the LT1952/LT1952-1 have externally adjustable slope compensation. Slope compensation can be programmed by inserting an external resistor (R_{SLOPE}) in series with the I_{SENSE} pin. The LT1952/LT1952-1 have a linear slope compensation ramp which sources current out of the I_{SENSE} pin of approximately 8µA at 0% duty cycle to 35µA at 80% duty cycle.

Overcurrent Detection and Soft-Start (OC Pin)

An added feature to the LT1952/LT1952-1 is a precise 100mV sense threshold at the OC pin used to detect overcurrent conditions in the converter and set a soft-start latch. The OC pin is connected directly to the source of the primary side MOSFET to monitor peak current in the MOSFET (Figure 7). The 107mV threshold is constant over the entire duty cycle range of the converter because it is unaffected by the slope compensation added to the I_{SENSE} pin.

Synchronizing

A SYNC pin allows the LT1952/LT1952-1 oscillator to be synchronized to an external clock. The SYNC pin can be driven from a logic level output, requiring less than 0.8V for a logic level low and greater than 2.2V for a logic level high. Duty cycle should run between 10% and 90%. To avoid loss of slope compensation during synchronization, the free running oscillator frequency (f_{OSC}) should be programmed to 80% of the external clock frequency (f_{SYNC}). The R_{SLOPE} resistor chosen for non-synchronized operation should be increased by 1.25x (= f_{SYNC}/f_{OSC}).

APPLICATIONS INFORMATION

Shutdown and Programming Undervoltage Lockout

The LT1952/LT1952-1 have an accurate 1.32V shutdown threshold at the SD_V_{SEC} pin. This threshold can be used in conjunction with a resistor divider to define the undervoltage lockout threshold (UVLO) of the system input voltage (V_S) to the power converter (Figure 3). A pin current hysteresis (10µA before part turn on, 0µA after part turn on) allows UVLO hysteresis to be programmed. Calculation of the ON/OFF thresholds for the supply (SV_{IN}) to the power converter can be made as follows:

$V_{S\ OFF}$ Threshold = 1.32[1 + (R1/R2)]

$V_{S\ ON}$ Threshold = SV_{IN} OFF + (10µA • R1)

A simple open drain transistor can be added to the resistor divider network at the SD_V_{SEC} pin to control the turn off of the LT1952/LT1952-1 (Figure 3).

The SD_V_{SEC} pin must not be left open since there must be an external source current >10µA to lift the pin past its 1.32V threshold for part turn on.

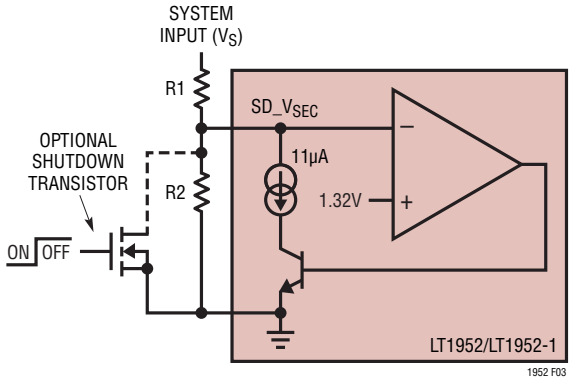

Figure 3. Programming Undervoltage Lockout (UVLO)

Micropower Start-Up: Selection of Start-Up Resistor and Capacitor for V_{IN}

The LT1952/LT1952-1 use turn-on voltage hysteresis at the V_{IN} pin and low start-up current to allow micro-power start-up (Figure 4). The LT1952/LT1952-1 monitor V_{IN} pin voltage to allow part turn on at 14.25V (7.75V LT1952-1) and part turn off at 8.75V (6.5V LT1952-1). Low start-up

APPLICATIONS INFORMATION

current (460µA LT1952; 400µA LT1952-1) allows a large resistor to be connected between system input supply and V_{IN}. Once the part is turned on, input current increases to drive the IC (4.5mA) and the output drivers (I_{DRIVE}). A large enough capacitor is chosen at the V_{IN} pin to prevent V_{IN} falling below its turn off threshold before an auxiliary winding in the converter takes over supply to V_{IN}. This technique allows a simple resistor/capacitor for start-up which draws low power from the system supply to the converter. The values for R_{START} and C_{START} are given by:

$$R_{START(MAX)} = (V_{S(MIN)} – V_{IN\ ON(max)})/I_{START(MAX)}$$

$$C_{START(MIN)} = (I_{Q(MAX)} + I_{DRIVE(MAX)}) \bullet t_{START}/V_{IN\ HYST(MIN)}$$

Example: (LT1952)

For $V_{S(MIN)}$ = 36V, $V_{IN\ ON(MAX)}$ = 15.75V, $I_{START(MAX)}$ = 700µA, $I_{Q(MAX)}$ = 5.5mA, $I_{DRIVE(MAX)}$ = 5mA, $V_{IN\ HYST(MIN)}$ = 3.75V and t_{START} = 100µs,

$$R_{START} = (36 – 15.75)/700µA = 28.9k \text{ (choose 28.7k)}$$

$$C_{START} = (5.5mA + 5mA) \bullet 100µs/3.75V = 0.28µF$$

(typically choose ≥ 1µF)

For system input voltages exceeding the absolute maximum rating of the LT1952/LT1952-1 V_{IN} pin, an external zener should be connected from the V_{IN} pin to ground. This covers the condition where V_{IN} charges past $V_{IN\ ON}$ but the part does not turn on because SD_V_{SEC} < 1.32V. In this condition V_{IN} will continue to charge towards system V_{IN}, possibly exceeding the rating for the V_{IN} pin. The zener voltage should obey $V_{IN\ ON(MAX)} < V_Z < 25V$.

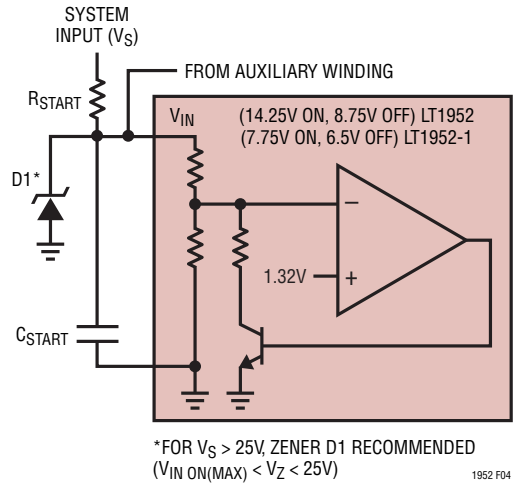

Figure 4. Low Power Start-Up

Programming Oscillator Frequency

The oscillator frequency (f_{OSC}) of the LT1952/LT1952-1 is programmed using an external resistor (R_{OSC}) connected between the R_{OSC} pin and ground. Figure 5 shows typical f_{OSC} vs R_{OSC} resistor values. The LT1952/LT1952-1 free-running oscillator frequency is programmable in the range of 100kHz to 500kHz.

Stray capacitance and potential noise pickup on the R_{OSC} pin should be minimized by placing the R_{OSC} resistor as close as possible to the R_{OSC} pin and keeping the area of the R_{OSC} node as small as possible. The ground side of the R_{OSC} resistor should be returned directly to the (analog ground) GND pin. R_{OSC} can be calculated by:

$$R_{OSC} = 9.125k\ [(4100k/f_{OSC}) – 1]$$

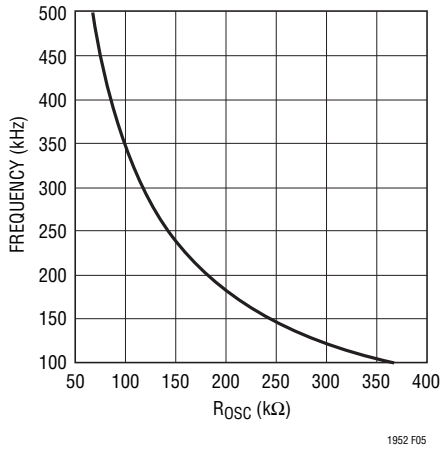

Figure 5. Oscillator Frequency (f_{OSC}) vs R_{OSC}

Programming Leading Edge Blank Time

For PWM controllers driving external MOSFETs, noise can be generated at the source of the MOSFET during gate rise time and some time thereafter. This noise can potentially exceed the OC and I_{SENSE} pin thresholds of the LT1952/LT1952-1 to cause premature turn off of SOUT and OUT in addition to false trigger of soft-start. The LT1952/LT1952-1 provide programmable leading edge blanking of the OC and I_{SENSE} comparator outputs to avoid false current sensing during MOSFET switching.

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Blanking is provided in 2 phases (Figure 6): The first phase automatically blanks during gate rise time. Gate rise times can vary depending on MOSFET type. For this reason the LT1952/LT1952-1 perform true 'leading edge blanking' by automatically blanking OC and I_{SENSE} comparator outputs until OUT rises to within 0.5V of V_{IN} or reaches its clamp level of 13V. The second phase of blanking starts after the leading edge of OUT has been completed. This phase is programmable by the user with a resistor connected from the BLANK pin to ground. Typical durations for this portion of the blanking period are from 45ns at R_{BLANK} = 10k to 540ns at R_{BLANK} = 120k. Blanking duration can be approximated as:

Blanking (extended) = $[45(R_{BLANK}/10k)]$ns

(see graph in Typical Performance Characteristics)

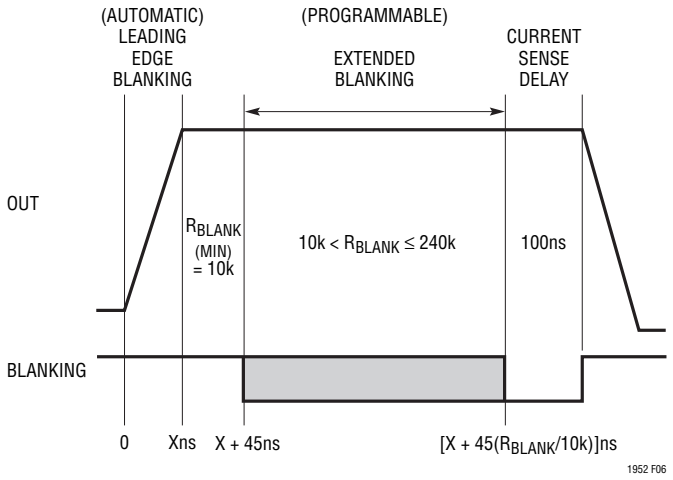

Figure 6. Leading Edge Blank Timing

Programming Current Limit (OC Pin)

The LT1952/LT1952-1 use a precise 107mV sense threshold at the OC pin to detect overcurrent conditions in the converter and set a soft-start latch. It is independent of duty cycle because it is not affected by slope compensation programmed at the I_{SENSE} pin. The OC pin monitors the peak current in the primary MOSFET by sensing the voltage across a sense resistor (R_S) in the source of the MOSFET. The current limit for the converter can be programmed by:

Current limit = $(107mV/R_S)(N_P/N_S) - (1/2)(I_{RIPPLE})$

where:

R_S = sense resistor in source of primary MOSFET

I_{RIPPLE} = p-p ripple current in the output inductor L1

N_S = number of transformer secondary turns

N_P = number of transformer primary turns

Programming Slope Compensation

The LT1952/LT1952-1 use a current mode architecture to provide fast response to load transients and to ease frequency compensation requirements. Current mode switching regulators which operate with duty cycles above 50% and have continuous inductor current must add slope compensation to their current sensing loop to prevent subharmonic oscillations. (For more information on slope compensation, see Application Note 19.) The LT1952/LT1952-1 have programmable slope compensation to allow a wide range of inductor values, to reduce susceptibility to PCB generated noise and to optimize loop bandwidth. The LT1952/LT1952-1 program slope compensation by inserting a resistor R_{SLOPE} in series with the I_{SENSE} pin (Figure 7). The LT1952/LT1952-1 generate a current at the I_{SENSE} pin which is linear from 0% duty cycle to the maximum duty cycle of the OUT pin. A simple calculation of $I(I_{SENSE}) \bullet R_{SLOPE}$ gives an added ramp to the voltage at the I_{SENSE} pin for programmable slope compensation. (See both graphs 'I_{SENSE} Pin Current vs. Duty Cycle' and 'I_{SENSE} Maximum Threshold vs Duty Cycle' in the Typical Performance Characteristics section.)

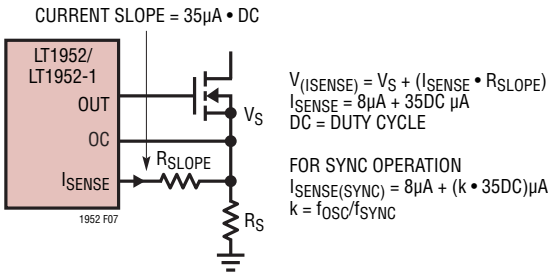

Figure 7. Programming Slope Compensation

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Programming Synchronous Rectifier Timing: SOUT to OUT delay ('t_{DELAY}')

The LT1952/LT1952-1 have an additional output SOUT which provides a ±50mA peak drive clamped to 12V. In applications requiring synchronous rectification for high efficiency, the LT1952/LT1952-1 SOUT provides a sync signal for secondary side control of the synchronous rectifier MOSFETs (Figure 11). Timing delays through the converter can cause non-optimum control timing for the synchronous rectifier MOSFETs. The LT1952/LT1952-1 provide a programmable delay (t_{DELAY}, Figure 8) between SOUT rising edge and OUT rising edge to optimize timing control for the synchronous rectifier MOSFETs to achieve maximum efficiency gains. A resistor R_{DELAY} connected from the DELAY pin to ground sets the value of t_{DELAY}. Typical values for t_{DELAY} range from 10ns with R_{DELAY} = 10k to 160ns with R_{DELAY} = 160k. (see graph in Typical Performance Characteristics)

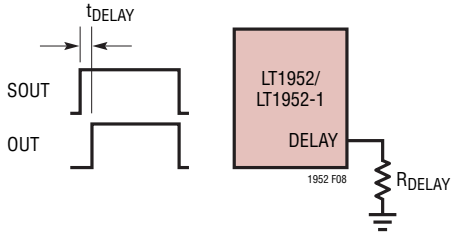

Figure 8. Programming SOUT to OUT Delay: t_{DELAY}

Programming Maximum Duty Cycle Clamp

For forward converter applications using the simplest topology of a single MOSFET on the primary, a maximum switch duty cycle clamp which adapts to transformer input voltage is necessary for reliable control of the MOSFET. This volt-second clamp provides a safeguard for transformer reset that prevents transformer saturation. The LT1952/LT1952-1 SD_V_{SEC} and SS_MAXDC pins provide a capacitor-less, programmable volt-second clamp solution using simple resistor ratios (Figure 9).

An increase of voltage at the SD_V_{SEC} pin causes the maximum duty cycle clamp to decrease. Deriving SD_V_{SEC} from a resistor divider connected to system input voltage creates the volt-second clamp. The maximum duty cycle clamp can be adjusted by programming voltage on the SS_MAXDC pin using a resistor divider from V_{REF}. An increase of voltage at the SS_MAXDC pin causes the maximum duty cycle clamp to increase.

To program the volt-second clamp, the following steps should be taken:

(1)The maximum operational duty cycle of the converter should be calculated for the given application.

(2)An initial value for the maximum duty cycle clamp should be calculated using the equation below with a first pass guess for SS_MAXDC.

Note: Since maximum operational duty cycle occurs at minimum system input voltage (UVLO), the voltage at the SD_V_{SEC} pin = 1.32V.

Max Duty Cycle Clamp (OUT pin)
= k • 0.522(SS_MAXDC(DC)/SD_V_{SEC}) – (t_{DELAY} • f_{OSC})

where,

SS_MAXDC(DC) = $V_{REF}(R_B/(R_T + R_B)$

SD_V_{SEC} = 1.32V at minimum system input voltage

t_{DELAY} = programmed delay between SOUT and OUT

k = $1.11 – 5.5e^{-7}$ • (f_{OSC})

(3) The maximum duty cycle clamp calculated in (2) should be programmed to be 10% greater than the maximum operational duty cycle calculated in (1). Simple adjustment of maximum duty cycle can be achieved by adjusting SS_MAXDC.

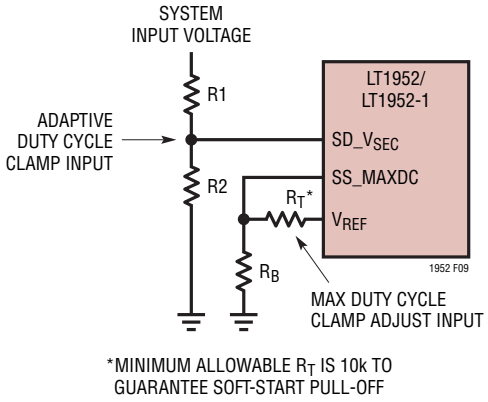

Figure 9. Programming Maximum Duty Cycle Clamp

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Example calculation for (2)

For R_T = 35.7k, R_B = 100k, V_{REF} = 2.5V, R_{DELAY} = 40k, f_{OSC} = 200kHz and SD_V_{SEC} = 1.32V, this gives SS_MAXDC(DC) = 1.84V, t_{DELAY} = 40ns and k = 1

Maximum Duty Cycle Clamp
= 1 • 0.522(1.84/1.32) – (40ns • 200kHz)
= 0.728 – 0.008 = 0.72 (Duty Cycle Clamp = 72%)

Note 1: To achieve the same maximum duty cycle clamp at 100kHz as calculated for 200kHz, the SS_MAXDC voltage should be reprogrammed by:

SS_MAXDC(DC) (100kHz)
= SS_MAXDC(DC) (200kHz) • k (200kHz)/k (100kHz)
= 1.84 • 1.0/1.055 = 1.74V (k = 1.055 for 100kHz)

Note 2 : To achieve the same maximum duty cycle clamp while synchronizing to an external clock at the SYNC pin, the SS_MAXDC voltage should be re-programmed as:

SS_MAXDC (DC) (fsync)
= SS_MAXDC (DC) (200kHz) • [(fosc/fsync) + 0.09(fosc/200kHz)0.6]

For SS_MAXDC (DC) (200kHz) = 1.84V for 72% duty cycle

SS_MAXDC (DC) (fsync = 250kHz) for 72% duty cycle
= 1.84 • [(200kHz/250kHz) + 0.09(1)0.6]
= 1.638V

Programming Soft-Start Timing

The LT1952/LT1952-1 have built-in soft-start capability to provide low stress controlled start-up from a list of fault conditions that can occur in the application (see Figure 1 and Figure 10). The LT1952/LT1952-1 provide true PWM soft-start by using the SS_MAXDC pin to control soft-start timing. The proportional relationship between SS_MAXDC voltage and switch maximum duty cycle clamp allows the SS_MAXDC pin to slowly ramp output voltage by ramping the maximum switch duty cycle clamp—until switch duty cycle clamp seamlessly meets the natural duty cycle of the converter. A capacitor C_{SS} on the SS_MAXDC pin and the resistor divider from V_{REF} used to program maximum switch duty cycle clamp, determine soft-start timing (Figure 11).

A soft-start event is triggered for the following faults:

(1) V_{IN} < 8.75V, or

(2) SD_V_{SEC} < 1.32V (UVLO), or

(3) OC > 107mV (overcurrent condition)

When a soft-start event is triggered, switching at SOUT and OUT is stopped immediately. A soft-start latch is set and SS_MAXDC pin is discharged. The SS_MAXDC pin can only recharge when the soft-start latch has been reset.

Note: A soft-start event caused by (1) or (2) above, also causes V_{REF} to be disabled and to fall to ground.

Soft-start latch reset requires all of the following:

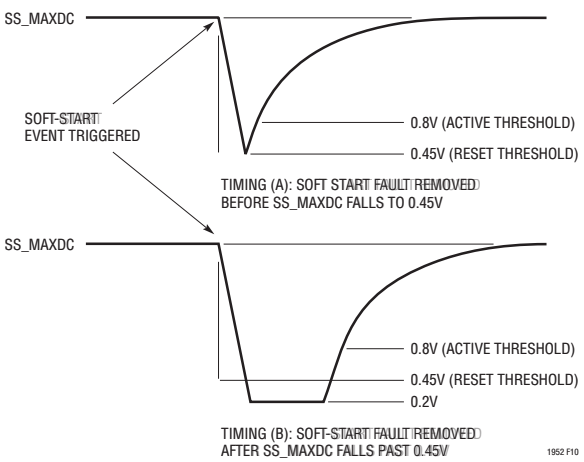
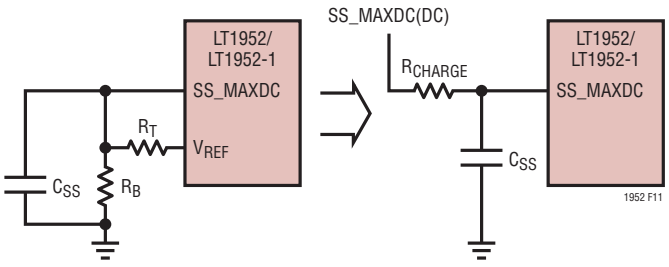


Figure 10. Soft-Start Timing



SS_MAXDC CHARGING MODEL
SS_MAXDC(DC) = V_{REF} [R_B/(R_T + R_B)]
R_{CHARGE} = [R_T • R_B/(R_T + R_B)]

Figure 11. Programming Soft-Start Timing

APPLICATIONS INFORMATION

(A) V_{IN} > 14.25* (7.75V LT1952-1), and

(B) SD_V_{SEC} > 1.32V, and

(C) OC < 107mV, and

(D) SS_MAXDC < 0.45V (SS_MAXDC reset threshold)

*V_{IN} > 8.75V (6.5V LT1952-1) is ok for latch reset if the latch was only set by overcurrent condition in (3) above.

SS_MAXDC Discharge Timing

It can be seen in Figure 10 that two types of discharge can occur for the SS_MAXDC pin. In timing (A) the fault that caused the soft-start event has been removed before SS_MAXDC falls to 0.45V. This means the soft-start latch will be reset when SS_MAXDC falls to 0.45V and SS_MAXDC will begin charging. In timing (B), the fault that caused the soft-start event is not removed until some time after SS_MAXDC has fallen past 0.45V. The SS_MAXDC pin continues to discharge to 0.2V and remains low until all faults are removed.

The time for SS_MAXDC to fall to a given voltage can be approximated as:

$$\text{SS\_MAXDC}\ (t_{FALL}) = (C_{SS}/I_{DIS}) \bullet [\text{SS\_MAXDC(DC)} - V_{SS(MIN)}]$$

where:

I_{DIS} = net discharge current on C_{SS}

C_{SS} = capacitor value at SS_MAXDC pin

SS_MAXDC(DC) = programmed DC voltage

$V_{SS(MIN)}$ = minimum SS_MAXDC voltage before recharge

$$I_{DIS} \sim 8e^{-4} + (V_{REF} - V_{SS(MIN)})[(1/2R_B) - (1/R_T)]$$

For faults arising from (1) and (2),
V_{REF} = 100mV.

For a fault arising from (3),
V_{REF} = 2.5V.

$$\text{SS\_MAXDC(DC)} = V_{REF}[R_B/(R_T + R_B)]$$

$V_{SS(MIN)}$ = SS_MAXDC reset threshold = 0.45V (if fault removed before t_{FALL})

Example:

For an overcurrent fault (OC > 100mV), V_{REF} = 2.5V, R_T = 35.7k, R_B = 100k, C_{SS} = 0.1µF and assume $V_{SS(MIN)}$ = 0.45V,

$$I_{DIS} \sim 8e^{-4} + (2.5 - 0.45)[(1/2 \bullet 100k) - (1/35.7k)] = 8e^{-4} + (2.05)(-0.23e^{-4}) = 7.5e^{-4}$$

SS_MAXDC(DC) = 1.84V

$$\text{SS\_MAXDC}\ (t_{FALL}) = (1e - 7/7.5e^{-4}) \bullet (1.84 - 0.45) = 1.85e{-}4\ \text{s}$$

If the OC fault is not removed before 185µs then SS_MAXDC will continue to fall past 0.45V towards a new $V_{SS(MIN)}$. The typical V_{OL} for SS_MAXDC at 150µA is 0.2V.

SS_MAXDC Charge Timing

When all faults are removed and the SS_MAXDC pin has fallen to its reset threshold of 0.45V or lower, the SS_MAXDC pin will be released and allowed to charge.

SS_MAXDC will rise until it settles at its programmed DC voltage—setting the maximum switch duty cycle clamp. The calculation of charging time for the SS_MAXDC pin between any two voltage levels can be approximated as an RC charging waveform using the model shown in Figure 11.

The ability to predict SS_MAXDC rise time between any two voltages allows prediction of several key timing periods:

(1)No Switching Period
(time from SS_MAXDC(DC) to $V_{SS(MIN)}$ + time from $V_{SS(MIN)}$ to $V_{SS(ACTIVE)}$)

(2)Converter Output Rise Time
(time from $V_{SS(ACTIVE)}$ to $V_{SS(REG)}$; $V_{SS(REG)}$ is the level of SS_MAXDC where maximum duty cycle clamp equals the natural duty cycle of the switch)

(3)Time For Maximum Duty Cycle Clamp within X% of Target Value

The time for SS_MAXDC to charge to a given voltage V_{SS} is found by re-arranging:

APPLICATIONS INFORMATION

$V_{SS}(t) = SS\_MAXDC(DC)\ (1 - e^{(-t/RC)})$

to give:

$t = RC \bullet (-1) \bullet \ln(1 - V_{SS}/SS\_MAXDC(DC))$

where:

V_{SS} = SS_MAXDC voltage at time t

SS_MAXDC(DC) = programmed DC voltage setting maximum duty cycle clamp = $V_{REF}(R_B/(R_T + R_B)$

$R = R_{CHARGE}$ (Figure 11) = $R_T \bullet R_B/(R_T + R_B)$

$C = C_{SS}$ (Figure 11)

Example (1) No Switching Period

The period of no switching for the converter, when a soft-start event has occurred, depends on how far SS_MAXDC can fall before recharging occurs and how long a fault exists. It will be assumed that a fault triggering soft-start is removed before SS_MAXDC can reach its reset threshold (0.45V).

No Switching Period = $t_{DISCHARGE} + t_{CHARGE}$

$t_{DISCHARGE}$ = discharge time from SS_MAXDC(DC) to 0.45V

t_{CHARGE} = charge time from 0.45V to $V_{SS(ACTIVE)}$

$t_{DISCHARGE}$ was already calculated earlier as 185µs.

t_{CHARGE} is calculated by assuming the following:

V_{REF} = 2.5V, R_T = 35.7k, R_B = 100k, C_{SS} = 0.1µF and $V_{SS(MIN)}$ = 0.45V.

$t_{CHARGE} = t(V_{SS} = 0.8V) - t(V_{SS} = 0.45V)$

Step 1:

$SS\_MAXDC(DC) = 2.5[100k/(35.7k + 100k)] = 1.84V$

$R_{CHARGE} = (35.7k \bullet 100k/135.7k) = 26.3k$

Step 2:

$t(V_{SS} = 0.45V)$ is calculated from,

$t = R_{CHARGE} \bullet C_{SS} \bullet (-1) \bullet \ln(1 - V_{SS}/SS\_MAXDC(DC))$
$= 2.63e^{4} \bullet 1e^{-7} \bullet (-1) \bullet \ln(1 - 0.45/1.84)$
$= 2.63e^{-3} \bullet (-1) \bullet \ln(0.755) = 7.3e^{-4}$ s

Step 3:

$t(V_{SS} = 0.8V)$ is calculated from:

$t = R_{CHARGE} \bullet CSS \bullet (-1) \bullet \ln(1 - V_{SS}/SS\_MAXDC(DC))$
$= 2.63e4 \bullet 1e^{-7} \bullet (-1) \bullet \ln(1 - 0.8/1.84)$
$= 2.63e{-}3 \bullet (-1) \bullet \ln(0.565) = 1.5e^{-3}$ s

From Step 1 and Step 2:

$t_{CHARGE} = (1.5 - 0.73)e^{-3}$ s = $7.7e^{-4}$ s

The total time of no switching for the converter due to a soft-start event:

$= t_{DISCHARGE} + t_{CHARGE} = 1.85e^{-4} + 7.7e^{-4} = 9.55e^{-4}$ s

Example (2) Converter Output Rise Time

The rise time for the converter output to reach regulation can be closely approximated as the time between the start of switching (SS_MAXDC = $V_{SS(ACTIVE)}$) and the time where converter duty cycle is in regulation (DC(REG)) and no longer controlled by SS_MAXDC (SS_MAXDC = $V_{SS(REG)}$). Converter output rise time can be expressed as:

Output Rise Time = $t(V_{SS(REG)}) - t(V_{SS(ACTIVE)})$

Step 1: Determine converter duty cycle DC(REG) for output in regulation.

The natural duty cycle DC(REG) of the converter depends on several factors. For this example it is assumed that DC(REG) = 60% for system input voltage near the undervoltage lockout threshold (UVLO). This gives SD_V_{SEC} = 1.32V.

Also assume that the maximum duty cycle clamp programmed for this condition is 72% for SS_MAXDC(DC) = 1.84V, f_{OSC} = 200kHz and R_{DELAY} = 40k.

Step 2: Calculate $V_{SS(REG)}$

To calculate the level of SS_MAXDC ($V_{SS(REG)}$) that no longer clamps the natural duty cycle of the converter, the equation for maximum duty cycle clamp must be used (see previous section 'Programming Maximum Duty Cycle Clamp').

The point where the maximum duty cycle clamp meets DC(REG) during soft-start is given by:

DC(REG) = Max Duty Cycle clamp

$0.6 = k \bullet 0.522(SS\_MAXDC(DC)/SD\_V_{SEC}) - (t_{DELAY} \bullet f_{OSC})$

APPLICATIONS INFORMATION

For SD_V_{SEC} = 1.32V, fOSC = 200kHz and R_{DELAY} = 40k

This gives k = 1 and t_{DELAY} = 40ns.

Re-arranging the above equation to solve for SS_MAXDC = $V_{SS(REG)}$

= [0.6 + (t_{DELAY} • f_{OSC})(SD_V_{SEC})]/(k • 0.522)
= [0.6 + (40ns • 200kHz)(1.32V)]/(1 • 0.522)
= (0.608)(1.32)/0.522 = 1.537V

Step 3: Calculate $t(V_{SS(REG)}) - t(V_{SS(ACTIVE)})$

Recall the time for SS_MAXDC to charge to a given voltage V_{SS} is given by:

$t = R_{CHARGE} \bullet C_{SS} \bullet (-1) \bullet \ln(1 - V_{SS}/SS\_MAXDC(DC))$

(Figure 11 gives the model for SS_MAXDC charging)

For R_T = 35.7k, R_B = 100k, R_{CHARGE} = 26.3k

For C_{SS} = 0.1µF, this gives $t(V_{SS(ACTIVE)})$
$= t(V_{SS(0.8V)}) = 2.63e^4 \bullet 1e^{-7} \bullet (-1) \bullet \ln(1 - 0.8/1.84)$
$= 2.63e^{-3} \bullet (-1) \bullet \ln(0.565) = 1.5e^{-3}$ s

$t(V_{SS(REG)}) = t(V_{SS(1.537V)}) = 26.3k \bullet 0.1\mu F \bullet -1 \bullet \ln(1 - 1.66/1.84) = 2.63e^{-3} \bullet (-1) \bullet \ln(0.146)$
$= 5e^{-3}$ s

The rise time for the converter output

$= t(V_{SS(REG)}) - t(V_{SS(ACTIVE)}) = (5 - 1.5)e^{-3}$ s
$= 3.5e^{-3}$ s

Example (3) Time For Maximum Duty Cycle Clamp to Reach Within X% of Target Value

A maximum duty cycle clamp of 72% was calculated previously in the section 'Programming Maximum Duty Cycle Clamp'. The programmed value used for SS_MAXDC(DC) was 1.84V.

The time for SS_MAXDC to charge from its minimum value $V_{SS(MIN)}$ to within X% of SS_MAXDC(DC) is given by:

t(SS_MAXDC charge time within X% of target)
$= t[(1 - (X/100) \bullet SS\_MAXDC(DC)] - t(V_{SS(MIN)})$

For X = 2 and $V_{SS(MIN)}$ = 0.45V, t(0.98 • 1.84) – t(0.45) = t(1.803) – t(0.45)

From previous calculations, t(0.45) = 7.3e – 4 s.

Using previous values for R_T, R_B, and C_{SS},

$t(1.803) = 2.63e^{-4} \bullet 1e^{-7} \bullet (-1) \bullet \ln(1 - 1.803/1.84)$
$= 2.63e^{-3} \bullet (-1) \bullet \ln(0.02) = 1.03e^{-2}$ s

Hence the time for SS_MAXDC to charge from its minimum reset threshold of 0.45V to within 2% of its target value is given by:

$t(1.803) - t(0.45) =$
$1.03e^{-2} - 7.3e^{-4} = 9.57e^{-3}$

Forward Converter Applications

The following section covers applications where the LT1952/LT1952-1 are used in conjunction with other LTC parts to provide highly efficient power converters using the single switch forward converter topology.

95% Efficient, 5V, Synchronous Forward Converter

The circuit in Figure 14 is based on the LT1952-1 to provide the simplest forward power converter circuit—using only one primary MOSFET. The SOUT pin of the LT1952-1 provides a synchronous control signal for the LTC1698 located on the secondary. The LTC1698 drives secondary side synchronous rectifier MOSFETs to achieve high efficiency. The LTC1698 also serves as an error amplifier and optocoupler driver.

Efficiency and transient response are shown in Figures 12 and 13. Peak efficiencies of 95% and ultra-fast transient response are superior to presently available power modules. Integrated soft-start, overcurrent detection and short-circuit hiccup mode provide low stress, reliable protection. In addition, the circuit in Figure 14 is an all-ceramic capacitor solution providing low output ripple voltage and improved reliability. The LT1952-based converter can be used to replace power module converters at a much lower cost. The LT1952 solution benefits from thermal conduction of the system board resulting in higher efficiencies and lower rise in component temperatures. The 7mm height allows dense packaging and the circuit can easily be adjusted to provide an output voltage from 1.23V to 26V. Higher currents are achievable by simple scaling of power components. The LT1952-1-based solution in Figure 14 is a powerful topology for replacement of a wide range of power modules.

APPLICATIONS INFORMATION

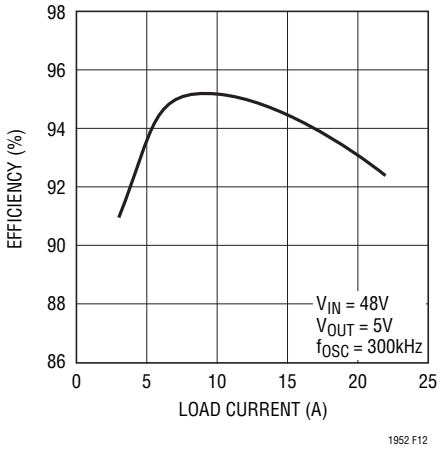


Figure 12. LT1952-Based Synchronous Forward Converter Efficiency vs Load Current (For Circuit in Figure 14)

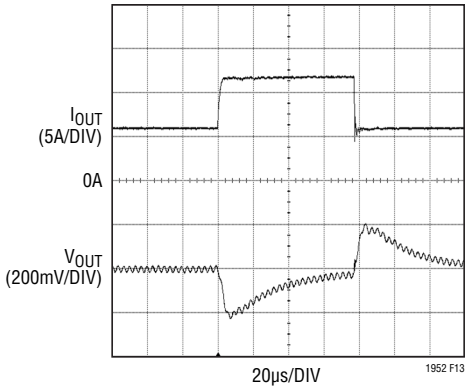


Figure 13. Output Voltage Transient Response (6A to 12A Load Step at 6A/µs)

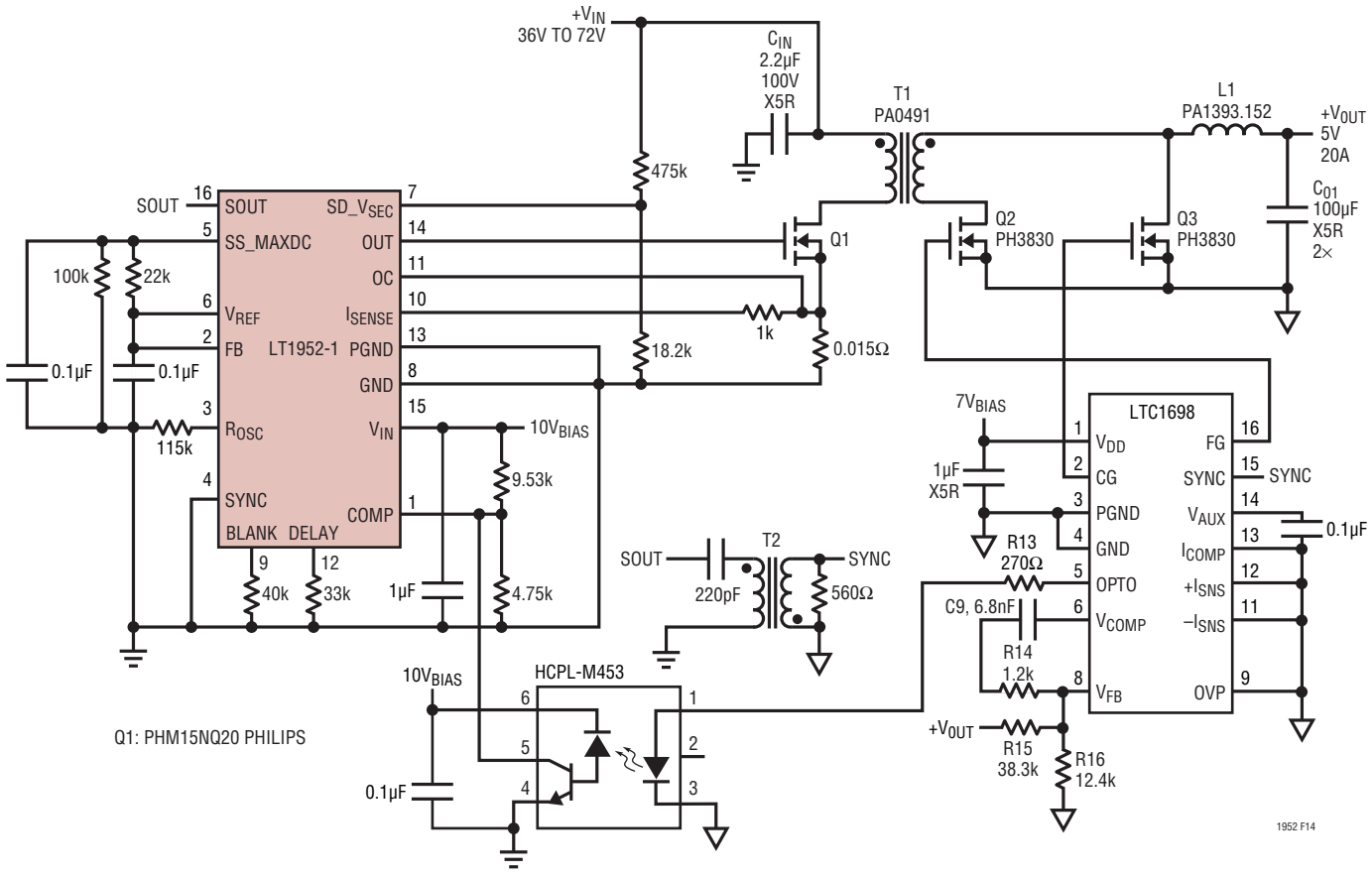


Figure 14. 36V to 72V Input to 5V at 20A Synchronous Forward Converter

APPLICATIONS INFORMATION

48V to Isolated 12V, 20A (No Opto-Coupler) 'Bus Converter'

The wide programmable range and accuracy of the LT1952/LT1952-1 Volt-Second clamp makes the LT1952/LT1952-1 an ideal choice for 'Bus Converter' applications where the Volt-Second clamp provides line regulation for the converter output. The 48V to 12V 20A 'Bus Converter' application in Figure16 shows a semi-regulated isolated output without the need for an optocoupler, optocoupler driver, reference or feedback network. Some 'Bus Converter' solutions run with a fixed 50% duty cycle resulting in an output variation of 2-to-1 for applications with a 72V to 36V input range. The LT1952/LT1952-1 use an accurate wide programmable range Volt-Second clamp to initially program and then control power supply output voltage to typically ±10% for the same 36V to 72V input range. Efficiency for the LT1952 based bus converter in Figure 16 achieves a high 94% at 20A (Figure 15). The solution is only slightly larger than 1/4 "brick" size and uses only ceramic capacitors for high reliability.

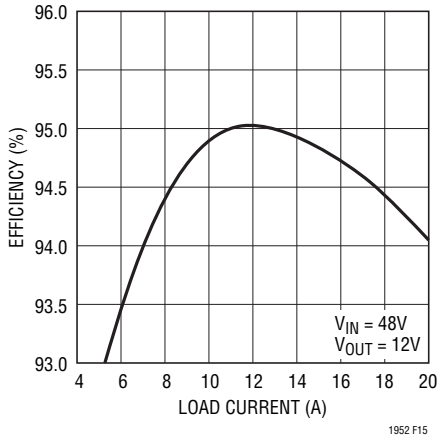


Figure 15. LT1952-Based Synchronous 'Bus Converter' Efficiency vs Load Current (For Circuit in Figure 16)

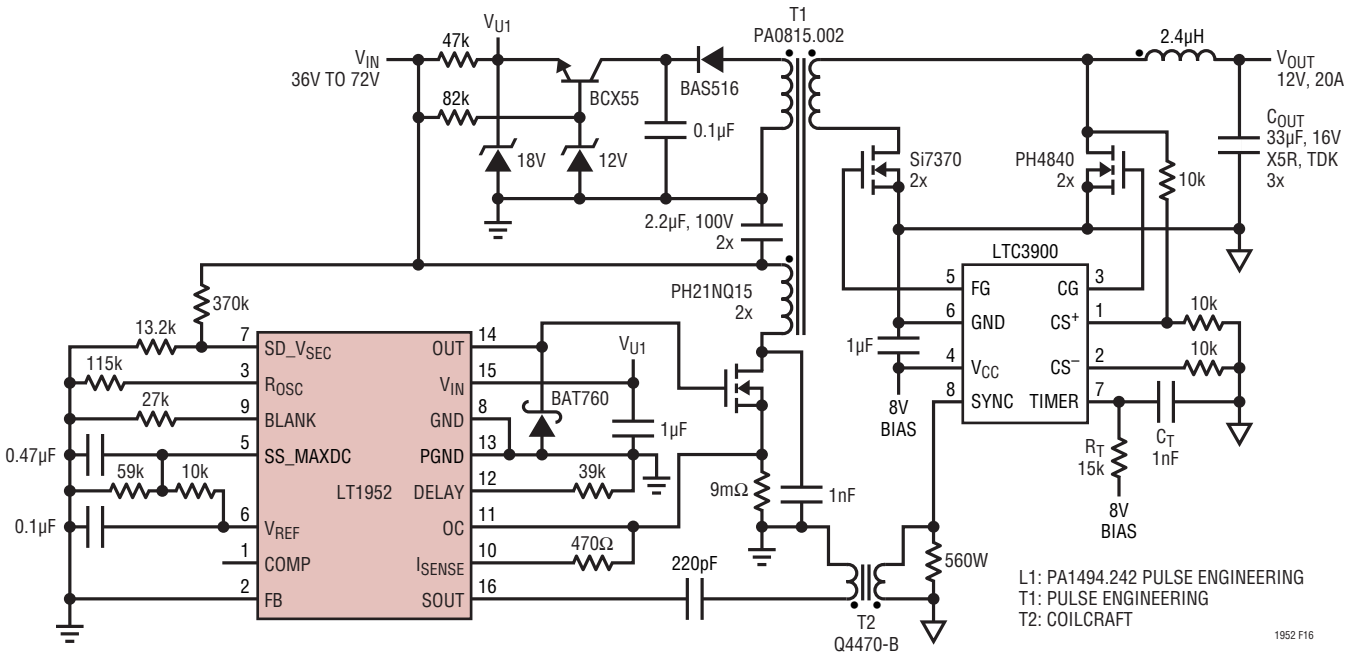


Figure 16. 36V to 72V Input to 12V at 20A No 'Optocoupler' Synchronous 'Bus Converter'

APPLICATIONS INFORMATION

36V to 72V Input, 3.3V 40A Converter

An LT1952-based synchronous forward converter provides the ideal solution for power supplies requiring high efficiency at low output voltages and high load currents. The 3.3V 40A solution in Figure 18 achieves peak efficiencies of 92.5% (Figure 17) by minimizing power loss due to rectification at the output. Synchronous rectifier control output SOUT, with programmable delay, optimizes timing control for a secondary side synchronous MOSFET controller (LTC3900) which results in high efficiency synchronous rectification. The LT1952/LT1952-1 use a precision current limit threshold at the OC pin combined with a soft-start hiccup mode to provide low stress output short-circuit protection. The maximum output current will vary only 10% over the full V_{IN} range. During short-circuit the average power dissipation of the circuit will be lower than 15% of maximum rated power thanks to a soft-start controlled hiccup mode.

This allows a significant reduction in power component sizing using the LT1952-based converter.

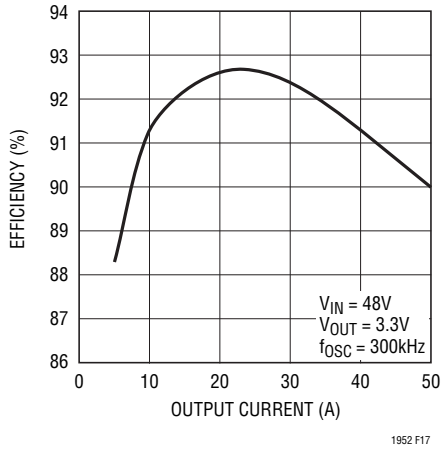


Figure 17. LT1952-Based Synchronous Forward Converter Efficiency vs Load Current (For Circuit in Figure 18)

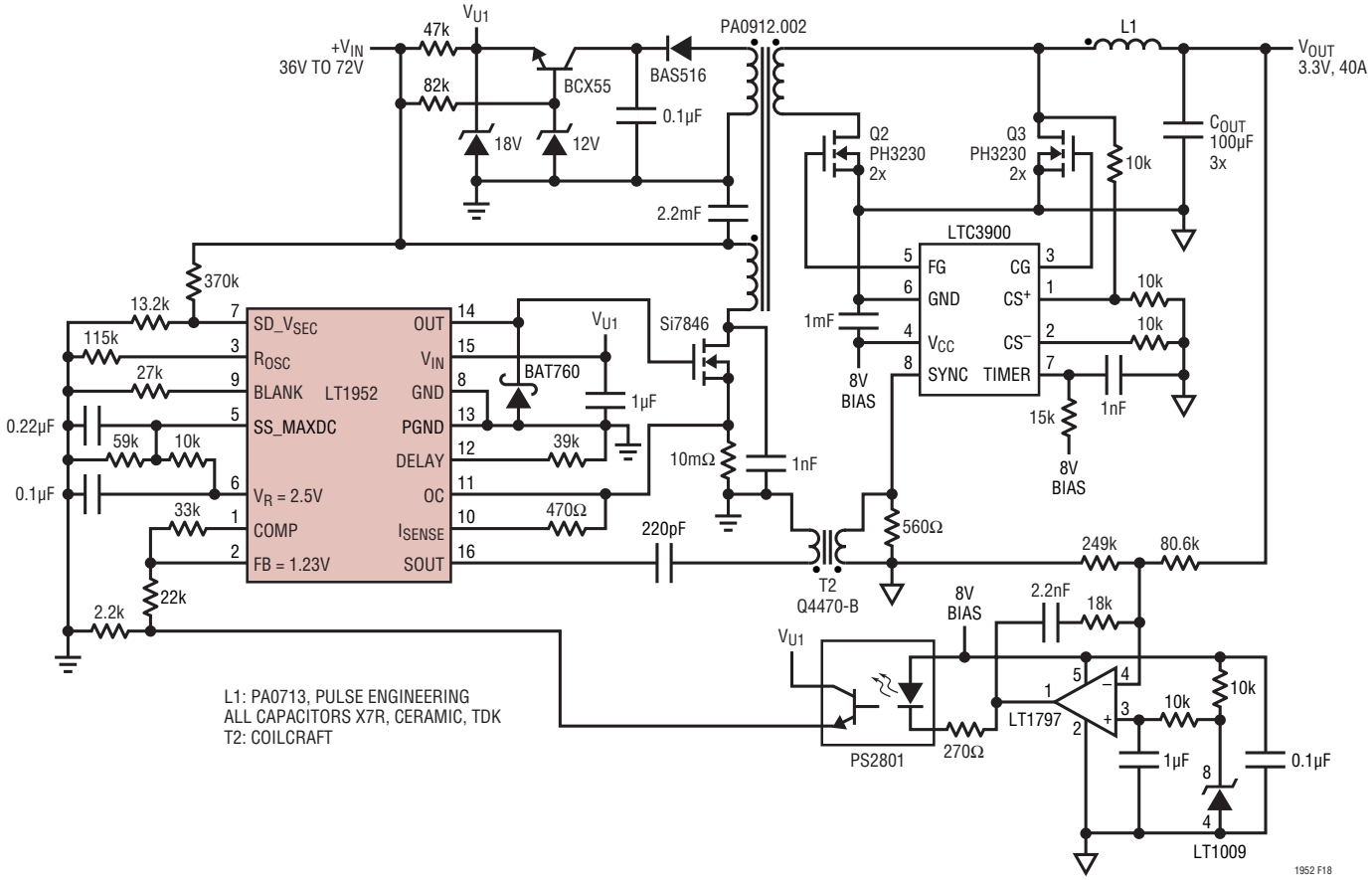


Figure 18. 36V to 72V, 3.3V at 40A Synchronous Forward Converter

APPLICATIONS INFORMATION

Bus Converter: Optimum Output Voltage Tolerance

The Bus Converter applications shown on page 1 and in Figure 16, provide semi-regulated isolated outputs without the need for an optocoupler, optocoupler driver, reference or feedback network. The LT1952/LT1952-1Volt-Second clamp adjusts switch duty cycle inversely proportional to input voltage to provide an output voltage that is regulated against input line variations. Some bus converters use a switch duty cycle limit which causes output voltage variation of typically ±33% over a 2:1 input voltage range. The LT1952/LT1952-1 typically provide a ±10% output variation for the same input variation. Typical output tolerance is further improved for the LT1952 by inserting a resistor from the system input voltage to the SS_MAXDC pin (Rx in Figure 19).

The LT1952/LT1952-1 electrical specifications for the OUT Max Duty Cycle Clamp show typical switch duty cycle to move from 72% to 33% for a 2x change of input voltage (SS_MAXDC pin = 1.84V). Since output voltage regulation follows V_{IN} • Duty Cycle, a switch duty cycle change of 72% to 36% (for a 2x input voltage change) provides minimal output voltage variation for the LT1952/LT1952-1 bus converter. To achieve this, an SS_MAXDC pin voltage increase of 1.09x (36/33) would be required at high input line. A resistor Rx inserted between the SS_MAXDC pin and system input voltage (Figure 19) increases SS_MAXDC voltage as input voltage increases, minimizing output voltage variation over a 2:1 input voltage change.

The following steps determine values for Rx, R_T and R_B:

(1)Program switch duty cycle at minimum system input voltage ($V_{S(MIN)}$)

(a)$R_{T(1)}$ = 10k (minimum allowed to still guarantee soft-start pull-down)

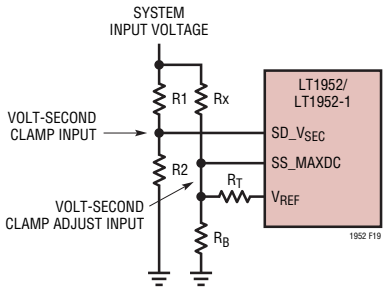


Figure 19. Optimal Programming of Maximum Duty Cycle Clamp for Bus Converter Applications (Adding Rx)

(b)Select switch duty cycle for the Bus Converter for a given output voltage at $V_{S(MIN)}$ and calculate SS_MAXDC voltage (SS1) (See Applications Information "Programming Maximum Duty Cycle Clamp")

(c)Calculate $R_{B(1)} = [SS1/(2.5 – SS1)] • R_{T(1)}$

(2)Calculate Rx:

$Rx = ([V_{S(MAX)} – V_{S(MIN)}]/[SS1 • (X – 1)]) • R_{THEV(1)}$

$R_{THEV(1)} = R_{B(1)} • R_{T(1)}/(R_{B(1)} + R_{T(1)})$, X = ideal duty cycle ($V_{S(MAX)}$)/actual duty cycle ($V_{S(MAX)}$)

(3)The addition of Rx causes an increase in the original programmed SS_MAXDC voltage SS1. A new value for $R_{B(1)}$ should be calculated to provide a lower SS_MAXDC voltage (SS2) to correct for this offset:

(a)$SS2 = SS1 – [(V_{S(MIN)} – SS1) • R_{THEV(1)}/Rx]$

(b)$R_{B(2)} = [SS2/(2.5 – SS2)] • R_{T(1)}$

(4)The thevinin resistance $R_{THEV(1)}$ used to calculate Rx should be re-established for R_T and R_B:

(a) R_B (final value) = $R_{B(2)} • (R_{THEV(1)}/R_{THEV(2)})$
(b) R_T (final value) = $R_{T(1)} • (R_{THEV(1)}/R_{THEV(2)})$
where $R_{THEV(2)} = R_{B(2)} • R_{T(1)}/(R_{B(2)} + R_{T(1)})$

Example:

For a Bus Converter running from 36V to 72V input, $V_{S(MIN)}$ = 36V, $V_{S(MAX)}$ = 72V.

choose $R_{T(1)}$ = 10k, SS_MAXDC = SS1 = 1.84V (for 72% duty cycle at $V_{S(MIN)}$ = 36V)

$R_{B(1)} = [1.84V/(2.5V – 1.84V)] • 10k = 28k$

$R_{THEV(1)} = [28k • 10k/(28k + 10k)] = 7.4k$

SS_MAXDC correction = 36%/33% = 1.09

$Rx = [(72V – 36V)/(1.84 • 0.09)] • 7.4k = 1.6M$

$SS2 = 1.84 – [(36V – 1.84) • 7.4k/1.6M] = 1.682V$

$R_{B(2)} = [1.682/(2.5 – 1.682)] • 10k = 20.6k$

$R_{THEV(2)} = [20.6k • 10k/(20.6k + 10k)] = 6.7k$

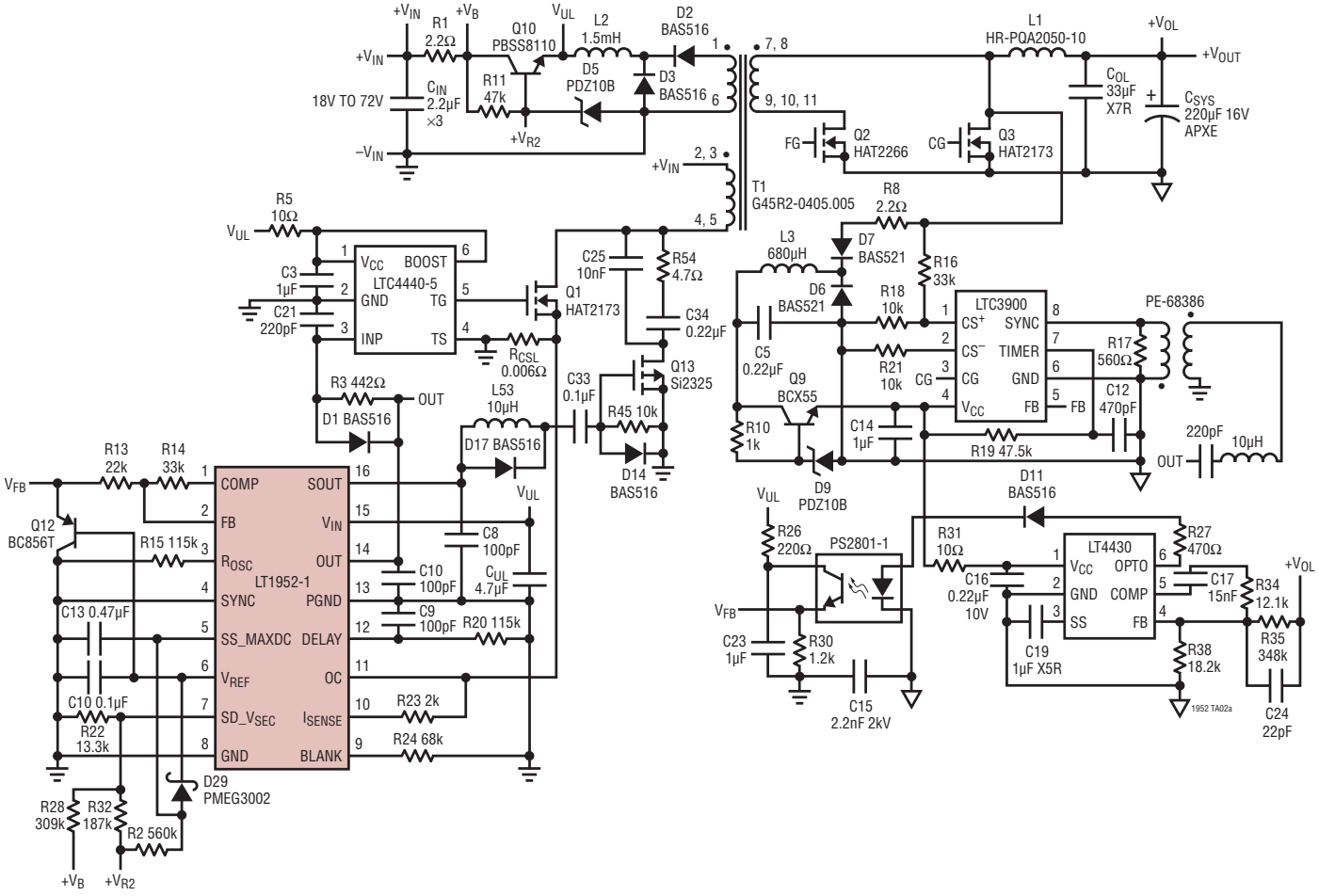
$R_{THEV(1)}/R_{THEV(2)} = 7.4k/6.7k = 1.104$

R_B (final value) = 20.6k • 1.104 = 22.7k (choose 22.6k)

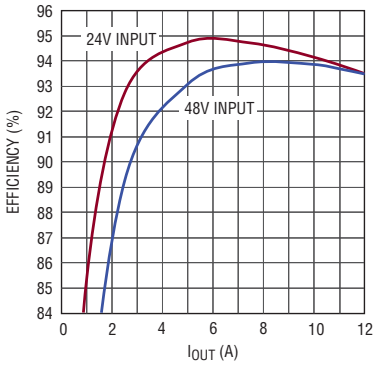
R_T (final value) = 10k • 1.104 = 11k

TYPICAL APPLICATIONS

Wide 18V to 72V Input, High Efficiency, 12V at 12A Output, Active Reset Forward Converter Fits in One-Eighth Brick Footprint

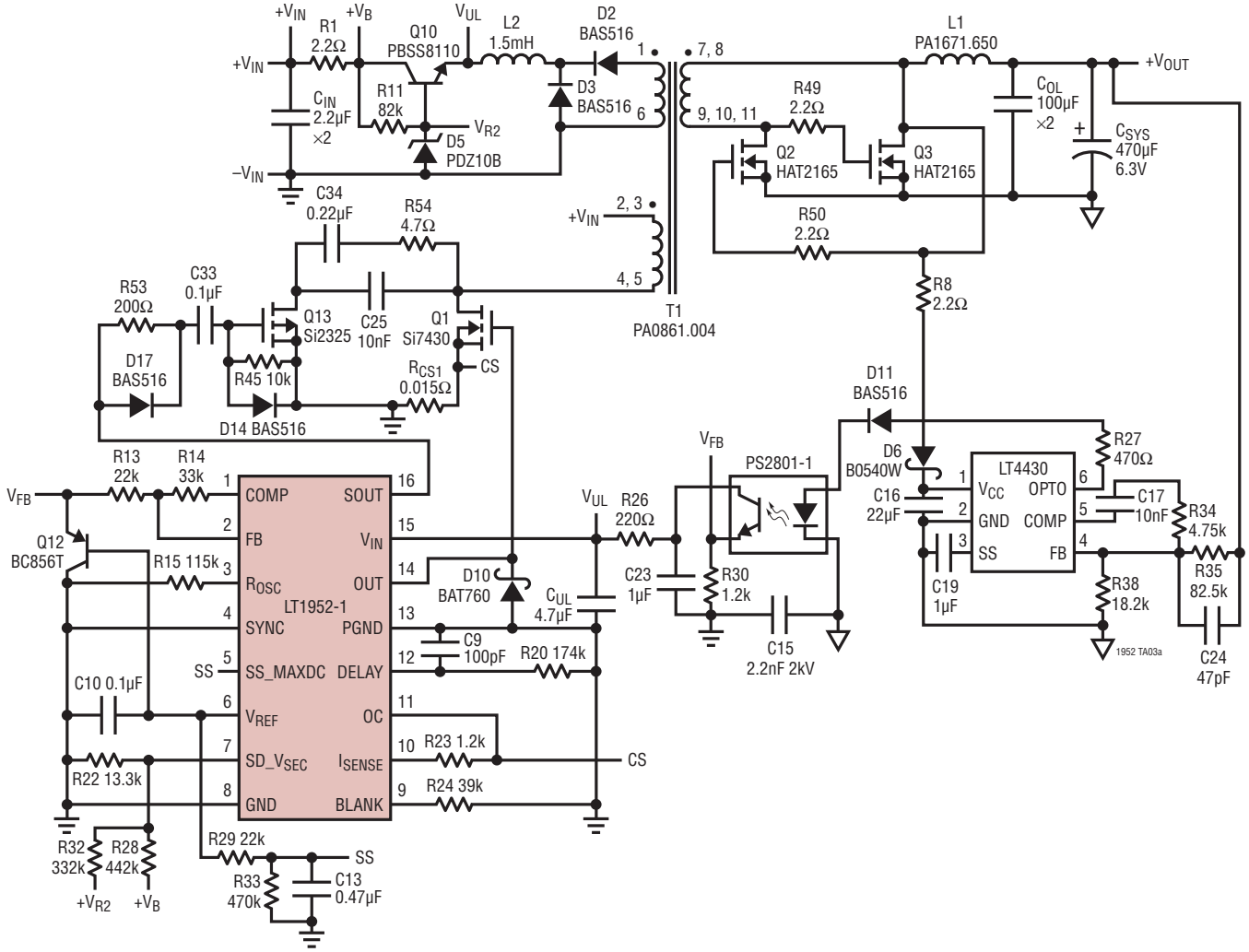


The 12V Output Converter Fits in a One-Eighth "Brick" Footprint and Has a Very High Efficiency Over 18V to 72V Input Voltage Range

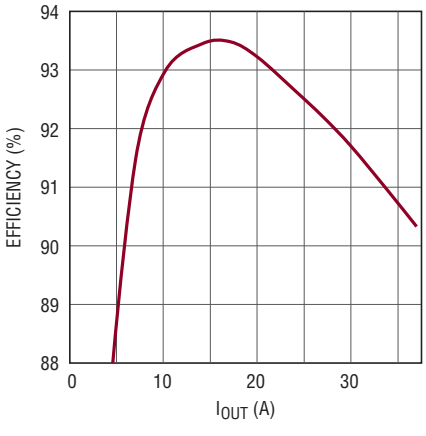


TYPICAL APPLICATIONS

High Efficiency 36V to 72V Input to 3.3V at 30A Output, Active Reset Forward Converter Fits in One-Eighth Brick Footprint



The High Efficiency of 3.3V Output Converter Allows Tight PCB Layout and Results in Low Component Temperature Rises

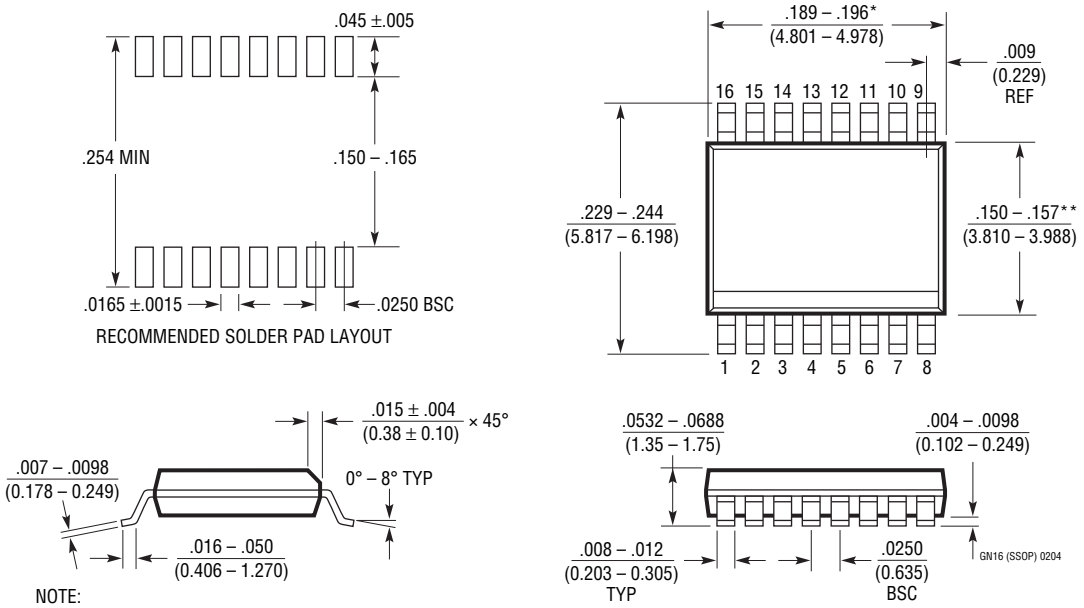


(Revision history begins at Rev E)

REV	DATE	DESCRIPTION	PAGE NUMBER
E	5/11	MP-grade parts added, changes reflected throughout the data sheet	1-28

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®3900	Synchronous Rectifier N-Channel MOSFET Driver for Forward Converters	Programmable Timeout and Reverse Inductor Current Protection, Transformer Synchronization, SSOP-16
LT4430	Secondary-Side Opto-Coupler Driver with Reference Voltage	Overshoot Control Prevents Output Overshoot During Start-up and Short-Circuit Recovery
LTC3726/LTC3725	Isolated Synchronous No Opto Forward Controller Chip Set	Ideal for Medium Power 24V or 48V Input Applications
LTC3705/LTC3726	2-Switch Synchronous Forward No Opto Isolated Controller Chip Set	Self-Starting Architecture Eliminates Need for a Bias Voltage on Primary Side
LTC3722/LTC2722-2	Synchronous Isolated Full-Bridge Controllers with Zero Voltage Switching	Ideal for High Power 24V or 48V Input Applications
LTC3723-1/LTC3723-2	Synchronous Push-Pull and Full-Bridge Controllers	High Efficiency with On-Chip MOSFET Drivers
LTC3721-1/LTC3721-2	Non-Synchronous Push-Pull and Full-Bridge Controllers	Minimizes External Components, On-Chip MOSFET Drivers
LT3748	100V No Opto Flyback Controller	$5V \le V_{IN} \le 100V$, Boundary Mode Operation, MSOP-16 with Extra High Voltage Pin Spacing
LTC3803/LTC3803-3/ LTC3803-5	Flyback DC/DC Controllers with Fixed 200kHz or 300kHz Operating Frequency	V_{IN} and V_{OUT} Limited Only by External Components, 6-Pin ThinSOT™ Package

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