

LT1638/LT1639

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	44V	Specified Temperature Range (Note 4)	
Input Differential Voltage.....	44V	LT1638C/LT1639C	-40°C to 85°C
Input Current.....	±25mA	LT1638I/LT1639I	-40°C to 85°C
Output Short-Circuit Duration (Note 2)	Continuous	LT1638H/LT1639H	-40°C to 125°C
Operating Temperature Range (Note 3)		Junction Temperature	150°C
LT1638C/LT1639C	-40°C to 85°C	DD Package	125°C
LT1638I/LT1639I	-40°C to 85°C	Storage Temperature Range.....	-65°C to 150°C
LT1638H/LT1639H	-40°C to 125°C	DD Package	-65°C to 125°C
		Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION

TOP VIEW MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 273^{\circ}\text{C/W}$	TOP VIEW N8 PACKAGE S8 PACKAGE 8-LEAD PDIP 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 150^{\circ}\text{C/W}$ (N8) $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 190^{\circ}\text{C/W}$ (S8)
TOP VIEW DD PACKAGE 8-LEAD (3mm × 3mm) PLASTIC DFN $T_{JMAX} = 125^{\circ}\text{C}$, $\theta_{JA} = 43^{\circ}\text{C/W}$ UNDERSIDE METAL INTERNALLY CONNECTED TO V^-	TOP VIEW N PACKAGE S PACKAGE 14-LEAD PDIP 14-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$ (N) $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 160^{\circ}\text{C/W}$ (S)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1638CMS8#PBF	LT1638CMS8#TRPBF	LTCY	8-Lead Plastic MSOP	–40°C to 85°C
LT1638IMS8#PBF	LT1638IMS8#TRPBF	LTCY	8-Lead Plastic MSOP	–40°C to 85°C
LT1638CDD#PBF	LT1638CDD#TRPBF	LAAL	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT1638IDD#PBF	LT1638IDD#TRPBF	LAAL	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LT1638CN8#PBF	LT1638CN8#TRPBF	LT1638CN8	8-Lead PDIP	–40°C to 85°C
LT1638IN8#PBF	LT1638IN8#TRPBF	LT1638IN8	8-Lead PDIP	–40°C to 85°C
LT1638CS8#PBF	LT1638CS8#TRPBF	1638	8-Lead Plastic SO	–40°C to 85°C
LT1638IS8#PBF	LT1638IS8#TRPBF	1638I	8-Lead Plastic SO	–40°C to 85°C
LT1638HS8#PBF	LT1638HS8#TRPBF	1638H	8-Lead Plastic SO	–40°C to 125°C
LT1639CN#PBF	LT1639CN#TRPBF	LT1639CN	14-Lead PDIP	–40°C to 85°C
LT1639IN#PBF	LT1639IN#TRPBF	LT1639IN	14-Lead PDIP	–40°C to 85°C
LT1639CS#PBF	LT1639CS#TRPBF	LT1639CS	14-Lead Plastic SO	–40°C to 85°C
LT1639IS#PBF	LT1639IS#TRPBF	LT1639IS	14-Lead Plastic SO	–40°C to 85°C
LT1639HS#PBF	LT1639HS#TRPBF	LT1639HS	14-Lead Plastic SO	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.
 $V_S = 3\text{V}, 0\text{V}$; $V_S = 5\text{V}, 0\text{V}$; $V_{CM} = V_{OUT} = \text{half supply}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1638C/LT1639C, LT1638I/LT1639I			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1638 N, S Packages $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	200	600 850 950	μV μV μV
		LT1639 N, S Packages $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	300	700 950 1050	μV μV μV
		LT1638 MS8 Package $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	350	900 1150 1450	μV μV μV
		LT1638 DD Package $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	400	1100 1350 1450	μV μV μV
	Input Offset Voltage Drift (Note 9)	LT1638/LT1639 N, S Packages	●	2	6	$\mu\text{V}/^\circ\text{C}$
		LT1638MS8, LT1638DD	●	2.5	7	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current	$V_{CM} = 44\text{V}$ (Note 5)	● ●	1	6 2.5	nA μA
I_B	Input Bias Current	$V_{CM} = 44\text{V}$ (Note 5)	●	20	50	nA
		$V_S = 0\text{V}$	●	8	30	μA
				0.1		nA
	Input Noise Voltage	0.1Hz to 10Hz		1		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$		20		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$		0.3		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential		1	2.5	$\text{M}\Omega$
		Common Mode, $V_{CM} = 0\text{V}$ to 44V		1.4	5.5	$\text{M}\Omega$
C_{IN}	Input Capacitance			5		pF
	Input Voltage Range		●	0	44	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0\text{V}$ to $V_{CC} - 1\text{V}$	●	88	98	dB
		$V_{CM} = 0\text{V}$ to 44V (Note 8)	●	80	88	dB
A_{VOL}	Large-Signal Voltage Gain	$V_S = 3\text{V}$, $V_O = 500\text{mV}$ to 2.5V , $R_L = 10\text{k}$	●	200	1500	V/mV
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	133		V/mV
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	100		V/mV
		$V_S = 5\text{V}$, $V_O = 500\text{mV}$ to 4.5V , $R_L = 10\text{k}$	●	400	1500	V/mV
V_{OL}	Output Voltage Swing Low	$V_S = 3\text{V}$, No Load	●	3	8	mV
		$V_S = 3\text{V}$, $I_{SINK} = 5\text{mA}$	●	250	450	mV
		$V_S = 5\text{V}$, No Load	●	3	8	mV
		$V_S = 5\text{V}$, $I_{SINK} = 10\text{mA}$	●	500	700	mV
V_{OH}	Output Voltage Swing High	$V_S = 3\text{V}$, No Load	●	2.94	2.98	V
		$V_S = 3\text{V}$, $I_{SOURCE} = 5\text{mA}$	●	2.25	2.40	V
		$V_S = 5\text{V}$, No Load	●	4.94	4.98	V
		$V_S = 5\text{V}$, $I_{SOURCE} = 10\text{mA}$	●	3.8	4.0	V
I_{SC}	Short-Circuit Current (Note 2)	$V_S = 3\text{V}$, Short to GND		10	15	mA
		$V_S = 3\text{V}$, Short to V_{CC}		15	25	mA
		$V_S = 5\text{V}$, Short to GND		15	20	mA
		$V_S = 5\text{V}$, Short to V_{CC}		15	25	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.
 $V_S = 3\text{V}$, 0V ; $V_S = 5\text{V}$, 0V ; $V_{CM} = V_{OUT} = \text{half supply}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LT1638C/LT1639C, LT1638I/LT1639I MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V}$ to 12.5V , $V_{CM} = V_O = 1\text{V}$	●	90	100		dB
	Reverse Supply Voltage	$I_S = -100\mu\text{A}$ per Amplifier	●	18	27		V
	Minimum Operating Supply Voltage		●		2.4	2.7	V
I_S	Supply Current per Amplifier (Note 6)		●		170	230 275	μA μA
GBW	Gain Bandwidth Product (Note 5)	$f = 5\text{kHz}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	650 550 500	1075		kHz kHz kHz
SR	Slew Rate (Note 7)	$A_V = -1$, $R_L = \infty$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	0.210 0.185 0.170	0.38		V/ μs V/ μs V/ μs

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.
 $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LT1638C/LT1639C, LT1638I/LT1639I MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1638 N, S Packages $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●		250	800 1000 1100	μV μV μV
		LT1639 N, S Packages $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●		350	900 1100 1200	μV μV μV
		LT1638 MS8 Package $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●		400	1050 1250 1550	μV μV μV
		LT1638 DDPackage $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●		450	1250 1450 1550	μV μV μV
	Input Offset Voltage Drift (Note 9)	LT1638/LT1639 N, S Packages LT1638MS8, LT1638DD	● ●		2 2.5	6 7	$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		●		1	6	nA
I_B	Input Bias Current		●		20	50	nA
	Input Noise Voltage	0.1Hz to 10Hz			1		μV_{P-P}
e_n	Input Noise Voltage Density	$f = 1\text{kHz}$			20		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 1\text{kHz}$			0.3		pA/ $\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	Differential Common Mode, $V_{CM} = -15\text{V}$ to 14V		1	2.5 500		M Ω M Ω
C_{IN}	Input Capacitance				4.5		pF
	Input Voltage Range		●	-15		29	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -15\text{V}$ to 29V	●	80	88		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 14\text{V}$, $R_L = 10\text{k}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● ●	200 125 100	500		V/mV V/mV V/mV
V_O	Output Voltage Swing	No Load $I_{OUT} = \pm 10\text{mA}$	● ●	± 14.9 ± 13.7	± 14.95 ± 14.0		V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, unless otherwise noted. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LT1638C/LT1639C, LT1638I/LT1639I			UNITS
				MIN	TYP	MAX	
I_{SC}	Short-Circuit Current (Note 2)	Short to GND	●	25	40		mA
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	20			mA
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	15			mA
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5\text{V}$ to $\pm 22\text{V}$	●	90	100		dB
I_S	Supply Current per Amplifier		●		205	280	μA
						350	μA
GBW	Gain Bandwidth Product	$f = 5\text{kHz}$	●	750	1200		kHz
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	650			kHz
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	600			kHz
SR	Slew Rate	$A_V = -1$, $R_L = \infty$, $V_O = \pm 10\text{V}$	●	0.225	0.4		V/ μs
		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	●	0.2			V/ μs
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	●	0.18			V/ μs

The ● denotes the specifications which apply over the full operating temperature range of $-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$. $V_S = 3\text{V}$, 0V ; $V_S = 5\text{V}$, 0V ; $V_{CM} = V_{OUT} = \text{Half Supply}$ unless otherwise specified. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		LT1638H/LT1639H			UNITS
				MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1638S8	●		200	650	μV
						3	mV
		LT1639S	●		300	750	μV
						3.2	mV
	Input Offset Voltage Drift (Note 9)		●			15	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current	$V_{CM} = 44\text{V}$ (Note 5)	●			15	nA
			●			10	μA
I_B	Input Bias Current	$V_{CM} = 44\text{V}$ (Note 5)	●			150	nA
			●			100	μA
	Input Voltage Range		●	0.3		44	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0.3\text{V}$ to $V_{CC} - 1\text{V}$	●	76			dB
		$V_{CM} = 0.3\text{V}$ to 44V	●	72			dB
A_{VOL}	Large-Signal Voltage Gain	$V_S = 3\text{V}$, $V_O = 500\text{mV}$ to 2.5V , $R_L = 10\text{k}$	●	200	1500		V/mV
				20			V/mV
		$V_S = 5\text{V}$, $V_O = 500\text{mV}$ to 4.5V , $R_L = 10\text{k}$	●	400	1500		V/mV
				35			V/mV
V_{OL}	Output Voltage Swing Low	No Load	●			15	mV
		$I_{SINK} = 5\text{mA}$	●			900	mV
		$V_S = 5\text{V}$, $I_{SINK} = 10\text{mA}$	●			1500	mV
V_{OH}	Output Voltage Swing High	$V_S = 3\text{V}$, No Load	●	2.9			V
		$V_S = 3\text{V}$, $I_{SOURCE} = 5\text{mA}$	●	2			V
		$V_S = 5\text{V}$, No Load	●	4.9			V
		$V_S = 5\text{V}$, $I_{SOURCE} = 10\text{mA}$	●	3.5			V
PSRR	Power Supply Rejection Ratio	$V_S = 3\text{V}$ to 12.5V , $V_{CM} = V_O = 1\text{V}$	●	80			dB
	Minimum Supply Voltage		●	2.7			V
	Reverse Supply Voltage	$I_S = -100\mu\text{A}$	●	18			V
I_S	Supply Current (Note 6)		●		170	230	μA
						450	μA
GBW	Gain Bandwidth Product (Note 5)	$f = 5\text{kHz}$	●	650	1075		kHz
				350			kHz
SR	Slew Rate (Note 7)	$A_V = -1$, $R_L = \infty$	●	0.21	0.38		V/ μs
				0.1			V/ μs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range of $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $V_{OUT} = 0\text{V}$, $V_{SHDN} = V^-$ unless otherwise specified. (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LT1638H/LT1639H			UNITS
			MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1638S8 ●		250	850 3.4	μV mV
		LT1639S ●		350	950 3.6	μV mV
	Input Offset Voltage Drift (Note 9)	●			15	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current	●			25	nA
I_B	Input Bias Current	●			250	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -14.7\text{V}$ to 29V ●	72			dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 14\text{V}$, $R_L = 10\text{k}$ ●	200 15	500		V/mV V/mV
V_O	Output Voltage Swing	No Load ●	± 14.8			V
		$I_{OUT} = \pm 5\text{mA}$ ●	± 14			V
		$I_{OUT} = \pm 10\text{mA}$ ●	± 13.4			V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5\text{V}$ to $\pm 22\text{V}$ ●	84			dB
	Minimum Supply Voltage	●	± 1.35			V
I_S	Supply Current	●		205	280 550	μA μA
GBW	Gain Bandwidth Product	$f = 5\text{kHz}$ ●	750 400	1200		kHz kHz
SR	Slew Rate	$A_V = -1$, $R_L = \infty$, $V_O = \pm 10\text{V}$, Measured at $V_O = \pm 5\text{V}$ ●	0.225 0.1	0.4		$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted.

Note 3: The LT1638C/LT1639C and LT1638I/LT1639I are guaranteed functional over the operating temperature range of -40°C to 85°C . The LT1638H/LT1639H are guaranteed functional over the operating temperature range of -40°C to 125°C .

Note 4: The LT1638C/LT1639C are guaranteed to meet specified performance from 0°C to 70°C and are designed, characterized and expected to meet specified performance from -40°C to 85°C but not

tested or QA sampled at these temperatures. The LT1638I/LT1639I are guaranteed to meet specified performance from -40°C to 85°C . The LT1638H/LT1639H are guaranteed to meet specified performance from -40°C to 125°C .

Note 5: $V_S = 5\text{V}$ limits are guaranteed by correlation to $V_S = 3\text{V}$ and $V_S = \pm 15\text{V}$ or $V_S = \pm 22\text{V}$ tests.

Note 6: $V_S = 3\text{V}$ limits are guaranteed by correlation to $V_S = 5\text{V}$ and $V_S = \pm 15\text{V}$ or $V_S = \pm 22\text{V}$ tests.

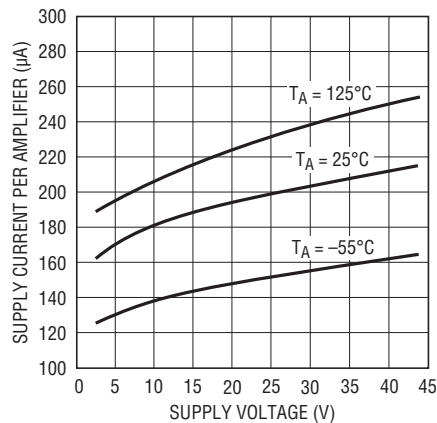
Note 7: Guaranteed by correlation to slew rate at $V_S = \pm 15\text{V}$, and GBW at $V_S = 3\text{V}$ and $V_S = \pm 15\text{V}$ tests.

Note 8: This specification implies a typical input offset voltage of 2mV at $V_{CM} = 44\text{V}$ and a maximum input offset voltage of 5mV at $V_{CM} = 44\text{V}$.

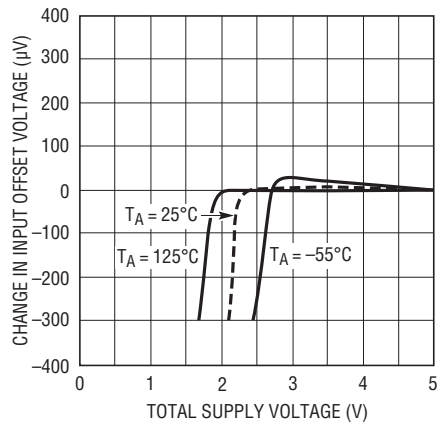
Note 9: This parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

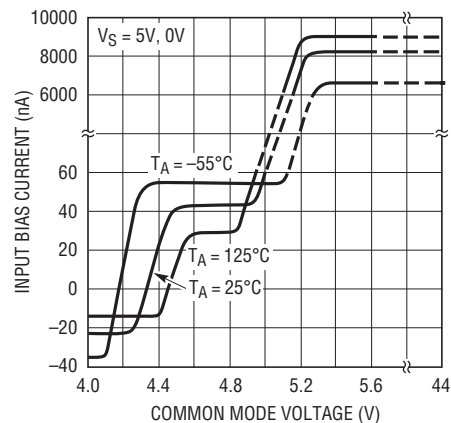
Supply Current vs Supply Voltage



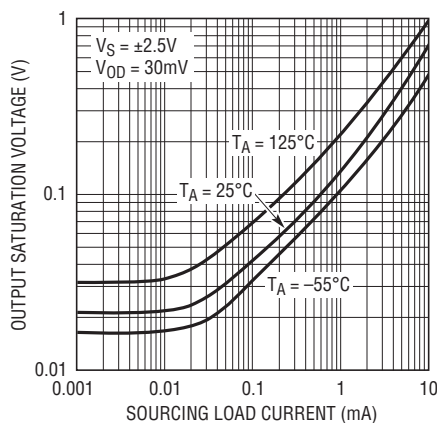
Minimum Supply Voltage



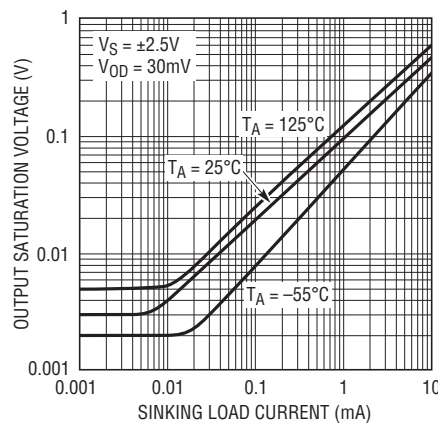
Input Bias Current vs Common Mode Voltage



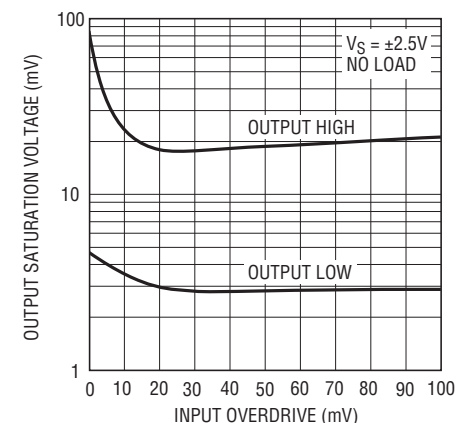
Output Saturation Voltage vs Load Current (Output High)



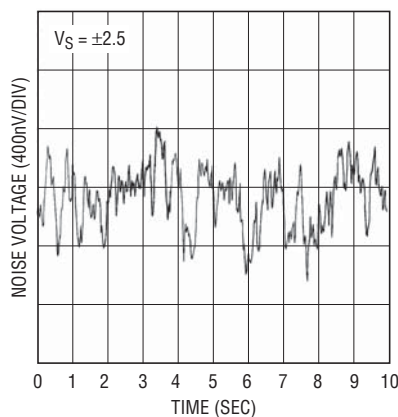
Output Saturation Voltage vs Load Current (Output Low)



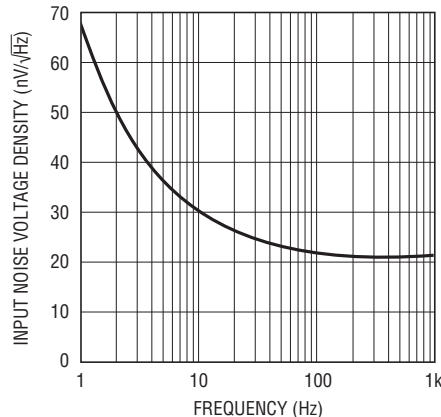
Output Saturation Voltage vs Input Overdrive



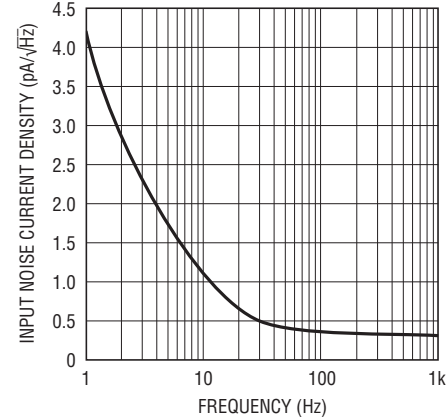
0.1Hz to 10Hz Noise Voltage



Noise Voltage Density vs Frequency

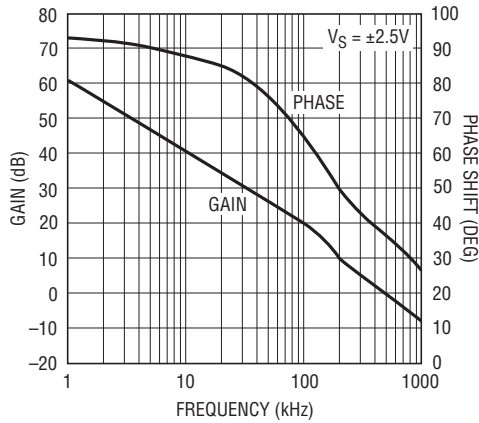


Input Noise Current Density vs Frequency



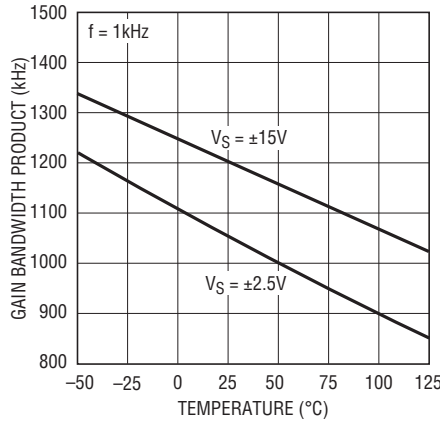
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase Shift vs Frequency



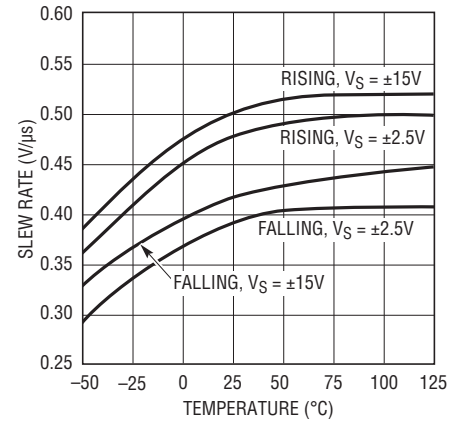
1638/39 G12

Gain Bandwidth Product vs Temperature



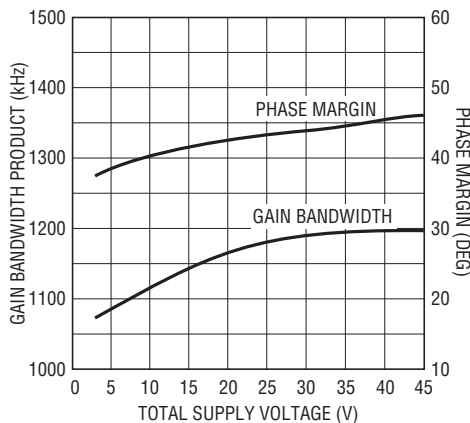
1638/39 G13

Slew Rate vs Temperature



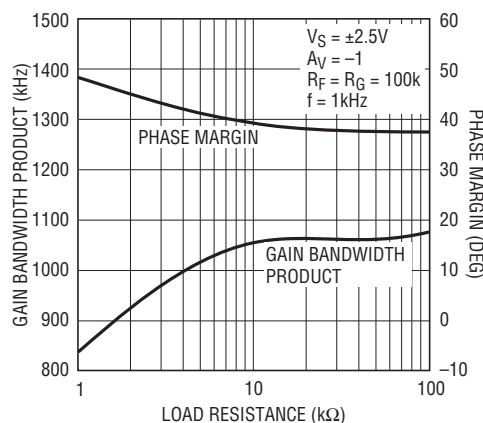
1638/39 G14

Gain Bandwidth Product and Phase Margin vs Supply Voltage



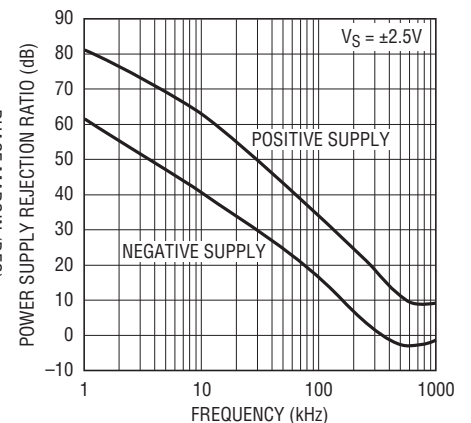
1638/39 G15

Gain Bandwidth Product and Phase Margin vs Load Resistance



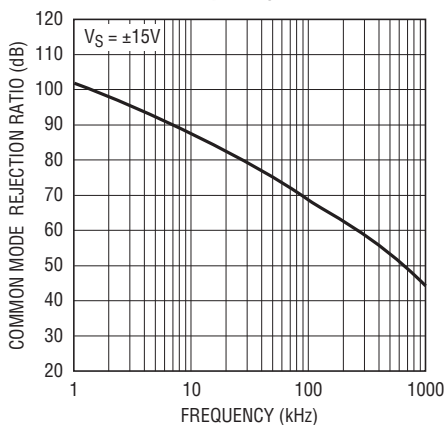
1638/39 G17

PSRR vs Frequency



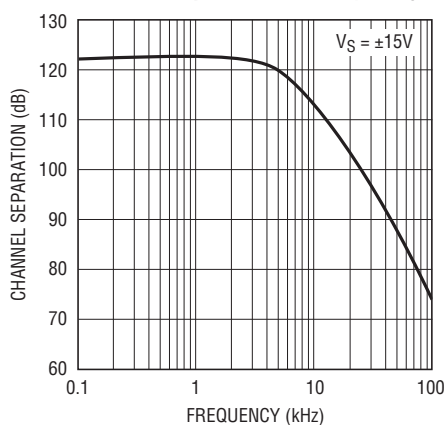
1638/39 G16

CMRR vs Frequency



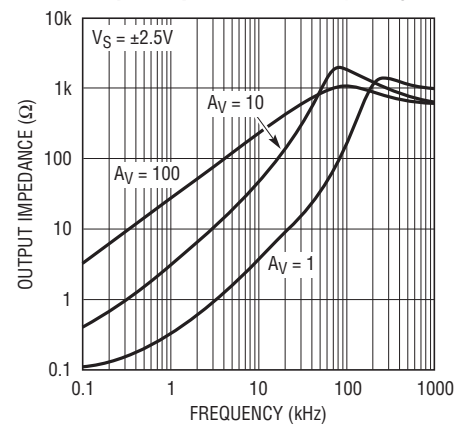
1638/39 G18

Channel Separation vs Frequency



1638/39 G19

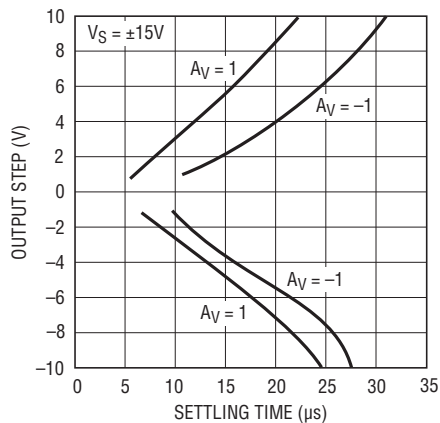
Output Impedance vs Frequency



1638/39 G20

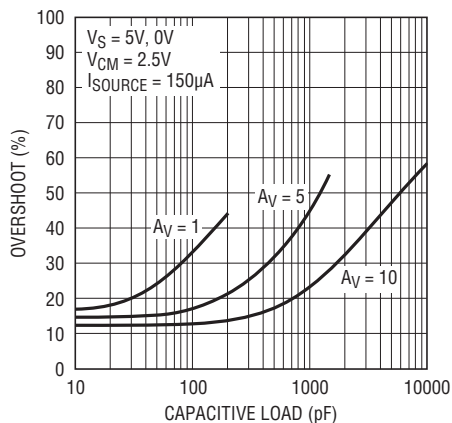
TYPICAL PERFORMANCE CHARACTERISTICS

Settling Time to 0.1% vs Output Step



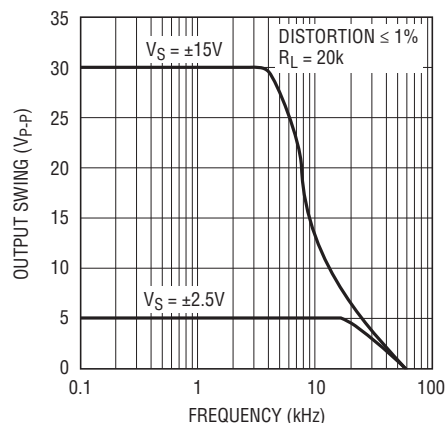
1638/39 G21

Capacitive Load Handling, Overshoot vs Capacitive Load



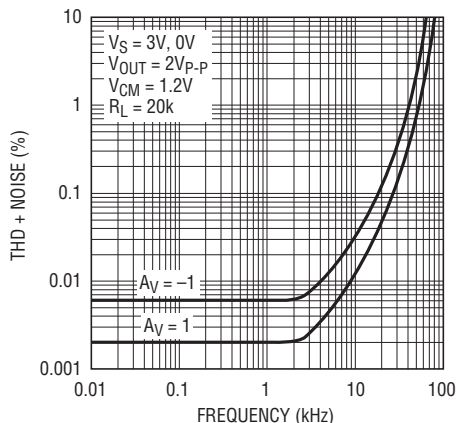
1638/39 G22

Undistorted Output Swing vs Frequency



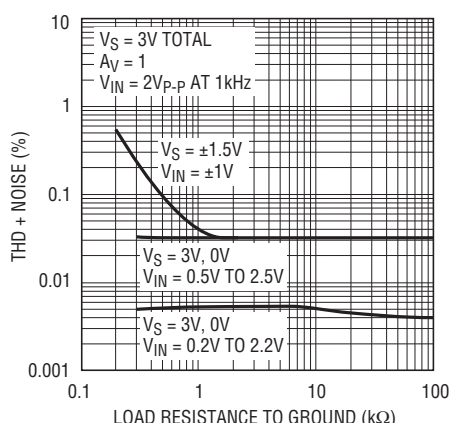
1638/39 G23

Total Harmonic Distortion + Noise vs Frequency



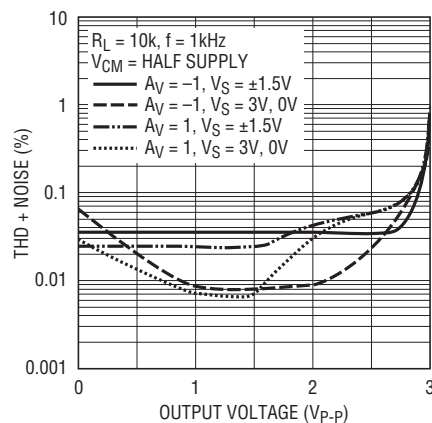
1638/39 G24

Total Harmonic Distortion + Noise vs Load Resistance



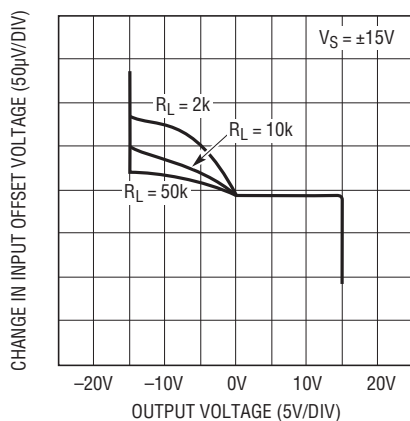
1638/39 G25

Total Harmonic Distortion + Noise vs Output Voltage



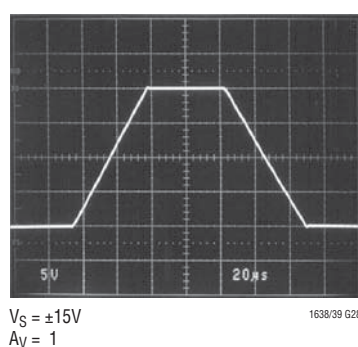
1638/39 G26

Open-Loop Gain



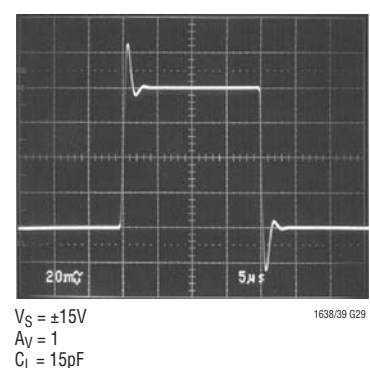
1638/39 G27

Large-Signal Response



1638/39 G28

Small-Signal Response



1638/39 G29

APPLICATIONS INFORMATION

Supply Voltage

The positive supply pin of the LT1638/LT1639 should be bypassed with a small capacitor (typically $0.1\mu\text{F}$) within an inch of the pin. When driving heavy loads an additional $4.7\mu\text{F}$ electrolytic capacitor should be used. When using split supplies, the same is true for the negative supply pin.

The LT1638/LT1639 are protected against reverse battery voltages up to 18V. In the event a reverse battery condition occurs, the supply current is less than 1nA.

The LT1638/LT1639 can be shut down by removing V^+ . In this condition the input bias current is less than 0.1nA, even if the inputs are 44V above the negative supply.

When operating the LT1638/LT1639 on total supplies of 10V or more, the supply must not be brought up faster than $1\text{V}/\mu\text{s}$. Increasing the bypass capacitor and/or adding a small resistor in series with the supply will limit the rise time.

Inputs

The LT1638/LT1639 have two input stages, NPN and PNP (see the Simplified Schematic), resulting in three distinct operating regions as shown in the Input Bias Current vs Common Mode typical performance curve.

For input voltages about 0.8V or more below V^+ , the PNP input stage is active and the input bias current is typically -20nA . When the input common mode voltage is within 0.5V of the positive rail, the NPN stage is operating and the input bias current is typically 40nA. Increases in temperature will cause the voltage at which operation switches from the PNP input stage to the NPN input stage to move towards V^+ . The input offset voltage of the NPN stage is untrimmed and is typically $600\mu\text{V}$.

A Schottky diode in the collector of each NPN transistor allow the LT1638/LT1639 to operate over the top, with either or both of its inputs above V^+ . At about 0.3V above V^+ the NPN input transistor is fully saturated and the input bias current is typically $8\mu\text{A}$ at room temperature. The input offset voltage is typically 2mV when operating above V^+ . The LT1638/LT1639 will operate with its inputs 44V above V^- regardless of V^+ .

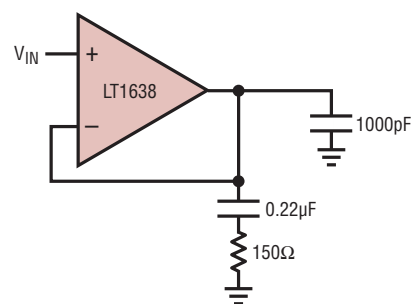
The inputs are protected against excursions of 2V below V^- by an internal 1k resistor in series with each input and a diode from the input to the negative supply. If the inputs can go more than 2V below V^- , an additional external resistor is required. A 10k resistor will protect the input against excursions as much as 10V below V^- . The input stage of the LT1638/LT1639 incorporates phase reversal protection to prevent the output from phase reversing for inputs below V^- . There are no clamping diodes between the inputs and the maximum differential input voltage is 44V.

Output

The output of the LT1638/LT1639 can swing within 20mV of the positive rail with no load, and within 3mV of the negative rail with no load. When monitoring voltages within 20mV of the positive rail or within 3mV of the negative rail, gain should be taken to keep the output from clipping. The LT1638/LT1639 are capable of sinking and sourcing over 40mA on $\pm 15\text{V}$ supplies; sourcing current capability is reduced to 20mA at 5V total supplies as noted in the electrical characteristics.

The LT1638/LT1639 are internally compensated to drive at least 200pF of capacitance under any output loading conditions. A $0.22\mu\text{F}$ capacitor in series with a 150Ω resistor between the output and ground will compensate these amplifiers for larger capacitive loads, up to 1000pF, at all output currents.

Optional Output Compensation for Capacitive Loads Greater than 200pF



Distortion

There are two main contributors of distortion in op amps: output crossover distortion as the output transitions from sourcing to sinking current and distortion caused by

16389fg

APPLICATIONS INFORMATION

nonlinear common mode rejection. If the op amp is operating inverting there is no common mode induced distortion. If the op amp is operating in the PNP input stage (input is not within 0.8V of V^+), the CMRR is very good, typically 98dB. When the LT1638 switches between input stages there is significant nonlinearity in the CMRR. Lower load resistance increases the output crossover distortion, but has no effect on the input stage transition distortion. For lowest distortion the LT1638/LT1639 should be operated single supply, with the output always sourcing

current and with the input voltage swing between ground and ($V^+ - 0.8V$). See the Typical Performance Characteristics curves.

Gain

The open-loop gain is almost independent of load when the output is sourcing current. This optimizes performance in single supply applications where the load is returned to ground. The typical performance curve of Open-Loop Gain for various loads shows the details.

TYPICAL APPLICATIONS

With 1.2MHz bandwidth, Over-The-Top capability, reverse-battery protection and rail-to-rail input and output features, the LT1638/LT1639 are ideal candidates for general purpose applications.

The lowpass slope limiting filter in Figure 1 limits the maximum dV/dt (not frequency) that it passes. When the input signal differs from the output by one forward diode drop, D1 or D2 will turn on. With a diode on, the voltage across R2 will be constant and a fixed current, $V_{DIODE}/R2$, will flow through capacitor C1, charging it linearly instead of exponentially. The maximum slope that the circuit will pass is equal to V_{DIODE} divided by $(R2)(C1)$. No matter how fast the input changes the output will never change any faster than the dV/dt set by the diodes and $(R2)(C)$.

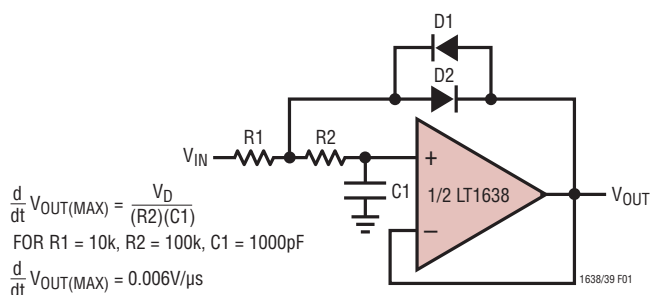


Figure 1. Lowpass Slope Limiting Filter

A modification of this application is shown in Figure 2 using references instead of diodes to set the maximum slope. By using references, the slope is independent of temperature. A scope photo shows a $1V_{P-P}$, 2kHz input signal with a 2V pulse added to the sine wave; the circuit passes the 2kHz signal but limits the slope of the pulse.

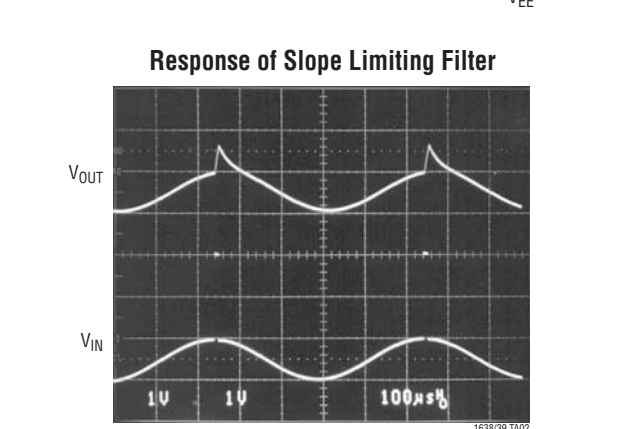
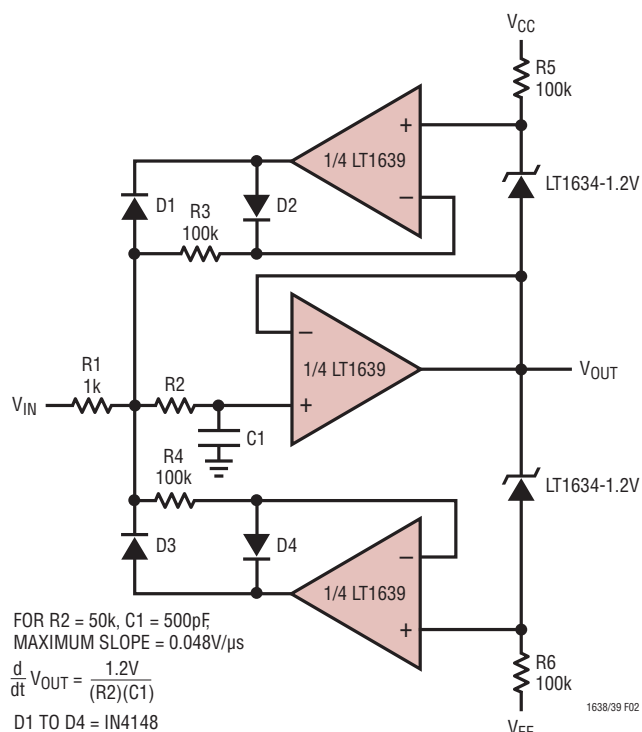


Figure 2. Lowpass Slope Limiting Filter with 0 TC

TYPICAL APPLICATIONS

The application in Figure 3 utilizes the Over-The-Top capabilities of the LT1638. The 0.2Ω resistor senses the load current while the op amp and NPN transistor form a closed loop making the collector current of Q1 proportional to the load current. As a convenient monitor, the $2k\Omega$ load resistor converts the current into a voltage. The positive supply rail, V^+ , is not limited to the 5V supply of the op amp and could be as high as 44V.

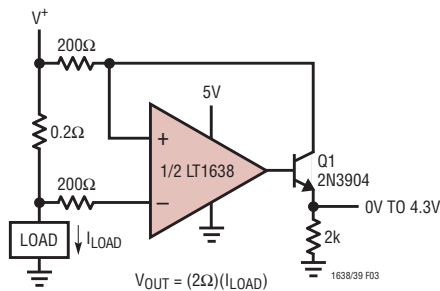


Figure 3. Positive Supply Rail Current Sense

The Figure 4 application uses the LT1638 in conjunction with the LT1634 micropower shunt reference. The supply current of the op amp also biases the reference. The drop across resistor R1 is fixed at 1.2V generating an output current equal to $1.2V/R1$.

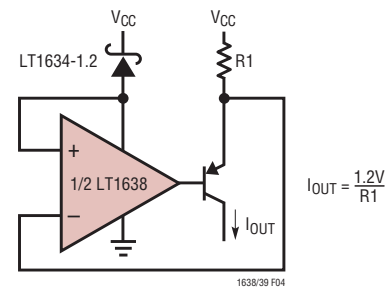
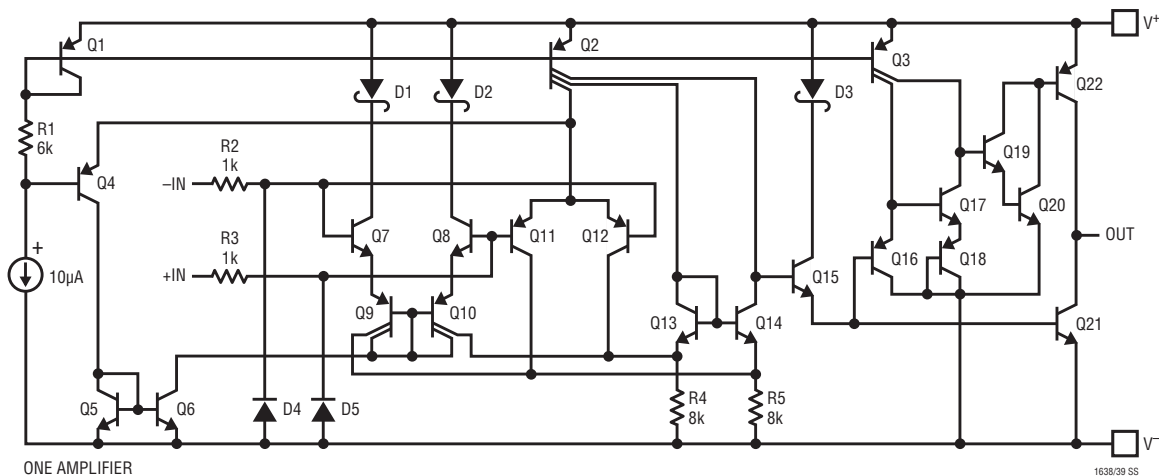


Figure 4. Current Source

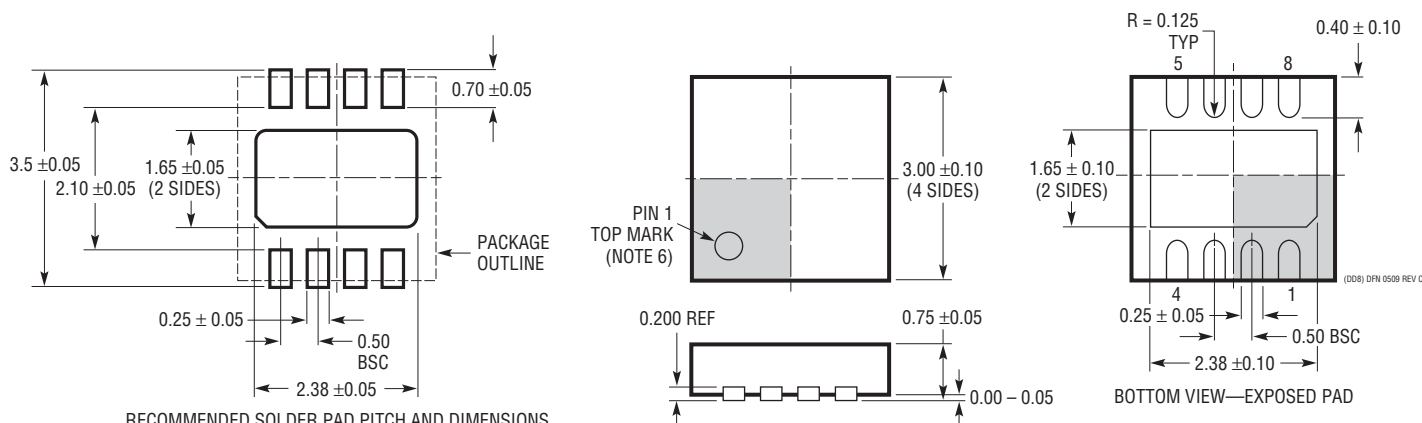
SIMPLIFIED SCHEMATIC



PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698 Rev C)

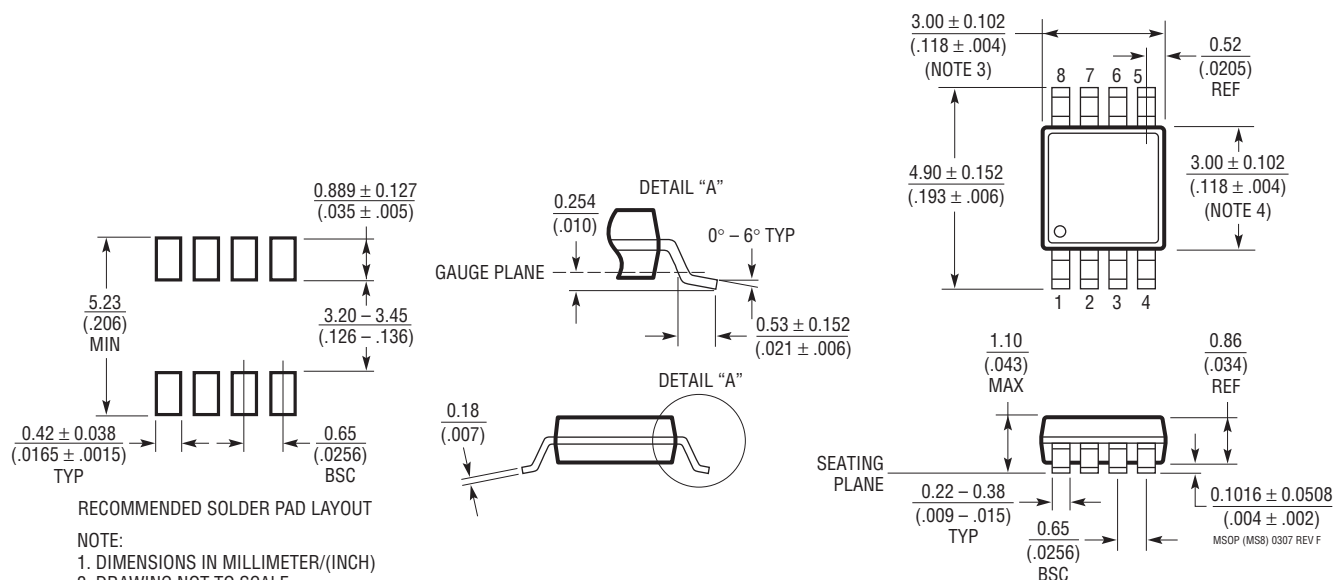


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660 Rev F)



RECOMMENDED SOLDER PAD LAYOUT

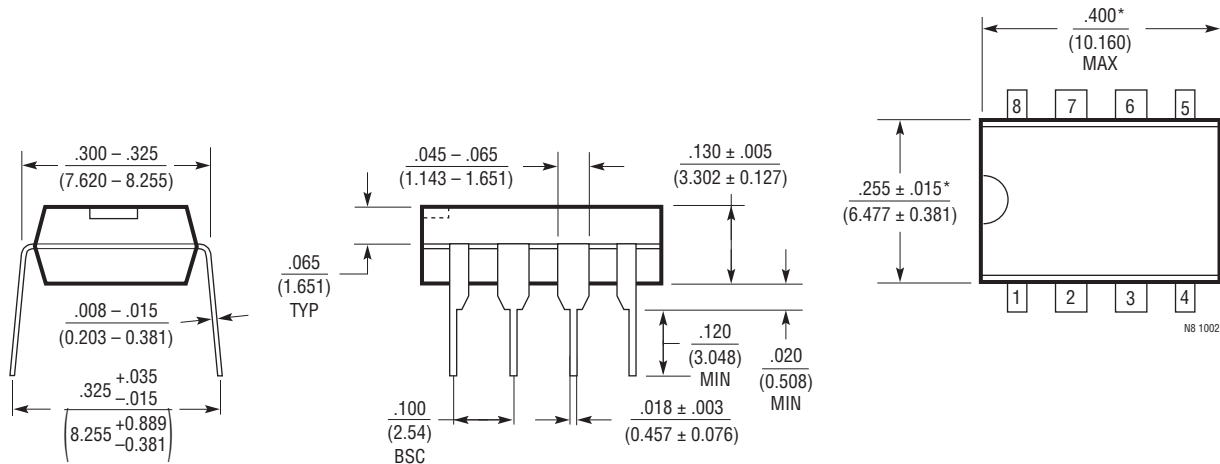
NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (0.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (0.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (0.004") MAX

PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

N8 Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510)

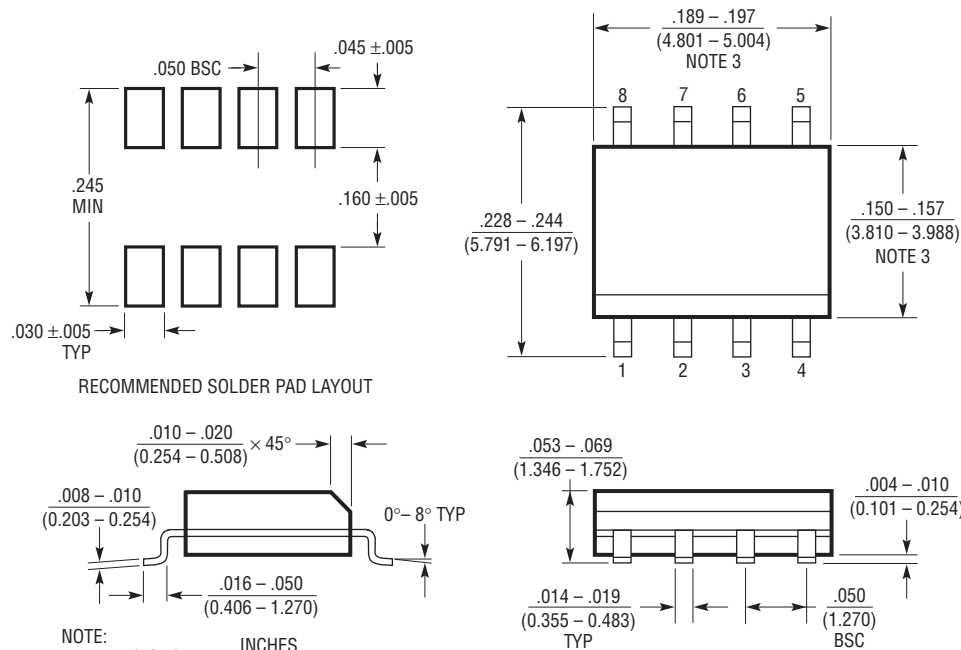


NOTE:

1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



NOTE:

1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

2. DRAWING NOT TO SCALE

3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

S08 0303

16389fg

REVISION HISTORY (Revision history begins at Rev E)

REV	DATE	DESCRIPTION	PAGE NUMBER
E	06/10	Updates to Supply Voltage section	11
F	09/10	Units on x-axis of G24 changed from Hz to kHz	10
G	10/11	Updated θ_{JA} values for MS8 and DD packages in Pin Configuration	2
		Corrected part numbers and revised column title to Specified Temperature Range in Order Information	3
		Deleted Note 10 from Electrical Characteristics	7

