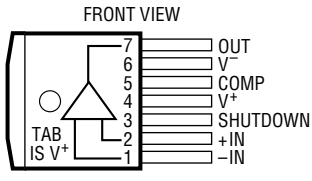
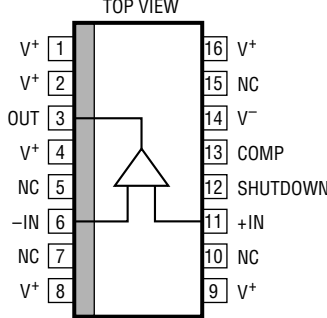
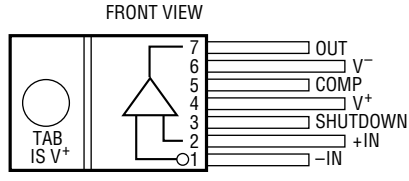


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 18V$	Operating Temperature Range	$-40^{\circ}C$ to $85^{\circ}C$
Input Current	$\pm 15mA$	Junction Temperature	$150^{\circ}C$
Output Short-Circuit Duration (Note 2)	Continuous	Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Specified Temperature Range (Note 3)	$0^{\circ}C$ to $70^{\circ}C$	Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

PACKAGE/ORDER INFORMATION

 <p>R PACKAGE 7-LEAD PLASTIC DD</p> <p>$\theta_{JA} = 25^{\circ}C/W$</p>	 <p>S PACKAGE 16-LEAD PLASTIC SO</p> <p>$\theta_{JA} = 40^{\circ}C/W$ (Note 3)</p>	 <p>T7 PACKAGE 7-LEAD TO-220</p> <p>$\theta_{JC} = 5^{\circ}C/W$</p>
ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER
LT1210CR	LT1210CS	LT1210CT7

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. $V_{CM} = 0V$, $\pm 5V \leq V_S \leq \pm 15V$, pulse tested, $V_{SD} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25^{\circ}C$		± 3	± 15 ± 20	mV mV
	Input Offset Voltage Drift			10		$\mu V/^{\circ}C$
I_{IN}^{+}	Noninverting Input Current	$T_A = 25^{\circ}C$		± 2	± 5 ± 20	μA μA
I_{IN}^{-}	Inverting Input Current	$T_A = 25^{\circ}C$		± 10	± 60 ± 100	μA μA
e_n	Input Noise Voltage Density	$f = 10kHz$, $R_F = 1k$, $R_G = 10\Omega$, $R_S = 0\Omega$		3.0		nV/\sqrt{Hz}
$+i_n$	Input Noise Current Density	$f = 10kHz$, $R_F = 1k$, $R_G = 10\Omega$, $R_S = 10k$		2.0		pA/\sqrt{Hz}
$-i_n$	Input Noise Current Density	$f = 10kHz$, $R_F = 1k$, $R_G = 10\Omega$, $R_S = 10k$		40		pA/\sqrt{Hz}
R_{IN}	Input Resistance	$V_{IN} = \pm 12V$, $V_S = \pm 15V$ $V_{IN} = \pm 2V$, $V_S = \pm 5V$	1.50 0.25	10 5		$M\Omega$ $M\Omega$
C_{IN}	Input Capacitance	$V_S = \pm 15V$		2		pF
	Input Voltage Range	$V_S = \pm 15V$ $V_S = \pm 5V$	± 12 ± 2	± 13.5 ± 3.5		V V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{CM} = 0\text{V}$, $\pm 5\text{V} \leq V_S \leq \pm 15\text{V}$, pulse tested, $V_{SD} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_S = \pm 15\text{V}$, $V_{CM} = \pm 12\text{V}$	● 55	62		dB
		$V_S = \pm 5\text{V}$, $V_{CM} = \pm 2\text{V}$	● 50	60		dB
	Inverting Input Current Common Mode Rejection	$V_S = \pm 15\text{V}$, $V_{CM} = \pm 12\text{V}$	●	0.1	10	$\mu\text{A/V}$
		$V_S = \pm 5\text{V}$, $V_{CM} = \pm 2\text{V}$	●	0.1	10	$\mu\text{A/V}$
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	● 60	77		dB
	Noninverting Input Current Power Supply Rejection	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	●	30	500	nA/V
		$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	●	0.7	5	$\mu\text{A/V}$
		$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	●			
A_V	Large-Signal Voltage Gain	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$, $R_L = 10\Omega$ (Note 3)		55	71	dB
		$V_S = \pm 15\text{V}$, $V_{OUT} = \pm 8.5\text{V}$, $R_L = 10\Omega$ (Note 3)	●	55	68	dB
		$V_S = \pm 5\text{V}$, $V_{OUT} = \pm 2\text{V}$, $R_L = 10\Omega$	●	55	68	dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}^-$	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$, $R_L = 10\Omega$ (Note 3)		100	260	k Ω
		$V_S = \pm 15\text{V}$, $V_{OUT} = \pm 8.5\text{V}$, $R_L = 10\Omega$ (Note 3)	●	75	200	k Ω
		$V_S = \pm 5\text{V}$, $V_{OUT} = \pm 2\text{V}$, $R_L = 10\Omega$	●	75	200	k Ω
V_{OUT}	Maximum Output Voltage Swing	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 10\Omega$ (Note 3)	●	± 10.0 ± 8.5	± 11.5	V V
		$T_A = 25^\circ\text{C}$, $V_S = \pm 5\text{V}$, $R_L = 10\Omega$	●	± 2.5 ± 2.0	± 3.0	V V
I_{OUT}	Maximum Output Current (Note 4)	$V_S = \pm 15\text{V}$, $R_L = 1\Omega$	●	1.1	2.0	A
I_S	Supply Current (Note 4)	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{SD} = 0\text{V}$	●	35	50 65	mA mA
		$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$		15	30	mA
	Supply Current, $R_{SD} = 51\text{k}$ (Notes 4, 5)	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$		15	30	mA
	Positive Supply Current, Shutdown	$V_S = \pm 15\text{V}$, $V_{SD} = 15\text{V}$	●		200	μA
	Output Leakage Current, Shutdown	$V_S = \pm 15\text{V}$, $V_{SD} = 15\text{V}$	●		10	μA
SR	Slew Rate (Note 6)	$T_A = 25^\circ\text{C}$, $A_V = 2$, $R_L = 400\Omega$		400	900	V/ μs
	Slew Rate (Note 4)	$T_A = 25^\circ\text{C}$, $A_V = 2$, $R_L = 10\Omega$			900	V/ μs
	Differential Gain (Notes 4, 7)	$V_S = \pm 15\text{V}$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 15\Omega$		0.3		%
	Differential Phase (Notes 4, 7)	$V_S = \pm 15\text{V}$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 15\Omega$		0.1		DEG
BW	Small-Signal Bandwidth	$A_V = 2$, $V_S = \pm 15\text{V}$, Peaking $\leq 1\text{dB}$, $R_F = R_G = 680\Omega$, $R_L = 100\Omega$		55		MHz
		$A_V = 2$, $V_S = \pm 15\text{V}$, Peaking $\leq 1\text{dB}$, $R_F = R_G = 576\Omega$, $R_L = 10\Omega$		35		MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Applies to short circuits to ground only. A short circuit between the output and either supply may permanently damage the part when operated on supplies greater than $\pm 10\text{V}$.

Note 3: Commercial grade parts are designed to operate over the temperature range of $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, but are neither tested nor guaranteed beyond $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. Industrial grade parts tested over $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ are available on special request. Consult factory.

Note 4: SO package is recommended for $\pm 5\text{V}$ supplies only, as the power dissipation of the SO package limits performance on higher supplies. For supply voltages greater than $\pm 5\text{V}$, use the TO-220 or DD package. See "Thermal Considerations" in the Applications Information section for details on calculating junction temperature. If the maximum dissipation of the package is exceeded, the device will go into thermal shutdown.

Note 5: R_{SD} is connected between the Shutdown pin and ground.

Note 6: Slew rate is measured at $\pm 5\text{V}$ on a $\pm 10\text{V}$ output signal while operating on $\pm 15\text{V}$ supplies with $R_F = 1.5\text{k}$, $R_G = 1.5\text{k}$ and $R_L = 400\Omega$.

Note 7: NTSC composite video with an output level of 2V .

SMALL-SIGNAL BANDWIDTH

$R_{SD} = 0\Omega$, $I_S = 30mA$, $V_S = \pm 5V$, Peaking $\leq 1dB$

A_V	R_L	R_F	R_G	-3dB BW (MHz)
-1	150	549	549	52.5
	30	590	590	39.7
	10	619	619	26.5
1	150	604	—	53.5
	30	649	—	39.7
	10	619	—	27.4
2	150	562	562	51.8
	30	590	590	38.8
	10	576	576	27.4
10	150	392	43.2	48.4
	30	383	42.2	40.3
	10	215	23.7	36.0

$R_{SD} = 0\Omega$, $I_S = 35mA$, $V_S = \pm 15V$, Peaking $\leq 1dB$

A_V	R_L	R_F	R_G	-3dB BW (MHz)
-1	150	604	604	66.2
	30	649	649	48.4
	10	665	665	46.5
1	150	750	—	56.8
	30	866	—	35.4
	10	845	—	24.7
2	150	665	665	52.5
	30	715	715	38.9
	10	576	576	35.0
10	150	453	49.9	61.5
	30	432	47.5	43.1
	10	221	24.3	45.5

$R_{SD} = 7.5k$, $I_S = 15mA$, $V_S = \pm 5V$, Peaking $\leq 1dB$

A_V	R_L	R_F	R_G	-3dB BW (MHz)
-1	150	562	562	39.7
	30	619	619	28.9
	10	604	604	20.5
1	150	634	—	41.9
	30	681	—	29.7
	10	649	—	20.7
2	150	576	576	40.2
	30	604	604	29.6
	10	576	576	21.6
10	150	324	35.7	39.5
	30	324	35.7	32.3
	10	210	23.2	27.7

$R_{SD} = 47.5k$, $I_S = 18mA$, $V_S = \pm 15V$, Peaking $\leq 1dB$

A_V	R_L	R_F	R_G	-3dB BW (MHz)
-1	150	619	619	47.8
	30	698	698	32.3
	10	698	698	22.2
1	150	732	—	51.4
	30	806	—	33.9
	10	768	—	22.5
2	150	634	634	48.4
	30	698	698	33.0
	10	681	681	22.5
10	150	348	38.3	46.8
	30	357	39.2	36.7
	10	205	22.6	31.3

$R_{SD} = 15k$, $I_S = 7.5mA$, $V_S = \pm 5V$, Peaking $\leq 1dB$

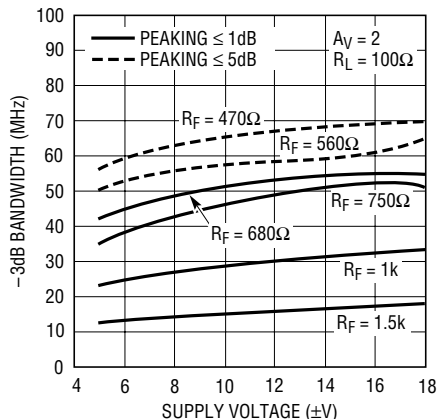
A_V	R_L	R_F	R_G	-3dB BW (MHz)
-1	150	536	536	28.2
	30	549	549	20.0
	10	464	464	15.0
1	150	619	—	28.6
	30	634	—	19.8
	10	511	—	14.9
2	150	536	536	28.3
	30	549	549	19.9
	10	412	412	15.7
10	150	150	16.5	31.5
	30	118	13.0	27.1
	10	100	11.0	19.4

$R_{SD} = 82.5k$, $I_S = 9mA$, $V_S = \pm 15V$, Peaking $\leq 1dB$

A_V	R_L	R_F	R_G	-3dB BW (MHz)
-1	150	590	590	34.8
	30	649	649	22.5
	10	576	576	16.3
1	150	715	—	35.5
	30	768	—	22.5
	10	649	—	16.1
2	150	590	590	35.3
	30	665	665	22.5
	10	549	549	16.8
10	150	182	20.0	37.2
	30	182	20.0	28.9
	10	100	11.0	22.5

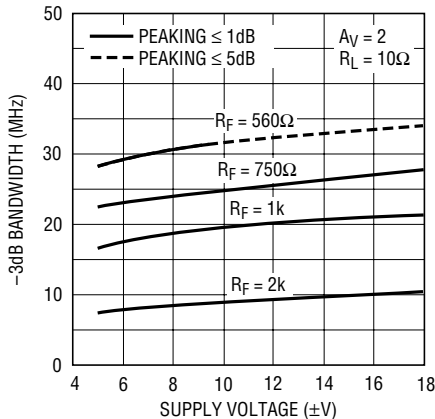
TYPICAL PERFORMANCE CHARACTERISTICS

Bandwidth vs Supply Voltage



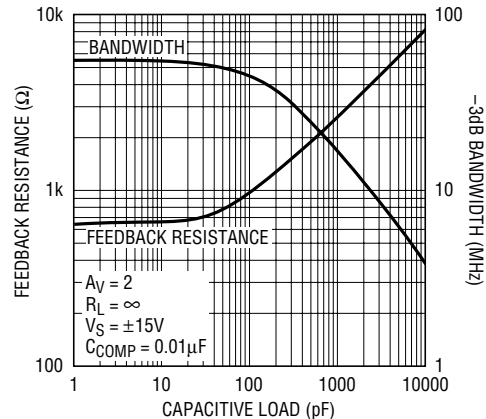
1210 G01

Bandwidth vs Supply Voltage



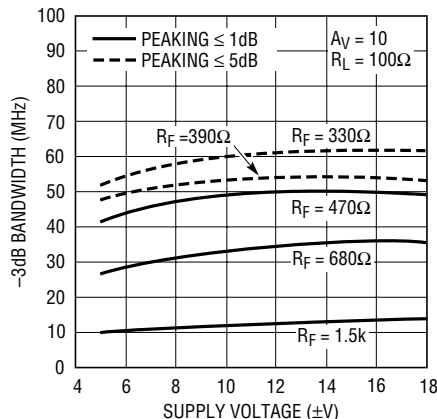
1210 G02

Bandwidth and Feedback Resistance vs Capacitive Load for Peaking $\leq 1dB$



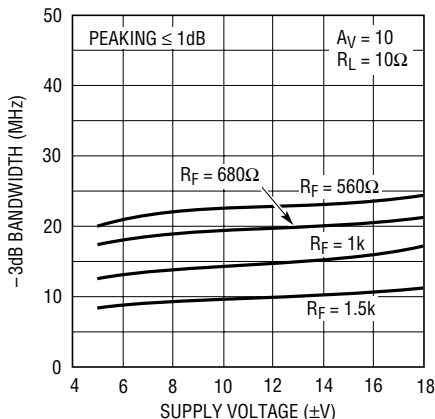
1210 G03

Bandwidth vs Supply Voltage



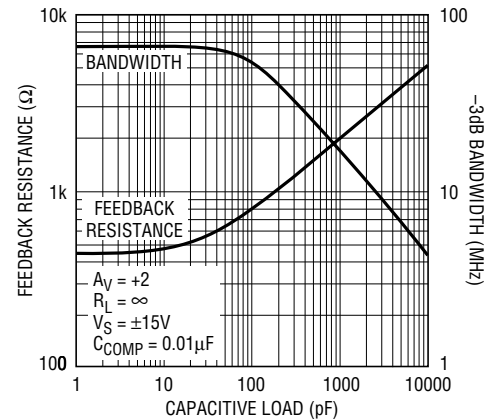
1210 G04

Bandwidth vs Supply Voltage



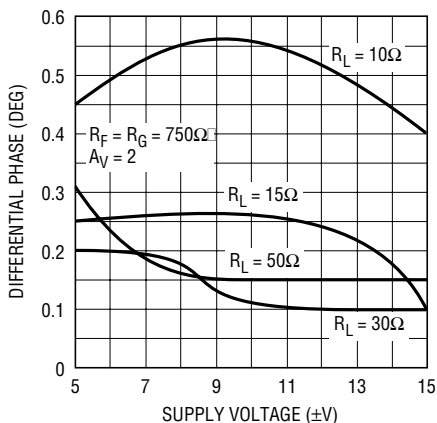
1210 G05

Bandwidth and Feedback Resistance vs Capacitive Load for Peaking $\leq 5dB$



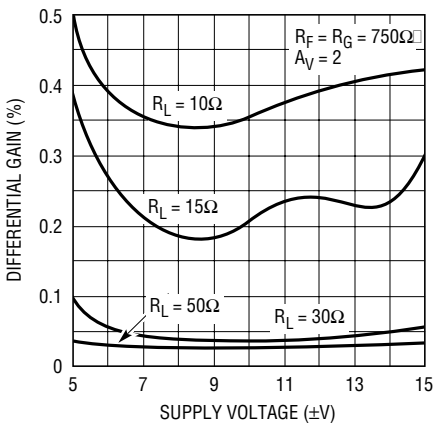
1210 G06

Differential Phase vs Supply Voltage



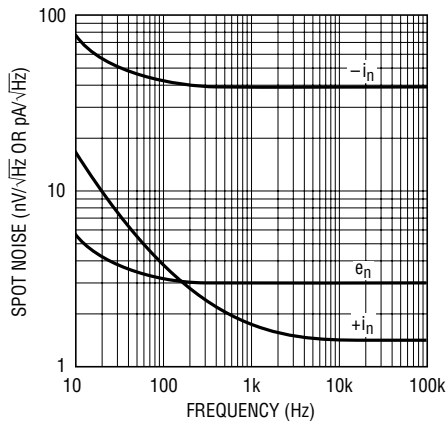
1210 G07

Differential Gain vs Supply Voltage



1210 G08

Spot Noise Voltage and Current vs Frequency

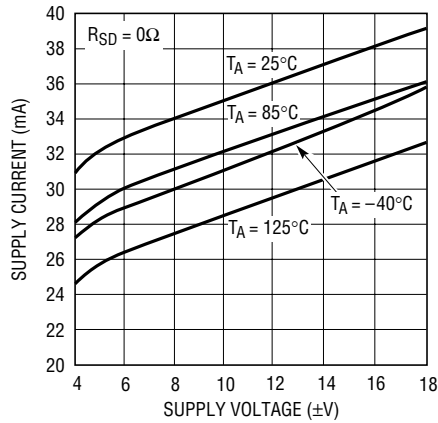
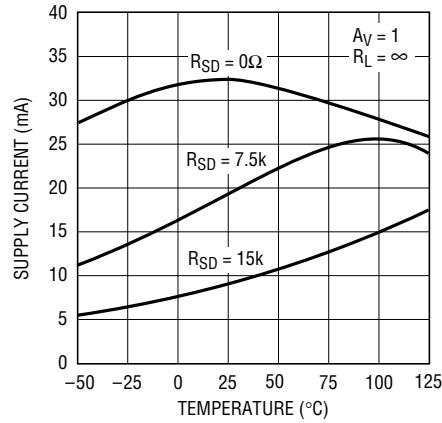
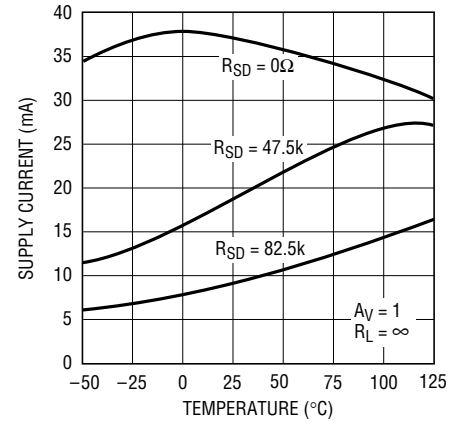


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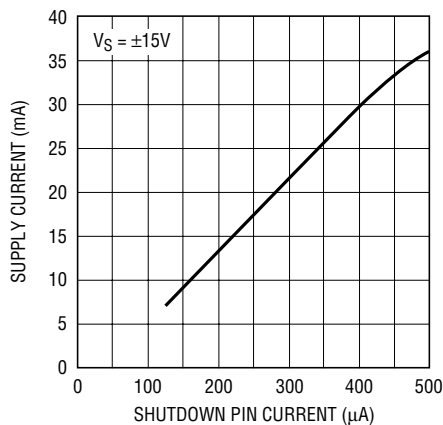
1210fa

TYPICAL PERFORMANCE CHARACTERISTICS

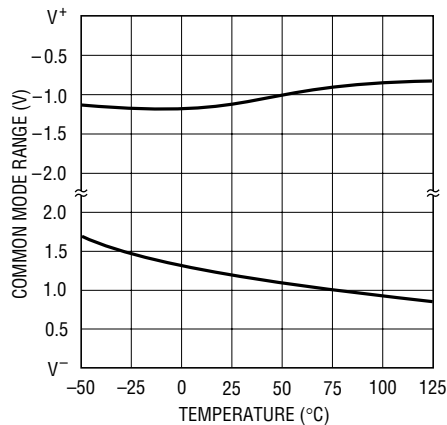
Supply Current vs Supply Voltage

Supply Current vs Ambient Temperature, $V_S = \pm 5V$ Supply Current vs Ambient Temperature, $V_S = \pm 15V$ 

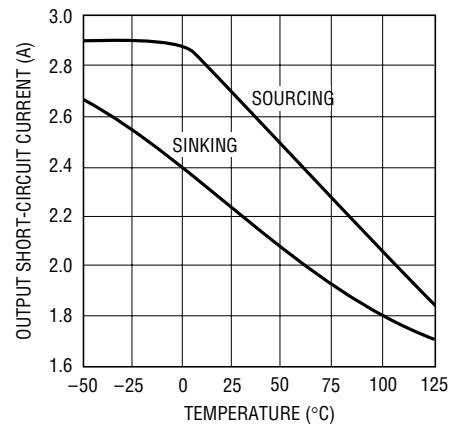
Supply Current vs Shutdown Pin Current



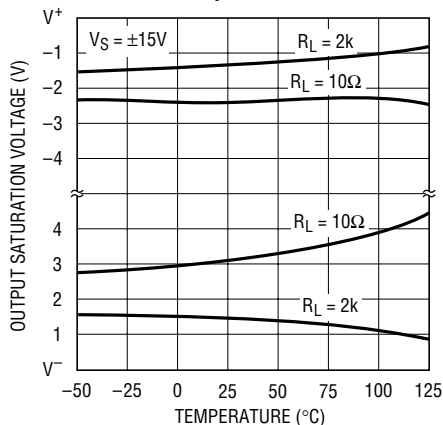
Input Common Mode Limit vs Junction Temperature



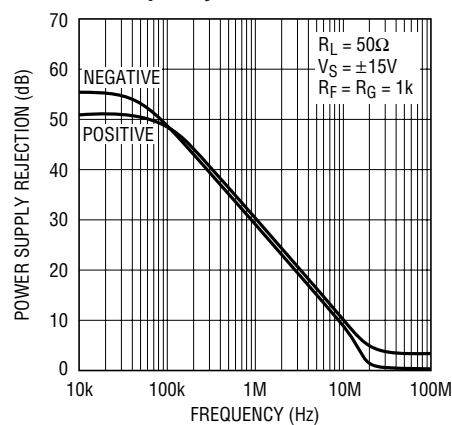
Output Short-Circuit Current vs Junction Temperature



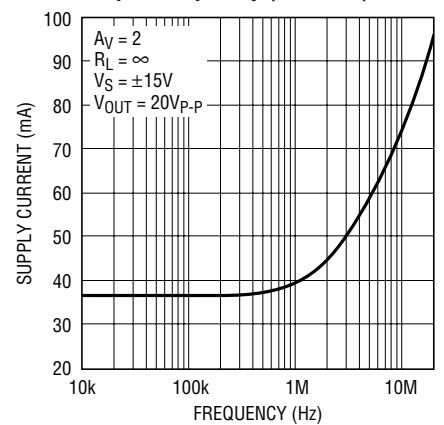
Output Saturation Voltage vs Junction Temperature



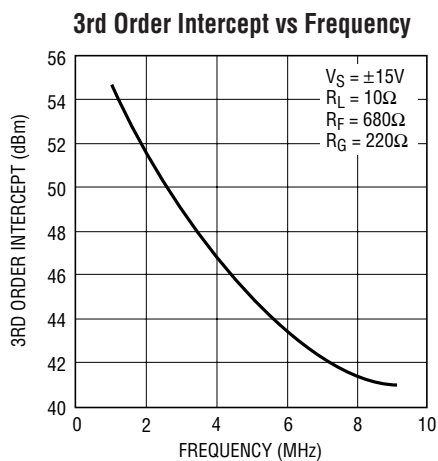
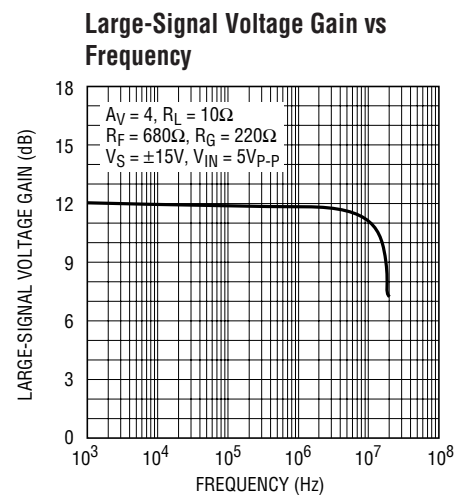
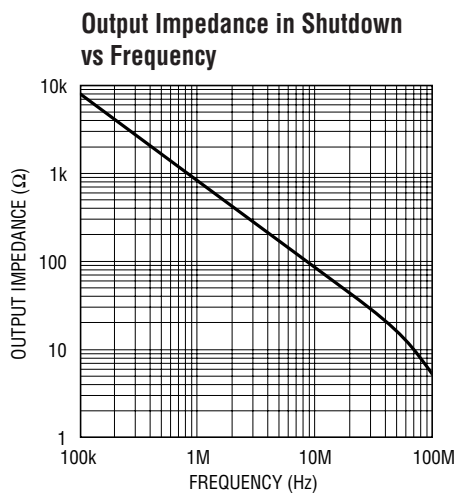
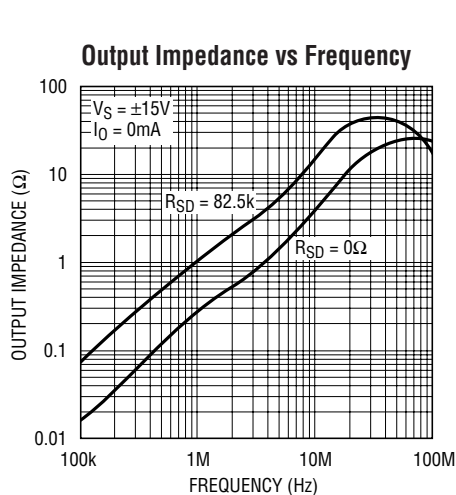
Power Supply Rejection Ratio vs Frequency



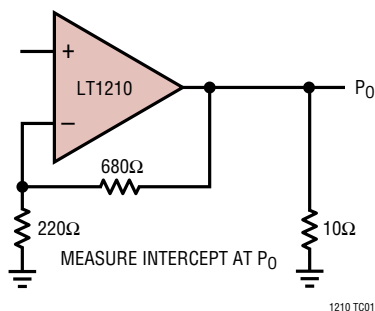
Supply Current vs Large-Signal Output Frequency (No Load)



TYPICAL PERFORMANCE CHARACTERISTICS



Test Circuit for 3rd Order Intercept



APPLICATIONS INFORMATION

The LT1210 is a current feedback amplifier with high output current drive capability. The device is stable with large capacitive loads and can easily supply the high currents required by capacitive loads. The amplifier will drive low impedance loads such as cables with excellent linearity at high frequencies.

Feedback Resistor Selection

The optimum value for the feedback resistors is a function of the operating conditions of the device, the load impedance and the desired flatness of response. The Typical AC Performance tables give the values which result in less than 1dB of peaking for various resistive loads and operating conditions. If this level of flatness is not required, a higher bandwidth can be obtained by use of a lower feedback resistor. The characteristic curves of Bandwidth vs Supply Voltage indicate feedback resistors for peaking up to 5dB. These curves use a solid line when the response has less than 1dB of peaking and a dashed line when the response has 1dB to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

For resistive loads, the COMP pin should be left open (see Capacitive Loads section).

Capacitive Loads

The LT1210 includes an optional compensation network for driving capacitive loads. This network eliminates most of the output stage peaking associated with capacitive loads, allowing the frequency response to be flattened. Figure 1 shows the effect of the network on a 200pF load. Without the optional compensation, there is a 6dB peak at 40MHz caused by the effect of the capacitance on the output stage. Adding a 0.01μF bypass capacitor between the output and the COMP pins connects the compensation and greatly reduces the peaking. A lower value feedback resistor can now be used, resulting in a response which is flat to ±1dB to 40MHz. The network has the greatest effect for C_L in the range of 0pF to 1000pF. The graphs of Bandwidth and Feedback Resistance vs Capacitive Load can be used to select the appropriate value of feedback resistor. The values shown are for 1dB and 5dB peaking at a gain of 2 with no resistive load. This is a worst-case condition, as the amplifier is more stable at higher gains and with some resistive load in parallel with the capaci-

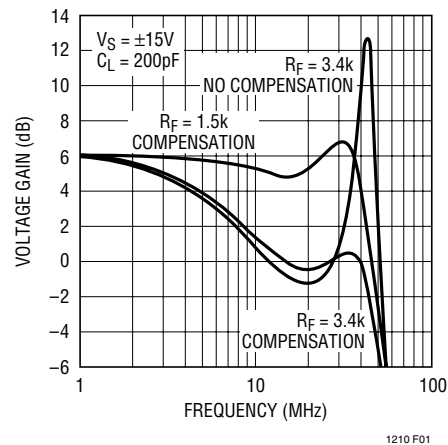


Figure 1

tance. Also shown is the -3dB bandwidth with the suggested feedback resistor vs the load capacitance.

Although the optional compensation works well with capacitive loads, it simply reduces the bandwidth when it is connected with resistive loads. For instance, with a 10Ω load, the bandwidth drops from 35MHz to 26MHz when the compensation is connected. Hence, the compensation was made optional. To disconnect the optional compensation, leave the COMP pin open.

Shutdown/Current Set

If the shutdown feature is not used, the SHUTDOWN pin must be connected to ground or V^- .

The Shutdown pin can be used to either turn off the biasing for the amplifier, reducing the quiescent current to less than 200μA, or to control the quiescent current in normal operation.

The total bias current in the LT1210 is controlled by the current flowing out of the Shutdown pin. When the Shutdown pin is open or driven to the positive supply, the part is shut down. In the shutdown mode, the output looks like a 70pF capacitor and the supply current is typically less than 100μA. The Shutdown pin is referenced to the positive supply through an internal bias circuit (see the Simplified Schematic). An easy way to force shutdown is to use open-drain (collector) logic. The circuit shown in Figure 2 uses a 74C904 buffer to interface between 5V logic and the LT1210. The switching time between the active and shutdown states is about 1μs. A 24k pull-up resistor speeds

1210fa

APPLICATIONS INFORMATION

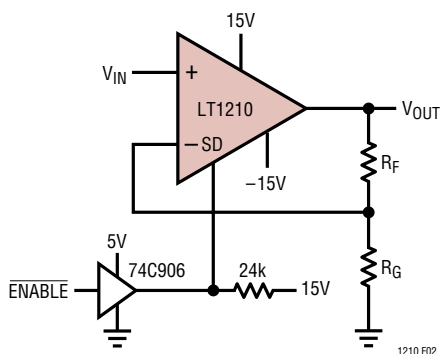


Figure 2. Shutdown Interface

up the turn-off time and ensures that the LT1210 is completely turned off. Because the pin is referenced to the positive supply, the logic used should have a breakdown voltage of greater than the positive supply voltage. No other circuitry is necessary as the internal circuit limits the Shutdown pin current to about 500 μ A. Figure 3 shows the resulting waveforms.

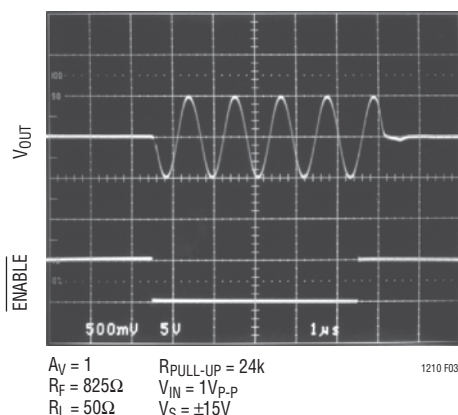


Figure 3. Shutdown Operation

For applications where the full bandwidth of the amplifier is not required, the quiescent current of the device may be reduced by connecting a resistor from the Shutdown pin to ground. The quiescent current will be approximately 65 times the current in the Shutdown pin. The voltage across the resistor in this condition is $V^+ - 3V_{BE}$. For example, a 82k resistor will set the quiescent supply current to 9mA with $V_S = \pm 15V$.

The photos in Figures 4a and 4b show the effect of reducing the quiescent supply current on the large-signal

response. The quiescent current can be reduced to 9mA in the inverting configuration without much change in response. In noninverting mode, however, the slew rate is reduced as the quiescent current is reduced.

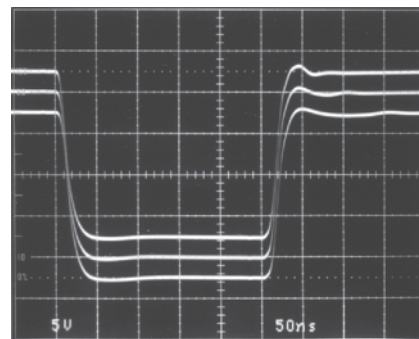


Figure 4a. Large-Signal Response vs I_Q , $A_V = -1$

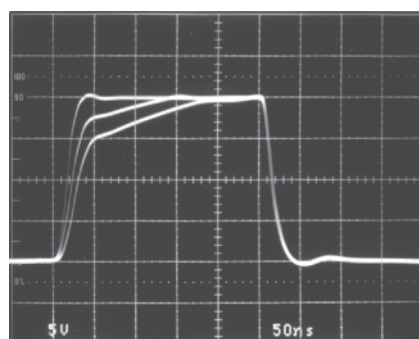


Figure 4b. Large-Signal Response vs I_Q , $A_V = 2$

Slew Rate

Unlike a traditional op amp, the slew rate of a current feedback amplifier is not independent of the amplifier gain configuration. There are slew rate limitations in both the input stage and the output stage. In the inverting mode, and for higher gains in the noninverting mode, the signal amplitude on the input pins is small and the overall slew rate is that of the output stage. The input stage slew rate is related to the quiescent current and will be reduced as the supply current is reduced. The output slew rate is set by the value of the feedback resistors and the internal capacitance. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way

1210fa

APPLICATIONS INFORMATION

the bandwidth is reduced. The photos in Figures 5a, 5b and 5c show the large-signal response of the LT1210 for various gain configurations. The slew rate varies from 770V/ μ s for a gain of 1, to 1100V/ μ s for a gain of -1 .

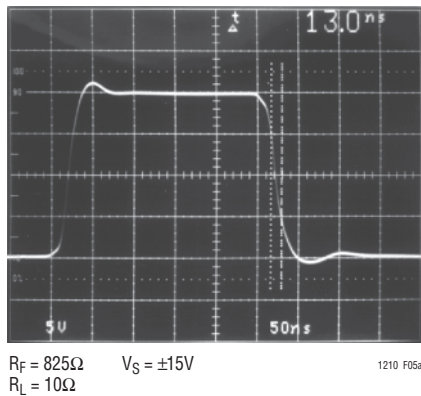


Figure 5a. Large-Signal Response, $A_V = 1$

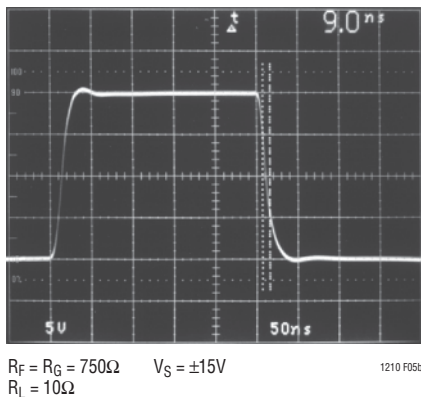


Figure 5b. Large-Signal Response, $A_V = -1$

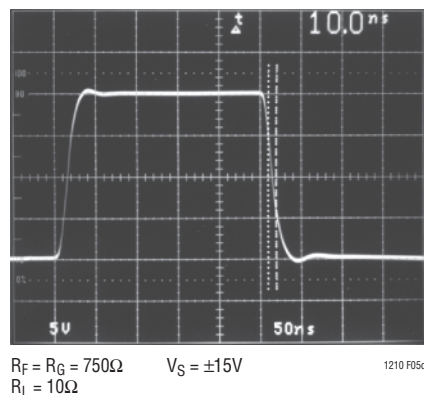


Figure 5c. Large-Signal Response, $A_V = 2$

When the LT1210 is used to drive capacitive loads, the available output current can limit the overall slew rate. In the fastest configuration, the LT1210 is capable of a slew rate of over 1V/ns. The current required to slew a capacitor at this rate is 1mA per picofarad of capacitance, so 10,000pF would require 10A! The photo (Figure 6) shows the large-signal behavior with $C_L = 10,000$ pF. The slew rate is about 150V/ μ s, determined by the current limit of 1.5A.

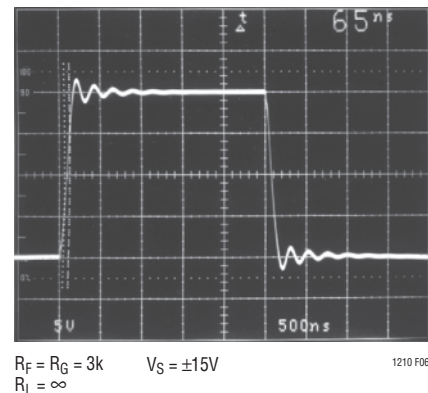


Figure 6. Large-Signal Response, $C_L = 10,000$ pF

Differential Input Signal Swing

The differential input swing is limited to about $\pm 6V$ by an ESD protection device connected between the inputs. In normal operation, the differential voltage between the input pins is small, so this clamp has no effect; however, in the shutdown mode the differential swing can be the same as the input swing. The clamp voltage will then set the maximum allowable input voltage. To allow for some margin, it is recommended that the input signal be less than $\pm 5V$ when the device is shut down.

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response), but it does not degrade the stability of the amplifier.

APPLICATIONS INFORMATION

Power Supplies

The LT1210 will operate from single or split supplies from $\pm 5\text{V}$ (10V total) to $\pm 15\text{V}$ (30V total). It is not necessary to use equal value split supplies, however the offset voltage and inverting input bias current will change. The offset voltage changes about $500\mu\text{V}$ per volt of supply mismatch. The inverting bias current can change as much as $5\mu\text{A}$ per volt of supply mismatch, though typically the change is less than $0.5\mu\text{A}$ per volt.

Power Supply Bypassing

To obtain the maximum output and the minimum distortion from the LT1210, the power supply rails should be well bypassed. For example, with the output stage pouring 1A current peaks into the load, a 1Ω power supply impedance will cause a droop of 1V, reducing the available output swing by that amount. Surface mount tantalum and ceramic capacitors make excellent low ESR bypass elements when placed close to the chip. For frequencies above 100kHz, use $1\mu\text{F}$ and 100nF ceramic capacitors. If significant power must be delivered below 100kHz, capacitive reactance becomes the limiting factor. Larger ceramic or tantalum capacitors, such as $4.7\mu\text{F}$, are recommended in place of the $1\mu\text{F}$ unit mentioned above.

Inadequate bypassing is evidenced by reduced output swing and “distorted” clipping effects when the output is driven to the rails. If this is observed, check the supply pins of the device for ripple directly related to the output waveform. Significant supply modulation indicates poor bypassing.

Thermal Considerations

The LT1210 contains a thermal shutdown feature which protects against excessive internal (junction) temperature. If the junction temperature of the device exceeds the protection threshold, the device will begin cycling between normal operation and an off state. The cycling is not harmful to the part. The thermal cycling occurs at a slow rate, typically 10ms to several seconds, which depends on the power dissipation and the thermal time constants of the package and heat sinking. Raising the ambient temperature until the device begins thermal shutdown gives a good indication of how much margin there is in the thermal design.

For surface mount devices heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PCB material can be very effective at transmitting heat between the pad area attached to the tab of the device, and a ground or power plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PCB material is high, the length/area ratio of the thermal resistance between the layer is small. Copper board stiffeners and plated through holes can also be used to spread the heat generated by the device.

Tables 1 and 2 list thermal resistance for each package. For the TO-220 package, thermal resistance is given for junction-to-case only since this package is usually mounted to a heat sink. Measured values of thermal resistance for several different board sizes and copper areas are listed for each surface mount package. All measurements were taken in still air on 3/32" FR-4 board with 2 oz copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape.

Table 1. R Package, 7-Lead DD

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500 sq. mm	2500 sq. mm	2500 sq. mm	25°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	27°C/W
125 sq. mm	2500 sq. mm	2500 sq. mm	35°C/W

*Tab of device attached to topside copper

Table 2. Fused 16-Lead SO Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE	BACKSIDE		
2500 sq. mm	2500 sq. mm	5000 sq. mm	40°C/W
1000 sq. mm	2500 sq. mm	3500 sq. mm	46°C/W
600 sq. mm	2500 sq. mm	3100 sq. mm	48°C/W
180 sq. mm	2500 sq. mm	2680 sq. mm	49°C/W
180 sq. mm	1000 sq. mm	1180 sq. mm	56°C/W
180 sq. mm	600 sq. mm	780 sq. mm	58°C/W
180 sq. mm	300 sq. mm	480 sq. mm	59°C/W
180 sq. mm	100 sq. mm	280 sq. mm	60°C/W
180 sq. mm	0 sq. mm	180 sq. mm	61°C/W

APPLICATIONS INFORMATION

T7 Package, 7-Lead TO-220

Thermal Resistance (Junction-to-Case) = 5°C/W

Calculating Junction Temperature

The junction temperature can be calculated from the equation:

$$T_J = (P_D)(\theta_{JA}) + T_A$$

where:

T_J = Junction Temperature

T_A = Ambient Temperature

P_D = Device Dissipation

θ_{JA} = Thermal Resistance (Junction-to-Ambient)

As an example, calculate the junction temperature for the circuit in Figure 7 for the SO and R packages assuming a 70°C ambient temperature.

The device dissipation can be found by measuring the supply currents, calculating the total dissipation and then subtracting the dissipation in the load and feedback network.

$$P_D = (76\text{mA})(10\text{V}) - (1.4\text{V})^2 / 10 = 0.56\text{W}$$

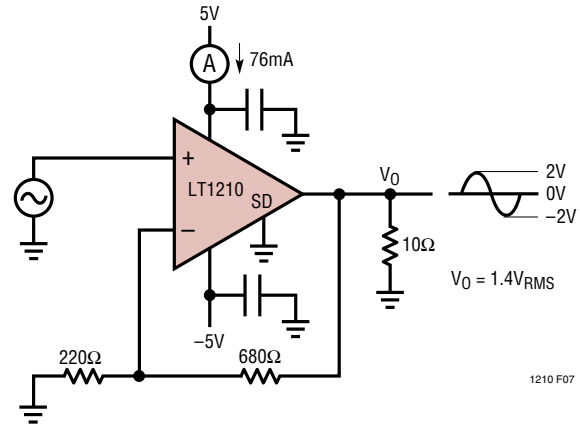


Figure 7

then:

$$T_J = (0.56\text{W})(46^\circ\text{C/W}) + 70^\circ\text{C} = 96^\circ\text{C}$$

for the SO package with 1000 sq. mm topside heat sinking

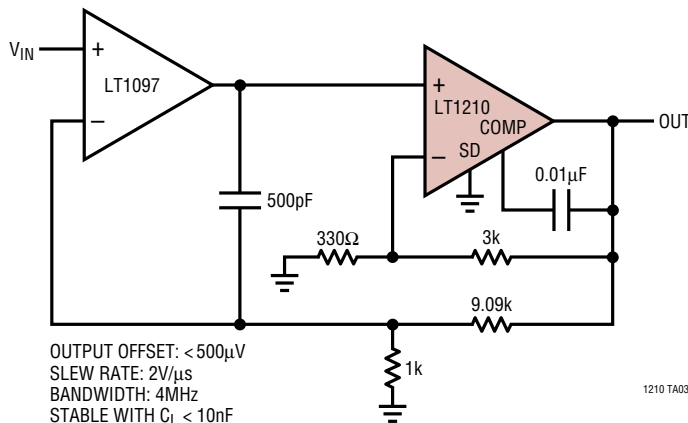
$$T_J = (0.56\text{W})(27^\circ\text{C/W}) + 70^\circ\text{C} = 85^\circ\text{C}$$

for the R package with 1000 sq. mm topside heat sinking

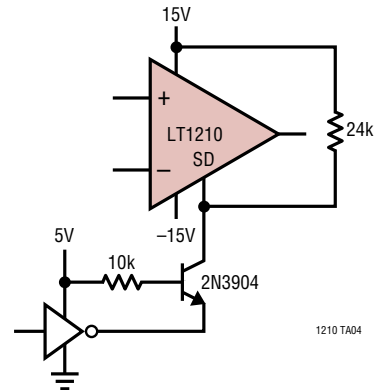
Since the maximum junction temperature is 150°C, both packages are clearly acceptable.

TYPICAL APPLICATIONS

Precision $\times 10$ High Current Amplifier



CMOS Logic to Shutdown Interface

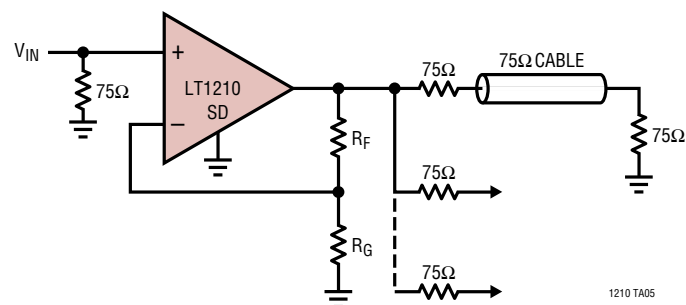


1210 TA04

1210 TA03

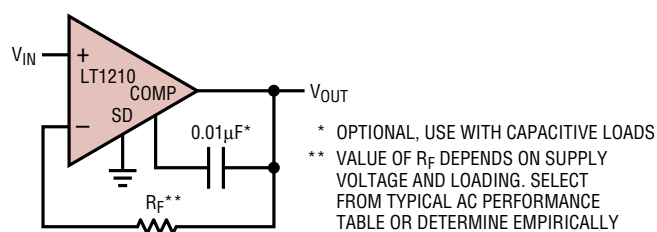
TYPICAL APPLICATIONS

Distribution Amplifier



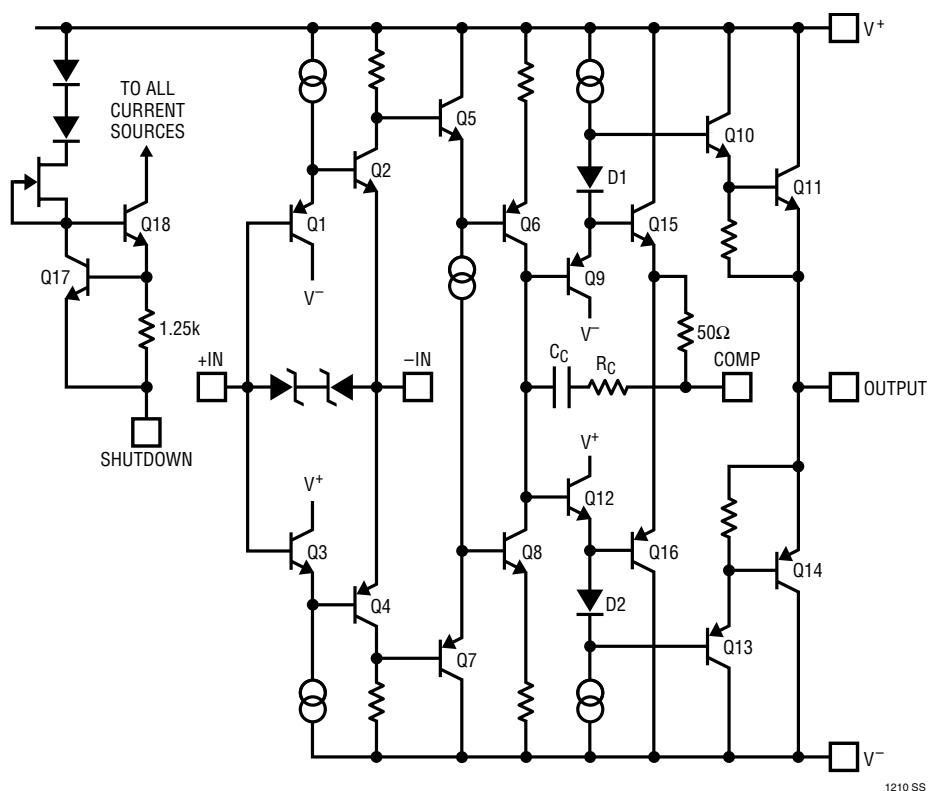
1210 TA05

Buffer $A_V = 1$



1210 TA06

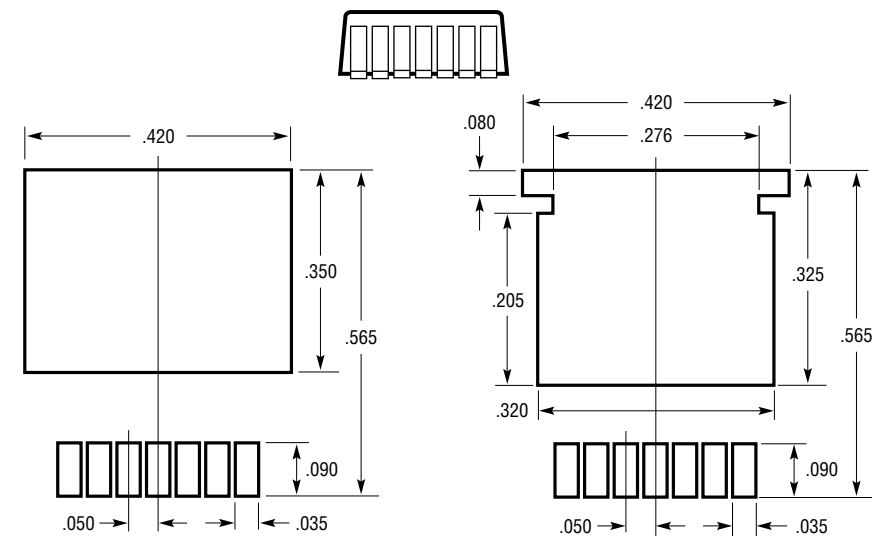
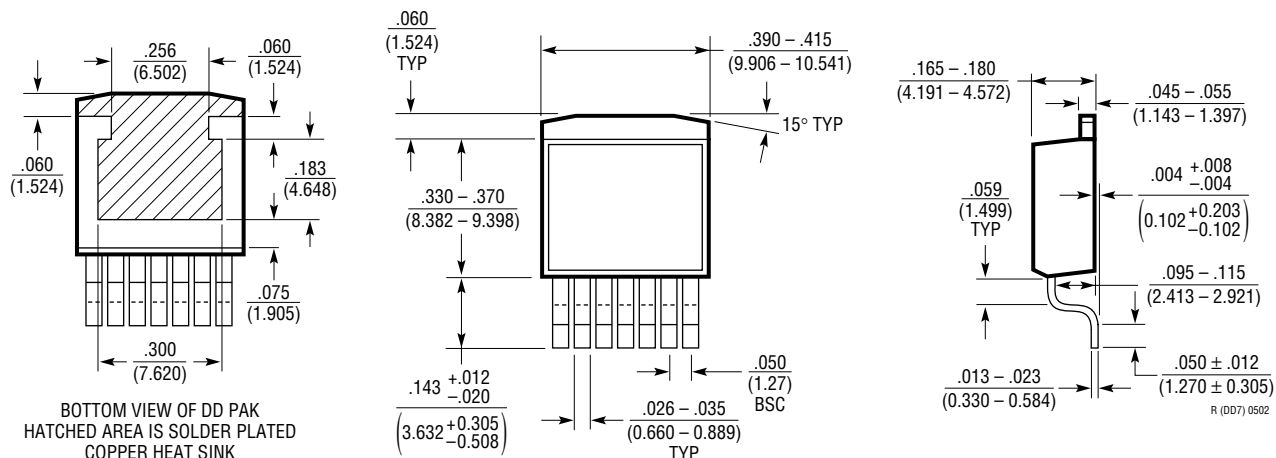
SIMPLIFIED SCHEMATIC



1210 SS

PACKAGE DESCRIPTION

R Package
7-Lead Plastic DD Pak
 (Reference LTC DWG # 05-08-1462)

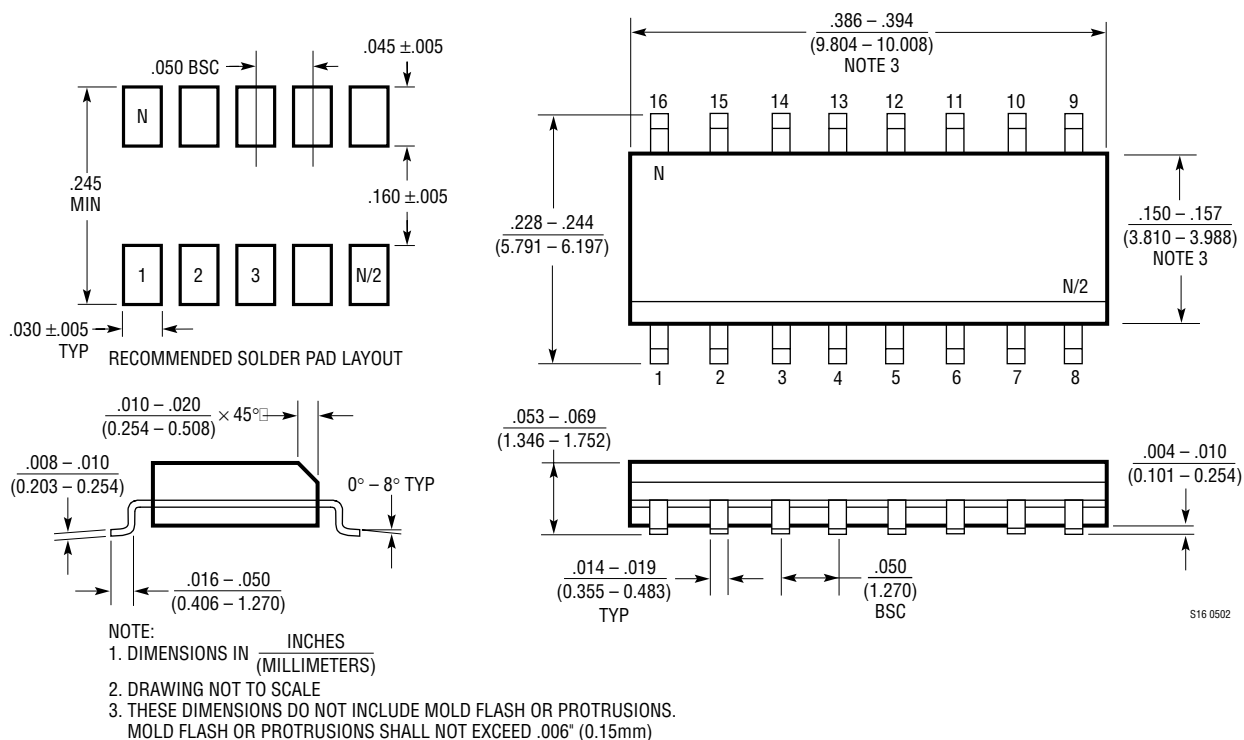


RECOMMENDED SOLDER PAD LAYOUT
 NOTE:
 1. DIMENSIONS IN INCH/(MILLIMETER)
 2. DRAWING NOT TO SCALE

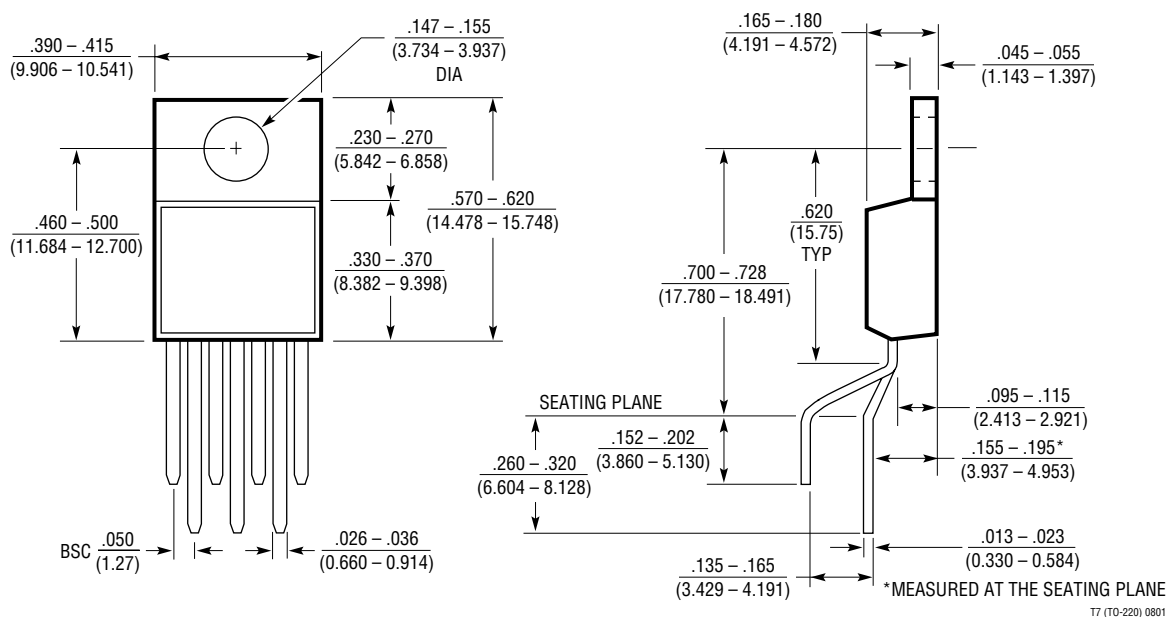
RECOMMENDED SOLDER PAD LAYOUT
 FOR THICKER SOLDER PASTE APPLICATIONS

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
 (Reference LTC DWG # 05-08-1610)

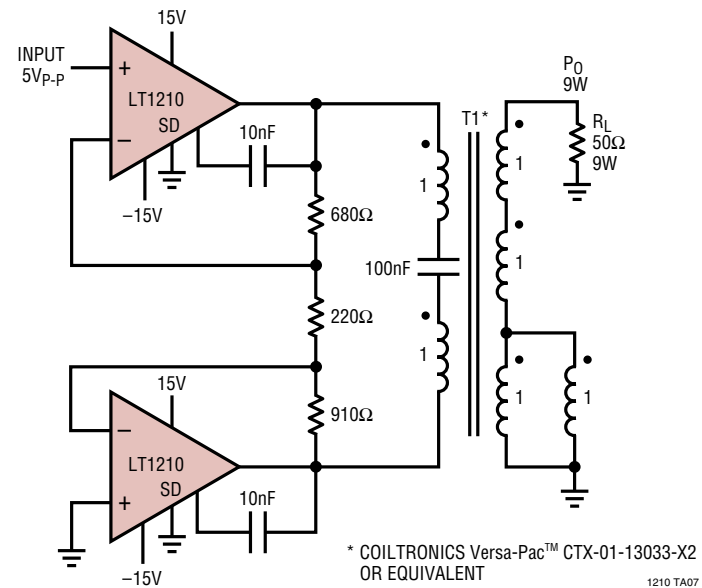


T7 Package
7-Lead Plastic TO-220 (Standard)
 (Reference LTC DWG # 05-08-1422)

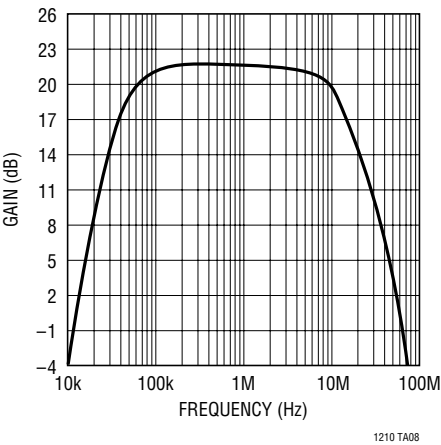


TYPICAL APPLICATION

Wideband 9W Bridge Amplifier



Frequency Response



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1010	Fast $\pm 150\text{mA}$ Power Buffer	20MHz Bandwidth, $75\text{V}/\mu\text{s}$ Slew Rate
LT1166	Power Output Stage Automatic Bias System	Sets Class AB Bias Currents for High Voltage/High Power Output Stages
LT1206	Single 250mA, 60MHz Current Feedback Amplifier	Shutdown Function, Stable with $C_L = 10,000\text{pF}$, $900\text{V}/\mu\text{s}$ Slew Rate
LT1207	Dual 250mA, 60MHz Current Feedback Amplifier	Dual Version of LT1206
LT1227	Single 140MHz Current Feedback Amplifier	Shutdown Function, $1100\text{V}/\mu\text{s}$ Slew Rate
LT1360	Single 50MHz, $800\text{V}/\mu\text{s}$ Op Amp	Voltage Feedback, Stable with $C_L = 10,000\text{pF}$
LT1363	Single 70MHz, $1000\text{V}/\mu\text{s}$ Op Amp	Voltage Feedback, Stable with $C_L = 10,000\text{pF}$