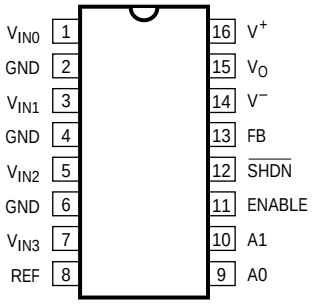
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
– Input Current (Pin 13) ..... ±15mA
+Input and Control/Logic Current (Note 1) ..... ±50mA
Output Short-Circuit Duration (Note 2) ..... Continuous
Specified Temperature Range (Note 3) ..... 0°C to 70°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature (Note 4) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



N PACKAGE
16-LEAD PDIP

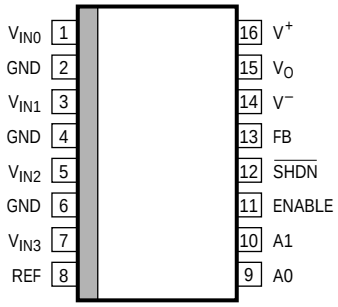
T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT1204CN*

*See Note 3

TOP VIEW



SW PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER PART NUMBER

LT1204CSW*

*See Note 3

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, ±5V ≤ V_S ≤ ±15V, V_{CM} = 0V, Pin 8 grounded and pulse tested unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Any Positive Input, T_A = 25°C			5	14	mV
			●			16	mV
	Offset Matching	Between Any Positive Input, V_S = ±15V	●		0.5	5	mV
	Input Offset Voltage Drift	Any Positive Input	●		40		µV/°C
I_{IN}^+	Positive Input Bias Current	Any Positive Input, T_A = 25°C			3	8	µA
			●			10	µA
I_{IN}^-	Negative Input Bias Current	T_A = 25°C			±20	±100	µA
			●			±150	µA
e_n	Input Noise Voltage	f = 1kHz, R_F = 1k, R_G = 10Ω, R_S = 0Ω			7		nV/√Hz
$+i_n$	Noninverting Input Noise Current Density	f = 1kHz			1.5		pA/√Hz
$–i_n$	Inverting Input Noise Current Density	f = 1kHz			40		pA/√Hz
C_{IN}	Input Capacitance	Input Selected			3.0		pF
		Input Deselected			3.5		pF
C_{OUT}	Output Capacitance	Disabled, Pin 11 Voltage = 0V			8		pF
R_{IN}	Positive Input Resistance, Any Positive Input	V_S = ±5V, V_{IN} = –1.5V, 2V, T_A = 25°C		5	20		MΩ
		V_S = ±15V, V_{IN} = ±5V	●	4	20		MΩ

ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, ±5V ≤ V_S ≤ ±15V, V_{CM} = 0V, Pin 8 grounded and pulse tested unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Input Voltage Range, Any Positive Input	V_S = ±5V, T_A = 25°C		2.0	2.5		V
				–1.5	–2.0		V
		V_S = ±15V	●	±5.0	±6.0		V
		V_S = ±15V, Pin 8 Voltage = –5V	●	3.75	4.0		V
CMRR	Common Mode Rejection Ratio	V_S = ±5V, V_{CM} = –1.5V, 2V, T_A = 25°C		48	55		dB
		V_S = ±15V, V_{CM} = ±5V	●	48	58		dB
	Negative Input Current Common Mode Rejection	V_S = ±5V, V_{CM} = –1.5V, 2V, T_A = 25°C			0.05	1	µA/V
		V_S = ±15V, V_{CM} = ±5V	●		0.05	1	µA/V
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±15V	●	60	76		dB
	Negative Input Current Power Supply Rejection	V_S = ±4.5V to ±15V	●		0.5	5	µA/V
A_{VOL}	Large-Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1k	●	57	73		dB
		V_S = ±5V, V_{OUT} = ±2V, R_L = 150Ω	●	57	66		dB
R_{OL}	Transresistance $\Delta V_O/\Delta I_{IN}^-$	V_S = ±15V, V_{OUT} = ±10V, R_L = 1k	●	115	310		kΩ
		V_S = ±5V, V_{OUT} = ±2V, R_L = 150Ω	●	115	210		kΩ
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 400Ω, T_A = 25°C		±12	±13.5		V
			●	±10			V
		V_S = ±5V, R_L = 150Ω, T_A = 25°C		±3.0	±3.7		V
			●	±2.5			V
I_{OUT}	Output Current	R_L = 0Ω, T_A = 25°C		35	55	125	mA
I_S	Supply Current (Note 5)	Pin 11 = 5V	●		19	24	mA
		Pin 11 = 0V	●		19	24	mA
		Pin 12 = 0V	●		1.5	3.5	mA
	Disabled Output Resistance	V_S = ±15V, Pin 11 = 0V, V_O = ±5V, R_F = R_G = 1k	●	14	25		kΩ
		V_S = ±15V, Pin 11 = 0V, V_O = ±5V, R_F = 2k, R_G = 222Ω	●	8	20		kΩ

DIGITAL INPUT CHARACTERISTICS

0°C ≤ T_A ≤ 70°C, V_S = ±15V, R_F = 2k, R_G = 220Ω, R_L = 400Ω unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	Pins 9, 10, 11, 12	●			0.8	V
V_{IH}	Input High Voltage	Pins 9, 10, 11, 12	●	2			V
I_{IL}	Input Low Current	Pins 9, 10 Voltage = 0V	●		1.5	6	µA
I_{IH}	Input High Current	Pins 9, 10 Voltage = 5V	●		10	150	nA
	Enable Low Input Current	Pin 11 Voltage = 0V	●		4.5	15	µA
	Enable High Input Current	Pin 11 Voltage = 5V	●		200	300	µA
$I_{\overline{SHDN}}$	Shutdown Input Current	Pin 12 Voltage 0V ≤ $V_{\overline{SHDN}}$ ≤ 5V	●		20	80	µA
t_{sel}	Channel-to-Channel Select Time (Note 6)	Pin 8 Voltage = –5V, T_A = 25°C			120	240	ns
t_{dis}	Disable Time (Note 7)	Pin 8 Voltage = –5V, T_A = 25°C			40	100	ns
t_{en}	Enable Time (Note 8)	Pin 8 Voltage = –5V, T_A = 25°C			110	200	ns
$t_{\overline{SHDN}}$	Shutdown Assert or Release Time (Note 9)	Pin 8 Voltage = –5V, T_A = 25°C			1.4	10	µs

AC CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$, $R_F = R_G = 1k$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_r, t_f	Small-Signal Rise and Fall Time	$R_L = 150\Omega$, $V_{OUT} = \pm125mV$		5.6		ns
SR	Slew Rate (Note 10)	$R_L = 400\Omega$	400	1000		V/µs
	Channel Select Output Transient	All $V_{IN} = 0V$, $R_L = 400\Omega$, Input Referred		40		mV
t_S	Settling Time	0.1%, $V_{OUT} = 10V$, $R_L = 1k$		70		ns
	All Hostile Crosstalk (Note 11)	SO PCB #028, $R_L = 100\Omega$, $R_S = 10\Omega$		92		dB
	Disable Crosstalk (Note 11)	SO PCB #028, Pin 11 Voltage = 0V, $R_L = 100\Omega$, $R_S = 50\Omega$		95		dB
	Shutdown Crosstalk (Note 11)	SO PCB #028, Pin 12 Voltage = 0V, $R_L = 100\Omega$, $R_S = 50\Omega$		92		dB
	All Hostile Crosstalk (Note 11)	PDIP PCB #029, $R_L = 100\Omega$, $R_S = 10\Omega$		76		dB
	Disable Crosstalk (Note 11)	PDIP PCB #029, Pin 11 Voltage = 0V, $R_L = 100\Omega$, $R_S = 50\Omega$		81		dB
	Shutdown Crosstalk (Note 11)	PDIP PCB #029, Pin 12 Voltage = 0V, $R_L = 100\Omega$, $R_S = 50\Omega$		76		dB
	Differential Gain (Note 12)	$V_S = \pm15V$, $R_L = 150\Omega$ $V_S = \pm5V$, $R_L = 150\Omega$		0.04 0.04		% %
	Differential Phase (Note 12)	$V_S = \pm15V$, $R_L = 150\Omega$ $V_S = \pm5V$, $R_L = 150\Omega$		0.06 0.12		DEG DEG

The ● denotes specifications which apply over the specified operating temperature range.

Note 1: Analog and digital inputs (Pins 1, 3, 5, 7, 9, 10, 11 and 12) are protected against ESD and overvoltage with internal SCRs. For inputs < ±6V the SCR will not fire, voltages above 6V will fire the SCRs and the DC current should be limited to 50mA. To turn off the SCR the pin voltage must be reduced to less than 2V or the current reduced to less than 10mA.

Note 2: A heat sink may be required depending on the power supply voltage.

Note 3: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C to 85°C are available on special request. Consult factory.

Note 4: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1204CN: $T_J = T_A + (P_D)(70°C/W)$
LT1204CS: $T_J = T_A + (P_D)(90°C/W)$

Note 5: The supply current of the LT1204 has a negative temperature coefficient. For more information see Typical Performance Characteristics.

Note 6: Apply 0.5V DC to Pin 1 and measure the time for the appearance of 5V at Pin 15 when Pin 9 goes from 5V to 0V. Pin 10 Voltage = 0V. Apply 0.5V DC to Pin 3 and measure the time for the appearance of 5V at Pin 15 when Pin 9 goes from 0V to 5V. Pin 10 Voltage = 0V. Apply 0.5V DC to Pin 5 and measure the time for the appearance of 5V at Pin 15 when Pin 9 goes from 5V to 0V. Pin 10 Voltage = 5V. Apply 0.5V DC to Pin 7 and measure the time for the appearance of 5V at Pin 15 when Pin 9 goes from 0V to 5V. Pin 10 Voltage = 5V.

Note 7: Apply 0.5V DC to Pin 1 and measure the time for the disappearance of 5V at Pin 15 when Pin 11 goes from 5V to 0V. Pins 9 and 10 are at 0V.

Note 8: Apply 0.5V DC to Pin 1 and measure the time for the appearance of 5V at Pin 15 when Pin 11 goes from 0V to 5V. Pins 9 and 10 are at 0V. Above a 1MHz toggle rate, t_{en} reduces.

Note 9: Apply 0.5V DC at Pin 1 and measure the time for the appearance of 5V at Pin 15 when Pin 12 goes from 0V to 5V. Pins 9 and 10 are at 0V. Then measure the time for the disappearance of 5V DC to 500mV at Pin 15 when Pin 12 goes from 5V to 0V.

Note 10: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with $R_F = 2k$, $R_G = 220\Omega$ and $R_L = 400\Omega$.

Note 11: V_{IN} = 0dBm ($0.223V_{RMS}$) at 10MHz on any 3 inputs with the 4th input selected. For Disable crosstalk and Shutdown crosstalk all 4 inputs are driven simultaneously. A 6dB output attenuator is formed by a 50Ω series output resistor and the 50Ω input impedance of the HP4195A Network Analyzer. $R_F = R_G = 1k$.

Note 12: Differential Gain and Phase are measured using a Tektronix TSG120 YC/NTSC signal generator and a Tektronix 1780R Video Measurement Set. The resolution of this equipment is 0.1% and 0.1°. Five identical MUXs were cascaded giving an effective resolution of 0.02% and 0.02°.

TYPICAL AC PERFORMANCE Measurements taken from SO Demonstration Board #028.

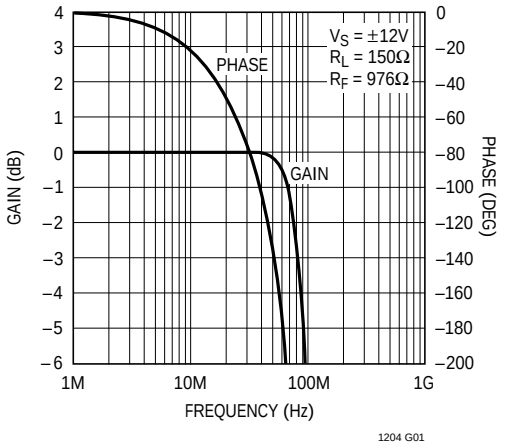
V_S (V)	A_V	R_L (Ω)	R_F (Ω)	R_G (Ω)	SMALL SIGNAL −3dB BW (MHz)	SMALL SIGNAL 0.1dB BW (MHz)	SMALL SIGNAL PEAKING (dB)
±15	1	150 1k	1.1k 1.6k	None None	88.5 95.6	48.3 65.8	0.1 0
±12	1	150 1k	976 1.3k	None None	82.6 90.2	49.1 63.6	0.1 0.1
±5	1	150 1k	665 866	None None	65.5 68.2	43.6 42.1	0.1 0.1
±15	2	150 1k	787 887	787 887	75.7 82.2	45.8 61.3	0 0.1
±12	2	150 1k	750 845	750 845	71.9 77.5	45.0 52.1	0 0
±5V	2	150 1k	590 649	590 649	58.0 62.1	32.4 42.7	0 0.1
±15	10	150 1k	866 1k	95.3 110	44.3 47.4	28.7 30.9	0.1 0.1
±12	10	150 1k	825 931	90.9 100	43.5 46.3	27.2 32.1	0 0.1
±5	10	150 1k	665 750	73.2 82.5	37.2 39.3	22.1 27.8	0 0.1

TRUTH TABLE

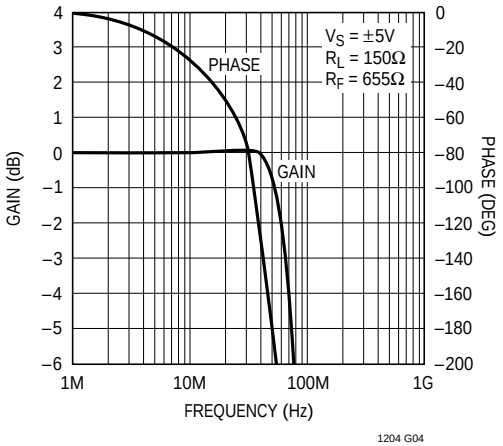
A1	A0	ENABLE	$\overline{\text{SHUTDOWN}}$	CHANNEL SELECTED
0	0	1	1	V_{IN0}
0	1	1	1	V_{IN1}
1	0	1	1	V_{IN2}
1	1	1	1	V_{IN3}
X	X	0	1	High Z Output
X	X	X	0	Off

TYPICAL PERFORMANCE CHARACTERISTICS

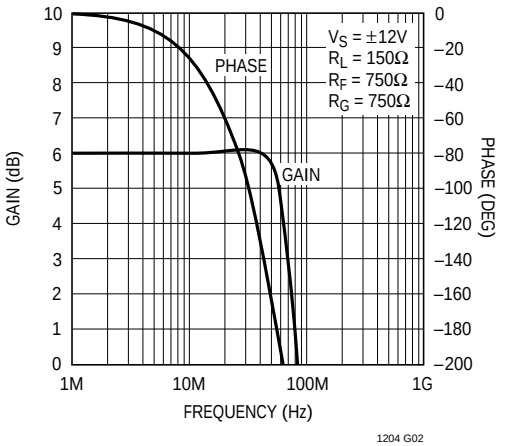
±12V Frequency Response, A_V = 1



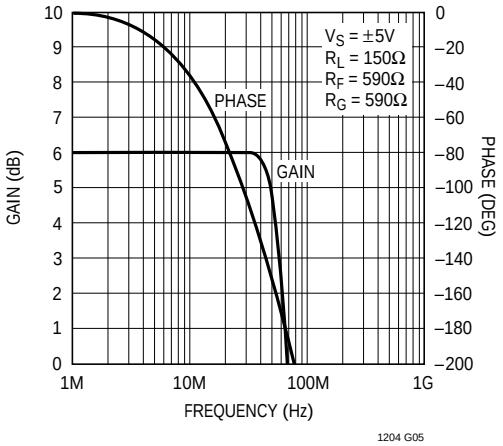
±5V Frequency Response, A_V = 1



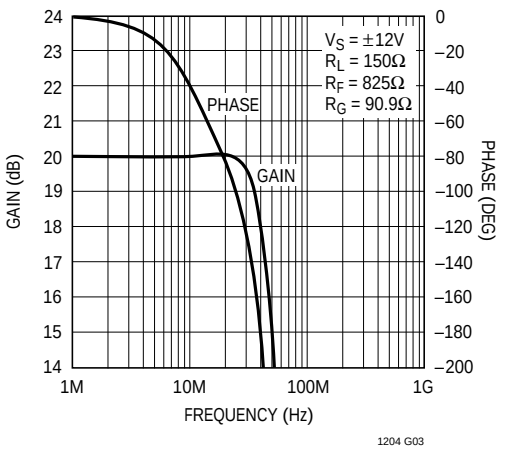
±12V Frequency Response, A_V = 2



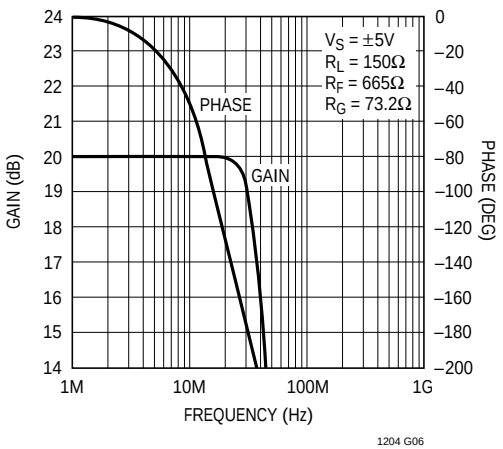
±5V Frequency Response, A_V = 2



±12V Frequency Response, A_V = 10

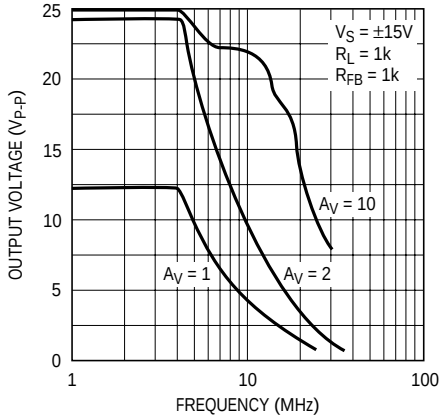


±5V Frequency Response, A_V = 10

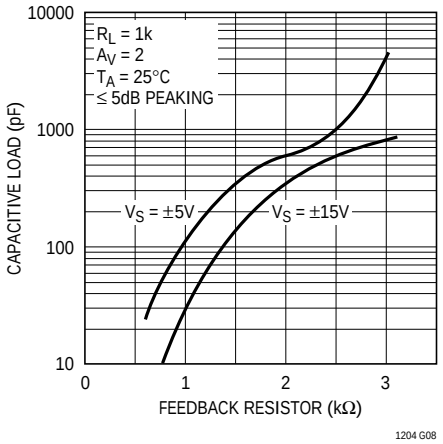


TYPICAL PERFORMANCE CHARACTERISTICS

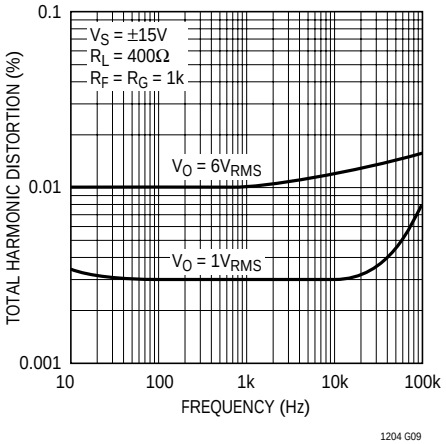
Maximum Undistorted Output vs Frequency



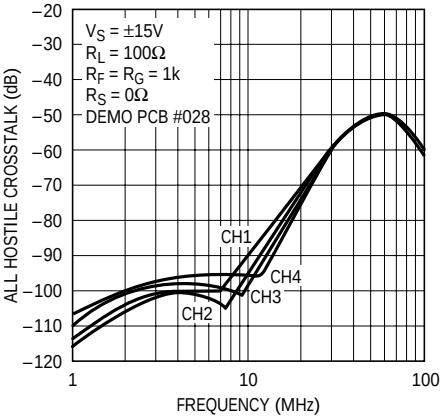
Maximum Capacitive Load vs Feedback Resistor



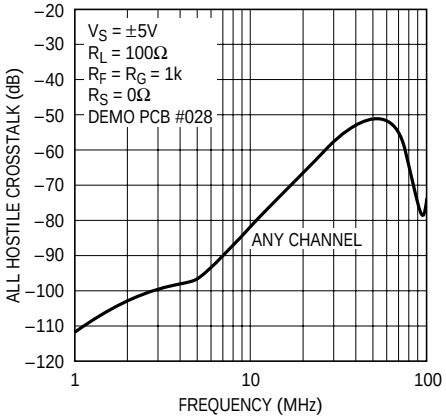
Total Harmonic Distortion vs Frequency



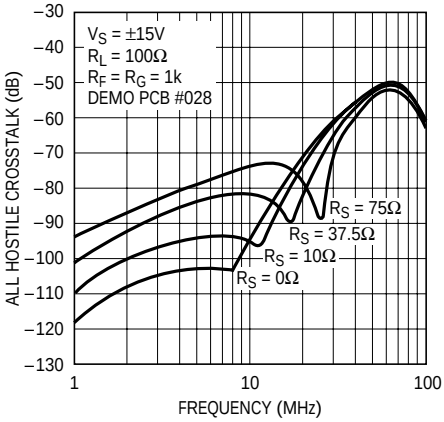
±15V All Hostile Crosstalk vs Frequency



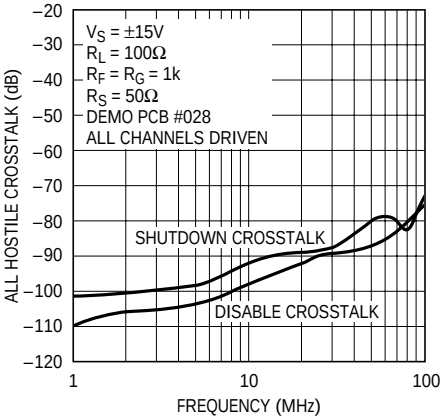
±5V All Hostile Crosstalk vs Frequency



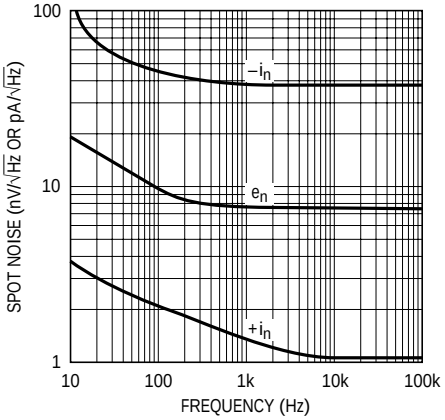
All Hostile Crosstalk vs Frequency, Various Source Resistance



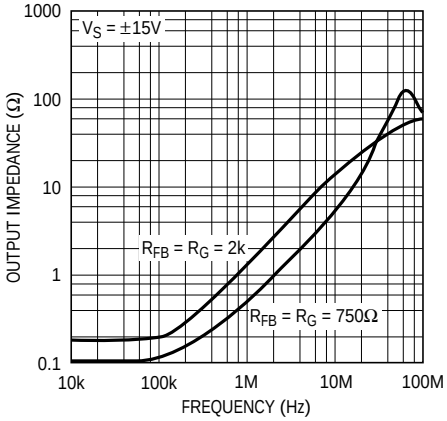
Disable and Shutdown Crosstalk vs Frequency



Spot Noise Voltage and Current vs Frequency

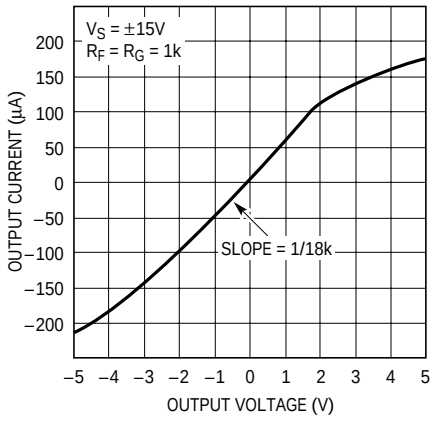


Amplifier Output Impedance vs Frequency

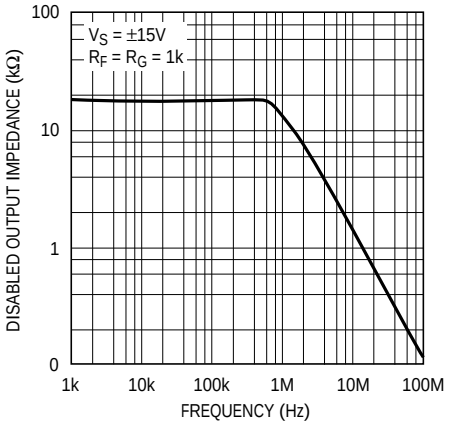


TYPICAL PERFORMANCE CHARACTERISTICS

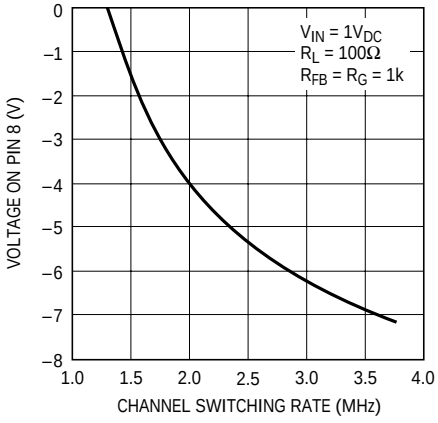
Output Disable V-I Characteristic



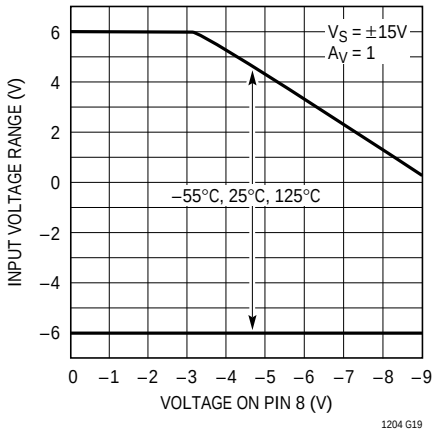
Disabled Output Impedance vs Frequency



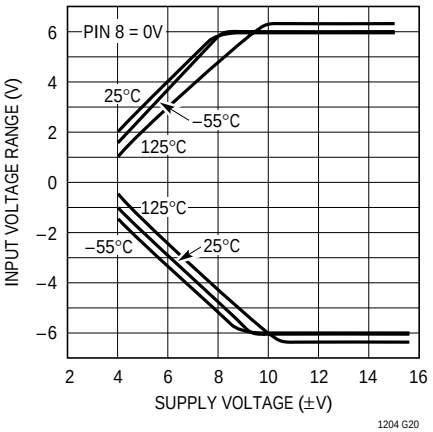
Maximum Channel Switching Rate vs Pin 8 Voltage



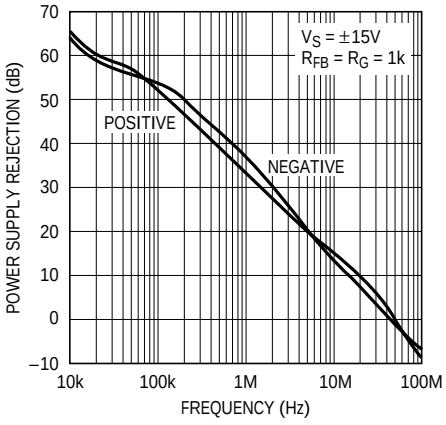
Input Voltage Range vs Pin 8 Voltage



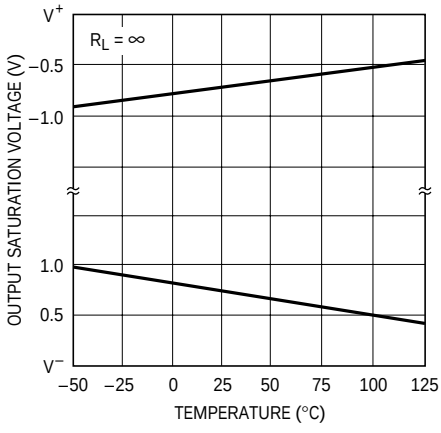
Input Voltage Range vs Supply Voltage



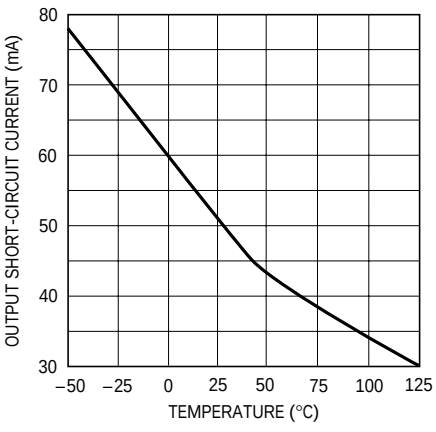
Power Supply Rejection vs Frequency



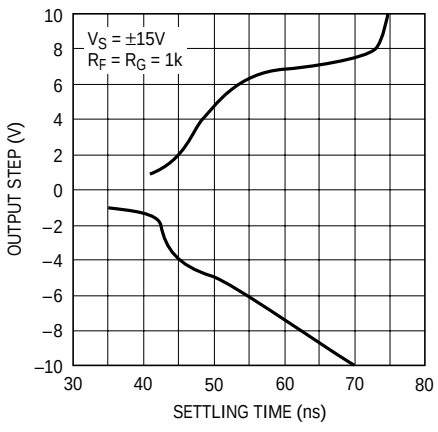
Output Saturation Voltage vs Temperature



Output Short-Circuit Current vs Temperature

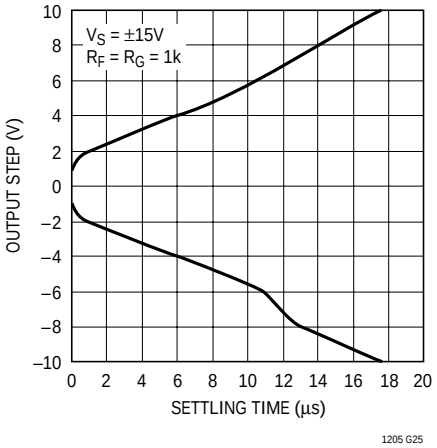


Settling Time to 10mV vs Output Step

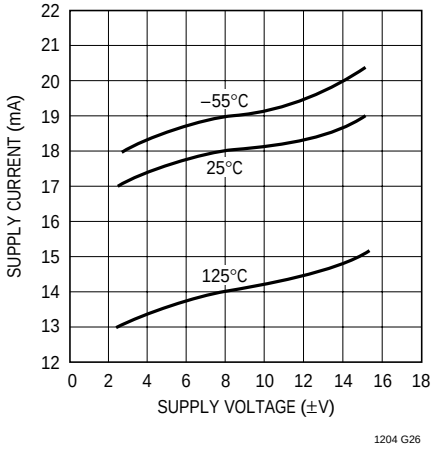


TYPICAL PERFORMANCE CHARACTERISTICS

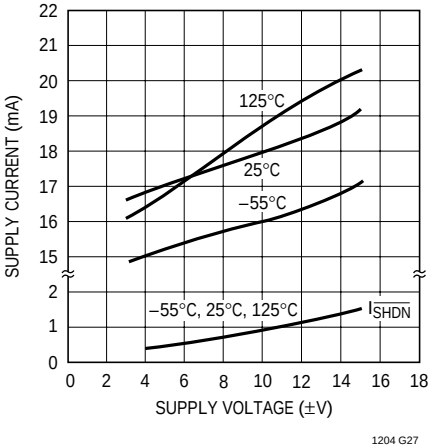
Settling Time to 1mV vs Output Step



Enabled Supply Current vs Supply Voltage



Disabled and Shutdown Supply Current vs Supply Voltage



APPLICATIONS INFORMATION

Logic Inputs

The logic inputs of the LT1204 are compatible with all 5V logic. All pins have ESD protection (>2kV), and shorting them to 12V or 15V will cause excessive currents to flow. Limit the current to less than 50mA when driving the logic above 6V.

Power Supplies

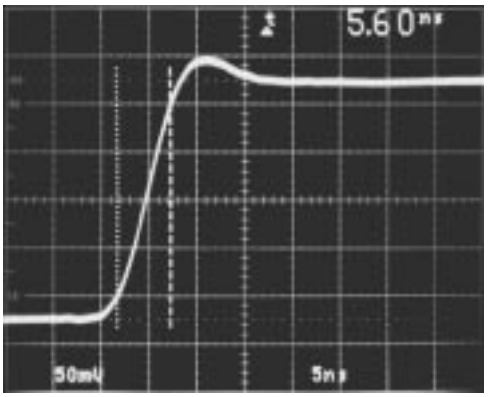
The LT1204 will operate from ±5V (10V total) to ±15V (30V total) and is specified over this range. It is not necessary to use equal value supplies, however, the offset voltage and inverting input bias current will change. The offset voltage changes about 600µV per volt of supply mismatch. The inverting bias current changes about 2.5µA per volt of supply mismatch. The power supplies should be bypassed with quality tantalum capacitors.

Feedback Resistor Selection

The small-signal bandwidth of the LT1204 is set by the external feedback resistors and internal junction capacitors. As a result the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed-loop gain and the load resistor. These effects are outlined in the resistor selection guide of the Typical AC Performance table. Bandwidths range as high as 95MHz and are specified over a very wide range of conditions. An advantage of the current feedback topology used in the LT1204 is well-controlled frequency response. In all cases of the performance table, the peaking is 0.1dB or less. If more peaking can be tolerated, larger bandwidths can be obtained by lowering the feedback resistor. For gains of 2 or less, the 0.1dB bandwidth is greater than 30MHz for all loads and supply voltages.

At high gains (low values of R_G) the disabled output resistance drops slightly due to loading of the internal buffer amplifier as discussed in Multiplexer Expansion.

Small-Signal Rise Time, A_V = 2



V_S = ±15V R_F = 1k
R_L = 150Ω R_G = 1k

APPLICATIONS INFORMATION

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response and overshoot in the transient response.

Capacitive Loads

The LT1204 can drive capacitive loads directly when the proper value of feedback resistor is used. The graph of Maximum Capacitive Load vs Feedback Resistor should be used to select the appropriate value. The value shown is for 5dB peaking when driving a 1k load at a gain of 2. This is a worst-case condition. The amplifier is more stable at higher gains and driving heavier loads. Alternatively, a small resistor (10Ω to 20Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present. The disadvantage is that the gain is a function of load resistance.

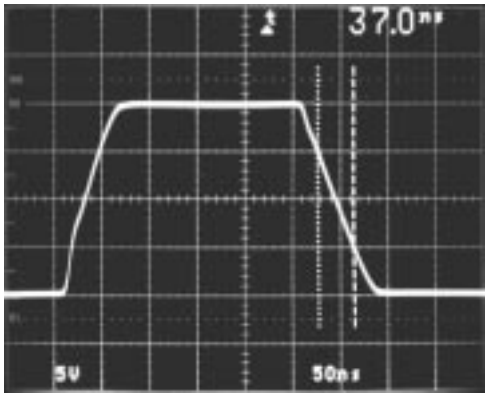
Slew Rate

The slew rate of the current feedback amplifier on the LT1204 is not independent of the amplifier gain the way slew rate is in a traditional op amp. This is because both the input and the output stage have slew rate limitations. In high gain settings the signal amplitude between the negative input and any driven positive input is small and the overall slew rate is that of the output stage. For gains less than 10, the overall slew rate is limited by the input stage.

The input slew rate of the LT1204 is approximately 135V/µs and is set by internal currents and capacitances. The output slew rate is set by the value of the feedback resistors and the internal capacitances. At a gain of 10 with a 1k feedback resistor and ±15 supplies, the output slew rate is typically 1000V/µs. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced.

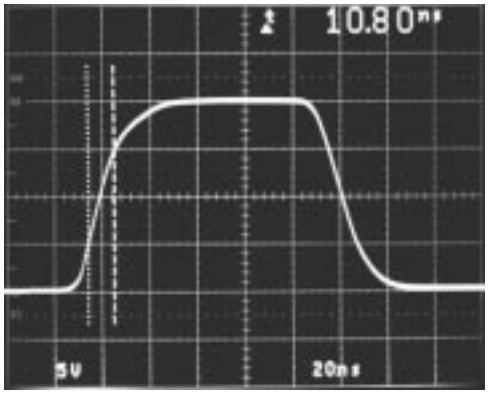
The graph, Maximum Undistorted Output vs Frequency, relates the slew rate limitations to sinusoidal inputs for various gain configurations.

Large-Signal Transient Response



V_S = ±15V
A_V = 2
R_F = 1k
R_G = 1k
R_L = 400Ω

Large-Signal Transient Response



V_S = ±15V
A_V = 10
R_F = 910Ω
R_G = 100Ω
R_L = 400Ω

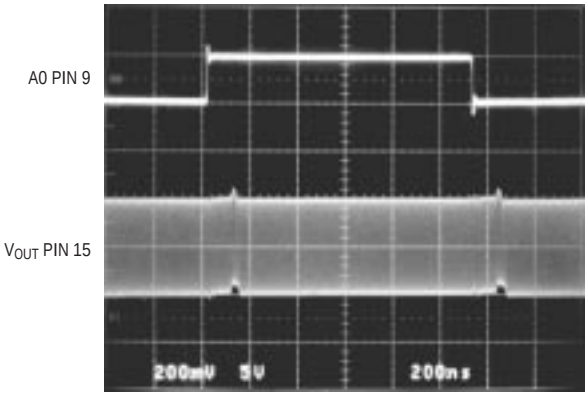
Switching Characteristics and Pin 8

Switching between channels is a "make-before-break" condition where both inputs are on momentarily. The buffers isolate the inputs when the "make-before-break" switching occurs. The input with the largest positive voltage determines the output level. If both inputs are equal, there is only a 40mV error at the input of the CFA during the transition. The reference adjust (Pin 8) allows the user to trade off positive input voltage range for switching time. For example, on ±15V supplies, setting the voltage on Pin 8 to –6.8V reduces the switching transient to a 50ns duration, and reduces the positive input range from 6V to 2.35V. The negative input range remains unchanged at –6V. When switching video "in picture," this short transient is imperceptible even on high quality

APPLICATIONS INFORMATION

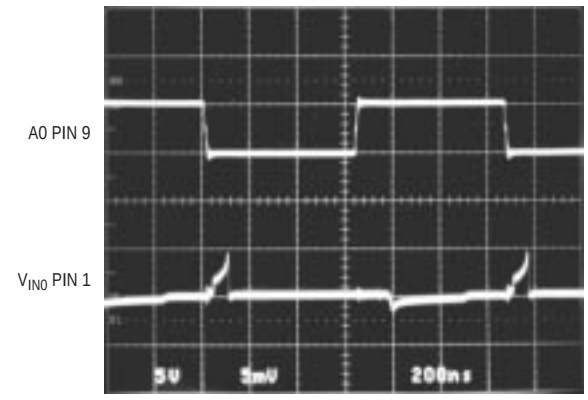
monitors. The reference pin has no effect when the LT1204 is operating on ±5V, and should be grounded. On supply voltages above ±8V, the range of voltages for Pin 8 should be between –6.5V and –7.5V. Reducing Pin 8 voltage below –7.5V turns "on" the "off" tee switch, and the isolation between channels is lost.

Channel-to-Channel Switching



V_{IN0} AND V_{IN1} CONNECTED TO 2MHz SINEWAVE
PIN 8 VOLTAGE = –6.8V, V_S = ±15V

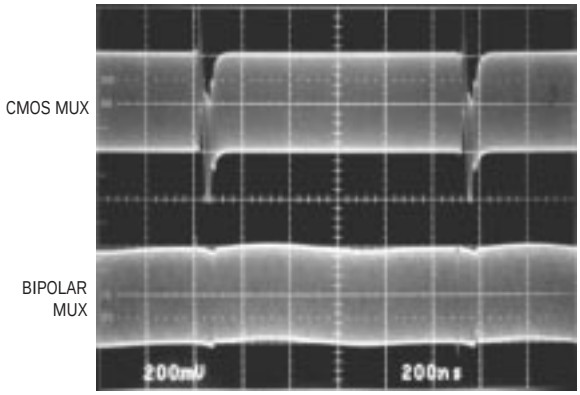
Transient at Input Buffer



SWITCHING BETWEEN V_{IN0} AND V_{IN1}
R_S = 50Ω, V_{REF} = –6.8V, V_S ±15V

Competitive video multiplexers built in CMOS are bidirectional and suffer from poor output-to-input isolation and cause transients to feed to the inputs. CMOS MUXs have been built with "break-before-make" switches to eliminate the talking between channels, but these suffer from output glitches large enough to interfere with sync circuitry. Multiplexers built on older bipolar processes that switch lateral PNP transistors take several microseconds to settle and blur the transition between pictures.

Competitive MUXs



V_{IN0} AND V_{IN1} CONNECTED TO 2MHz SINEWAVE

Crosstalk

The crosstalk, or more accurately all hostile crosstalk, is measured by driving a signal into any three of the four inputs and selecting the 4th input with the logic control. This 4th input is either shorted to ground or terminated in an impedance. All hostile crosstalk is defined as the ratio in decibel of the signal at the output of the CFA to the signal on the three driven inputs, and is input-referred. Disable crosstalk is measured with all four inputs driven and the part disabled. Crosstalk is critical in many applications where video multiplexers are used. In professional video systems, a crosstalk figure of –72dB is a desirable specification.

The key to the outstanding crosstalk performance of the LT1204 is the use of tee switches (see Figure 1). When the tee switch is on (Q2 off) Q1 and Q3 are a pair of emitter followers with excellent AC response for driving the CFA.

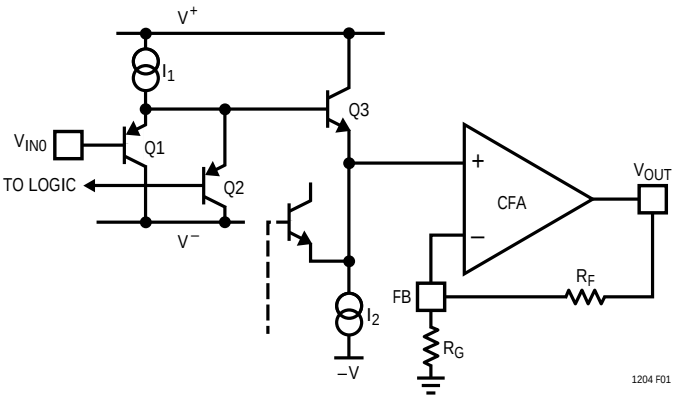


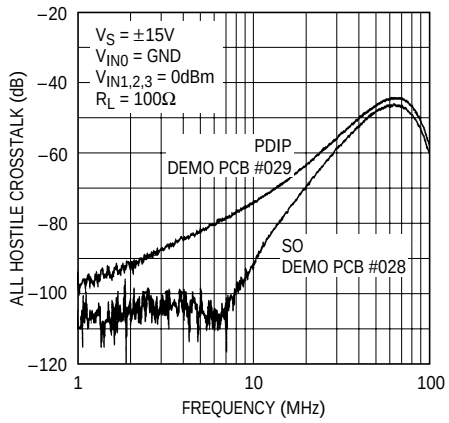
Figure 1. Tee Switch

APPLICATIONS INFORMATION

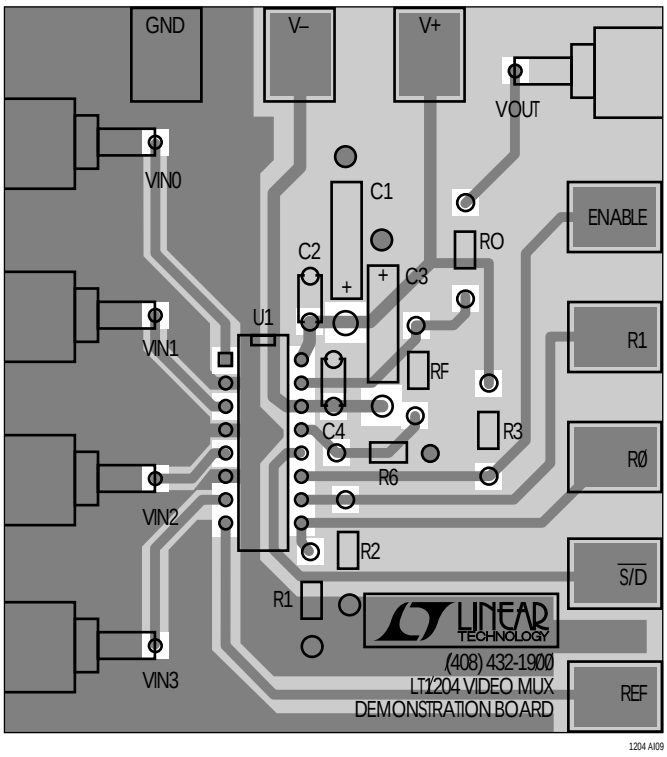
When the decoder turns off the tee switch (Q2 on) the emitter base junctions of Q1 and Q3 become reverse-biased while Q2 emitter absorbs current from I_1. Not only do the reverse-biased emitter base junctions provide good isolation, but any signal at V_{IN0} coupling to Q1 emitter is further attenuated by the shunt impedance of Q2 emitter. Current from I_2 is routed to any on switch.

Crosstalk performance is a strong function of the IC package, the PC board layout as well as the IC design. The die layout utilizes grounds between each input to isolate adjacent channels, while the output and feedback pins are on opposite sides of the die from the input. The layout of a PC board that is capable of providing –90dB all hostile crosstalk at 10MHz is not trivial. That level corresponds to a 30µV output below a 1V input at 10MHz. A demonstration board has been fabricated to show the component and ground placement required to attain these crosstalk numbers. A graph of all hostile crosstalk for both the PDIP and SO packages is shown. It has been found empirically from these PC boards that capacitive coupling across the package of greater than 3fF (0.003pF) will diminish the rejection, and it is recommended that this proven layout be copied into designs. The key to the success of the SO PC board #028 is the use of a ground plane guard around Pin 13, the feedback pin.

All Hostile Crosstalk

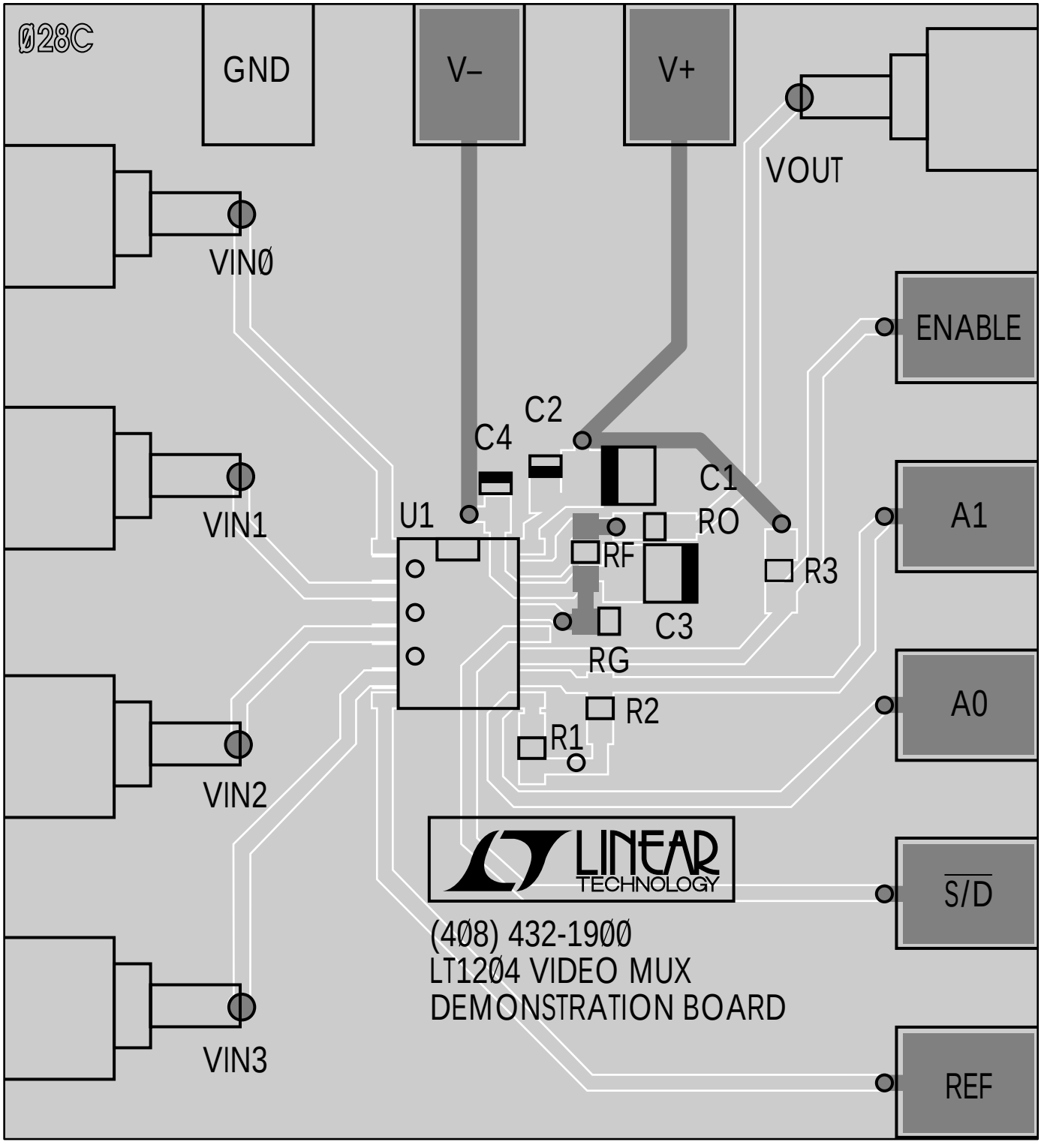


PDIP PC Board #029, Component Side



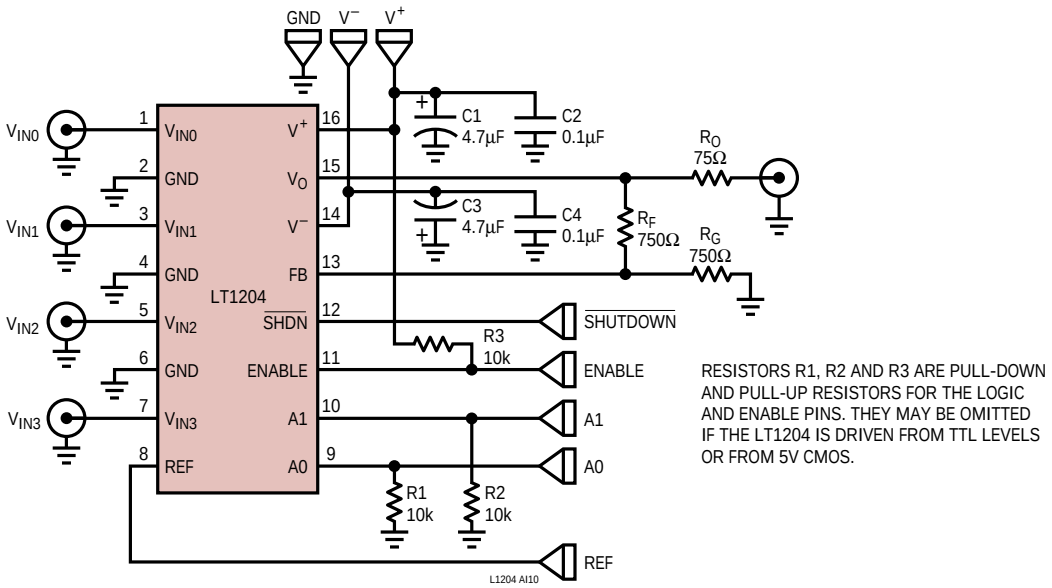
APPLICATIONS INFORMATION

SOL PC Board #028, Component Side



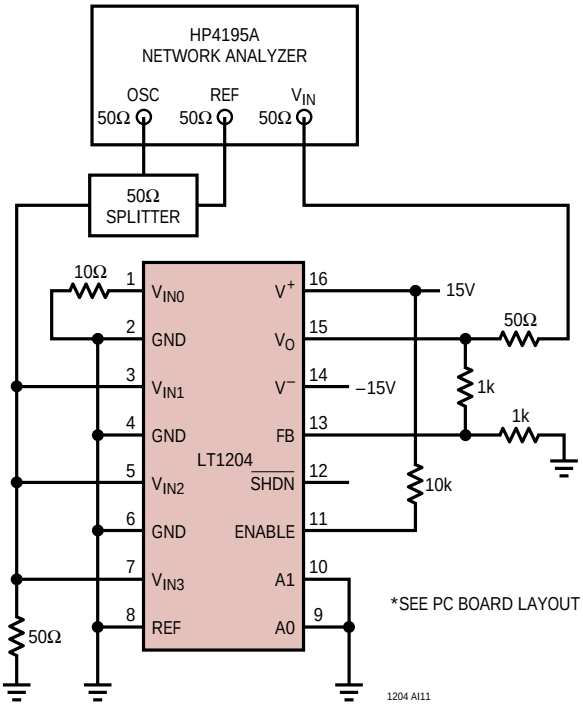
APPLICATIONS INFORMATION

Demonstration PC Board Schematic

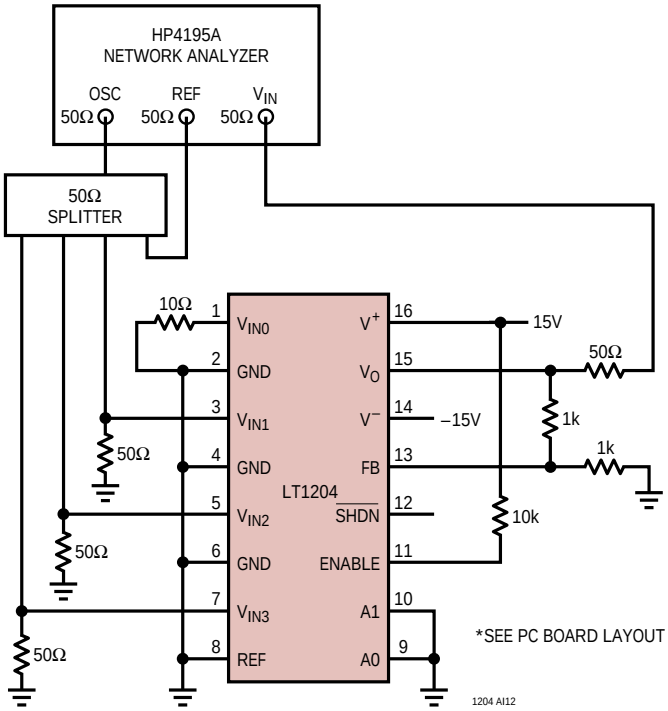


RESISTORS R1, R2 AND R3 ARE PULL-DOWN AND PULL-UP RESISTORS FOR THE LOGIC AND ENABLE PINS. THEY MAY BE OMITTED IF THE LT1204 IS DRIVEN FROM TTL LEVELS OR FROM 5V CMOS.

All Hostile Crosstalk Test Setup*



Alternate All Hostile Crosstalk Setup*

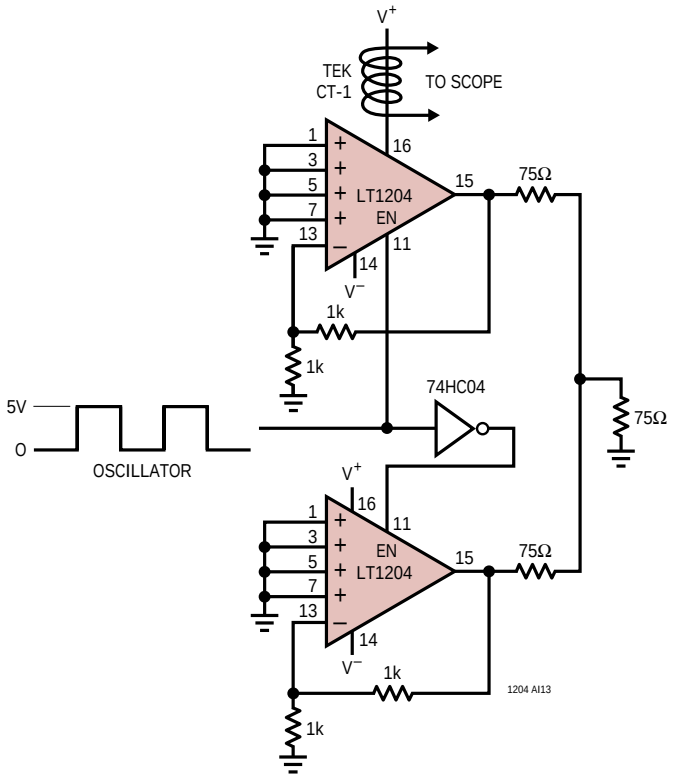


APPLICATIONS INFORMATION

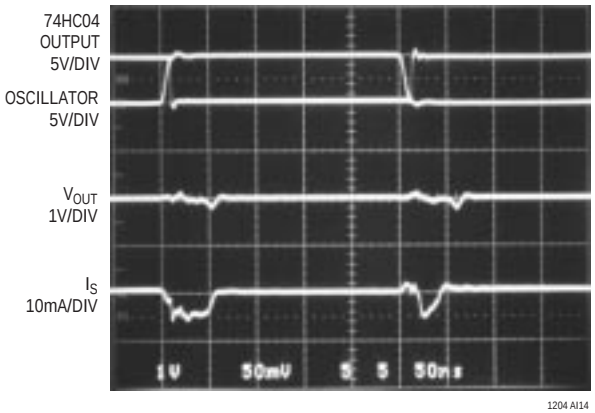
Multiplexer Expansion Pin 11 and Pin 12

To expand the number of MUX inputs, LT1204s can be paralleled by shorting their outputs together. The multiplexer disable logic has been designed to prevent shoot-through current when two or more amplifiers have their outputs shorted together. (Shoot-through current is a spike of power supply current caused by both amplifiers being on at once.)

Monitoring Supply Current Spikes



Timing and Supply Current Waveforms



The multiplexer uses a circuit to ensure the disabled amplifiers do not load or alter the cable termination. When the LT1204 is disabled (Pin 11 low) the output stage is turned off and an active buffer senses the output and drives the feedback pin to the CFA (Figure 2). This bootstraps the feedback resistors and raises the true output impedance of the circuit. For the condition where $R_F = R_G$ = 1k, the Disable Output Resistance is typically raised to 25k and drops to 20k for A_V = 10, R_F = 2k and R_G = 222Ω due to loading of the feedback buffer. Operating the Disable feature with R_G < 100Ω is not recommended.

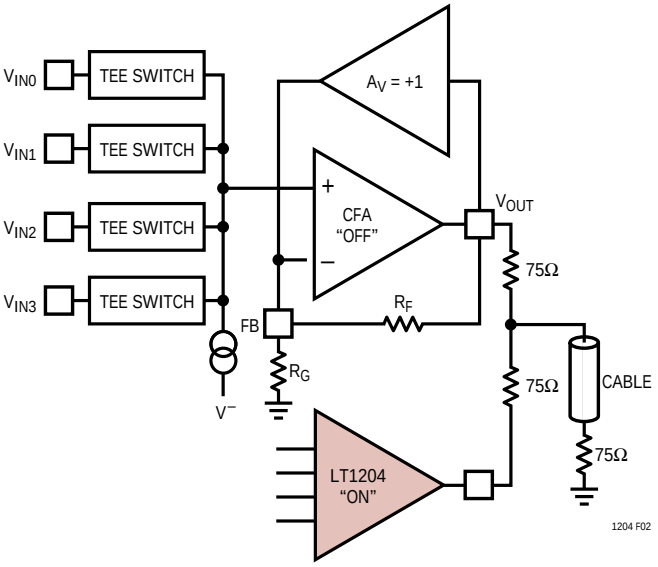


Figure 2. Active Buffer Drives FB Pin 13

A shutdown feature (Pin 12 low) reduces the supply current to 1.5mA and lowers the power dissipation when the LT1204 is not in use. If the part is shut down, the bootstrapping is inoperative and the feedback resistors will load the output. If the CFA is operated at a gain of +1, however, the feedback resistor will not load the output even in shutdown because there is no resistive path to ground, but there will be a –6dB loss through the cable system.

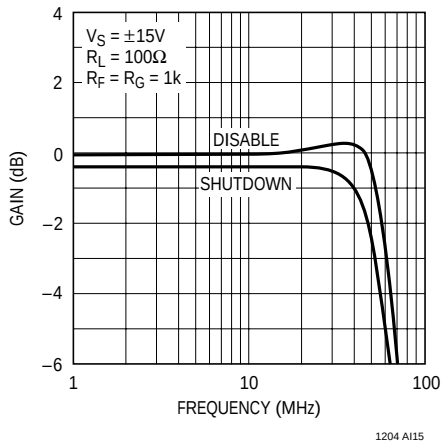
A frequency response plot shows the effect of using the disable feature versus using the shutdown feature. In this example four LT1204s were connected together at their outputs forming a 16-to-1 MUX. The plot shows the effect of the bootstrapping circuit that eliminates the

APPLICATIONS INFORMATION

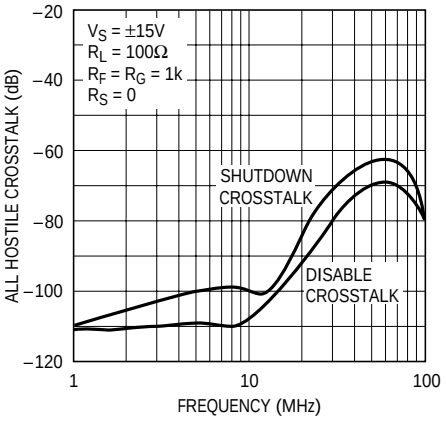
improper cable termination due to feedback resistors loading the cable.

The limit to the number of expanded inputs is set by the acceptable error budget of the system.

16-to-1 MUX Response Using Disable vs Shutdown



16-to-1 Multiplexer All Hostile Crosstalk



For a 64-to-1 MUX we need sixteen LT1204s. The equivalent load resistance due to the feedback resistor R_{EQ} in Disable is 25k/15 = 1.67k. See Figure 3.

$$V_O = \frac{75R_{EQ}}{75(75) + 150R_{EQ}}, V_O = 0.489V$$

This voltage represents a 2.1% loading error. If the shutdown feature is used instead of the disable feature, then the LT1204 could expand to only an 8-to-1 MUX for the same error.

As a practical matter the gain error at frequency is also set by capacitive loading. The disabled output capacitance of the LT1204 is about 8pF, and in the case of sixteen LT1204s, it would represent a 128pF load. The combination of 1.67k and 128pF correspond to about a 0.3dB roll-off at 5MHz.

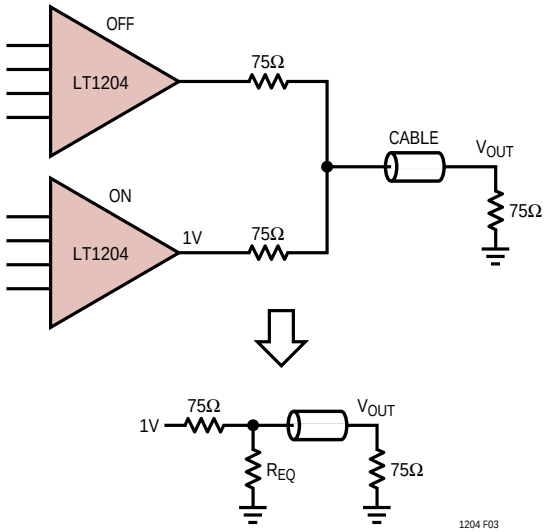


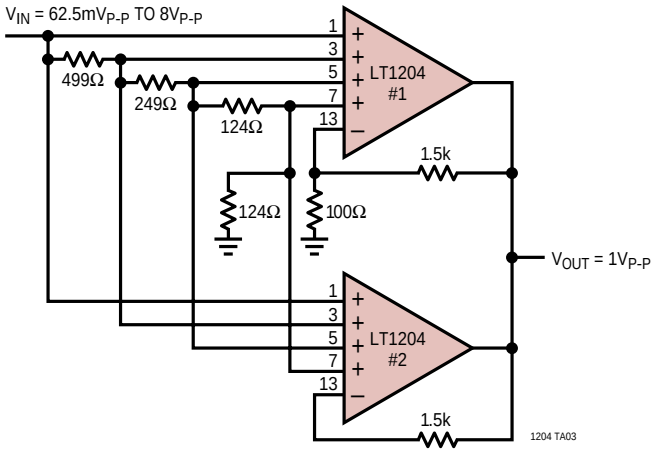
Figure 3. Equivalent Loading Schematic

TYPICAL APPLICATIONS

Programable Gain Amplifier (PGA)

Two LT1204s and seven resistors make a Programable Gain Amplifier with a 128-to-1 gain range. The gain is proportional to 2^N where N is the 3-bit binary value of the select logic. An input attenuator alters the input signal by 1, 0.5, 0.25 and 0.125 to form an amplifier with a gain of 16, 8, 4, 2, when LT1204 #1 is selected. LT1204 #2 is connected to the same attenuator. When enabled (LT1204 #1 disabled), it results in gain of 1, 0.5, 0.25 and 0.125. The wide input common mode range of the LT1204 is needed to accept inputs of $8V_{P-P}$.

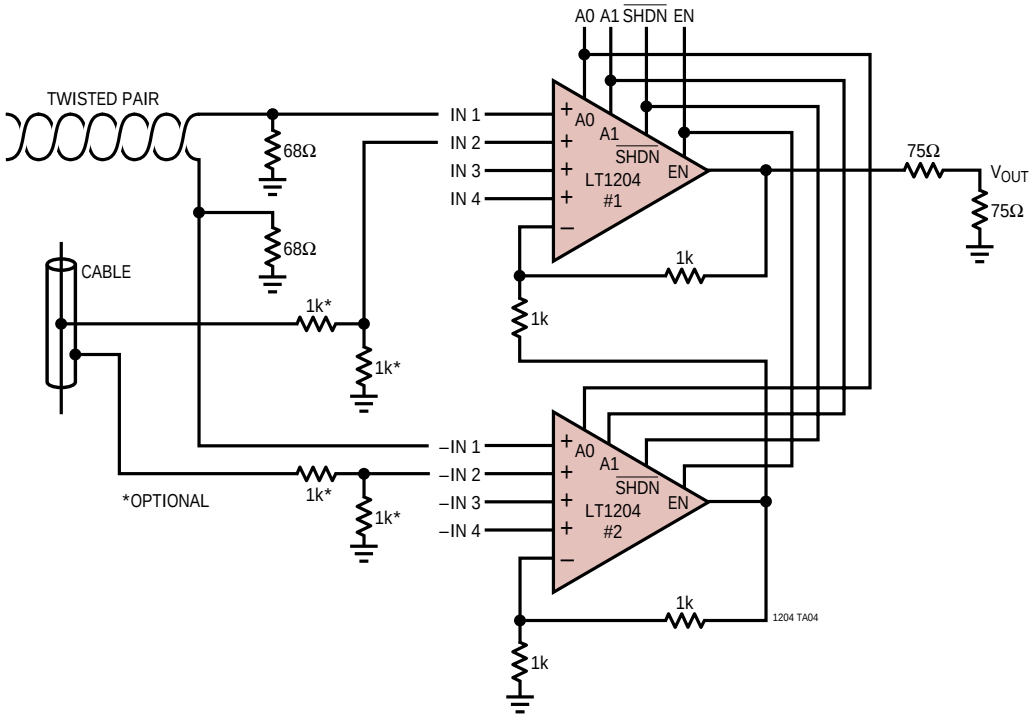
Programable Gain Amplifier Accepts Inputs from 62.5mV$_{P-P}$ to 8V$_{P-P}$



4-Input Differential Receiver

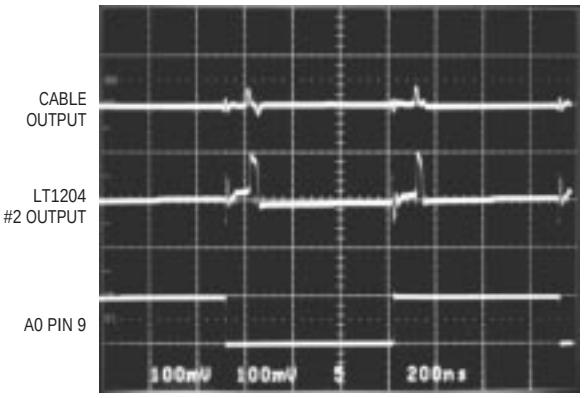
LT1204s can be connected inverting and noninverting as shown to make a 4-input differential receiver. The receiver can be used to convert differential signals sent over a low cost twisted pair to a single-ended output or used in video loop-thru connections. The logic inputs A0 and A1 are tied together because the same channels are selected on each LT1204. By using the Disable feature, the number of differential inputs can be increased by adding pairs of LT1204s and tying the outputs of the noninverting LT1204s (#1) together. Switching transients are reduced in this receiver because the transient from LT1204 #2 subtracted from the transient of LT1204 #1.

4-Input Differential Receiver



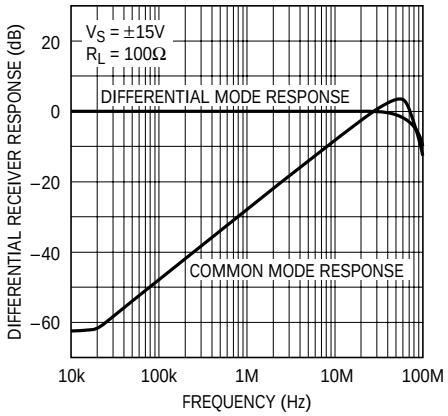
TYPICAL APPLICATIONS

Differential Receiver Switching Waveforms



1204 TA05

Differential Receiver Response

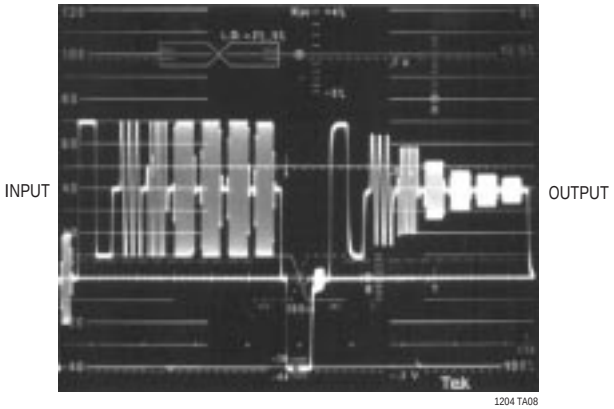


1204 TA06

4-Input Twisted-Pair Driver

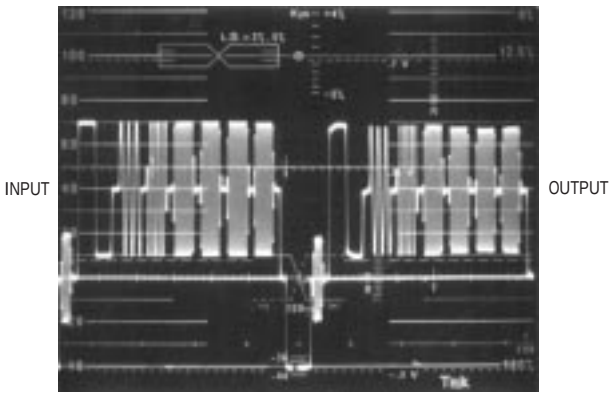
It is possible to send and receive color composite video signals appreciable distances on a low cost twisted pair. The cost advantage of this technique is significant. Standard 75Ω RG-59/U coaxial cable cost between 25¢ and 50¢ per foot. PVC twisted pair is only pennies per foot. Differential signal transmission resists noise because the interference is present as a common mode signal. The LT1204 can select one of four video cameras for instance, and drive the video signal on to the twisted pair. The circuit uses an LT1227 current feedback amplifier connected with a gain of –2, and an LT1204 with a gain of 2. The 47Ω resistors back-terminate the low cost cable in its characteristic impedance to prevent reflections. The receiver for the differential signal is an LT1193 connected for a gain of 2. Resistors R1, R2 and capacitors C1, C2 are used for cable compensation for loss through the twisted pair. Alternately, a pair of LT1204s can be used to perform the differential to single-ended conversion.

Multiburst Pattern Passed Through 1000 Feet of Twisted Pair, No Cable Compensation



1204 TA08

Multiburst Pattern Passed Through 1000 Feet of Twisted Pair, with Cable Compensation



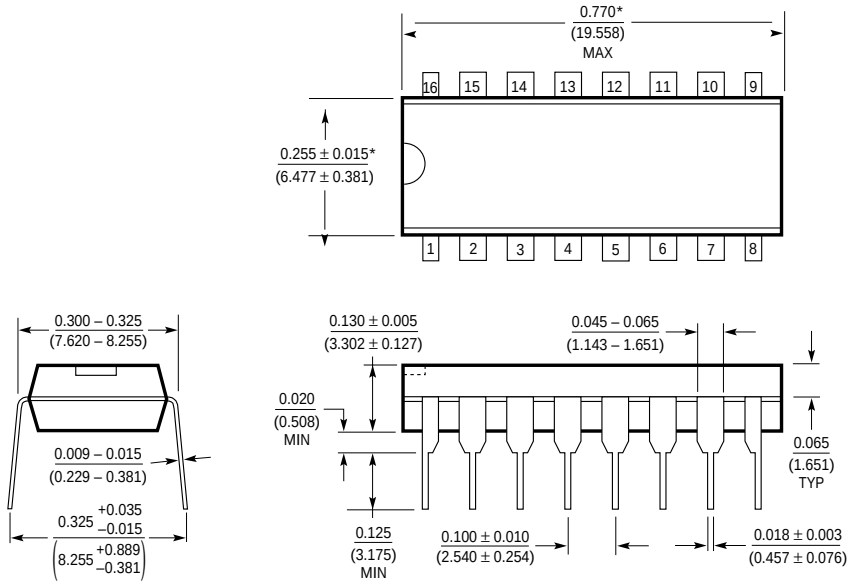
1204 TA09

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead PDIP (Narrow 0.300)

(LTC DWG # 05-08-1510)

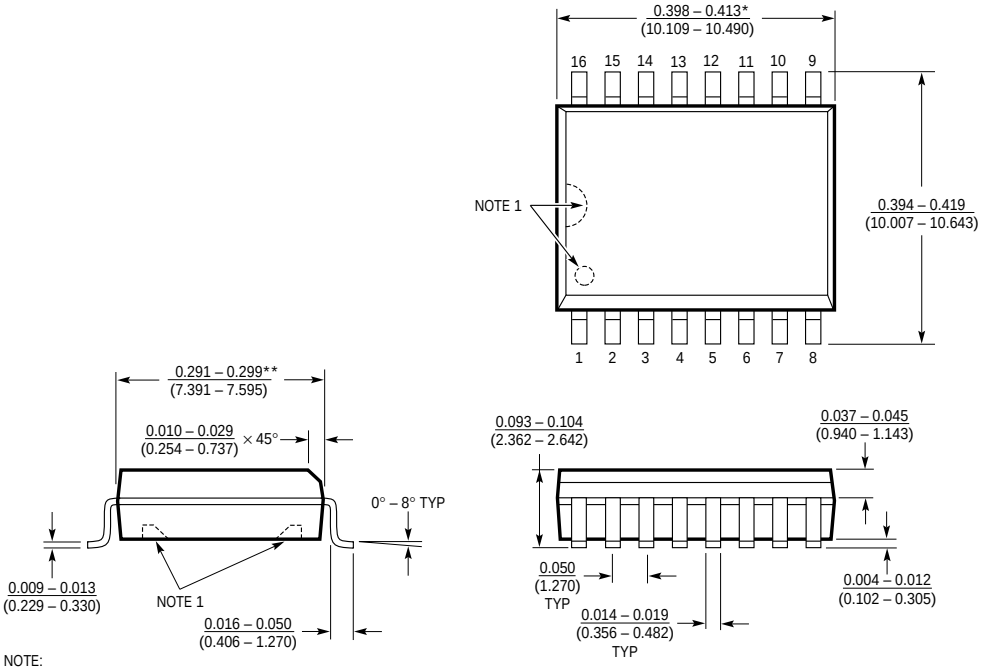


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1197

SW Package
16-Lead Plastic Small Outline (Wide 0.300)

(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

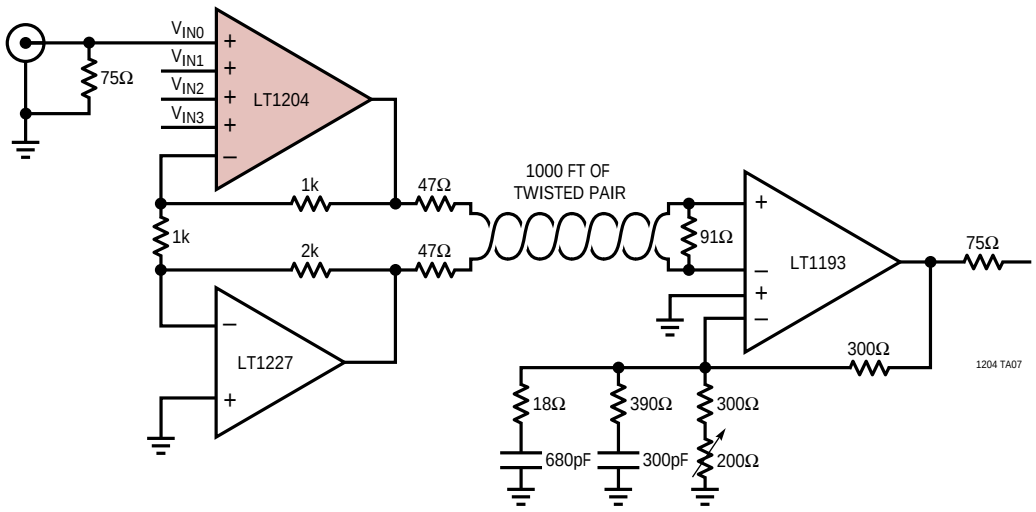
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S16 (WIDE) 0396

TYPICAL APPLICATION

4-Input Twisted-Pair Driver/Receiver



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1203/LT1205	150MHz Video Multiplexer	High Speed, but No Cable Driving
LT1259/LT1260	Dual and Triple Current Feedback Amplifiers	Low Cost, with Shutdown
LT1675	RGB Multiplexer with Current Feedback Amplifiers	Very High Speed, Pixel Switching

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