

ORDER NUMBER(S):**LPC47N217N-ABZJ for 56-pin QFN Lead-free ROHS Compliant package****LPC47N217N-ABZJ-TR for 56-pin QFN Lead-free ROHS Compliant package (tape and reel)**

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Copyright © 2009 SMSC or its subsidiaries. All rights reserved.

Circuit diagrams and other information relating to SMSC products are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. SMSC reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your local SMSC sales office to obtain the latest specifications before placing your product order. The provision of this information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights or other intellectual property rights of SMSC or others. All sales are expressly conditional on your agreement to the terms and conditions of the most recently dated version of SMSC's standard Terms of Sale Agreement dated before the date of your order (the "Terms of Sale Agreement"). The product may contain design defects or errors known as anomalies which may cause the product's functions to deviate from published specifications. Anomaly sheets are available upon request. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer. Copies of this document or other SMSC literature, as well as the Terms of Sale Agreement, may be obtained by visiting SMSC's website at <http://www.smSC.com>. SMSC is a registered trademark of Standard Microsystems Corporation ("SMSC"). Product names and company names are the trademarks of their respective holders.

SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE. IN NO EVENT SHALL SMSC BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF SMSC OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER OR NOT SMSC HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.



General Description

The SMSC LPC47N217N is a 3.3V PC 99, PC2001, and ACPI 2.0 compliant Super I/O Controller. The LPC47N217N implements the LPC interface, a pin reduced ISA interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The part also includes 13 GPIO pins.

The LPC47N217N incorporates a 16C550A compatible UART and one Multi-Mode parallel port with ChiProtect™ circuitry plus EPP and ECP support. The LPC47N217N is easy to use and offers lower system cost and reduced board area.

The LPC47N217N offers a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI CLKRUN# support, relocatable configuration ports, and three DMA channel options.

The parallel port is compatible with IBM PC/AT architectures, as well as IEEE 1284 EPP and ECP. The parallel port ChiProtect™ circuitry prevents damage caused by an attached powered printer when the LPC47N217N is not powered.

The LPC47N217N features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the parallel port and UART.

The LPC47N217N supports the ISA Plug-and-Play Standard register set (Version 1.0a) and provides the recommended functionality to support Windows operating systems, PC99, and PC2001. The I/O Address, DMA Channel, and Hardware IRQ of each device in the LPC47N217N may be reprogrammed through the internal configuration registers. There are multiple I/O address location options, a Serialized IRQ interface, and three DMA channels.

Block Diagram

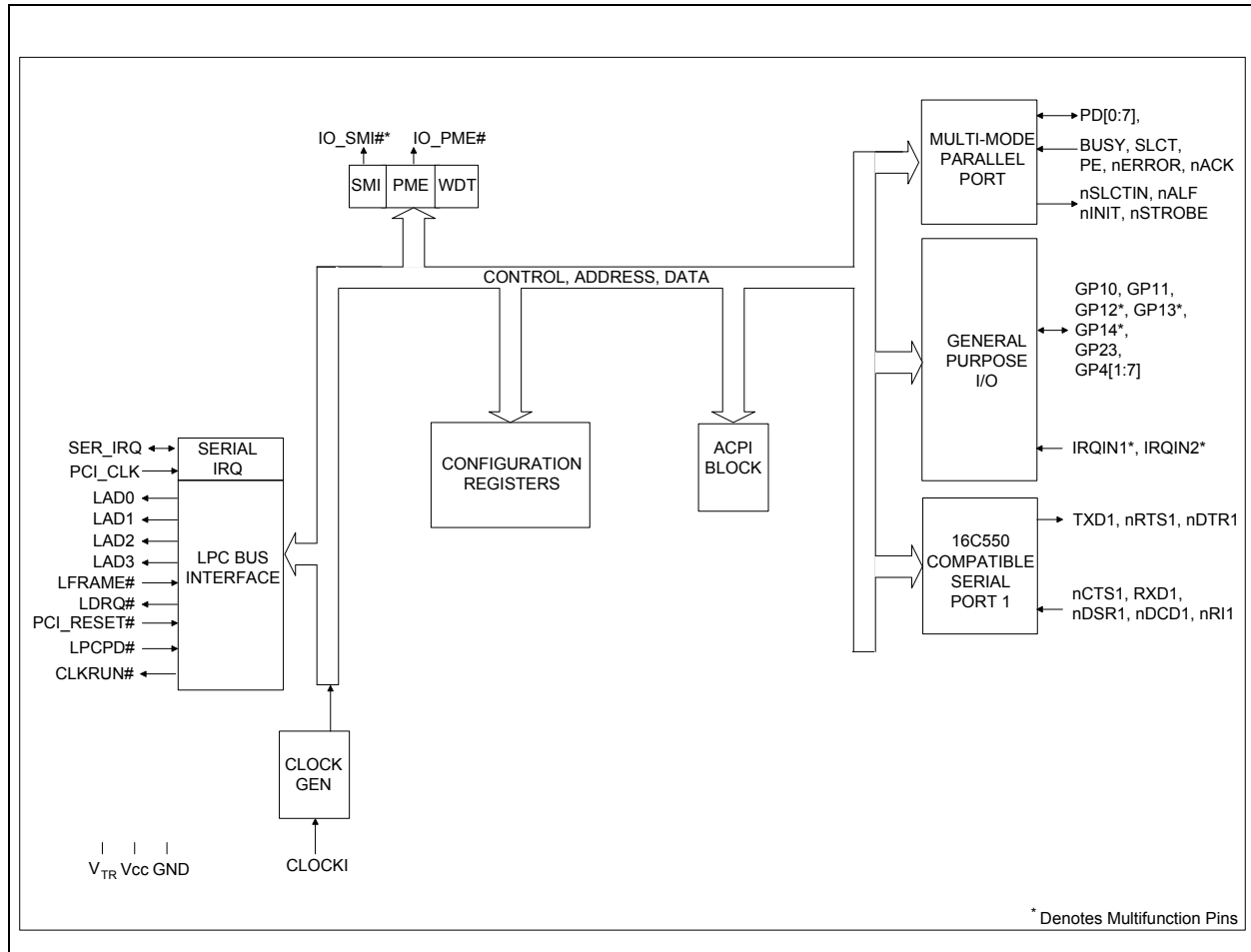


Figure 1 LPC47N217N Block Diagram

REVISION HISTORY

REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL RELEASE	2/07/04	S.K.IJUEV
B	REMOVE "PRELIMINARY" NOTE	10/10/04	S.K.IJUEV
C	LIBRARY FROM 0.95 TO 0.55 ADDED D2/E2 VARIATIONS TABLE	7/20/05	S.K.IJUEV

TOP VIEW

BOTTOM VIEW

SIDE VIEW

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	—	1.00	—	OVERALL PKG HEIGHT
A1	0	0.02	0.05	—	STANDOFF
A2	—	—	0.90	—	MOLD THICKNESS
D/E	7.85	8.00	8.15	—	"X"/"Y" BODY SIZE
D1/E1	7.55	—	7.95	—	"X"/"Y" MOLD SIZE
D2/E2	SEE VARIATIONS			—	"X"/"Y" EXPOSED PAD SIZE
L	0.30	—	0.50	—	TERMINAL LENGTH
b	0.18	0.25	0.30	2	TERMINAL WIDTH
e	0.50 BSC			—	TERMINAL PITCH

D2 / E2 VARIATIONS

MIN	NOM	MAX	NOTE	CATALOG PART
4.15	4.30	4.45	—	USB3250, USB3500 & EMC2700

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETER.
- POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS $\pm 0.05\text{mm}$ AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
- DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

3-D VIEWS

PACKAGE OUTLINE

56 TERMINAL QFN, 8x8mm BODY, 0.5mm PITCH

MO-56-QFN-8x8

JEDEC MO-220

1 OF 1