ORDER NUMBER(S):

LPC47N217N-ABZJ for 56-pin QFN Lead-free ROHS Compliant package

LPC47N217N-ABZJ-TR for 56-pin QFN Lead-free ROHS Compliant package (tape and reel)

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

General Description

The SMSC LPC47N217N is a 3.3V PC 99, PC2001, and ACPI 2.0 compliant Super I/O Controller. The LPC47N217N implements the LPC interface, a pin reduced ISA interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The part also includes 13 GPIO pins.

The LPC47N217N incorporates a 16C550A compatible UART and one Multi-Mode parallel port with ChiProtect™ circuitry plus EPP and ECP support. The LPC47N217N is easy to use and offers lower system cost and reduced board area.

The LPC47N217N offers a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI CLKRUN# support, relocatable configuration ports, and three DMA channel options.

The parallel port is compatible with IBM PC/AT architectures, as well as IEEE 1284 EPP and ECP. The parallel port ChiProtect™ circuitry prevents damage caused by an attached powered printer when the LPC47N217N is not powered.

The LPC47N217N features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the parallel port and UART.

The LPC47N217N supports the ISA Plug-and-Play Standard register set (Version 1.0a) and provides the recommended functionality to support Windows operating systems, PC99, and PC2001. The I/O Address, DMA Channel, and Hardware IRQ of each device in the LPC47N217N may be reprogrammed through the internal configuration registers. There are multiple I/O address location options, a Serialized IRQ interface, and three DMA channels.

PRODUCT PREVIEW

Block Diagram

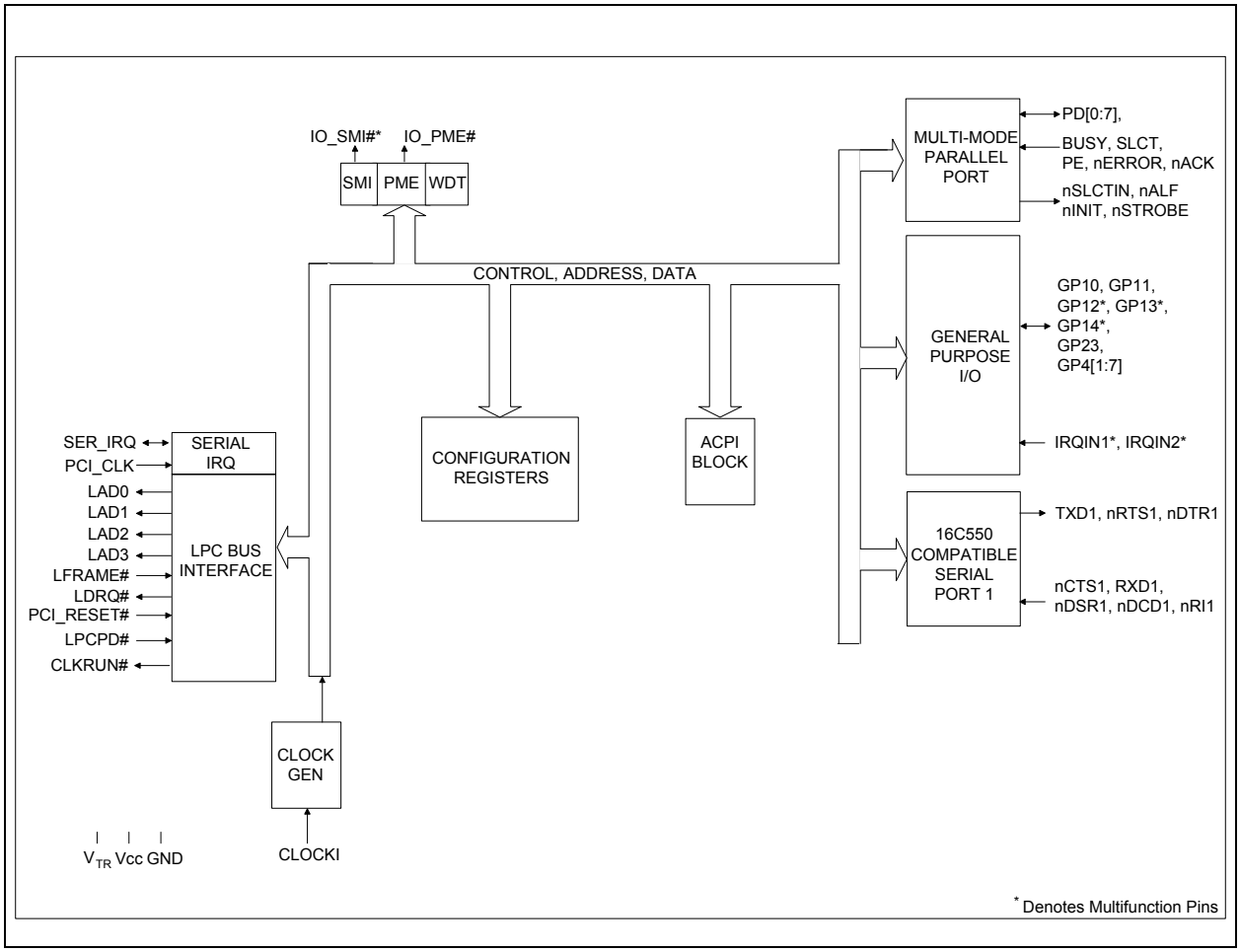

Figure 1 LPC47N217N Block Diagram

PRODUCT PREVIEW

Package Outline

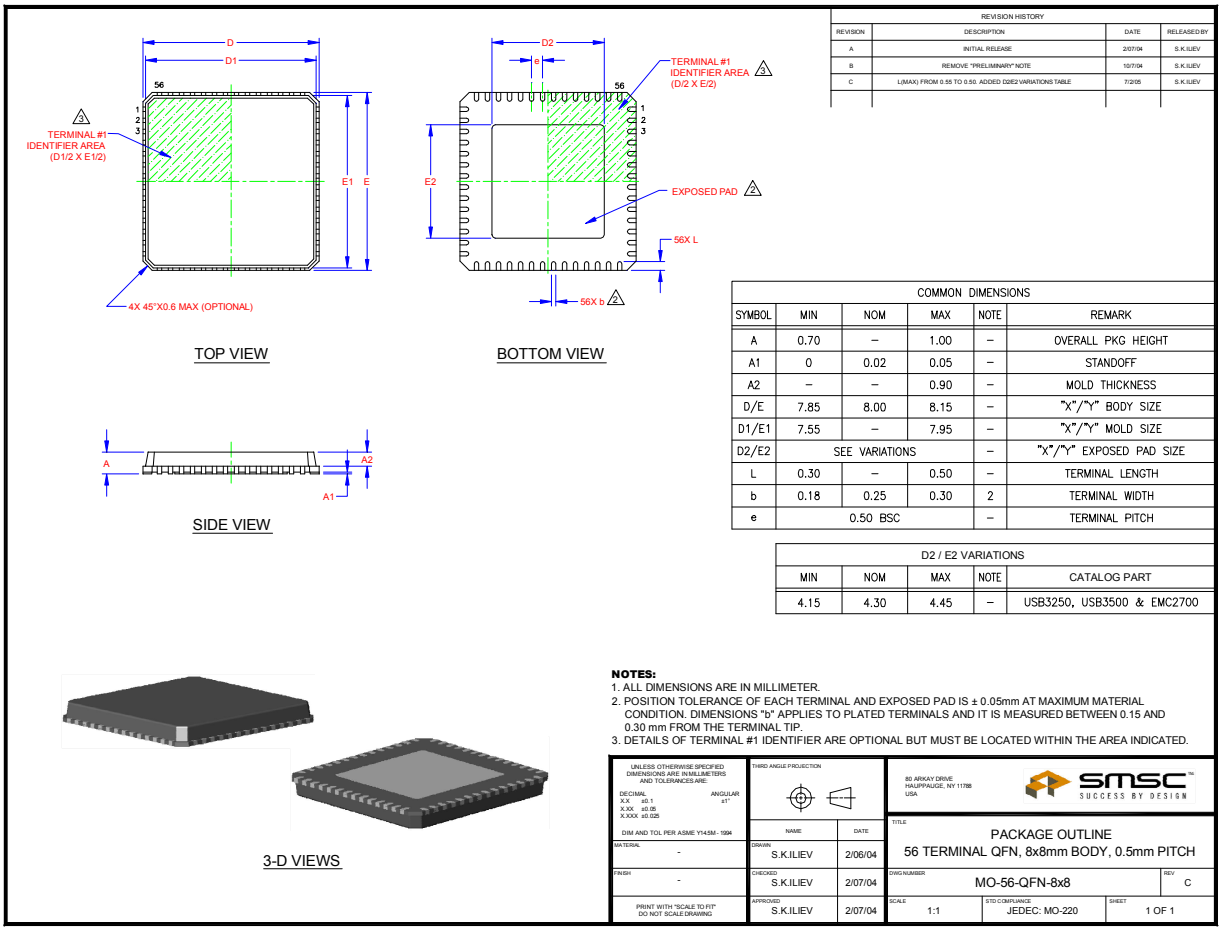

Figure 2 LPC47N217N 56-Pin QFN Package, 8x8mm Body, 0.5mm Pitch