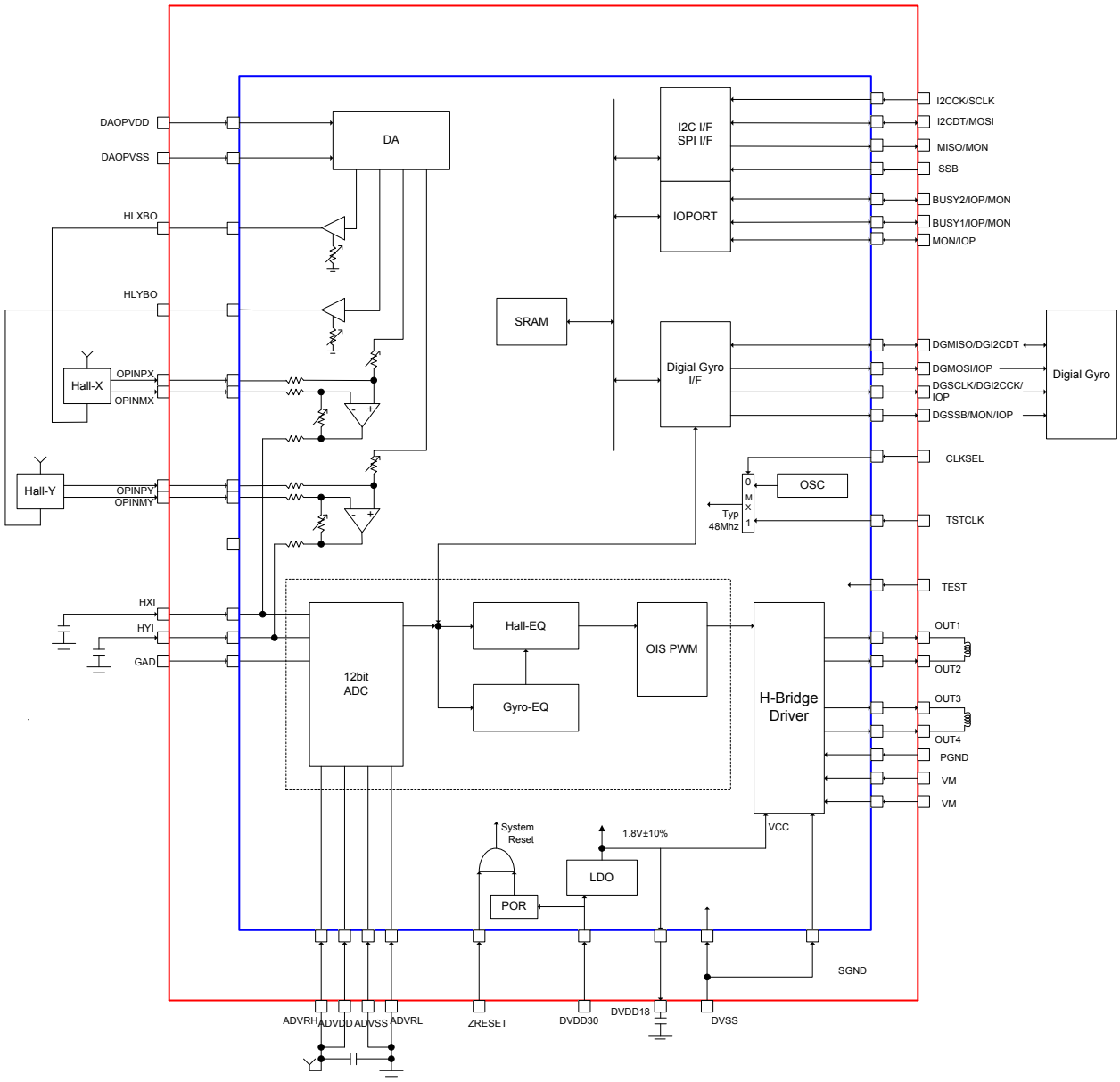
Block Diagram

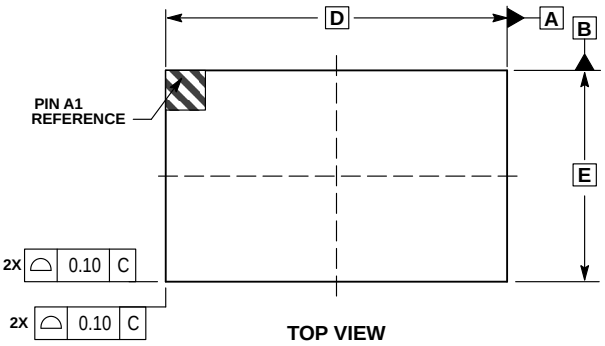


Example of wiring diagram [Hall] in LC898121XA (WLP40)

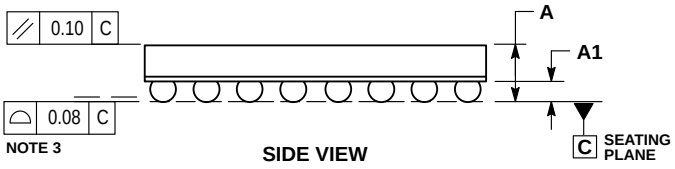
Package Dimensions

unit : mm

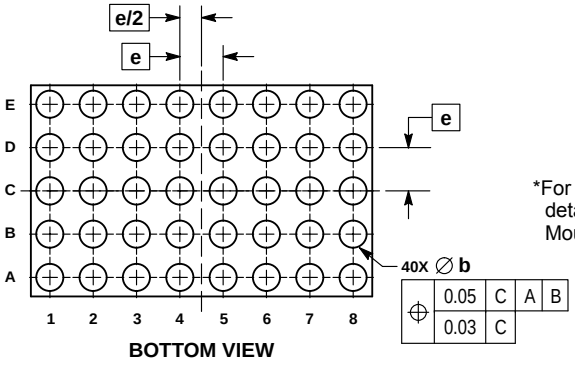
WLCSP40, 2.44x3.94
CASE 567JB
ISSUE O



TOP VIEW



SIDE VIEW

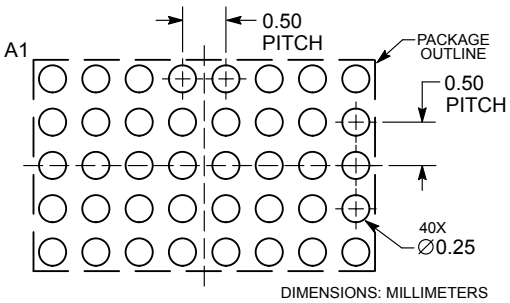


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS MIN	MAX
A	---	0.65
A1	0.15	0.24
b	0.22	0.32
D	2.44 BSC	
E	3.94 BSC	
e	0.50 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment

WLP40

Bottom View

	E	D	C	B	A
8	OPINPX	OPINMY	ADVDD	ADVSS	HXI
7	OPINMX	OPINPY	ADVRH	ADVRL	HYI
6	HLXBO	HLYBO	DAOPVDD	DAOPVSS	I2CCK
5	DGSCLK	DGMOSI	GAD	MISO	I2CDT
4	DGMISO	DGSSB	MON	SSB	DVDD18
3	DVSS	CLKSEL	TSTCLK	TEST	DVDD30
2	VM	BUSY2	BUSY1	ZRESET	VM
1	OUT4	OUT3	PGND	OUT2	OUT1

Driver
AD 3V
VGA&DAC 3V
Digital GND
Digital 3V VDD
Logic Core 1.8V VDD (Output)

<typ> I : INPUT, O : OUTPUT, B : BIDIRECTION, P : Power

Ball No	Pin Name	type	Description
A1	OUT1	O	Driver Output
A2	VM	P	Driver VDD (2.6V to 5.5V)
A3	DVDD30	P	Logic 3V VDD (2.6V to 3.6V)
A4	DVDD18	P	LDO Power supply out (Logic Core VDD (typ 1.8 V))
A5	I2CDT	B	I2C_IF data (B) / SPI IF data (I)
A6	I2CCK	I	I2C_IF clock / SPI IF clock
A7	HYI	I	Hall-Y AD input
A8	HXI	I	Hall-X AD input
B1	OUT2	O	Driver output
B2	ZRESET	I	HardWafer Reset
B3	TEST	I	SPI & External clock case sets [1]. other cases set [0]
B4	SSB	B	SPI I/F Chip Select (I) / General-purpose IOPORT(B) / inner signal monitor(O)
B5	MISO	B	SPI I/F data(O) / inner signal monitor / General-purpose IOPORT
B6	DAOPVSS	P	DA&OpAmp VSS
B7	ADVRL	I	ADC ReferenceVoltage Low input
B8	ADVSS	I	AD GND
C1	PGND	P	Driver GND
C2	BUSY1	B	BUSY1(O) / General-purpose IOPORT(B) / inner signal monitor(O)
C3	TSTCLK	I	CLKSEL=1 : External Clock, CLKSEL=0 : change pin of I^2C(0) and SPI(1)
C4	MON	B	inner signal monitor / general-purpose IOPORT
C5	GAD	I	General AD input
C6	DAOPVDD	P	DA&OpAmp VDD (2.6V to 3.6V)
C7	ADVRH	I	ADC ReferenceVoltage High input
C8	ADVDD	P	AD VDD (2.6V to 3.6V)
D1	OUT3	O	Driver output
D2	BUSY2	B	BUSY2 (O) / General-purpose IOPORT(B) / inner signal monitor(O)
D3	CLKSEL	I	change pin of OSC(0) and External clock(1)
D4	DGSSB	B	Digital Gyro SPI IF Chip Select(O) / inner signal monitor(O) / General-purpose IOPORT(B)
D5	DGMOSI	B	Digital Gyro (4-wire) IF data(O) / General-purpose IOPORT(B)
D6	HLYBO	O	Hall-Y Bias (Current drive)
D7	OPINPY	I	Hall-Y OpAmp input+
D8	OPINMY	I	Hall-Y OpAmp input-
E1	OUT4	O	Driver output
E2	VM	P	Driver VDD (2.6V to 5.5V)
E3	DVSS	P	Logic GND
E4	DGMISO	B	Digital Gyro SPI IF data(I) / Digital Gyro I^2C IF data(B)
E5	DGSCLK	B	Digtal Gyro SPI IF clock (O) /Digital Gyro I^2C IF clock(O) / General purpose IOPORT (B)
E6	HLXBO	O	Hall-Y Bias (Current drive)
E7	OPINMX	I	Hall-X OpAmp input-
E8	OPINPX	I	Hall-X OpAmp input+

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898121XA-MH	WLCP40, 2.44x3.94 (Pb-Free / Halogen Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF