Order Numbers:

LAN8700C-AEZG for 36-pin, QFN lead-free RoHS compliant package

LAN8700iC-AEZG for (Industrial Temp) 36-pin, QFN lead-free RoHS compliant package

4900 pcs per tray

LAN8700C-AEZG-TR for 36-pin, QFN lead-free RoHS compliant package (tape and reel)

3000 pcs per reel

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

General Description

The SMSC LAN8700/LAN8700i is a low-power, industrial temperature (LAN8700i), variable I/O voltage, analog interface IC with HP Auto-MDIX support for high-performance embedded Ethernet applications. The LAN8700/LAN8700i can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.8V linear regulator. An option is available to disable the linear regulator to optimize system designs that have a 1.8V power plane available.

0.1 Architectural Overview

The LAN8700/LAN8700i consists of an encoder/decoder, scrambler/descrambler, wave-shaping transmitter, output driver, twisted-pair receiver with adaptive equalizer and baseline wander (BLW) correction, and clock and data recovery functions. The LAN8700/LAN8700i can be configured to support either the Media Independent Interface (MII) or the Reduced Media Independent Interface (RMII).

The LAN8700/LAN8700i is compliant with IEEE 802.3-2005 standards (MII Pins tolerant to 3.6V) and supports both IEEE 802.3-2005 compliant and vendor-specific register functions. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10-Mbps (10BASE-T) operation on Category 3 and Category 5 unshielded twisted-pair cable, and 100-Mbps (100BASE-TX) operation on Category 5 unshielded twisted-pair cable.

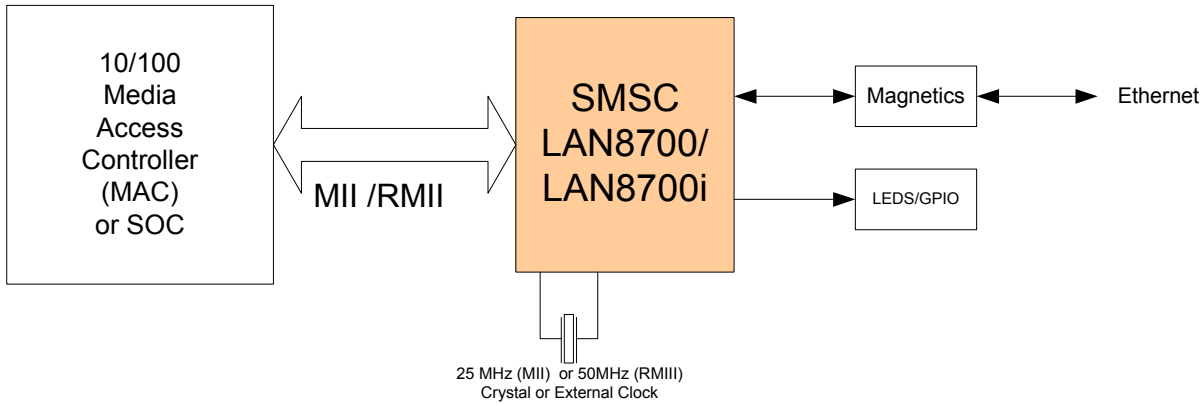

Figure 1 LAN8700/LAN8700i System Block Diagram

Hubs and switches with multiple integrated MACs and external PHYs can have a large pin count due to the high number of pins needed for each MII interface. An increasing pin count causes increasing cost.

The RMII interface is intended for use on Switch based ASICs or other embedded solutions requiring minimal pincount for ethernet connectivity. RMII requires only 6 pins for each MAC to PHY interface plus one common reference clock. The MII requires 16 pins for each MAC to PHY interface.

The SMSC LAN8700/LAN8700i is capable of running in RMII mode. Please contact your SMSC sales representative for the latest RMII specification.

The LAN8700/LAN8700i referenced throughout this document applies to both the commercial temperature and industrial temperature components. The LAN8700i refers to only the industrial temperature component.

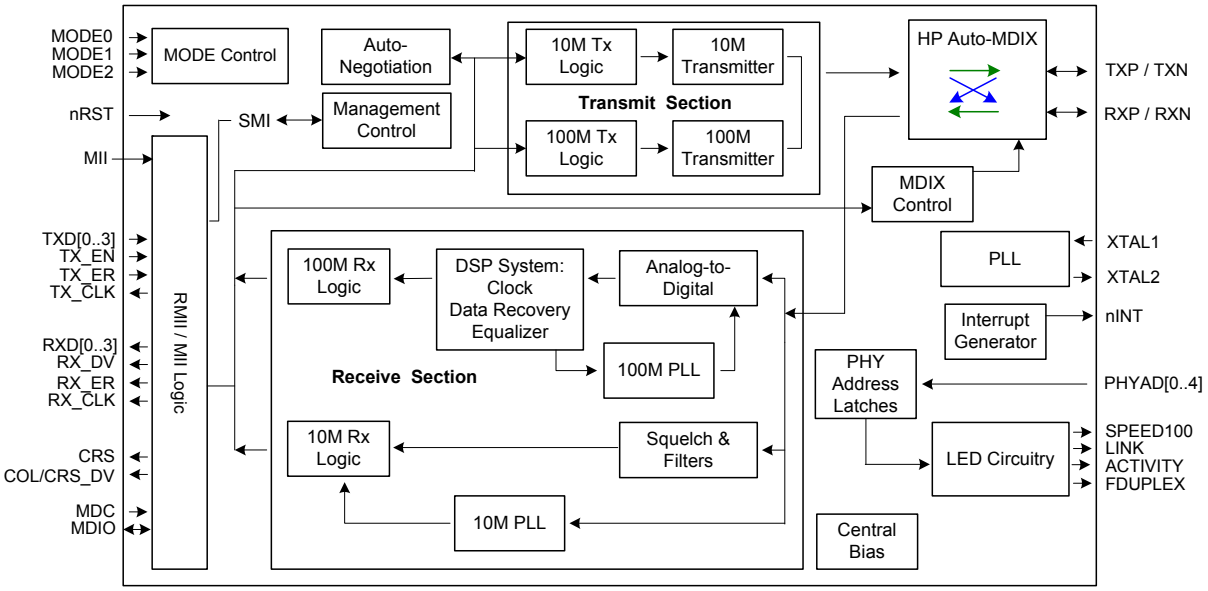

Figure 2 LAN8700/LAN8700i Architectural Overview

Pin Diagram

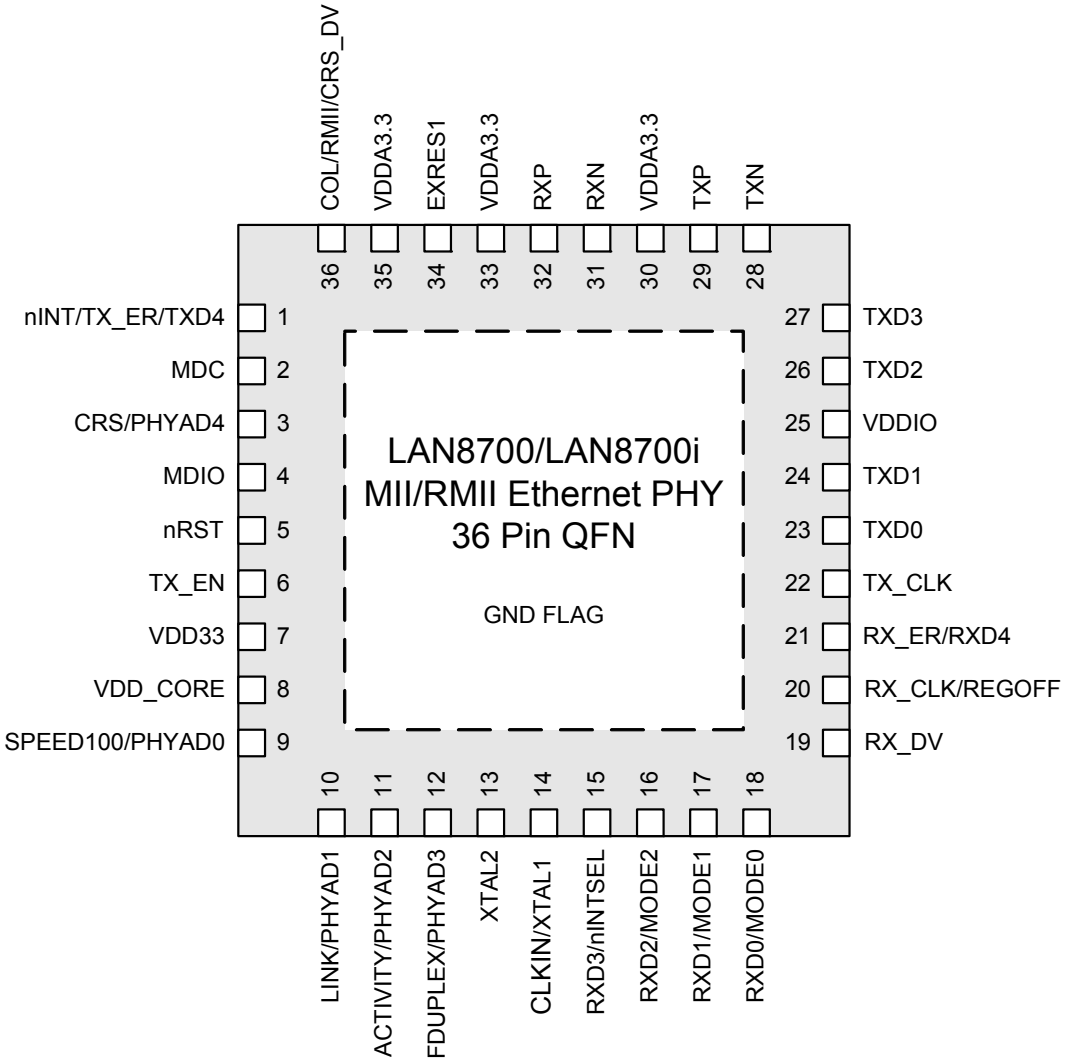

Figure 3 LAN8700/LAN8700i Package Pin Diagram (Top View)

Table 1 LAN8700/LAN8700i 36-PIN QFN Pinout

PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	nINT/TX_ER/TXD4	19	RX_DV
2	MDC	20	RX_CLK/REGOFF
3	CRS/PHYAD4	21	RX_ER/RXD4
4	MDIO	22	TXCLK
5	nRST	23	TXD0
6	TX_EN	24	TXD1
7	VDD33	25	VDDIO
8	VDD_CORE	26	TXD2
9	SPEED100/PHYAD0	27	TXD3
10	LINK/PHYAD1	28	TXN
11	ACTIVITY/PHYAD2	29	TXP
12	FDUPLEX/PHYAD3	30	VDDA3.3
13	XTAL2	31	RXN
14	CLKIN/XTAL1	32	RXP
15	RXD3/nINTSEL	33	VDDA3.3
16	RXD2/MODE2	34	EXRES1
17	RXD1/MODE1	35	VDDA3.3
18	RXD0/MODE0	36	COL/MII/CRS_DV

PRODUCT PREVIEW

Pin Description

This section describes the signals on each pin. When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

I/O Signals

I Input. Digital LVCMOS levels.

O Output. Digital LVCMOS levels.

I/O Input or Output. Digital LVCMOS levels.

Note: The digital signals are not 5V tolerant.They are variable voltage from +1.6V to +3.6V.

AI Input. Analog levels.

AO Output. Analog levels.

Table 2 MII Signals

SIGNAL NAME	TYPE	DESCRIPTION
TXD0	I	**Transmit Data 0**: Bit 0 of the 4 data bits that are accepted by the PHY for transmission.
TXD1	I	**Transmit Data 1**: Bit 1 of the 4 data bits that are accepted by the PHY for transmission.
TXD2	I	**Transmit Data 2**: Bit 2 of the 4 data bits that are accepted by the PHY for transmission **Note:** This signal should be grounded in RMII Mode.
TXD3	I	**Transmit Data 3**: Bit 3 of the 4 data bits that are accepted by the PHY for transmission. **Note:** This signal should be grounded in RMII Mode
nINT/ TX_ER/ TXD4	I/O	**MII Transmit Error**: When driven high, the 4B/5B encode process substitutes the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in 10Base-T operation. **MII Transmit Data 4:** In Symbol Interface (5B Decoding) mode, this signal becomes the MII Transmit Data 4 line, the MSB of the 5-bit symbol code-group. **Notes:** ▪ This signal is not used in RMII Mode. ▪ This signal is mux’d with nINT
TX_EN	I	**Transmit Enable**: Indicates that valid data is presented on the TXD[3:0] signals, for transmission. In RMII Mode, only TXD[1:0] have valid data.
TX_CLK	O	**Transmit Clock**: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode. **Note:** This signal is not used in RMII Mode
RXD0/ MODE0	I/O	**Receive Data 0**: Bit 0 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 0:** set the default MODE of the PHY.

Table 2 MII Signals (continued)

SIGNAL NAME	TYPE	DESCRIPTION
RXD1/ MODE1	I/O	**Receive Data 1**: Bit 1 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 1:** set the default MODE of the PHY.
RXD2/ MODE2	I/O	**Receive Data 2**: Bit 2 of the 4 data bits that are sent by the PHY in the receive path. **PHY Operating Mode Bit 2:** set the default MODE of the PHY. **Notes:** ▪ RXD2 is not used in RMII Mode.
RXD3/ nINTSEL	I/O	**Receive Data 3**: Bit 3 of the 4 data bits that are sent by the PHY in the receive path. **nINTSEL**: On power-up or external reset, the mode of the nINT/TXER/TXD4 pin is selected. ▪ When RXD3/nINTSEL is floated or pulled to VDDIO, nINT is selected for operation on pin nINT/TXER/TXD4 (default). ▪ When RXD3/nINTSEL is pulled low to VSS through a resistor, TXER/TXD4 is selected for operation on pin nINT/TXER/TXD4. **Notes:** ▪ RXD3 is not used in RMII Mode ▪ If the nINT/TXER/TXD4 pin is configured for nINT mode, then a pull-up resistor is needed to VDDIO on the nINT/TXER/TXD4 pin.
RX_ER/ RXD4/	O	**Receive Error**: Asserted to indicate that an error was detected somewhere in the frame presently being transferred from the PHY. **MII Receive Data 4**: In Symbol Interface (5B Decoding) mode, this signal is the MII Receive Data 4 signal, the MSB of the received 5-bit symbol code-group. Unless configured in this mode, the pin functions as RX_ER. **Note:** This pin has an internal pull-down resistor, and must not be high during reset. The RX_ER signal is optional in RMII Mode.
RX_DV	O	**Receive Data Valid**: Indicates that recovered and decoded data nibbles are being presented on RXD[3:0]. **Note:** This pin has an internal pull-down resistor, and must not be high during reset. This signal is not used in RMII Mode.
RX_CLK/ REGOFF	I/O	**Receive Clock**: In MII mode, this pin is the receive clock output. 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode. **Note:** This signal is not used in RMII Mode. **Regulator Off**: This pin may be used to configure the internal 1.8V regulator off. This pin is sampled during the power-on sequence to determine if the internal regulator should turn on. When the regulator is disabled, external 1.8V must be supplied to VDD_CORE, and the voltage at VDD33 must be at least 2.64V before voltage is applied to VDD_CORE.

Table 2 MII Signals (continued)

SIGNAL NAME	TYPE	DESCRIPTION
COL/ RMII/ CRS_DV	I/O	**MII Mode Collision Detect**: Asserted to indicate detection of collision condition. **RMII –** MII/RMII mode selection is latched on the rising edge of the internal reset (nreset) based on the following strapping: ■ Float this pin for MII mode or pull-high with an external resistor to VDDIO to set the device in RMII mode. **RMII Mode CRS_DV (Carrier Sense/Receive Data Valid)** Asserted to indicate when the receive medium is non-idle. When a 10BT packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. In 10BT, half-duplex mode, transmitted data is not looped back onto the receive data pins, per the RMII standard.
CRS/ PHYAD4	I/O	**Carrier Sense**: Indicates detection of carrier. **Note:** This signal is mux'd with PHYAD4

Table 3 LED Signals

SIGNAL NAME	TYPE	DESCRIPTION
SPEED100/ PHYAD0	I/O	**LED1 –** SPEED100 indication. Active indicates that the selected speed is 100Mbps. Inactive indicates that the selected speed is 10Mbps. **Note:** This signal is mux'd with PHYAD0
LINK/ PHYAD1	I/O	**LED2 –** LINK ON indication. Active indicates that the Link (100Base-TX or 10Base-T) is on. **Note:** This signal is mux'd with PHYAD1
ACTIVITY/ PHYAD2	I/O	**LED3 –** ACTIVITY indication. Active indicates that there is Carrier sense (CRS) from the active PMD. **Note:** This signal is mux'd with PHYAD2
FDUPLEX/ PHYAD3	I/O	**LED4 –** DUPLEX indication. Active indicates that the PHY is in full-duplex mode. **Note:** This signal is mux'd with PHYAD3

Table 4 Management Signals

SIGNAL NAME	TYPE	DESCRIPTION
MDIO	I/O	**Management Data Input/OUTPUT**: Serial management data input/output.
MDC	I	**Management Clock**: Serial management clock.

Table 5 Boot Strap Configuration Inputs (Note 1)

SIGNAL NAME	TYPE	DESCRIPTION
CRS/ PHYAD4	I/O	**PHY Address Bit 4:** set the default address of the PHY. This signal is mux'd with CRS **Note:** This signal is mux'd with CRS
FDUPLEX/ PHYAD3	I/O	**PHY Address Bit 3:** set the default address of the PHY. **Note:** This signal is mux'd with FDUPLEX
ACTIVITY/ PHYAD2	I/O	**PHY Address Bit 2:** set the default address of the PHY. **Note:** This signal is mux'd with ACTIVITY
LINK/ PHYAD1	I/O	**PHY Address Bit 1:** set the default address of the PHY. **Note:** This signal is mux'd with LINK
SPEED100/ PHYAD0	I/O	**PHY Address Bit 0:** set the default address of the PHY. **Note:** This signal is mux'd with SPEED100
RXD2/ MODE2	I/O	**PHY Operating Mode Bit 2:** set the default MODE of the PHY. **Note:** This signal is mux'd with RXD2
RXD1/ MODE1	I/O	**PHY Operating Mode Bit 1:** set the default MODE of the PHY. **Note:** This signal is mux'd with RXD1
RXD0/ MODE0	I/O	**PHY Operating Mode Bit 0:** set the default MODE of the PHY. **Note:** This signal is mux'd with RXD0
RX_CLK/ REGOFF	I/O	**Internal Regulator off:** disable the internal +1.8v regulator. This signal is mux'd with RX_CLK. ▪ Float to enable the internal +1.8v regulator. ▪ Pull up with a resistor to VDDIO to disable the internal regulator.
COL/ RMII/ CRS_DV	I/O	**Digital Communication Mode:** set the digital communications mode of the PHY to RMII or MII. This signal is muxed with the Collision signal (MII mode) and Carrier Sense/ receive Data Valid (RMII mode) ▪ Float for MII mode. ▪ Pull up with a resistor to VDDIO for RMII mode.
RXD3/ nINTSEL	I/O	**nINT pin mode select:** set the mode of pin 1. ▪ Default, left floating pin 1 is nINT, active low interrupt output. **Note:** For nINT mode, tie nINT/TXD4/TXER to VDDIO with a resistor. ▪ Pulled to VSS by a resistor, pin 1 is TX_ER/TXD4, Transmit Error or Transmit data 4 (5B mode). **Note:** For TXD4/TXER mode, do not tie nINT/TXD4/TXER to VDDIO or Ground.

Note 1 On nRST transition high, the PHY latches the state of the configuration pins in this table.

Table 6 General Signals

SIGNAL NAME	TYPE	DESCRIPTION
nINT/ TX_ER/ TXD4	I/O	**LAN Interrupt** – Active Low output. Place an external resistor pull-up to VCC 3.3V. **Note:** This signal is mux'd with TXER/TXD4
nRST	I	**External Reset** – input of the system reset. This signal is active LOW.
CLKIN/ XTAL1	I/O	**Clock Input** – 25 Mhz or 50 MHz external clock or crystal input. In MII mode, this signal is the 25 MHz reference input clock In RMII mode, this signal is the 50 MHz reference input clock which is typically also driven to the RMII compliant Ethernet MAC clock input.
XTAL2	O	**Clock Output** – 25 MHz crystal output. **Note:** Float this pin if using an external clock being driven through CLKIN/XTAL1

Table 7 10/100 Line Interface

SIGNAL NAME	TYPE	DESCRIPTION
TXP	AO	**Transmit Data Positive**: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
TXN	AO	**Transmit Data Negative**: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
RXP	AI	**Receive Data Positive**: 100Base-TX or 10Base-T differential receive inputs from magnetics.
RXN	AI	**Receive Data Negative**: 100Base-TX or 10Base-T differential receive inputs from magnetics.

Table 8 Analog References

SIGNAL NAME	TYPE	DESCRIPTION
EXRES1	AI	Connects to reference resistor of value 12.4K-Ohm, 1% connected as described in the Analog Layout Guidelines.

Table 9 Power Signals

SIGNAL NAME	TYPE	DESCRIPTION
VDDIO	POWER	+1.6V to +3.6V Variable I/O Pad Power
VDD33	POWER	+3.3V Core Regulator Input.
VDDA3.3	POWER	+3.3V Analog Power

Table 9 Power Signals (continued)

SIGNAL NAME	TYPE	DESCRIPTION
VDD_CORE	POWER	+1.8V (Core voltage) - 1.8V for digital circuitry on chip. Supplied by the on-chip regulator unless configured for regulator off mode using the RX_CLK/REGOFF pin. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. When using the on-chip regulator, place a 4.7uF ±20% capacitor with ESR < 1ohm near this pin and connect the capacitor from this pin to ground. X5R or X7R ceramic capacitors are recommended since they exhibit an ESR lower than 0.1ohm at frequencies greater than 10kHz.
VSS	POWER	Exposed Ground Flag. The flag must be connected to the ground plane with an array of vias as described in the Analog Layout Guidelines

Package Outline

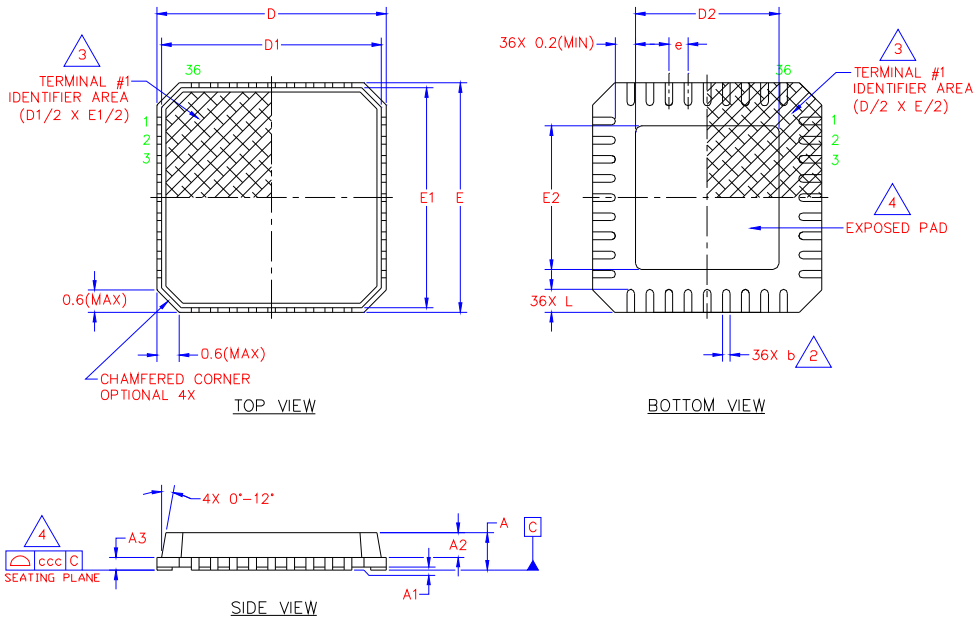

Figure 4 36-Pin QFN Package Outline, 6 x 6 x 0.90 mm Body (Lead-Free)

Table 10 36-Pin QFN Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	0.80	~	1.00	Overall Package Height
A1	0	~	0.05	Standoff
A2	0.60	~	0.80	Mold Thickness
A3		0.20 REF		Copper Lead-frame Substrate
D	5.85	~	6.15	X Overall Size
D1	5.55	~	5.95	X Mold Cap Size
D2	3.55	~	3.85	X exposed Pad Size
E	5.85	~	6.15	Y Overall Size
E1	5.55	~	5.95	Y Mold Cap Size
E2	3.55	~	3.85	Y exposed Pad Size
L	0.35	~	0.75	Terminal Length
e		0.50 Basic		Terminal Pitch
b	0.18	~	0.30	Terminal Width
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Dimension b applies to plated terminals and is measured between 0.15mm and 0.30mm from the terminal tip. Tolerance on the true position of the terminal is ± 0.05 mm at maximum material conditions (MMC).
3. Details of terminal #1 identifier are optional but must be located within the zone indicated.
4. Coplanarity zone applies to exposed pad and terminals.