Figure 2. Pin Connection

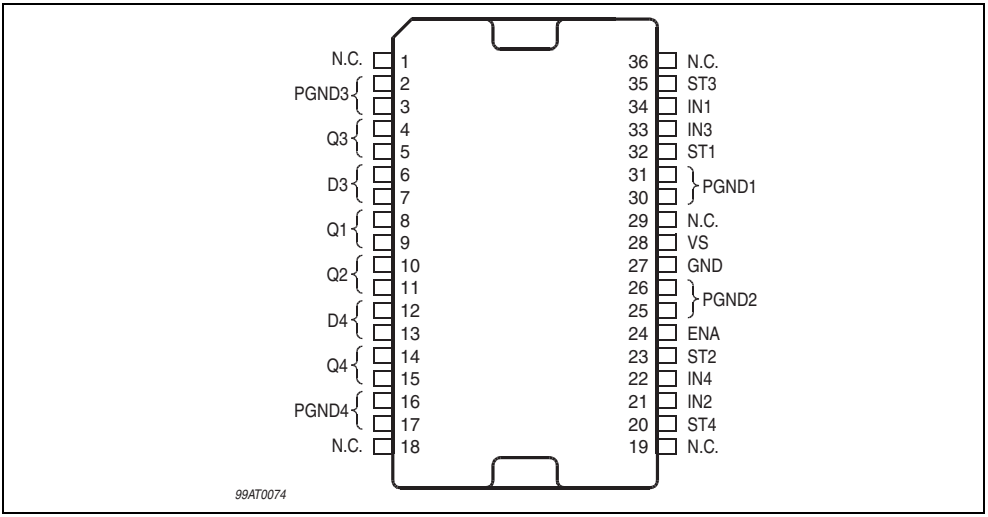


Table 1. Pin Description

N°	Pin	Function
1, 18, 19, 36	N.C.	(GND)
2, 3	PGND3	Power Ground Channel 3
4, 5	Q3	Power Output Channel 3 (3A switch)
6, 7	D3	Recirculation Diode Channel 3
8, 9	Q1	Power Output Channel 1 (5A switch)
10, 11	Q2	Power Output Channel 2 (5A switch)
12, 13	D4	Recirculation Diode Channel 4
14, 15	Q4	Power Output Channel 4 (3A switch)
16, 17	PGND4	Power Ground Channel 4
20	ST4	Status Output Channel 4
21	IN2	Control Input Channel 2
22	IN4	Control Input Channel 4
23	ST2	Status Output Channel 2
24	ENA	Enable
25, 26	PGND2	Power Ground Channel 2
27	GND	Signal Ground
28	VS	Supply Voltage
29	N.C.	Not Connected
30, 31	PGND1	Power Output Channel 3
32	ST1	Status Output Channel 1
33	IN3	Control Input Channel 3
34	IN1	Control Input Channel 1

Table 2. Thermal Data

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
T_j	Junction temperature		-40		150	°C
T_{jc}	Junction temperature during clamping (life time)	Σt = 30min Σt = 15min			175 190	°C °C
T_{stg}	Storage temperature		-55		150	°C
$R_{th\ j\text{-}case}$	Thermal resistance junction to case				2	°C/W

Table 3. Absolute Maximum Ratings

The absolute maximum ratings are the limiting values for this device. Damage may occur if this device is subjected to conditions which are beyond these values.

Symbol	Parameter	Test Conditions	Value	Unit
Voltages				
V_S	Supply voltage range		-0.3 to 40	V
V_Q, V_D	max. static Output voltage		40	V
V_{IN}, V_{EN}	Input voltage range (IN1 to IN4, EN)	$\|I_I\|$ < 10mA	-1.5 to 6	V
V_{ST}	Status output voltage range	$\|I_I\|$ < 1mA	-0.3 to 6	V
V_{DRmax}	max. Reverse breakdown voltage free wheeling diodes D3, D4	I_R = 100 µA	55	V
Currents				
$I_{Q\ 1/2}$	Output current at reversal supply for Q1, Q2		-4	A
$I_{Q\ 3/4}$	Output current at reversal supply for Q3, Q4		-2	A
I_{ST}	Status output current range		-1 to 1	mA
$E_{Q1/2}$	max. Discharging energy for inductive loads per channel Q1, Q2	T_j = 25°C	50	mJ
		T_j = 150°C	30	mJ
I_{FDmax}	max. load current free wheeling diodes	t < 5ms	3	A
ESD Protection				
Supply and Signal pins		versus GND	±2	kV
Output pins (Q_X, D_X)		versus common ground (=short of SGND with all PGND)	±4	kV

Note: Human Body Model according to MIL883C. The device withstands ST1 class level.

Table 4. Operating Range.

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
V_S	Supply voltage		4.8		18	V
T_j	Junction temperature		-40		150	°C

Table 5. Electrical Characteristcs

The electrical characteristics are valid within the operating range **(Table 4)**, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Power Supply						
I_S	Supply current	$V_{IN1...IN4, ENA}$ = H			8	mA
I_Q	Quiescent current (outputs OFF)	V_{ENA} = L			6	mA
$I_{D3/4}$	Quiescent current at pins D3/4	$V_{D3/4} \leq 18V$; $V_{IN3/4}$ = L	10		400	µA
Diagnostic Functions						
$V_{QU1\ to\ 4}$	Output open load voltage threshold	$V_S \geq 6.5V$ V_{EN} = X; V_{IN} = L	0.3	0.33	0.36	x V_S
$I_{QU1\ to\ 4}$	Output open load current threshold	$V_S \geq 6.5V$ V_{EN} = H; V_{IN} = H	50		140	mA
$I_{QO1/2}$	Overload current threshold Q 1, 2	$V_S \geq 6.5V$	5	7.5	9	A
$I_{QO3/4}$	Overload current threshold Q 3, 4	$V_S \geq 6.5V$	3	5	8	A
T_{th}	Overtemperature shutdown threshold	2)	175		210	°C
T_{hy}	Overtemperature hysteresis			10		°C
V_{thPGL}	Power-GND-loss threshold		1.5	2.5	3.5	V
V_{thSGL}	Signal-GND-loss threshold		150	330	510	mV
Power Outputs (Q1 to Q4)						
$R_{DSON1/2}$	Static drain-source ON-resistance Q1, Q2	I_Q = 1A; $V_S \geq 9.5V$ T_j = 25°C		0.2		Ω
		T_j = 125°C 3)			0.5	Ω
		T_j = 150°C 4)			0.5	Ω
$R_{DSON3,4}$	Static drain-source ON-resistance Q3, Q4	I_Q = 1A; $V_S \geq 9.5V$ T_j = 25°C		0.35		Ω
		T_j = 125°C 3)			0.75	Ω
		T_j = 150°C 4)			0.75	Ω
V_Z	Z-diode clamping voltage = threshold of flyback detection Q3/4	$I_Q \geq 100mA$, pos. supply $V_{D3/4}$	45		60	V
V_C	Clamping voltage	$I_Q \geq 100mA$, neg. supply $V_{D3/4}$	4		10	V
I_{PD}	Output pull down current	V_{ENA} = H, V_{IN} = L	10	20	50	µA

Table 5. Electrical Characteristcs

The electrical characteristics are valid within the operating range **(Table 4)**, unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{Qlk}	Output leakage current	V_{ENA} = L,T_j = 25°C			1	µA
		T_j = 125°C			5	µA
$V_{FD3/4}$	Forward voltage of free wheeling diodes D3, D4	$I_{D3/4}$ = -1.5A	0.5		1.75	V
R_{PD0}	Gate pull down resistor for nonsupplied V_S	V_S = 0V, $V_{D3/4} \geq$ 6.5V	0.3		3	kΩ
Timings						
t_{ON}	Output ON delay time	I_Q = 1A 1)	0	5	20	µs
t_f	Output ON fall time	I_Q = 1A 1)	0.5	1.5	8	µs
t_{OFF}	Output OFF delay time	I_Q = 1A 1)	0	10	30	µs
t_r	Output OFF rise time	I_Q = 1A 1)	0.5	1.5	5	µs
t_{DSO}	Overload switch-OFF delay time		6	30	65	µs
t_D	Output OFF status delay time		0.75	1.5	2.25	ms
t_{filter}	error detection filter time	2)	5.8		35	µs
t_{OLOFF}	OLOFF error detection filter time		20		70	µs
Digital Inputs (IN1 to IN4, ENA)						
V_{IL}	Input low voltage		-1.5		1	V
V_{IH}	Input high voltage		2		6	V
V_{IHy}	Input voltage hysteresis	2)	50	100		mV
I_{IN}	Input pull down current	V_{IN} = 5V, $V_S \geq$ 6.5V	8	20	40	µA
Digital Outputs (ST1 to ST4)						
V_{STL}	Status output voltage in low state 5)	$I_{ST} \leq$ 40µA	0		0.4	V
V_{STH}	Status output voltage in high state 5)	$I_{ST} \geq$ -40µA	2.5		3.45	V
		$I_{ST} \geq$ -120µA	2		3.45	V
R_{DIAGL}	R_{OUT} + R_{DSON} in low state		0.3	0.64	1.5	kΩ
R_{DIAGH}	R_{OUT} + R_{DSON} in high state		1.5	3.2	7	kΩ

(1).See **chapter 2.0 Timing Diagrams**; resistive load condition; $V_S \geq$ 9V

(2).This parameter will not be tested but assured by design

(3).Wafer-measurement

(4).Measured on P-SO36 devices

(5).Short circuit between two digital outputs (one in high the other in low state) will lead to the defined result "LOW"

1.0 FUNCTIONAL DESCRIPTION

1.1 Overview

The four low-side switches are designed to drive inductive loads (relays, electromagnetic valves). For the 3A switches (Q3/4) integrated free-wheeling diodes (D3/4) are available and can be used as recirculation path for inductive loads. If either integrated nor external free-wheeling diodes are used the output voltage is clamped internally during discharge of inductive loads. The switches are controlled by CMOS compatible inputs (IN1-4) if the enable input is set to “high”. The status of each switch is monitored by the related status output (ST1-4).

1.2 Input Circuits

The control and enable inputs are active high, featuring switching thresholds with hysteresis and pull-down current sources. Not connected inputs are interpreted as “LOW”. If the enable input is set to “LOW” the outputs are switched off independent of the control input state (IN1-4).

1.3 Switching Stages

The four power outputs consist of DMOS-power transistors. The output stages are protected against short circuit to supply. Integrated output voltage clamp limits the output voltage in case of inductive load current flyback. Internal pull down current sources are provided at the outputs to assure a defined conditon in OFF mode. They will be disconnected in the disable mode (ENA=L). If the supply of the device gets lost but the loads and D3/4 are still supplied, an internal pull down resistor discharges the gate of the DMOS-power transistor to avoid switch on due to capacitive coupling.

1.4 Status Outputs

The CMOS compatible status outputs indicate the state of the drivers (LOW-level indicates driver in OFF state, HIGH-level indicates driver in ON state). If an error occurs the status output voltage changes like described in **chapter 1.6 Error Detection**.

1.5 Protective Circuits

The outputs are protected against current overload, overtemperature, and Power-GND-loss.

1.6 Error Detection

Two main error types are distinguished in the diagnostic logic. If current overload, overtemperature, signal-GND-loss or a power-GND-loss occurs, the status output signal is inverted, an internal register is set and the driver is shutdown. The reset is done by switching off the corresponding control input or the enable input for at least the time t_D (defined to 1.5ms typ.). See also **Figure 6** in **chapter 2.0 Timing Diagrams**.

All other errors (openload, active output voltage clamp) only cause an inverted status output signal but no shutdown of the driver. An internal register is set too, but the reset is triggered automatically after the time t_D, if the error condition is no longer valid (see **Figure 7** and **Figure 8**).

Excepting the detection of the active output voltage clamp all errors are digitally filtered before they are interpreted by the diagnostic logic.

The table 6 below shows the different failure conditions monitored in ON and OFF state:

Table 6.

	ON State ENA = HIGH, IN = HIGH	OFF State ENA = HIGH, IN = LOW	typ. Filter time	Reset done by
Overloading of output (also shorted load to supply)	X		18µs	ENA or INx = “LOW” for t ≥ 1.5ms (typ.)
Open load (under voltage detection)		X	44µs	internal timer (1.5ms typ.)

Table 6.

	ON State ENA = HIGH, IN = HIGH	OFF State ENA = HIGH, IN = LOW	typ. Filter time	Reset done by
Open load (under current detection)	X		18µs	internal timer (1.5ms typ.)
Overtemperature	X		18µs	ENA or INx = "LOW" for t ≥ 1.5ms (typ.)
Power-GND-loss	X	X	18µs	ENA or INx = "LOW" for t ≥ 1.5ms (typ.)
Signal-GND-loss	X	X	18µs	ENA or INx = "LOW" for t ≥ 1.5ms (typ.)
Output voltage clamp active (Q3/4 only)		X	-	internal timer (1.5ms typ.)

1.7 Diagnostic Output at Pulse Width Operation (PWM)

If an input is operated with a pulsed signal ($f \geq 1/t_D$ = 667 Hz typ.), the status does not follow each single pulse. An internal delay t_D of typ. 1.5ms leads to a continuous status output signal (see **Figure 4** in **chapter 2.0 Timing Diagrams**).

1.8 Diagnostic Table

In general the diagnostic follows the input signal in normal operating conditions. If any error is detected the diagnostic is inverted.

Table 7.

Operating Condition	Enable Input ENA	Control Input IN	Power Output Q	Status Output ST
Normal function	L	L	OFF	L
	L	H/PWM	OFF	L
	H	L	OFF	L
	H	H/PWM	ON	H
Open load or short to ground	L	L	OFF	X
	L	H/PWM	OFF	X
	H	L	OFF	H
	H	H/PWM	ON	L
Overload or short to supply	H	H/PWM	OFF	L
Latched overload	H	H/PWM	OFF	L
	H –> L	X	OFF	L
Reset latch	H	H/PWM –> L	OFF	L
Overtemperature	H	H/PWM	OFF	L
Latched overtemperature	H	H/PWM	OFF	L
	H –> L	X	OFF	L
Reset latch	H	H/PWM –> L	OFF	L

2.0 TIMING DIAGRAMS

Figure 3. Output slope with Resistive Load

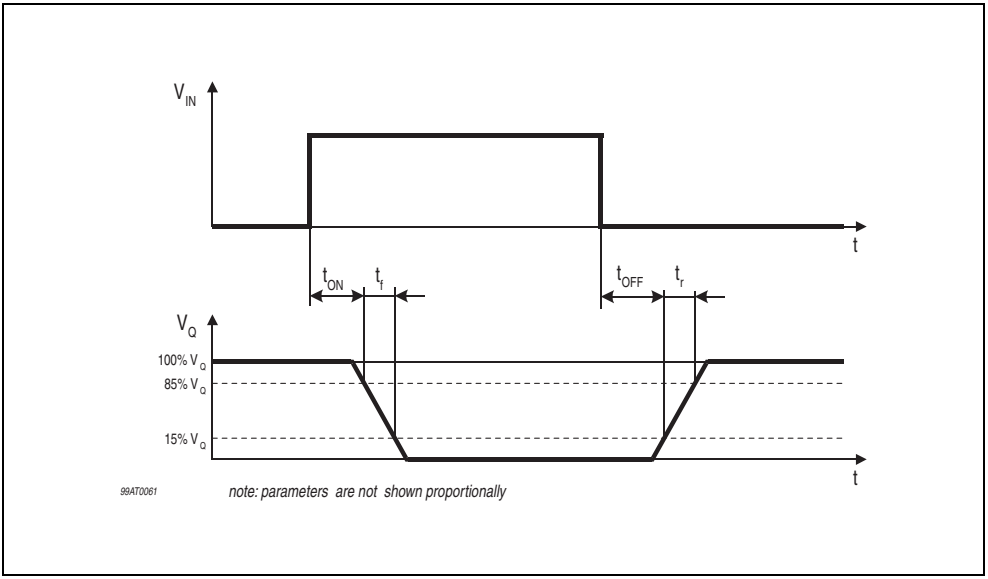


Figure 4. Diagnostic Output at PWM operation

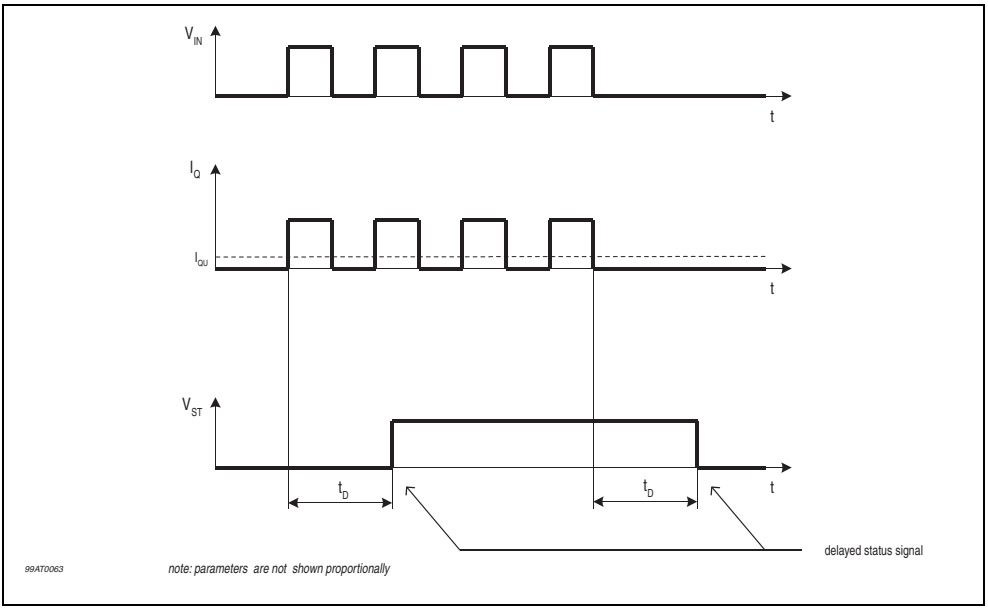


Figure 5. Overload Detection

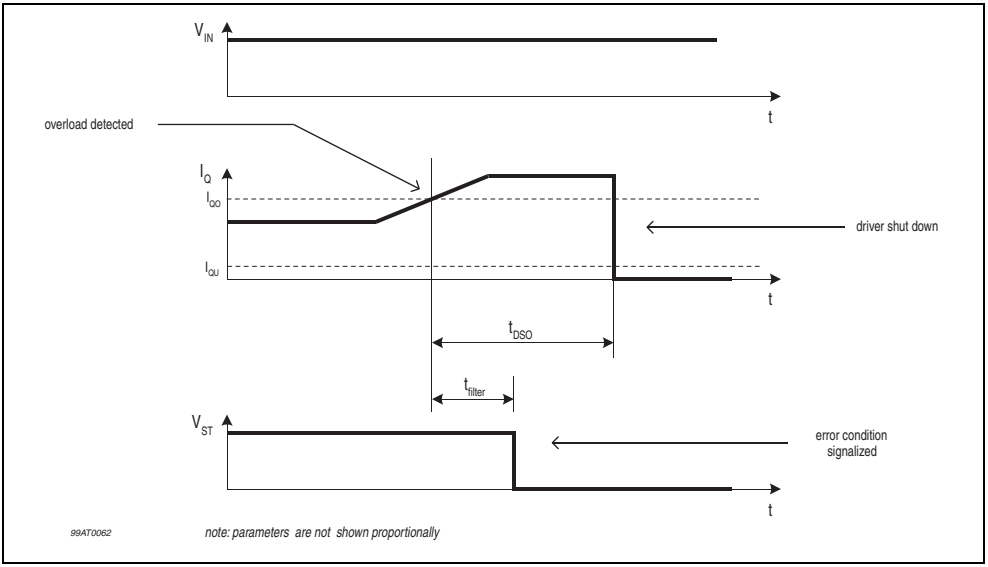


Figure 6. Driver Shut Down in Case of Overload

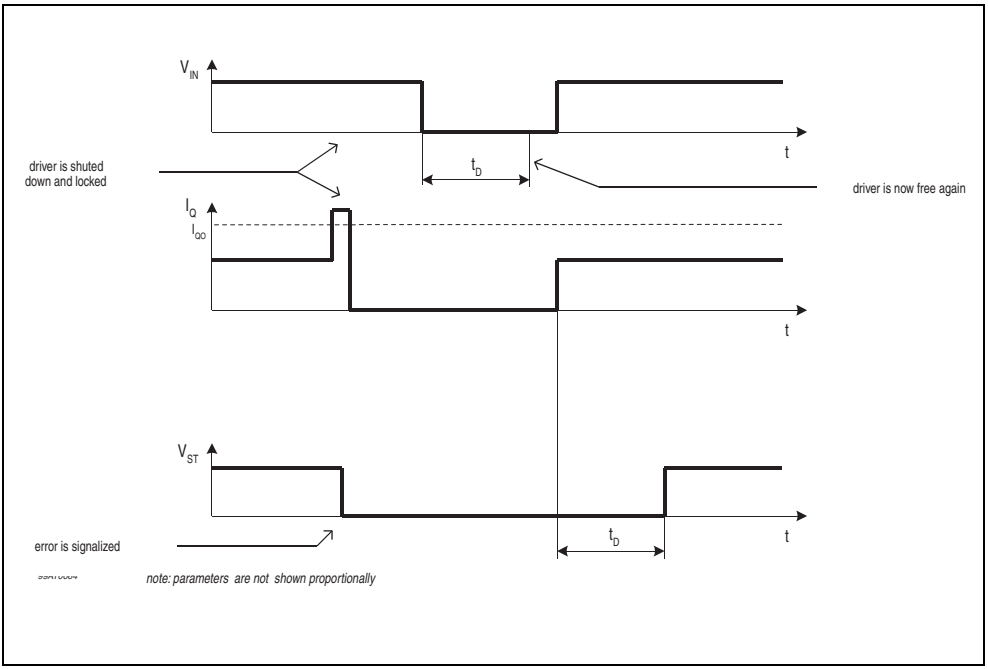


Figure 7. Under Current Condition

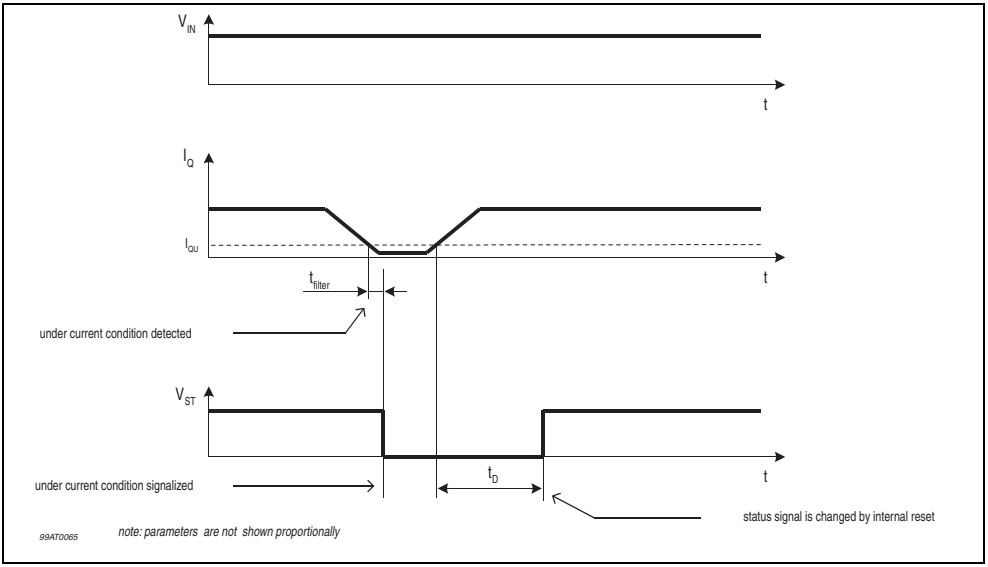


Figure 8. Open Load Condition in Off State

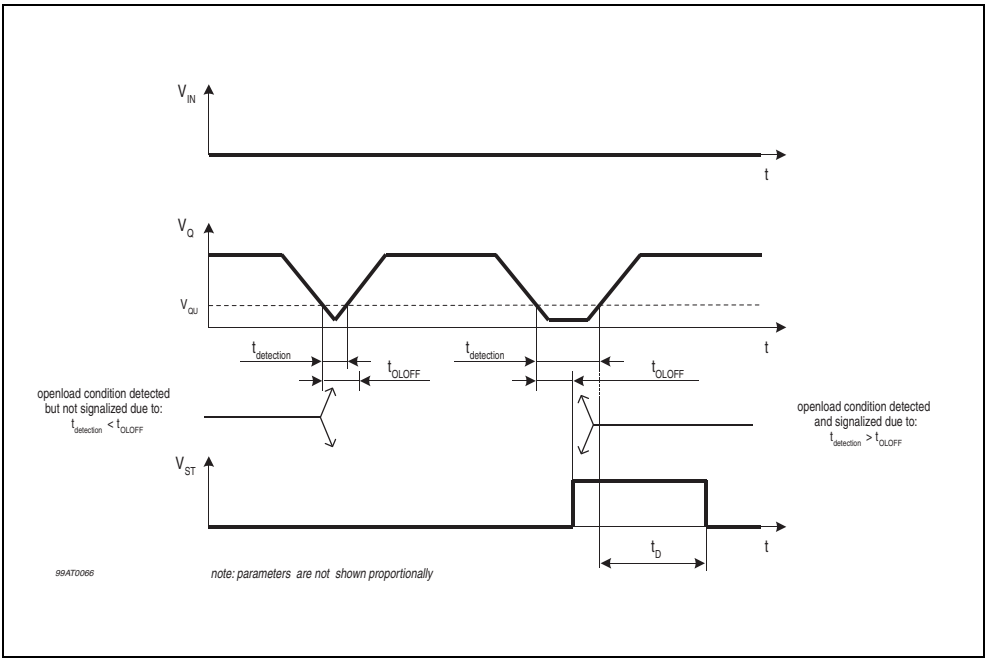
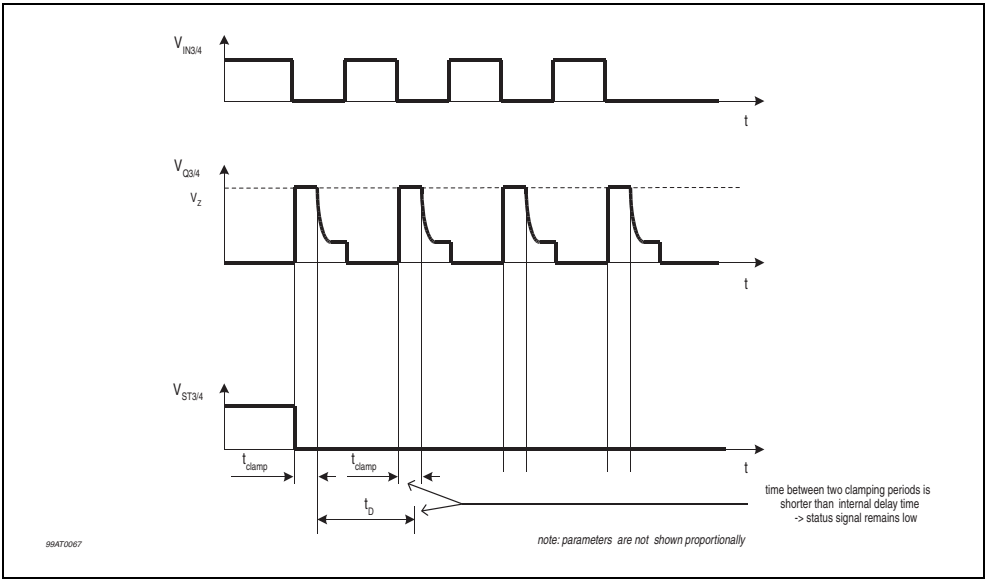


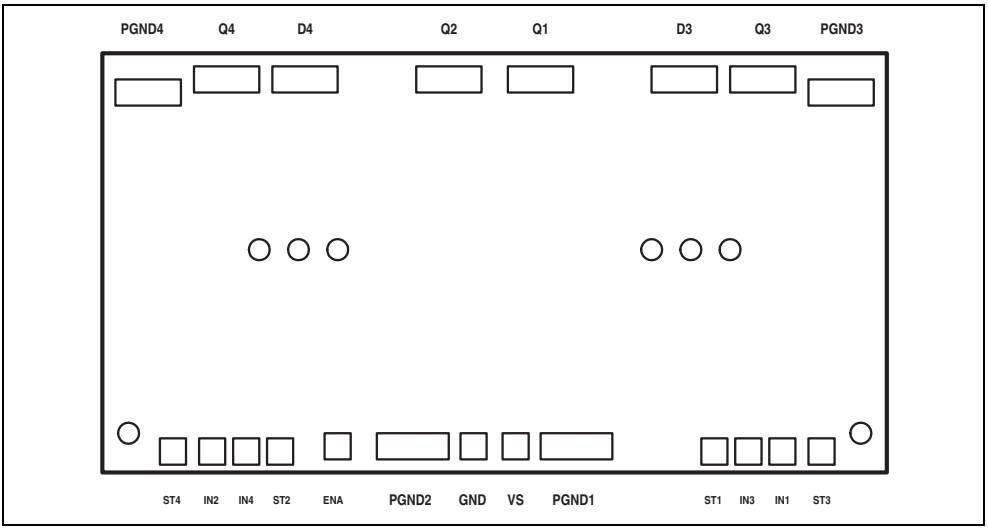
Figure 9. Output Voltage Clamp Detection



3.0 PAD POSITIONS

Chip Size: 5.17 x 2.76 mm^2

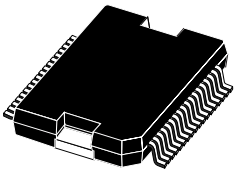
Figure 10.



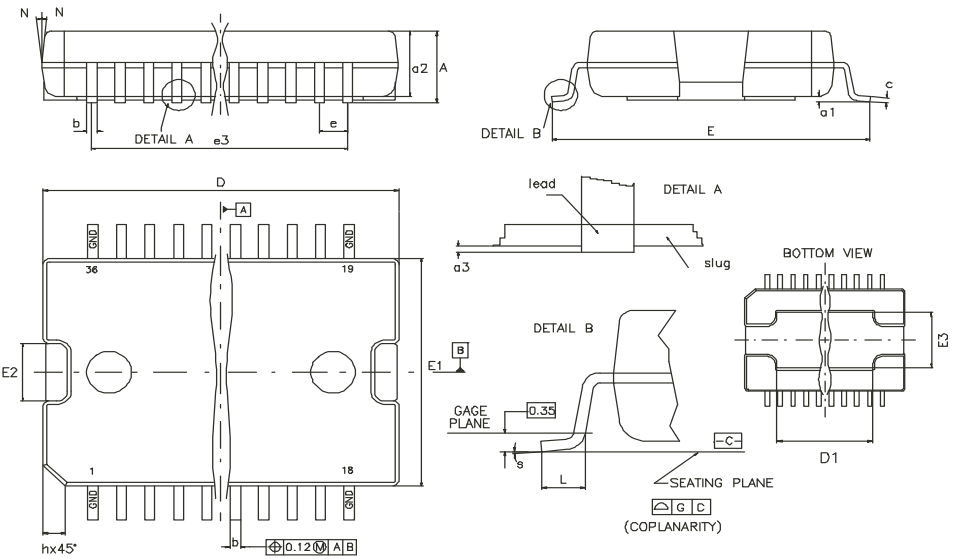
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10			0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.5	0.5472		0.5709
E1	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.80		6.20	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10			0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.8		1.10	0.0315		0.0433
N	10° (max)					
s	8° (max)					

Note: “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO-36



0096119 C

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com