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1 Overview

The L5963 integrates two switching mode synchronous step down converters, a linearly regulated power supply, a protected high side driver and voltage detectors. To guarantee a robust operation, all the outputs have independent thermal protection and current limitation.

The two switching mode synchronous step-down converters employ voltage mode control and feed forward functions to provide good load regulation and line regulation. Each converter has its own enable. The users can adjust the output voltage of the two converters by an external resistor divider. If the converters need to work with a frequency different from the free running frequency, in order to consider EMC performance in system level, they can be synchronized to an external clock by applying it on the SYNCIN pin. The frequency should be higher than half of the free running frequency. If there are more than one L5963 in the system they can work in Master-Slave configuration, to make sure all L5963 have the same operating frequency of the Master device. This Master-Slave function is implemented by a dedicated pin SYNCOUT which always gives the operating frequency of DC/DC1.

A dedicated voltage detector is integrated in the first switching converter to monitor DC/DC1 output. When the output voltage of DC/DC1 goes above the threshold, SW1OK is released and goes back to high with configurable delay set by a capacitor on the SW1OKDLY pin.

The linear regulator can work as standby regulator with low I_q or as a non-standby regulator. Connecting its enable ENLDO to its supply VINLDO the regulator works as a standby regulator, while connecting ENLDO to a voltage lower than 5 V the regulator works as non-standby regulator, with higher load capability but also higher quiescent current.

In standby state, i.e. only the linear regulator is powered and works as a standby regulator, with a load below 100 µA the device has a quiescent current of just 25 µA.

The small drop-out voltage of the linear regulator allows its use with low operating supply voltage.

In many cases, the linear regulator has to provide voltages to devices which need the reset function, like a MCU: this is provided by the LDOOK output, that is pulled low when VOUTLDO goes below a threshold. Once VOUTLDO returns above that threshold, with a specified hysteresis, LDOOK goes back to high with a configurable delay set by a capacitor on pin LDOOKDLY.

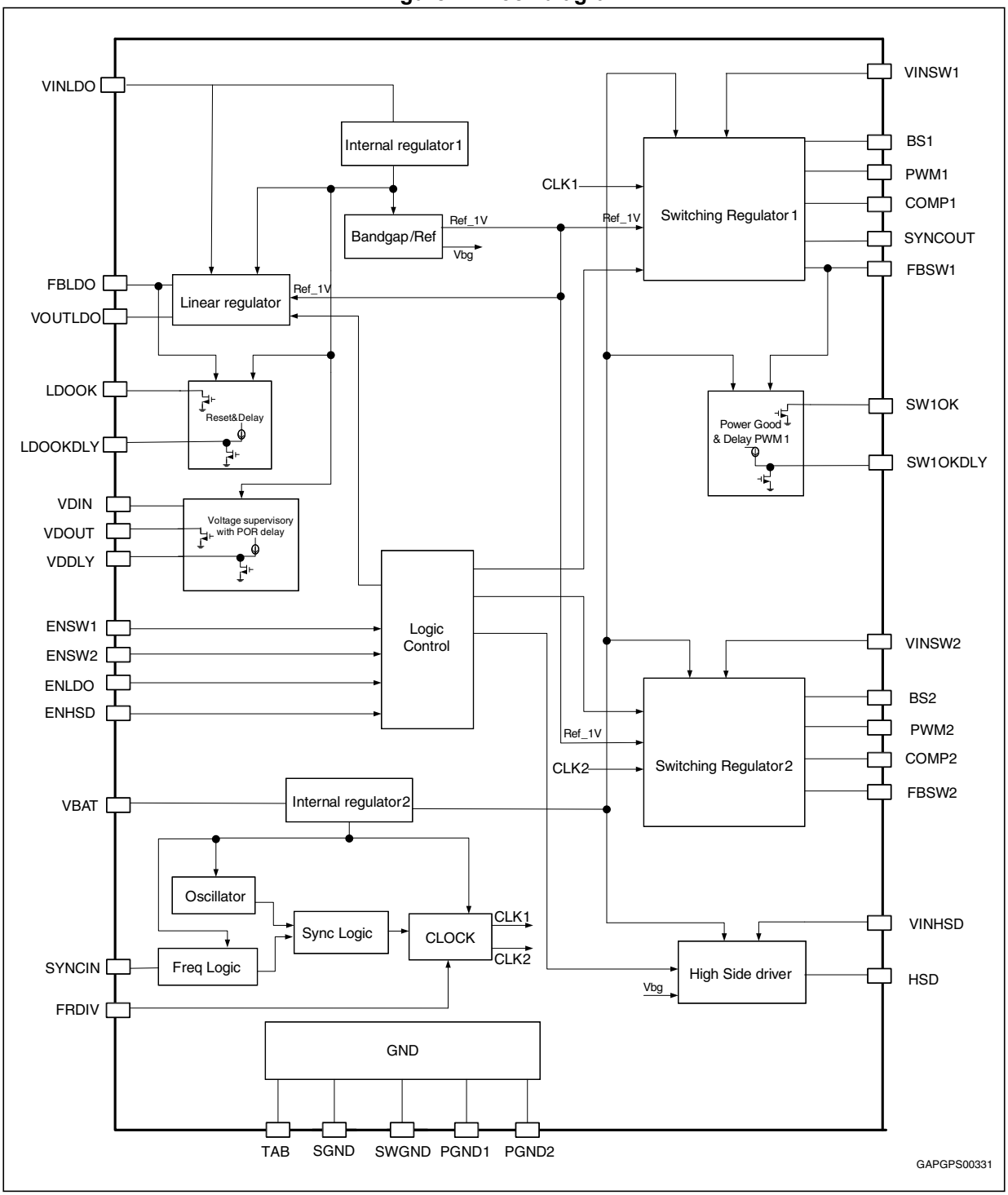
The high side driver is enabled by a dedicated pin and has a very low drop-out voltage. Protection circuits, like independent thermal protection, OCP, OVP and some special protections (loss of GND, SPU, short to supply and so on), are implemented to make it very robust.

L5963 also embeds a voltage monitor (VDOUT), adjustable by means of an external resistor divider, that can be used to sense the battery or other voltages in the system. Sensing voltage is fed to pin VDIN. For instance, VDOUT might be used to monitor the output of DC/DC2, realizing in this way the Power Good function for that block. VDOUT is pulled low when voltage on VDIN goes below the specified threshold. Once VDIN returns above that threshold, with a specified hysteresis, VDOUT goes back to high with a configurable delay set by a capacitor on pin LDOOKDLY

Two different packages are available. The PowerSSO-36 slug-down allows to dissipate the heat on the board and reduce the application size. The slug has to be connected to the ground plane. This is the package suggested for standard applications. When this is not enough, because the L5963 is used as pre-regulator for high consuming applications and both the 2 DC-DC are working at high currents, the PSSO36 slug-up allows the use of a heat-sink to make easier power dissipation.

2 Block diagram

Figure 1. Block diagram



3 Application diagrams

Figure 2. Example of a typical application diagram

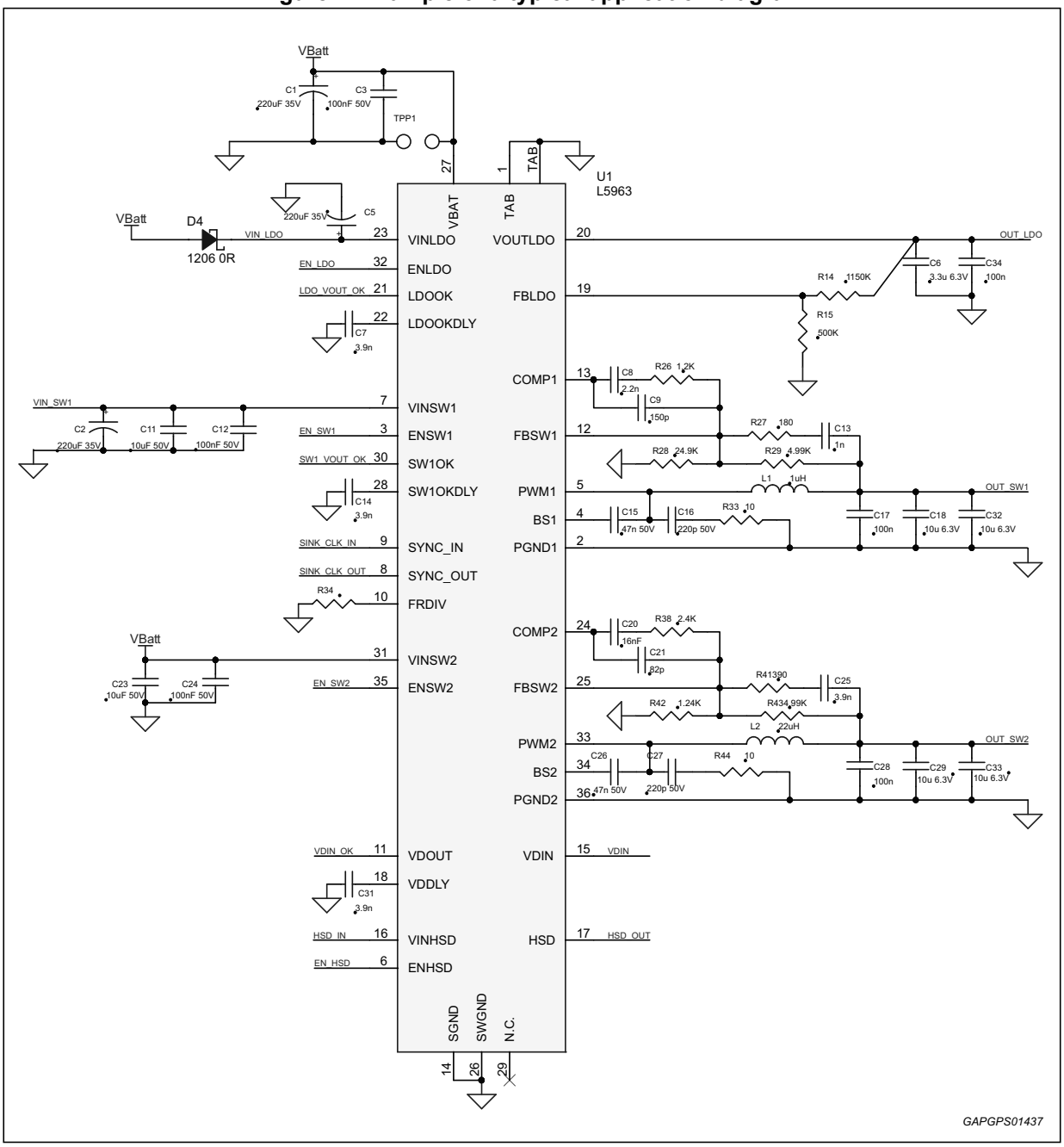
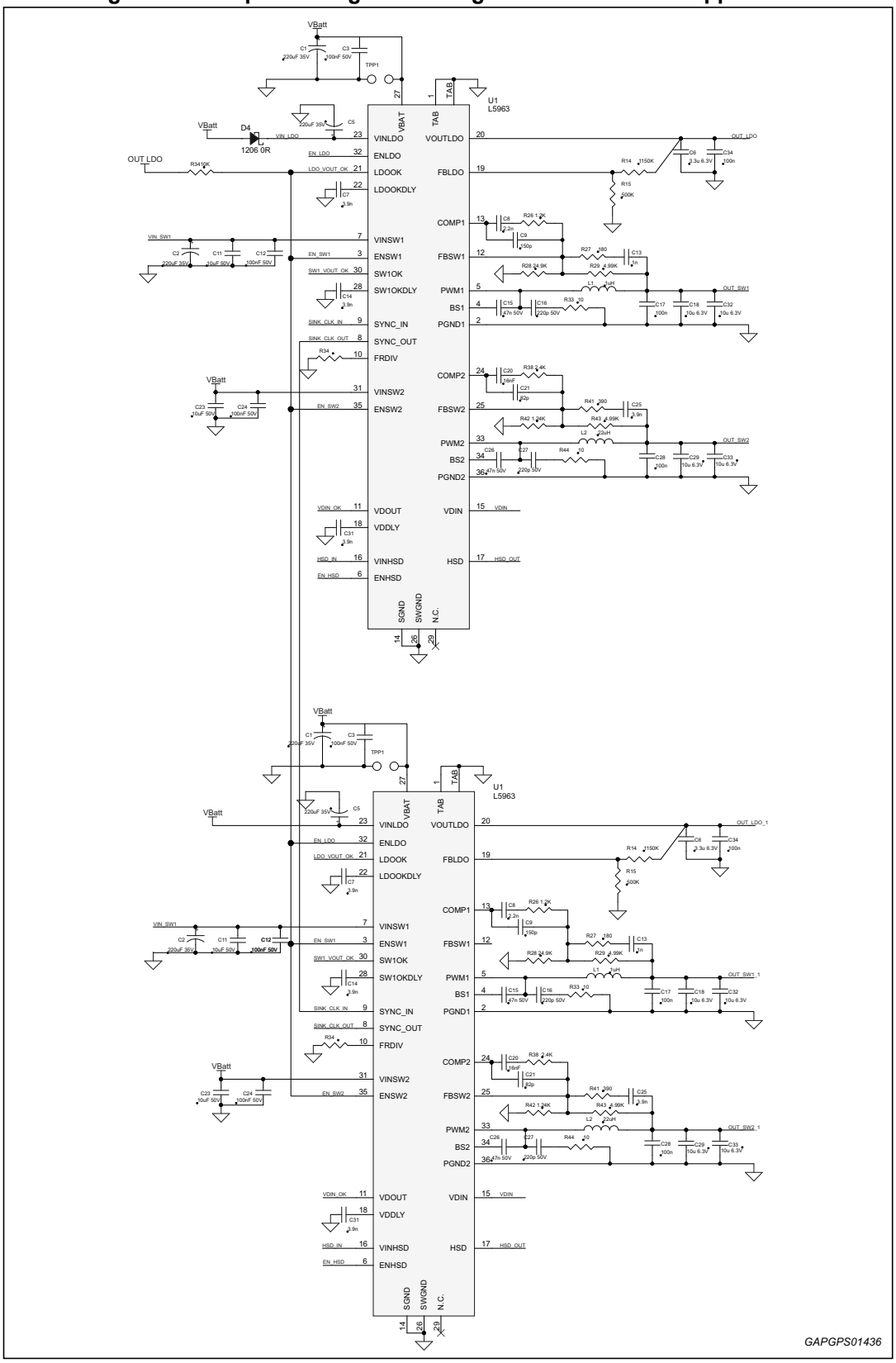


Figure 3. Example of usage of two regulators in the same application



4 Pins description

Figure 4. PowerSSO-36 pinout configuration

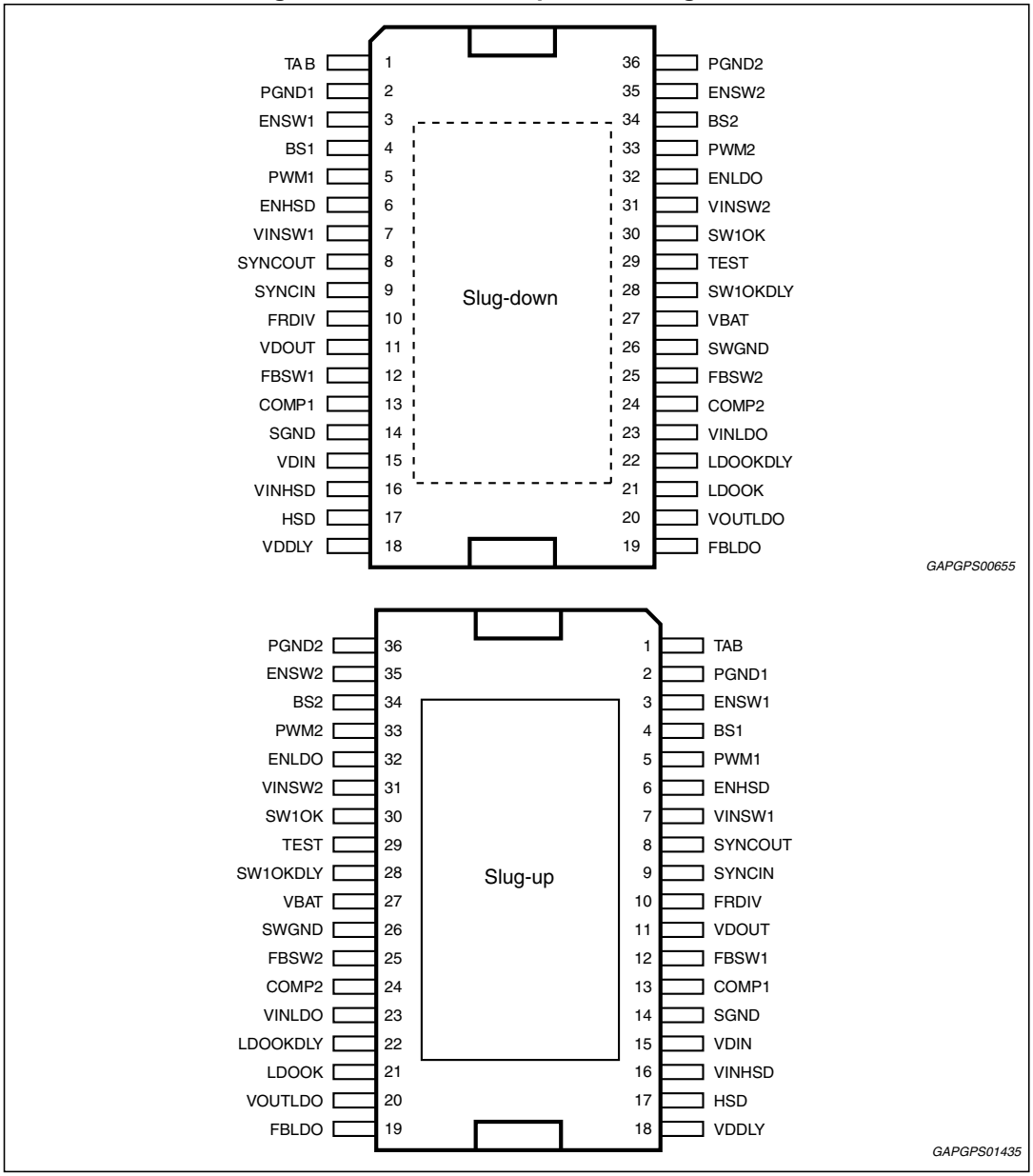


Table 2. PowerSSO-36 pins description

Pin #	Name	Type	Function
1	TAB	n.a.	Device slug terminal. To be connected to ground
2	PGND1	Ground	Switching regulator 1 power ground
3	ENSW1	Input	Switching regulator 1 enable. 1.8/3.3 V compatible
4	BS1	Supply	Switching regulator 1 boosted supply

Table 2. PowerSSO-36 pins description (continued)

Pin #	Name	Type	Function
5	PWM1	Output	Switching regulator 1 switching output
6	ENHSD	Input	Enable for High Side Driver. 1.8/3.3 V compatible
7	VINSW1	Supply	Switching regulator 1 supply voltage
8	SYNCOUT	Output	External synchronization output (push-pull)
9	SYNCIN	Input	External synchronization input
10	FRDIV	Input/output	Switching frequency divider setting
11	VDOUT	Output	Voltage detector output (open drain)
12	FBSW1	Input/output	Switching regulator 1 feedback voltage
13	COMP1	Input/output	Switching regulator 1 compensation
14	SGND	Ground	Ground for linear blocks
15	VDIN	Input	Voltage detector threshold setting
16	VINHSD	Supply	High Side Driver supply
17	HSD	Output	High Side Driver output
18	VDDLY	Input/output	Voltage Detector delay setting
19	FBLDO	Input/output	LDO feedback voltage
20	VOUTLDO	Output	LDO output
21	LDOOK	Output	LDO voltage detector output (open drain)
22	LDOOKDLY	Input/output	LDOOK delay setting
23	VINLDO	Supply	LDO supply
24	COMP2	Input/output	Switching regulator 2 compensation
25	FBSW2	Input/output	Switching regulator 2 feedback voltage
26	SWGND	Ground	Low-power switching ground
27	VBAT	Supply	Common linear blocks supply voltage
28	SW1OKDLY	Input/output	SW1OK delay setting
29	TEST	n.a.	Pin for testing purposes. To be left unconnected
30	SW1OK	Output	Switching regulator 1 voltage detector output (open drain)
31	VINSW2	Supply	Switching regulator 2 supply voltage
32	ENLDO	Input	LDO enable. 1.8/3.3 V compatible
33	PWM2	Output	Switching regulator 2 switching output
34	BS2	Supply	Switching regulator 2 boosted supply
35	ENSW2	Input	Switching regulator 2 enable. 1.8/3.3 V compatible
36	PGND2	Ground	Switching regulator 2 power ground

Figure 5. VQFPN-48 pinout configuration

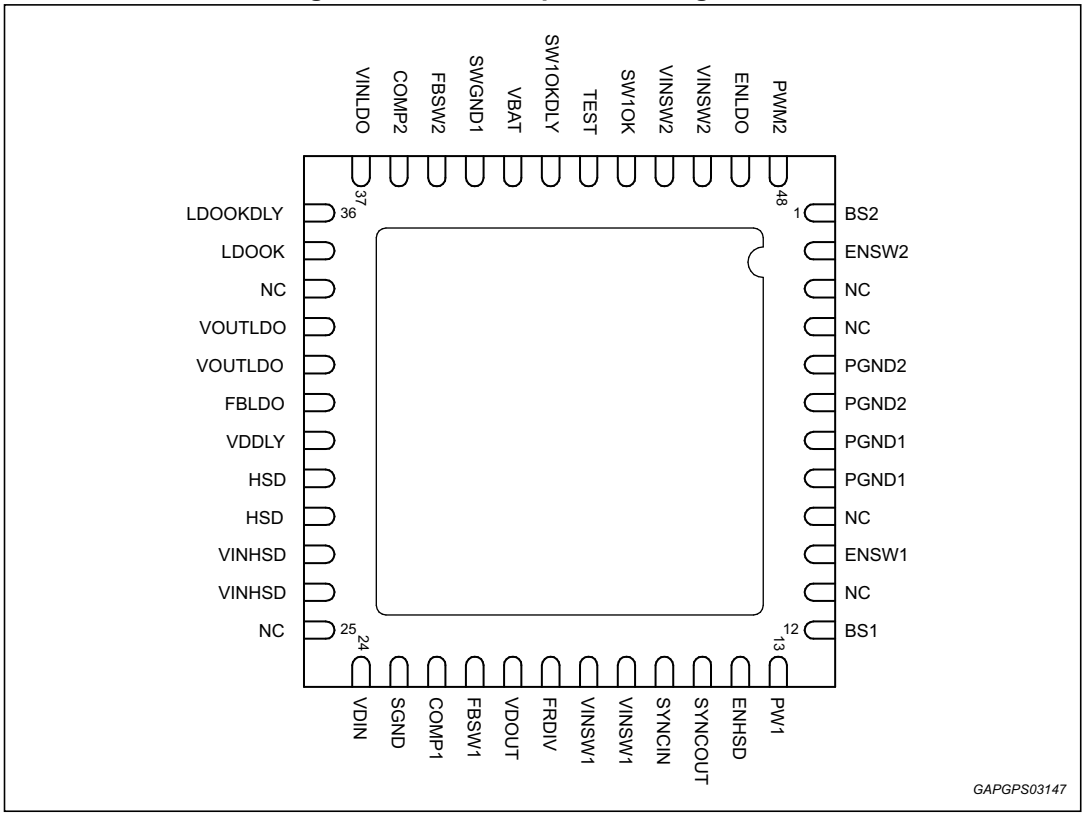


Table 3. VQFPN-48 pins description

Pin #	Name	Type	Function
1	BS2	Supply	Switching regulator 2 boosted supply
2	ENSW2	Input	Switching regulator 2 enable. 1.8/3.3 V compatible
3	NC	N.C.	Not connected
4	NC	N.C.	Not connected
5	PGND2	Ground	Switching regulator 2 power ground
6	PGND2	Ground	Switching regulator 2 power ground
7	PGND1	Ground	Switching regulator 1 power ground
8	PGND1	Ground	Switching regulator 1 power ground
9	NC	N.C.	Not connected
10	ENSW1	Input	Switching regulator 1 enable. 1.8/3.3 V compatible
11	NC	N.C.	Not connected
12	BS1	Supply	Switching regulator 1 boosted supply
13	PWM1	Output	Switching regulator 1 switching output
14	ENHSD	Input	Enable for High Side Driver. 1.8/3.3 V compatible
15	SYNCOUT	Output	External synchronization output (push-pull)

Table 3. VQFPN-48 pins description (continued)

Pin #	Name	Type	Function
16	SYNCIN	Input	External synchronization input
17	VINSW1	Supply	Switching regulator 1 supply voltage
18	VINSW1	Supply	Switching regulator 1 supply voltage
19	FRDIV	Input/output	Switching frequency divider setting
20	VDOUT	Output	Voltage detector output (open drain)
21	FBSW1	Input/output	Switching regulator 1 feedback voltage
22	COMP1	Input/output	Switching regulator 1 compensation
23	SGND	Ground	Ground for linear blocks
24	VDIN	Input	Voltage detector threshold setting
25	NC	N.C.	Not connected
26	VINHSD	Supply	High Side Driver supply
27	VINHSD	Supply	High Side Driver supply
28	HSD	Output	High Side Driver output
29	HSD	Output	High Side Driver output
30	VDDLY	Input/output	Voltage Detector delay setting
31	FBLDO	Input/output	LDO feedback voltage
32	VOUTLDO	Output	LDO output
33	VOUTLDO	Output	LDO output
34	NC	N.C.	Not connected
35	LDOOK	Output	LDO voltage detector output (open drain)
36	LDOOKDLY	Input/output	LDOOK delay setting
37	VINLDO	Supply	LDO supply
38	COMP2	Input/output	Switching regulator 2 compensation
39	FBSW2	Input/output	Switching regulator 2 feedback voltage
40	SWGND1	Ground	Low-power switching ground
41	VBAT	Supply	Common linear blocks supply voltage
42	SW1OKDLY	Input/output	SW1OK delay setting
43	TEST	n.a.	Pin for testing purposes. To be left unconnected
44	SW1OK	Output	Switching regulator 1 voltage detector output (open drain)
45	VINSW2	Supply	Switching regulator 2 supply voltage
46	VINSW2	Supply	Switching regulator 2 supply voltage
47	ENLDO	Input	LDO enable. 1.8/3.3 V compatible
48	PWM2	Output	Switching regulator 2 switching output

5 Electrical specifications

5.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Pin name / symbol	Parameter	Value	Unit
$VBAT_{OP}$ VIN_{OP}	Operating input voltage	-0.3 to +26	V
$VBAT_{MAX}$ VIN_{MAX}	Maximum transient supply voltage	-0.3 to +40	V
PGND1/2, SGND, SWGND, TAB	Ground pins voltage	-0.3 to +0.3	V
ENLDO	LDO enable pin voltage	-0.3 to +40	V
V_{pinop}	Other pins operating voltage	-0.3 to +3.6	V
V_{pinmax}	Other pins voltage	-0.3 to +4.6	V
T_{op}	Operating ambient temperature range	-40 to +105	°C
T_{stg}	Storage temperature range	-55 to +150	°C
T_j	Junction temperature	150	°C

5.2 Thermal data

Table 5. Thermal data (PowerSSO-36)

Symbol	Parameter	Board	Value	Unit
$R_{th\ j\text{-}a\text{-}2s}$	Thermal resistance junction-to-ambient (Max) (slug down configuration)	2s	53	°C/W
$R_{th\ j\text{-}a\text{-}2s2p}$		2s2p	27	°C/W
$R_{th\ j\text{-}a\text{-}2s2pv}$		2s2p+vias	22	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case (Max)		1.5	°C/W

Table 6. Thermal data (VQFPN-48)

Symbol	Parameter	Board	Value	Unit
$R_{th\ j\text{-}a\text{-}2s}$	Thermal resistance junction-to-ambient (Max)	2s	66	°C/W
$R_{th\ j\text{-}a\text{-}2s2p}$		2s2p	32	°C/W
$R_{th\ j\text{-}a\text{-}2s2pv}$		2s2p+vias	26	°C/W
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case (Max)		2.2	°C/W

5.3 Electrical characteristics

VBAT = VIN = 14.4 V, T_{amb} = 25 °C unless otherwise specified.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Inputs and controls						
$VBAT_{OP}$	VBAT operating range	Standby mode VOUTLDO = 1.2 V/100 mA VOUTLDO = 3.3 V/100 mA	 3.5 4	 - -	 26 26	 V V
I_q	Total quiescent current	Shutdown mode	-	1.5	2	µA
		Standby mode; $Iload_{LDO}$ = 100 µA	-	23	28	
OV_{VBAT}	Overvoltage shut-down threshold on VBAT	VBAT rising	27	29	31	V
UV_{VBAT}	Undervoltage shut-down threshold on VBAT	VBAT falling VDOUT forced to 0 V	2.7	3	3.3	V
Hys_{UV}	Hysteresis on UV_{VBAT}	-	-	0.1	0.5	V
ENmin	Min voltage for enable pins high level	-	1.6	-	-	V
ENmax	Max voltage for enable pins low level	-	-	-	1	V
R_{FRDIV}	Thresholds of value of resistor connected between FRDIV pin and ground	fsw_{SW2} = fsw_{SW1}	0	-	30	kΩ
		fsw_{SW2} = $fsw_{SW1/2}$	60	-	70	
		fsw_{SW2} = $fsw_{SW1/4}$	110	-	115	
		fsw_{SW2} = $fsw_{SW1/8}$	180	-	∞	
Voltage detector						
THR_{VDIN}	Voltage Detector input voltage threshold	-	0.9	0.94	0.98	V
Hys_{VDIN}	Voltage Detector input voltage hysteresis	-	-	30	40	mV
$Vmax_{VDOUT}$	VDOUT saturation voltage	I = 1 mA in VDOUT pin	-	-	0.1	V
I_{VDDLY}	VDDLY output current	-	6	9	12	µA
THR_{VDDLY}	VDDLY threshold	-	2.1	2.3	2.5	V
Linear regulator						
V_{FBLDO}	Feedback voltage	I_{load} = 100 mA	990	1000	1010	mV
UV_{LDO}	Undervoltage shut-down threshold on LDO	VINLDO decreasing	-	2.2	2.4	V
Hys_{LDO}	Hysteresis on UVLDO	-	-	-	100	mV
LdR_{LDO}	FBLDO load regulation	10 mA < I_{load} < 250 mA	-	5	-	mV
LnR_{LDO}	FBLDO line regulation	3.5 < VINLDO < 26 V Iload = 100 mA	-	1	-	mV

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ΔV_{FBLDO} / V_{FBLDO}	FBLDO Undershoot/overshoot(1)	5 mA ↔ 250 mA Iload transition	-5	-	5	%
		8 ↔ 18 V VINLDO transition	-5	-	5	
Vdo_{LDO}	Drop-out voltage	VOUTLDO = 3.3 V Iload = 250 mA VOUTLDO decreasing of 100 mV	-	270	320	mV
$Ishort_{LDO}$	Short circuit current limit	VOUTLDO shorted to ground	-	350	420	mA
$Ishort_{ST-BY}$		VOUTLDO (st-by) shorted to ground	-	65	80	mA
$PSRR_{LDO}$	Power supply rejection ratio	Iload = 50 mA, 10 Hz < f < 10 kHz 1 Vac_{pp} on VINLDO	-	70	-	dB
n_{LDO}	Output noise	20 Hz < f < 20 kHz Iload = 5 mA	-	100	-	µV
TSD_{LDO}	Thermal shut-down temperature	Temperature rising	150	160	-	°C
Hys_{TSDLDO}	Hysteresis on thermal shutdown temperature	-	5	-	15	°C
Co	Output capacitance(1)	-	3	-	-	µF
ESR	Output capacitor ESR(1)	-	-	-	0.2	Ω
Voltage detector on LDO						
THR_{LDOOK} / V_{FBLDO}	LDOOK threshold as percentage of FBLDO voltage	-	91	94	97	%
Hys_{LDOOK}	Hysteresis on LDOOK	-	-	90	-	mV
$Vmax_{LDOOK}$	LDOOK saturation voltage	I = 1 mA in LDOOK pin	-	-	0.2	V
$Tglitch_{LDOOK}$	Glitch filter time for LDO-OK	-	5	12	20	µs
$I_{LDOOKDLY}$	LDOOKDLY output current	-	7	10	13	µA
$THR_{LDOOKDLY}$	LDOOKDLY threshold	-	2	2.2	2.4	V
Switching regulators(2)						
V_{FBSWx}	Feedback voltage	I_{load} = 100 mA	980	1000	1020	mV
LdR_{SWx}	FBSWx load regulation(3)	50 mA < I_{load} < 1 A	-	1	-	mV
LnR_{SWx}	FBSWx line regulation(3)	3.5 V < VINSWx < 26 V	-	1	-	mV
UV_{SW1}	Undervoltage shut-down threshold on SW1	VINSWx decreasing	-	2.8	3	V
Hys_{SW1}	Hysteresis on UV_{SW1} (3)	-	-	0.15	-	V
UV_{SW2}	Undervoltage shut-down threshold on SW2	VINSWx decreasing	-	2.8	3	V
Hys_{SW2}	Hysteresis on UV_{SW2} (3)	-	-	0.15	-	V
ΔV_{FBSWx} / V_{FBSWx}	FBSWx pin undershoot/overshoot(3)	500 mA ↔ 1.5 A Iload transition	-5	-	5	%
		8 ↔ 18 V VINSWx transition	-5	-	5	%

Table 7. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$Ilim_{SW1}$	Peak current limitation on sw1	-	2.5	3	3.5	A
$Ilim_{SW2}$	Peak current limitation on sw2	-	3	3.5	4	A
fsw	Free-run switching frequency	-	225	250	275	kHz
fsync	Switching frequency range(3)	50% duty-cycle wave on SYNC pin	250	-	2000	kHz
Ron_{HS}	High side MOS on resistance(3)	VINSWx > 3.5 V; including bonding wires	-	85	-	mΩ
Ron_{LS}	Low side MOS on resistance(3)	Including bonding wires	-	105	-	mΩ
η	Efficiency(3)	Free run frequency VOUTSW1/2 = 5 V; Iload = 2.5 A VOUTSW1/2 = 5 V; Iload = 1 A	-	 90 93	-	%
$\Delta V_{FBSWx} / \Delta t$	FB pin slope at turn-on(3)	Including bonding wires	-	0.95	-	V/ms
TSD_{SWx}	Thermal shutdown temperature	Temperature rising	150	160	-	°C
Hys_{TSDSWx}	Hysteresis on thermal shutdown temperature	-	5	-	15	°C
THR_{SW1OK} / V_{FBSW1}	SW1OK threshold as percentage of FBSW1 voltage	-	91	94	97	%
Hys_{SW1OK}	Hysteresis on SW1OK	-	-	35	50	mV
$Vmax_{SW1OK}$	SW1OK saturation voltage	I = 1 mA in SW1OK pin	-	-	0.2	V
$Tglitch_{SW1OK}$	Glitch filter time for SW1-OK	-	9	13	17	µs
$I_{SW1OKDLY}$	SW1OKDLY output current	-	6	10	13	µA
$THR_{SW1OKDLY}$	SW1OKDLY threshold	-	2	2.2	2.4	V
t_{on-min}	Minimum on time(3)	-	-	20	-	ns
High side driver						
$Vdrop_{HSD}$	Output saturation	I_{load} = 0.5 A	-	140	170	mV
$Ishort_{HSD}$	Short circuit current limit	-	0.7	1	1.3	A
TSD_{HSD}	Thermal shut-down temperature	Temperature rising	150	160	-	°C
Hys_{TSDHSD}	Hysteresis on thermal shutdown temperature	-	5	-	15	°C

1. Not tested at ATE.
2. Tests involving switching frequencies higher than 1 MHz are guaranteed by design.
3. Test guaranteed by application measurements.

Figure 6. PSRR LDO 50 mA load vs. frequency

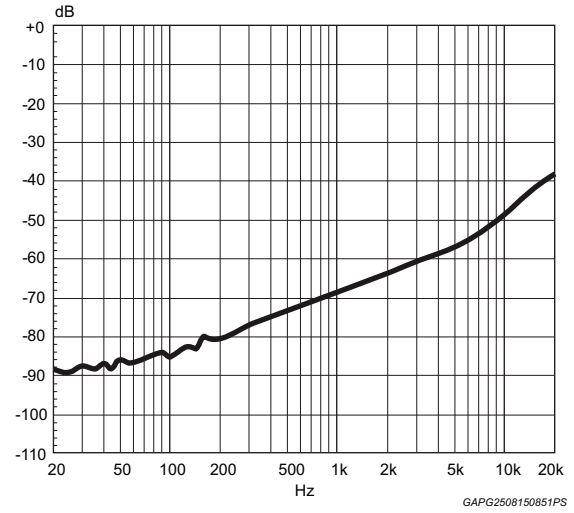


Figure 7. Efficiency vs. output current (VIN = 14 V, fsw = 2 MHz)

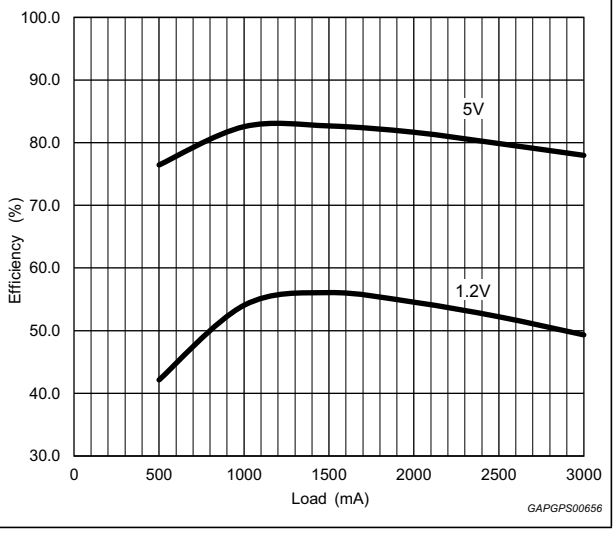
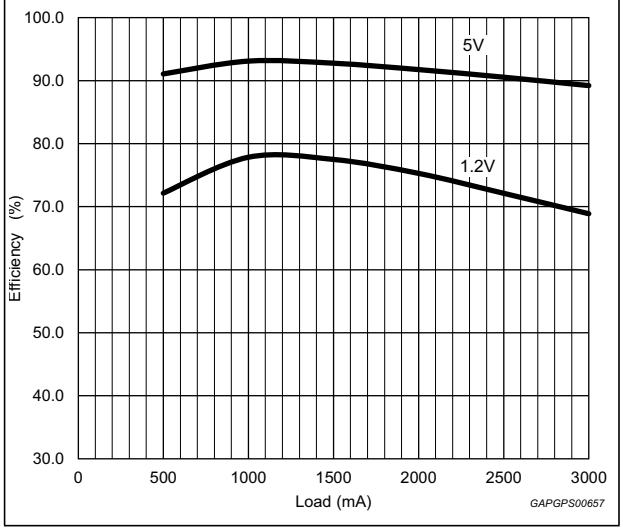


Figure 8. Efficiency vs. output current (VIN = 14 V, fsw = 250 kHz)



6 Functional Description

6.1 Operative modes

L5963 has three main operative modes:

- Shutdown mode: all enable pins are low and the device is completely off. In this condition the quiescent current is typically 1.5 µA.
- Standby mode: the linear regulator is configured as stand-by regulator by connecting ENLDO directly to VINLDO. In this condition the quiescent current is typically 25 µA.
- Normal mode: the linear regulator works as LDO and/or other blocks (DC/DC or HSD) are turned on.

6.2 Blocks functional description

6.2.1 Unregulated supply input voltage (VINLDO)

This terminal provides the power for internal circuitry to bias band-gap reference, standby regulator and other circuitry in the device.

If backup function is needed, an external capacitor connected to this pin shall be charged through an external diode which is used to block reverse discharging. With backup function, when the system battery is removed or drops too low suddenly, the internal bias and regulator can operate correctly for a certain time, which avoids MCU to work abnormally and allows MCU to have enough time to turn-off.

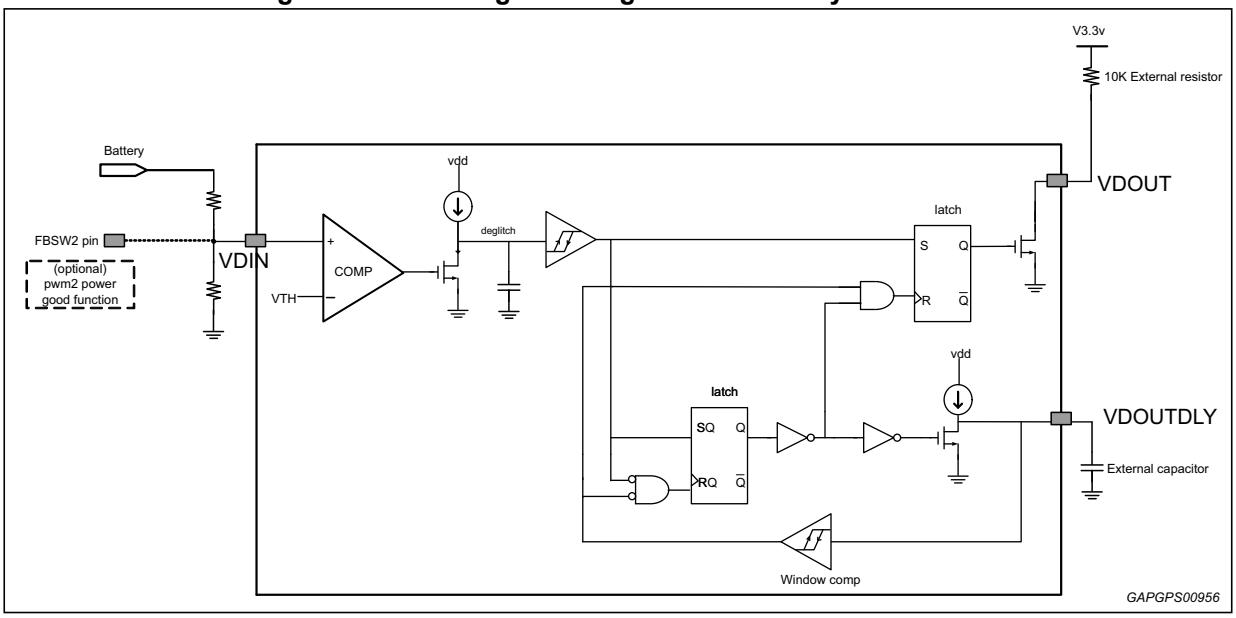
6.2.2 Low voltage warning monitor (related pins: VDIN, VDOUT, VDDLY)

An external voltage can be sensed through the VDIN pin. This voltage is scaled using an external resistor network and compared with an internal threshold to detect a low voltage condition (*Figure 9.*). Once the input voltage is below the threshold, the low voltage warning output terminal (VDOUT) is pulled low after the designed glitch-filtering (~12 µs). VDOUT is an open drain output. If the input returns above the threshold with the specified hysteresis, VDOUT is released after a defined delay, determined by the capacitor on pin VDDLY. The threshold is fixed to 0.95 V typ.

The capacitor on VDDLY pin sets VDOUT delay. A current source (~9 µA) on this pin charges the external capacitor to generate the required delay, programmable by adjusting the value of the capacitor.

This voltage monitor can also be used to monitor DC/DC2 output. Changing the ratio of the external resistor divider the low voltage warning threshold can be adjusted.

Figure 9. Low voltage warning monitor & delay schematic



6.2.3 Power-good reset (related pins: LDOOK, LDOOKDLY)

LDOOK monitors the regulator output VOUTLDO. Its circuit topology is the same as the voltage detector one (*Figure 9*). Its threshold is fixed to 95% typ of the feedback voltage, and the hysteresis is always ~2% typ. Pin LDOOK is an open drain output, and pin LDOOKDLY is used to adjust the delay in the release of LDOOK output.

6.2.4 Power-good function of DC/DC1 (related pins: SW1OK, SW1OKDLY)

SW1OK monitors DC/DC1 output. Its circuit topology is the same as the voltage detector one (*Figure 9*). Its threshold can't be adjusted, it is always 95% typ of the feedback voltage, and the hysteresis is ~35mV typ. Pin SW1OK is an open drain output, and pin SW1OKDLY is used to adjust its delay.

6.2.5 Over voltage shutdown

Two internal over voltage shutdown (OV) blocks are included in L5963. One (OV1) senses VBAT pin, the other (OV2) detects VINLDO pin.

If VBAT gets too high, to prevent any damage, DC/DC1, DC/DC2 and the high-side driver are disabled by OV1. They will be turned on once VBAT returns below the detection threshold with the specified hysteresis.

If the linear regulator works as a non-standby regulator and VINLDO gets too high, to prevent any damage the LDO is disabled by OV2. It is turned on once VINLDO returns below the detection threshold with the specified hysteresis.

On the contrary, the linear regulator works as a standby regulator, OV2 doesn't intervene and the regulator continues to work even if VINLDO increases.

6.2.6 Power ground (PGND1 and PGND2)

PGND1 pin and PGND2 pin are power ground references for the DC/DC1 and DC/DC2 respectively. All switching nodes are referred to these two pins.

6.2.7 Signal ground (SGND)

This pin is the ground reference for standby regulator, HSD and internal bias.

6.2.8 PWM signal ground (SWGND)

This pin is the ground reference for signal part of DC/DC1 and DC/DC2.

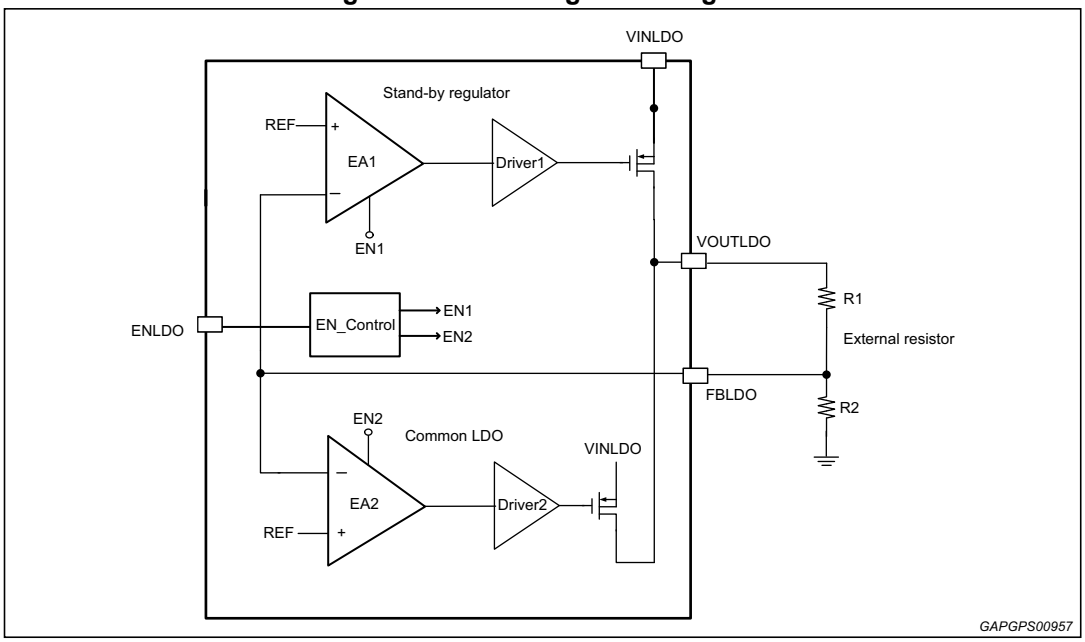
6.2.9 TAB

TAB is connected to the device substrate.

This pin must be connected to GND to guarantee the substrate is always at the lowest potential to avoid parasitic activation.

6.2.10 Linear regulator

Figure 10. Linear regulator diagram



The linear regulator has two operative modes: standby mode and non-standby mode. Its output voltage is set by an external resistor divider through the feedback pin FBLDO.

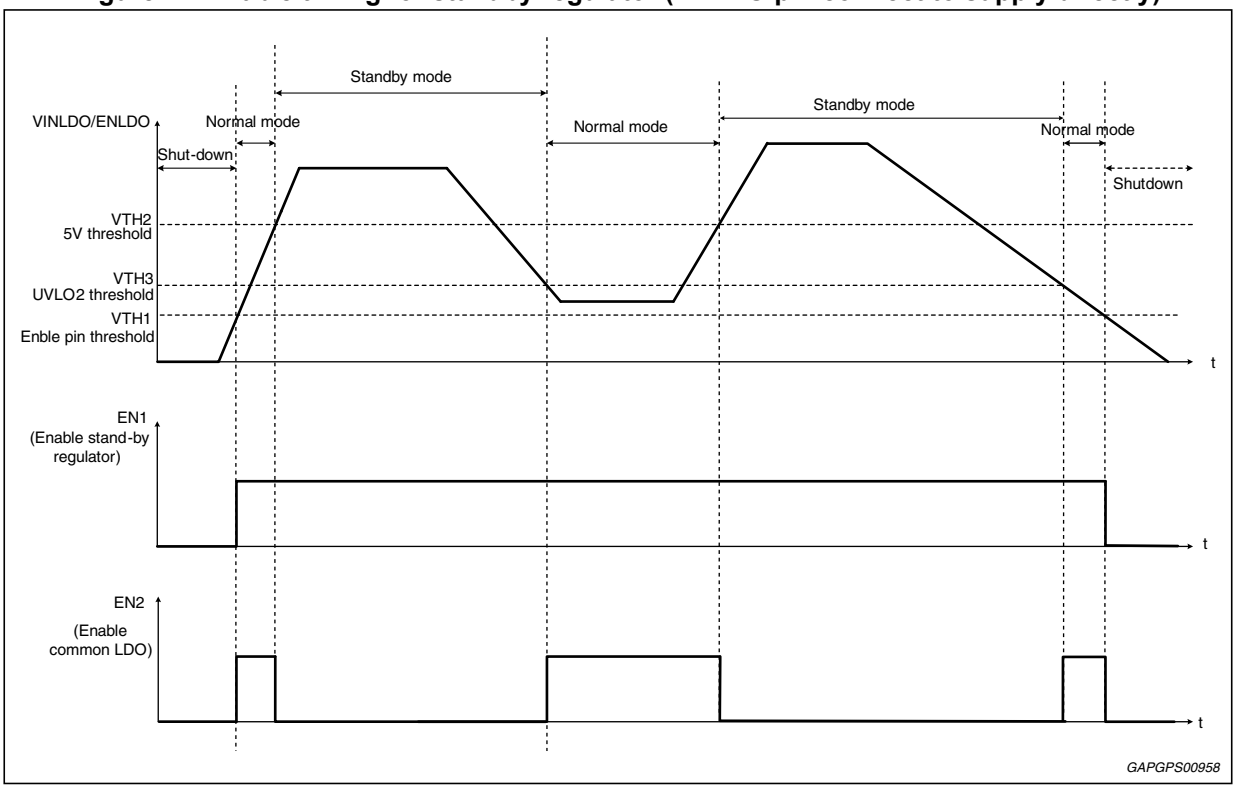
As a standby regulator, the current capability is reduced to 50 mA and the quiescent current minimized.

In this case, the external resistor divider should be in the Mega ohm order to reduce total quiescent current.

As a non standby regulator, it has higher load capability (up to 250 mA).

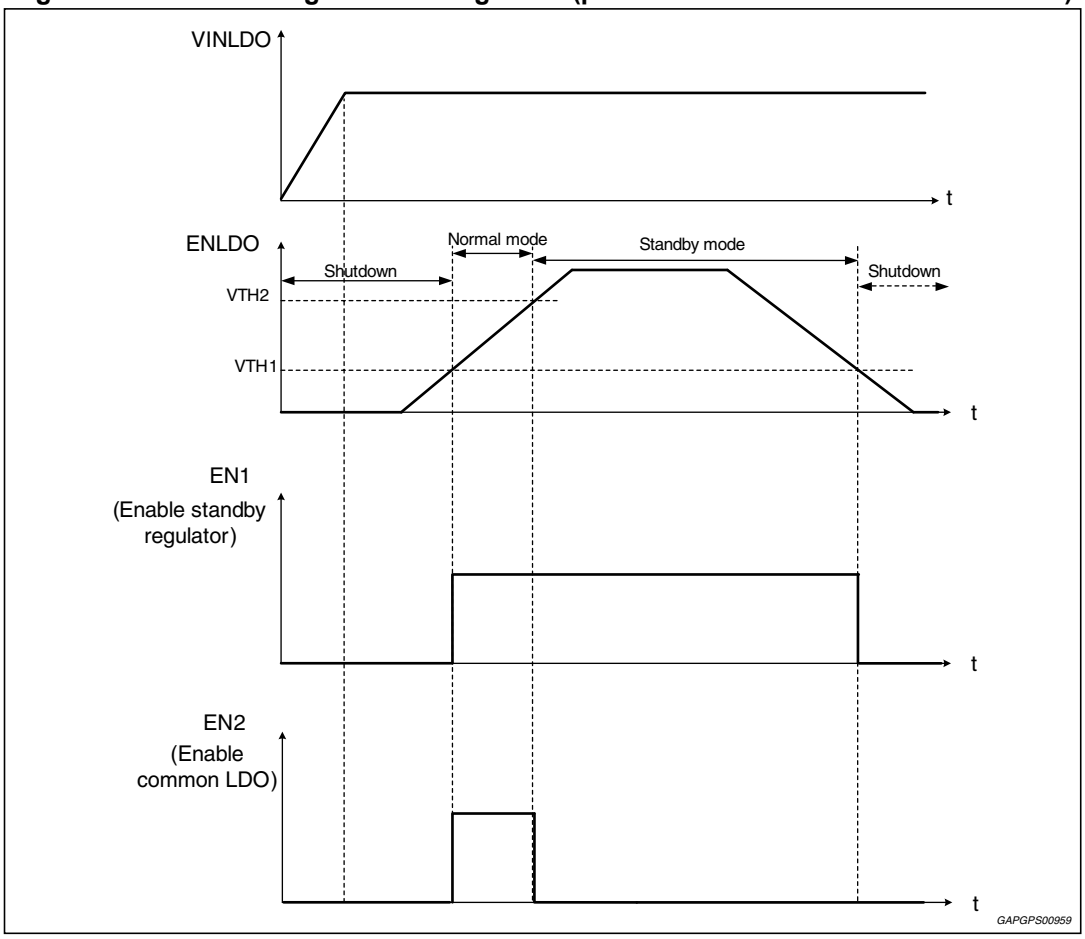
Connecting ENLDO pin directly to its supply VINLDO (it should be higher than 5 V), the regulator works as a standby regulator. Once ENLDO is ever higher than 5 V, the regulator works as a standby regulator till VINLDO is powered down, to reset a flag stored in an internal register.

Figure 11. Enable timing for standby regulator (ENLDO pin connect to supply directly)



The linear regulator works as a non-standby regulator if ENLDO is <5 V.

Figure 12. Enable timing for linear regulator (pin ENLDO isn't connected to VINLDO)



The linear regulator operates with output voltages down to 1.2 V, and offers a maximum dropout voltage of 500 mV at rated load current.

This regulator has an independent thermal protection and a current-limiting circuit.

It should be always supplied (by VINLDO) with a voltage not lower than 3.5 V because, even if not used, it gives the common supply to all internal blocks which have to stay alive when the battery drops too low (backup functionality).

6.2.11 High-side driver (HSD)

The HSD pin is the output of the high side driver. It has a dedicated enable pin ENHSD. Following protections are implemented:

- Over-current protection
- Short to supply
- Short to ground
- Short through the load to -1 V
- Unpowered short to supply
- Loss of ground
- Over voltage protection

Thermal protection

The HSD has an independent thermal shutdown protection.

If the local die temperature exceeds the thermal shutdown detection threshold, the HSD is disabled. It is enabled once the local die temperature falls below the detection threshold with the specified hysteresis. The invoking of thermal shut down on HSD does not directly affect any other outputs or circuitry in the IC.

Short to ground

The high side driver output is protected against shorts to ground. The faulted output returns to its pre-fault operating condition once the fault is removed.

Short to supply

The high-side driver is protected against shorts to battery. In such an event, the IC is not damaged. External components connected directly to the IC are not damaged by such exposure.

Loss of ground protection

The high side driver is protected against excessive leakage current to an external ground during a loss of supply ground (i.e. ground is open). During this event, the HSD is disabled and the IC is not damaged.

Loss of battery protection (Unpowered shorts to battery, SPU)

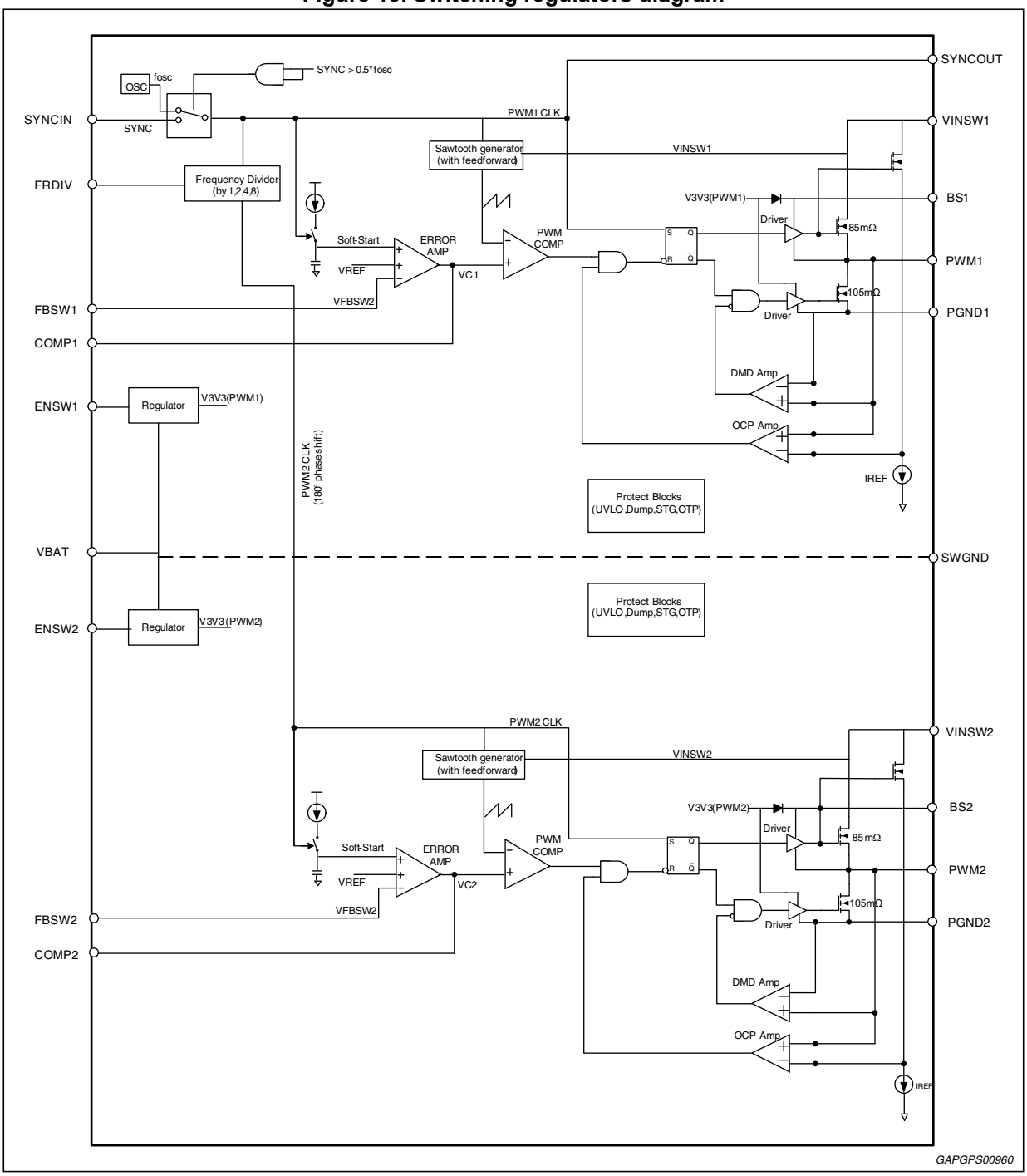
The high-side driver is protected against unpowered shorts to battery. In such an event, in typical applicative conditions, the IC will not suffer any damage.

Below-ground protection

The HSD output can be brought below ground by the inductive load. In this case, Power PMOS is turned on to charge the output, protecting itself.

6.2.12 Switching regulators

Figure 13. Switching regulators diagram



L5963 embeds two synchronous DC/DC converters that incorporate all the control and necessary protection circuitries to satisfy a wide range of applications. DC/DC1 and DC/DC2 are enabled by pin ENSW1 and pin ENSW2 respectively. The two switching converters employ voltage mode control and feed forward function to provide good load regulation and line regulation.

Both switching regulators can operate up to a 100% duty cycle. Once every four switching periods, the PWM output is forced low for 100ns typ to refresh the bootstrap capacitor.

Their features include:

- Wide input voltage range (from 3.5 V to 26 V)
- Min output of 1 V
- 250 kHz free-run frequency and synchronization range from 250 kHz to 2 MHz. The voltage feed forward is implemented in all frequency range
- Internal 85 mΩ high-side and 105 mΩ low-side switching MOSFET
- Up to 3 A load current capability
- Power ok (SW1OK) output
- Internal soft start function to minimize startup inrush current
- Pulse-by-pulse current limiting (OCP)
- Discontinuous mode detection (DMC)
- Over temperature protection (OTP)
- UVLO with stop threshold at 2.8 V (typ)
- Load dump protection
- Externally adjustable compensation
- Stable with ceramic output capacitors

Oscillator/switching frequency

The internal oscillator provides a constant frequency clock of 250 kHz. The switching frequency of DC/DC1 and DC/DC2 are determined by the internal frequency clock and the external synchronization clock.

When no clock is applied to the SYNCIN pin or the synchronization clock is lower than 125 kHz (half of the internal clock), the two switching regulators work both with the internal 250 kHz clock. When the SYNCIN pin has a synchronization clock larger than 125 kHz, the external synchronization clock is adopted.

There is a phase shift of 180° between PWM1 and PWM2, and the frequency of PWM2 can be the same, 1/2, 1/4, 1/8 of PWM1 one. The division factor is programmed by FRDIV pin. The switching clock of DC/DC1 can be sent out by pin SYNCOUT to synchronize another device, in view of reducing EM disturbance.

Internal high-side and low-side Power MOSFET / Bootstrap structure

The two synchronous switching regulators don't need the external Schottky diode. Each of them integrates a high-side and a low-side n-channel Power MOSFET, which allows a very low drop voltage under high load current operation (up to 3 A).

The Bootstrap structure is used to drive the high-side n-channel Power MOSFET. A Bootstrap capacitor of about 47 nF is needed.

Internal soft start function (SS)

To reduce the inrush current during startup, an internal soft start is implemented. The total soft start time is about 400 µs and it doesn't change with operating frequency.

Pulse-by-pulse current limiting (OCP)

The current in the upper MOSFET is monitored and if it exceeds the pulse-by-pulse over-current threshold (ILIM) then the upper MOSFET is turned off. Normal PWM operation resumes on the next oscillator clock pulse. DC/DCs' embed leading edge blanking to prevent falsely triggering the pulse-by-pulse current limit when the upper MOSFET is turned on. The blanking time is about 100 ns, so the minimum switching on time should be bigger than 100 ns:

Equation 1

$$\frac{D}{f_{SW}} > 100ns \Rightarrow f_{SW} < \frac{D}{100ns} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{100ns}$$

From the above equation, when the input and output voltage are already known, the switching frequency should be within the range of the above equation, otherwise the OCP function is not guaranteed. Pulse-by-pulse current limiting is always active. The threshold of OCP is about 3.5 A for dc-dc1 and 4A for dc-dc2.

Low-Side Over Current Protection (LS OCP)

LS OCP protects DC/DCs by limiting inductor current, when either the load is too high at high frequency or when the output of the converter is shorted to ground.

The current in the low-side MOSFET is monitored and, if it exceeds the pulse-by-pulse overcurrent threshold (ILIM), it prevents the turning on of the high-side MOSFET in the successive switching period.

In high frequency and high load conditions, the inductor current cannot decrease even if HS OCP is triggered due to the blanking time, which results in the inductor current getting higher and higher every switching period. If inductor current reaches LS OCP threshold, that is set to a level higher than HS OCP one, PWM switching is stopped, waiting for the inductor current to decrease to a lower value. PWM switching will recover as soon as LS OCP is released.

If high load and high frequency conditions remain, for instance in case of a short circuit being present on the regulator output, another LS OCP will occur. Upon removal of the short circuit PWM switching will immediately recover, bringing the regulator back to normal operation.

Discontinuous Mode Detection (DMD)

In order to save quiescent current when switching regulators are working in light load condition, L5963 embeds a Discontinuous Mode Detection (DMD) circuit: DMD prevents inductor current to continuously flow to ground during T_{off} by turning off LS MOSFET and leaving PWM in tristate.

Over temperature protection (OTP)

Each DC/DC has its own OTP, which detects the local temperature and shuts down the regulator when temperature reaches the specified threshold.

Dump protection

If the voltage on VBAT supply exceeds the over-voltage shut-down threshold, DC/DCs are disabled. Once VBAT returns to working conditions, the output recovers to the normal state.

Under voltage lock out (UVLO)

The UVLO circuit generates the shutdown signal to turn off DC/DCs when VBAT is lower than the specified threshold. They are turned back on once VBAT goes above the detection threshold with the specified hysteresis.

7 Application information

7.1 Output inductor (Lo)

The value of the output inductor (Lo) is usually calculated to satisfy the peak-to-peak ripple current requirement. For the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of the maximum current.

For example, if $\Delta I_L = I_{Ripple} = 0.3 \times I_{OUT(max)}$.

Where, $I_{OUT(max)}$ is the maximum output current.

Then, the inductor value can be estimated by the following equation:

Equation 2

$$L \geq \frac{V_{OUT}}{f_{SW} \times \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right)$$

Where, f_{SW} is the switching frequency, $V_{IN(max)}$ is the maximum input voltage.

If V_{OUT} = 3.3 V, $V_{IN(max)}$ = 26 V, f_{SW} = 250 kHz, ΔI_L = 0.3 x 3 A = 0.9 A

Equation 3

$$L \geq \frac{3.3}{250 \times 10^3 \times 0.9} \times \left(1 - \frac{3.3}{26}\right) \mu H = 12.8 \mu H$$

The next higher available value should be used, so L = 15 µH.

The peak current flowing in Inductor is $I_{L(peak)} = I_{OUT(max)} + \Delta I_L / 2$.

If the Inductor value decreases, the peak current increases. The peak current has to be lower than the current limit of the device.

An inductor having saturation current higher than the device current limit has to be chosen.

7.2 Output capacitors (COUT)

Output capacitors are selected to support load transients and output ripple current, as well as to get loop stability.

The amount of voltage ripple can be calculated by the output ripple current flowing in the Inductor:

Equation 4

$$\Delta V_{out} = ESR \times \Delta I_L + \frac{\Delta I_L}{8 \times C_{out} \times f_{sw}}$$

Usually the first term is dominant. However, if a ceramic capacitor (which is recommended) is adopted, the first term on the above equation can be neglected as the ESR value is very low.

For example, in case V_{out} = 3.3 V, V_{in} = 14 V, f_{SW} = 250 kHz, ΔI_L = 0.3 x 3 A = 0.9 A, in order to have a ΔV_{out} = 5%* V_{out} =0.165 V, a 4.7 µF ceramic capacitor is needed. In case of not negligible ESR (electrolytic or tantalum capacitors), the capacitor is chosen taking into account its ESR value.

In the above example, if a 100 µF with ESR = 100 mΩ electrolytic capacitor is chosen, the voltage drop on ESR dominates and the voltage ripple is 90 mV.

The output capacitor is also important to sustain the output voltage during a load transient. In general, minimizing the ESR value and increasing the output capacitance results in a better transient response. The ESR can be minimized by simply adding more capacitors in parallel, or by using higher quality capacitors. If ceramic capacitors are chosen, in presence of a fast load transient the output voltage will change by the amount.

Equation 5

$$\Delta V_{out} = \frac{L}{2} \times \frac{I_{out(max)}^2 - I_{out(min)}^2}{C_{out} \times V_{out}}$$

Where:

$I_{out(max)}$, $I_{out(min)}$ refer to the worst case load in the system and ΔV_{out} is the tolerance of the regulated output voltage, 5% of V_{out}.

For example, V_{out} = 5 V, V_{in} = 14 V, $I_{out(max)}$ =1.5 A, $I_{out(min)}$ = 0.5 A, L = 22 µH

Equation 6

$$C_{out} = \frac{L}{2} \times \frac{I_{out\,(max)}^2 - I_{out\,(min)}^2}{\Delta V_{out} \times V_{out}} = 17.6\,\mu F$$

So two 10 µF ceramic capacitors in parallel are needed.

The output capacitor is also important for loop stability: it fixes the double LC filter pole and the zero due to its ESR. In *Section 7.5: Compensation network*, it will be illustrated how to consider its effect in the system stability.

7.3 Input capacitors (C_{IN})

The input capacitors must be chosen to support the maximum input operating voltage and the maximum RMS input current required by the device.

The input capacitors must deliver the RMS current according to below equation:

Equation 7

$$I_{rms} = I_o\sqrt{D \times (1-D)}$$

Where Io is the maximum DC output current and D is the duty cycle. This function has a maximum at D = 0.5 and it is equal to $I_o/2$.

Equation 8

$$D = \frac{V_{out} + V_{dl}}{V_{in} - V_{dh} + V_{dl}}$$

V_{dl} is the voltage drop across the low side DMOS, and V_{dh} is the voltage drop across the high side DMOS.

For example, with 20% duty cycle, the input/output current multiplier is 0.400. Therefore, if the regulator is delivering 3 A of steady-state load current, the input capacitor(s) must support 0.400 × 3 A or 1.2 Arms.

Ceramic capacitors can deliver quite a bit of current but their total capacitance is relatively low. Electrolytic capacitors typically offer much more capacitance than ceramic capacitors, but can typically deliver a current of 100 to 500 mArms. So a good design will employ both types of capacitors with the ceramic capacitors placed closest to the input pins of the device. As a result, ceramic capacitors which have very low ESR and inductance are the best for filtering the high frequency switching noise, and electrolytic capacitors are typically able to provide more current over extended periods of time where VIN would otherwise droop.

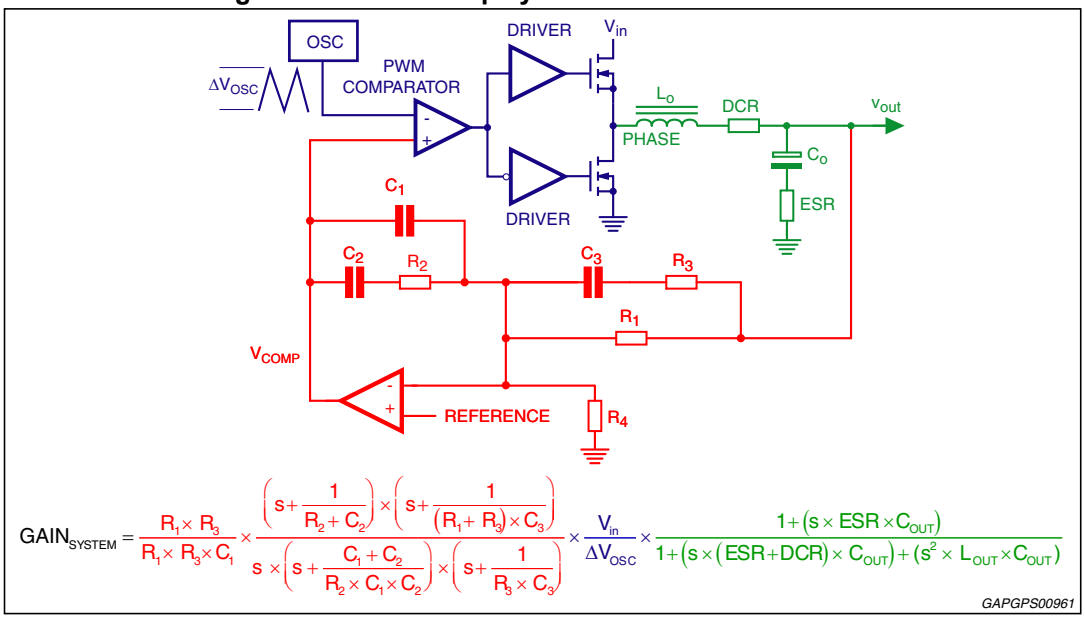
7.4 Bootstrap capacitor (CBOOT)

A bootstrap capacitor must be connected between the BOOT and SW pins to provide floating gate drive to the high-side MOSFET. For most applications 47 nF is sufficient. This should be a ceramic capacitor with a voltage rating of at least 6 V.

7.5 Compensation network

The compensation network has to assure stability and good dynamic performance. The loop of the device is based on the voltage mode control, compatible with TYPE III compensation network (*Figure 14*). The error amplifier is a voltage operational amplifier with large bandwidth, which is much larger than the closed-loop one.

Figure 14. Closed loop system with TYPE III network



$$GAIN_{SYSTEM} = \frac{R_1 \times R_3}{R_1 \times R_3 \times C_1} \times \frac{\left(s + \frac{1}{R_2 + C_2}\right) \times \left(s + \frac{1}{(R_1 + R_3) \times C_3}\right)}{s \times \left(s + \frac{C_1 + C_2}{R_2 \times C_1 \times C_2}\right) \times \left(s + \frac{1}{R_3 \times C_3}\right)} \times \frac{V_{in}}{\Delta V_{osc}} \times \frac{1 + (s \times ESR \times C_{OUT})}{1 + (s \times (ESR + DCR) \times C_{OUT}) + (s^2 \times L_{OUT} \times C_{OUT})}$$

The above figure shows the closed loop system with a TYPE III compensation network and presents the closed loop transfer function. See the guidelines for calculation of TYPE III network below:

1. Choose a value for R_1, usually between 2 k and 5 kΩ.
2. Choose a gain (R_2/R_1) that shifts the Open Loop Gain up to give the desired bandwidth. This allows the 0 dB crossover to occur in the frequency range where the Type III network has its second plateau in the gain. The following equation calculates an R_2 that accomplishes this, given the system parameters and a chosen R_1.

Equation 9

$$R_2 = \frac{DWB}{F_{LC}} \times \frac{\Delta V_{osc}}{V_{IN}} \times R_1$$

3. C2 is calculated by placing the zero at 50% of the output filter double pole frequency:

Equation 10

$$C_2 = \frac{1}{\pi \times R_2 \times F_{LC}}$$

4. C1 can be calculated by placing the first pole at the ESR zero frequency:

Equation 11

$$C_1 = \frac{C_2}{2 \times \pi \times R_2 \times C_2 \times F_{ESR} - 1}$$

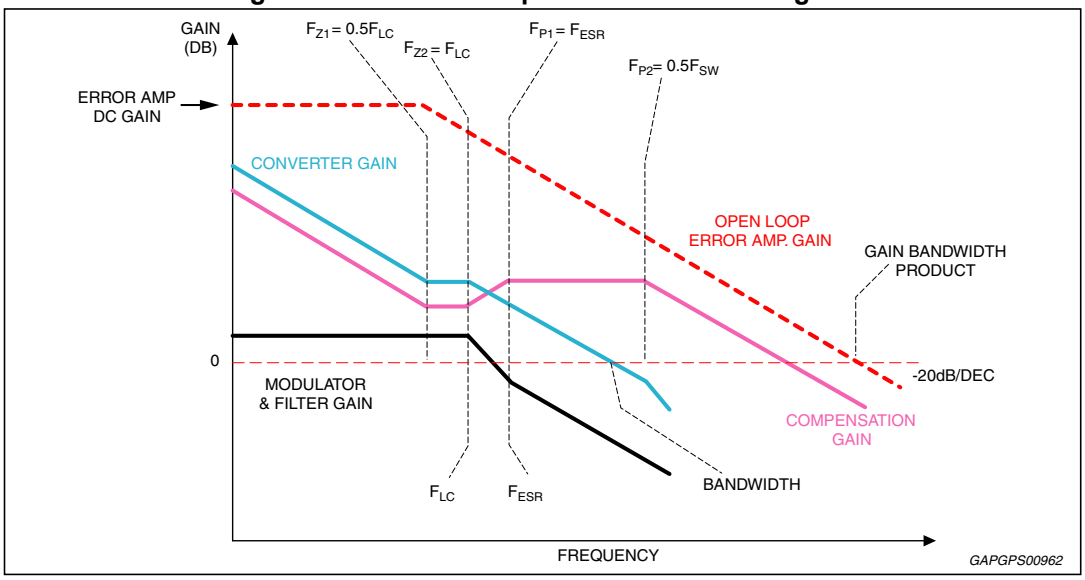
5. Set the second pole at half the switching frequency and also set the second zero at the output filter double pole. This combination brings the following equation:

Equation 12

$$R_3 = \frac{R_1}{\frac{F_{SW}}{2 \times F_{LC}} - 1} \; ; \quad C_3 = \frac{1}{\pi \times R_3 \times F_{SW}}$$

The figure below shows the asymptotic Bode gain plot for the TYPE III compensated system and the gain and phase equations for the compensated system

Figure 15. TYPE III compensated network diagram



Here an example of calculating the external components network step by step.

Suppose the requirements for a dc-dc regulator are the following:

Input voltage minimum $V_{in(min)}$	8 V
Input voltage maximum $V_{in(max)}$	26 V
Input voltage typical $V_{in(typ)}$	14 V
Output voltage buck regulator 1- VBUCK 1	Min = 4.75 V, Max = 5.25 V
Converter switching frequency, fsw	250 kHz
Maximum output current on buck regulator 1-VBUCK 1	3 A
Maximum ripple current I_{Ripple}	0.3* I_{out}
Load transition requirement	500 mA ↔ 1.5 A in Δt = TBD

Assume TYPE III Compensation network.

STEP 1 - Calculate the inductor value

Using *Equation 13*, to find the inductor value, assume inductor ripple current of 0.9 A.

Equation 13

$$L \geq \frac{V_{out}}{F_{SW} \times \Delta I_L}\left(1 - \frac{V_{out}}{V_{in\ (max)}}\right) = \frac{5}{250 \times 10^3 \times 0.9}\left(1 - \frac{5}{26}\right) \mu H \approx 18\ \mu H$$

The next higher available value should be used, so L = 22 µH.

STEP 2 - Inductor peak current

Using *Equation 14*, the peak inductor current is:

Equation 14

$$I_{L(peak)} = I_{out(max)} + \Delta I_L /2 = 3\ A + (0.9/2)\ A = 3.45\ A$$

STEP 3 - Calculate the output capacitance

Using *Equation 15*, the output capacitance is:

Equation 15

$$C_{out} = \frac{L}{2} \times \frac{I_{out\,(max)}^2 - I_{out\,(min)}^2}{\Delta V_{out} \times V_{out}} = \frac{22 \times 10^{-6}}{2} \times \frac{1.5^2 - 0.5^2}{5\% \times 5 \times 5} = 17.6\,\mu F$$

So choose two 10 µF ceramic capacitors in parallel, and the voltage ripple is within the spec.

Equation 16

$$\Delta V_{out} = ESR \times \Delta I_L + \frac{\Delta I_L}{8 \times C_{out} \times f_{sw}} = \frac{0.9}{8 \times 20 \times 10^{-6} \times 250 \times 10^3} = 22.5\,mV$$

(ESR can be neglect due to ceramic cap)

STEP 4 - Calculate loop compensation values.

Using *Equation 17* to determine the "double pole":

Equation 17

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \cdot C_{out}}} = \frac{1}{2 \times 3.14 \times \sqrt{22 \times 10^{-6} \times 20 \times 10^{-6}}} = 7.59\ kHz$$

Using *Equation 18* to determine the zero due to the ESR of the output capacitor C_{out} with ESR = 10 mΩ:

Equation 18

$$f_{ESR} = \frac{1}{2\pi \times C_{out} \times ESR} = \frac{1}{2 \times 3.14 \times 20 \times 10^{-6} \times 10 \times 10^{-3}} = 796\,kHz$$

DBW = f_c = 0.14 x f_{sw} = 35kHz

Choose R1 = 5 kΩ, using *Equation 19*:

Equation 19

$$R4 = \frac{R1}{\frac{V_{out}}{V_{REF}} - 1} = \frac{5k}{\frac{5}{1} - 1} = 1.25k\Omega$$

R4 =1.24 kΩ

PWM modulator gain.

Equation 20

$$Gain_{modulator} = \frac{V_{IN}}{\Delta V_{OSC}} = \frac{14}{1.5}$$

Where V_{IN} is the typical input operating voltage, ΔV_{OSC} is the saw-tooth peak-to-peak value.

Using *Equation 21*:

Equation 21

$$R2 = \frac{DBW}{f_{LC}} \times \frac{\Delta V_{OSC}}{V_{IN}} \times R1 = \frac{35k}{7.59k} \times \frac{1.5}{14} \times 5k = 2.46k$$

R2 = 2.4 kΩ

Using *Equation 22*:

Equation 22

$$C2 = \frac{1}{\pi \times R2 \times f_{LC}} = \frac{1}{3.14 \times 2.4 \times 10^3 \times 7.59 \times 10^3} = 17.5 \times 10^{-9}\,F$$

Choose C2 = 16 nF

Using *Equation 23*:

Equation23

$$C1 = \frac{1}{2\pi \times R2 \times C2 \times f_{ESR} - 1} = \frac{16 \times 10^{-9}}{2 \times 3.14 \times 2.4 \times 10^3 \times 16 \times 10^{-9} \times 796 \times 10^3 - 1} = 83.3 \times 10^{-9}\,F$$

Choose C1= 82 nF.

Using *Equation 24*:

Equation 24

$$R3 = \frac{R1}{\frac{f_{SW}}{2 \times f_{LC}} - 1} = \frac{5k}{\frac{250 \times 10^3}{2 \times 7.59 \times 10^3} - 1} = 323\Omega$$

Choose R3 = 330 Ω.

Using *Equation 25*:

Equation 25

$$C3 = \frac{1}{\pi \times R3 \times f_{SW}} = \frac{1}{3.14 \times 330 \times 250 \times 10^3} = 3.86 \times 10^{-9} F$$

Choose C3 = 3.9 nF.

This is a table to summarize components value for different output voltage cases:

Table 8. Components value for different output voltage cases

V_{OUT}(V)	Fsw (Hz)	Lo (µH)	Co (µF)	R1 (kΩ)	R2 (kΩ)	R3 (Ω)	R4 (kΩ)	C1 (pF)	C2 (nF)	C3 (nF)
5	2M	2.7	4.7	4.99	1.2	220	1.24	33	5.6	0.68
	250k	22	2x10	4.99	2.4	390	1.24	82	16	3.9
3.3	2M	2.2	10	4.99	1.5	180	2.15	56	6.2	0.82
	250k	15	2x10	4.99	2	470	2.15	100	16	3.3
1.2	2M	1.5	2x10	4.99	1.8	160	24.9	100	5.6	1
	250k	6.8	2x10	4.99	1.2	680	24.9	150	16	2.2

8 Thermal design

The PCB design should take into account also thermal aspects.

The maximum power manageable by the IC depends on how the board is designed and on the package junction to ambient thermal resistance.

The temperature inside the IC (junction temperature) should not exceed 150 °C or one or more thermal shut-down protections intervene.

The total power dissipation is approximately given by the sum of the power dissipation of the two dc-dc regulators and the linear regulator:

$$Pd = Pdpwm1 + Pdpwm2 + Pdldo$$

Where:

$Pd_{issDC/DC} = Iload_{DC/DC} \times Vout_{DC/DC} \times (1-\eta)/\eta$;

η is the efficiency, as shown in *Figure 7* and *8*.

$P_{dissLDO} = Iload_{LDO} \times (VINLDO-VOUTLDO)$

The junction temperature is estimated in this way:

$$T_j = T_a + Pd \times R_{thj-a}$$

Where:

T_a is the maximum ambient temperature;

$R_{thj-amb}$ is the junction to ambient thermal resistance, as defined in *Table 5* and *Table 6*.

The slug has to be connected to the ground plane, whenever possible.

According to below formula and considering TSD_TH thermal shutdown minimum threshold at 150 °C, maximum suggested power dissipation, for a slug-down configuration, can be easily retrieved:

$$P_{DISS\_suggested} = (T_{SHD} - T_{amb}) / R_{thj-a}$$

Table 9. Maximum suggested power for L5963 in PSSO36 slug-down package

Symbol	T_{amb} 105 °C	T_{amb} 80 °C
$R_{th\ j-a-2s}$	0.85 W	1.32 W
$R_{th\ j-a-2s2p}$	1.66 W	2.6 W
$R_{th\ j-a-2s2pvias}$	2.05 W	3.2 W

Table 10. Maximum suggested power for L5963 in QFN48 package

Symbol	T_{amb} 105 °C	T_{amb} 80 °C
$R_{th\ j-a-2s}$	0.68 W	1.06 W
$R_{th\ j-a-2s2p}$	1.41 W	1.19 W
$R_{th\ j-a-2s2pvias}$	1.73 W	2.7 W

It is possible to improve performance and application thermal behavior, adopting some expedients:

- Use the bottom layer as heat-sink,
- Shield inner layer tracks with ground planes,
- Use large paths for ground connections, instead of narrow and long paths with sharp corners, and transfer all ground connections to other layers by a proper number of vias,
- Place compensation network very close to the chip to reduce noise,
- Put coils and capacitors close to the pins, and build output path with large and short tracks.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

9.1 Package variation

This device use package Variations Option B to define exposed pad (see *Table 11*) or slug-up (see *Table 12*) dimensions.

9.2 PowerSSO-36 (exposed pad) package information

Figure 16. PowerSSO-36 (exposed pad) package outline

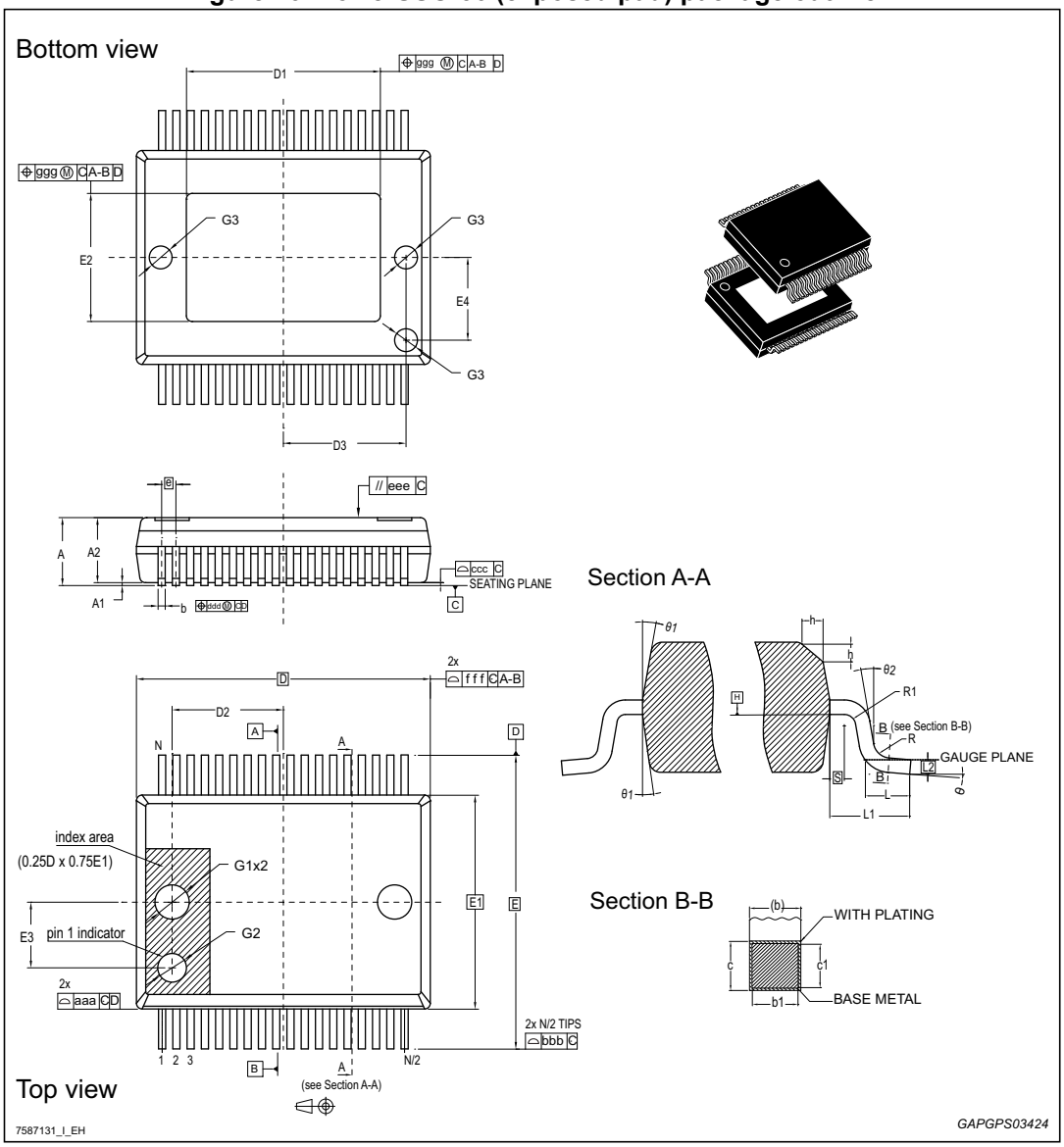


Table 11. PowerSSO-36 exposed pad package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	-	8°	0°	-	8°
Θ1	5°	-	10°	5°	-	10°
Θ2	0°	-	-	0°	-	-
A	2.15	-	2.45	0.0846	-	0.0965

Table 11. PowerSSO-36 exposed pad package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1	0.0	-	0.1	0.0	-	0.0039
A2	2.15	-	2.35	0.0846	-	0.0925
b	0.18	-	0.32	0.0071	-	0.0126
b1	0.13	0.25	0.3	0.0051	0.0098	0.0118
c	0.23	-	0.32	0.0091	-	0.0126
c1	0.2	0.2	0.3	0.0079	0.0079	0.0118
D[2]	10.30 BSC			0.4055 BSC		
D1	VARIATION					
D2	-	3.65	-	-	0.1437	-
D3	-	4.3	-	-	0.1693	-
e	0.50 BSC			0.0197 BSC		
E	10.30 BSC			0.4055 BSC		
E1[2]	7.50 BSC			0.2953 BSC		
E2	VARIATION					
E3	-	2.3	-	-	0.0906	-
E4	-	2.9	-	-	0.1142	-
G1	-	1.2	-	-	0.0472	-
G2	-	1	-	-	0.0394	-
G3	-	0.8	-	-	0.0315	-
h	0.3	-	0.4	0.0118	-	0.0157
L	0.55	0.7	0.85	0.0217	-	0.0335
L1	1.40 REF			0.0551 REF		
L2	0.25 BSC			0.0098 BSC		
N	36			1.4173		
R	0.3	-	-	0.0118	-	-
R1	0.2	-	-	0.0079	-	-
S	0.25	-	-	0.0098	-	-

Table 11. PowerSSO-36 exposed pad package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Tolerance of form and position						
aaa		0.2			0.0079	
bbb		0.2			0.0079	
ccc		0.1			0.0039	
ddd		0.2			0.0079	
eee		0.1			0.0039	
ffff		0.2			0.0079	
ggg		0.15			0.0059	
VARIATIONS						
Option A						
D1	6.5	-	7.1	0.2559	-	0.2795
E2	4.1	-	4.7	0.1614	-	0.1850
Option B						
D1	4.9	-	5.5	0.1929	-	0.2165
E2	4.1	-	4.7	0.1614	-	0.1850
Option C						
D1	6.9	-	7.5	0.2717	-	0.2953
E2	4.3	-	5.2	0.1693	-	0.2047

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is ‘0.25 mm’ per side D and ‘0.15 mm’ per side E1. D and E1 are Maximum plastic body size dimensions including mold mismatch.

9.3 PowerSSO-36 (slug-up) package information

Figure 17. PowerSSO-36 (slug-up) package outline

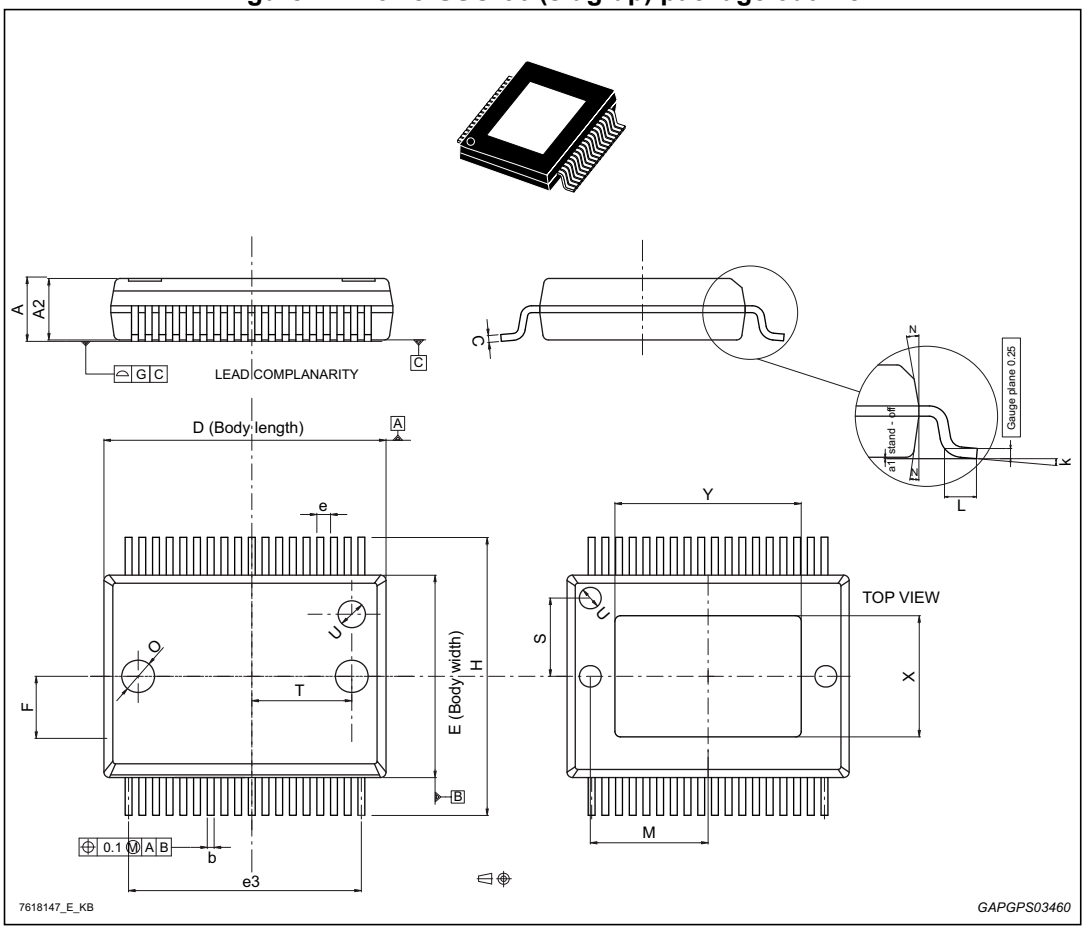


Table 12. PowerSSO-36 slug-up package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.15	-	2.45	0.0846	-	0.0965
A2	2.15	-	2.35	0.0846	-	0.0925
a1	0	-	0.10		-	0.0039
b	0.18	-	0.36	0.0071	-	0.0142
c	0.23	-	0.32	0.0091	-	0.0126
D[2]	10.10	-	10.50	0.3976	-	0.4134
E[2]	7.4	-	7.6	0.2913	-	0.2992
e	-	0.5	-	-	0.0197	-
e3	-	8.5	-	-	0.3346	-

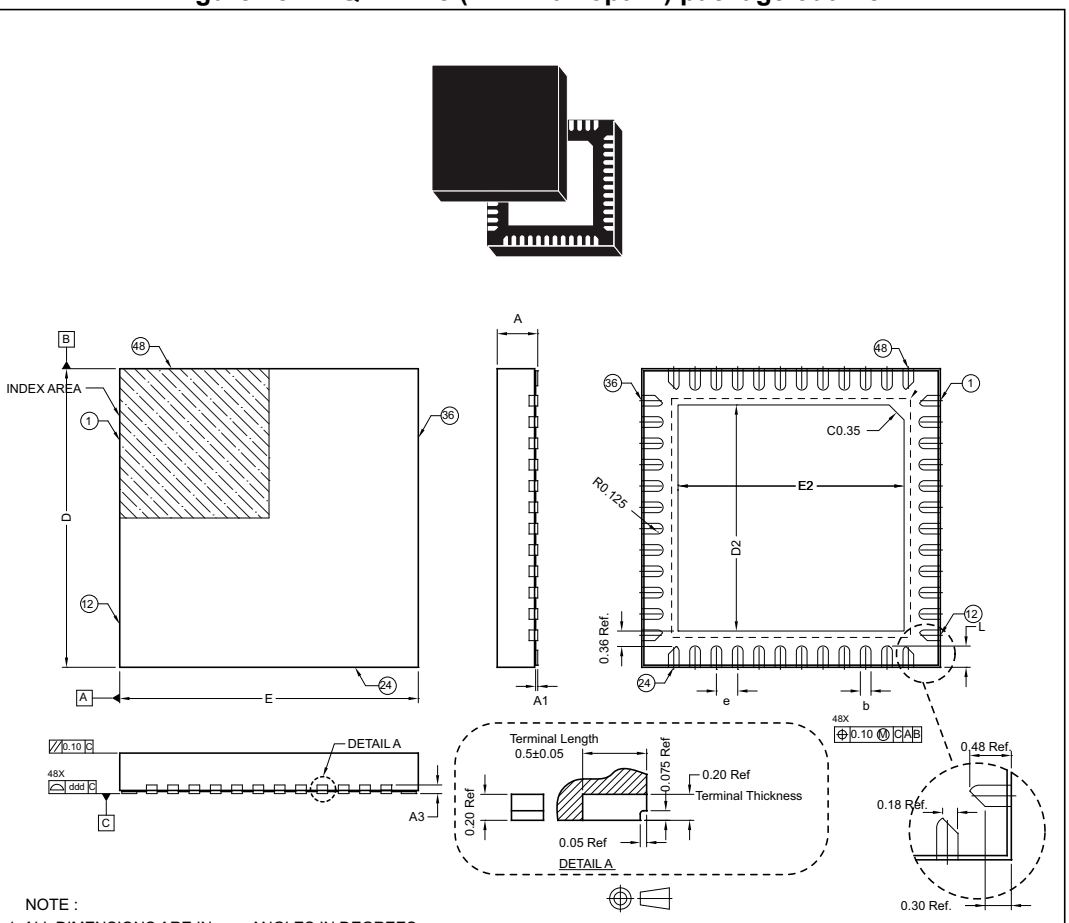
Table 12. PowerSSO-36 slug-up package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	-	2.3	-	-	0.0906	-
G	-	-	0.10	-	-	0.0039
H	10.10	-	10.50	0.3976	-	0.4134
h	-	-	0.40	-	-	0.0157
k	0°	-	8°	0°	-	8°
L	0.55	-	0.85	0.0217	-	0.0335
M	-	4.3	-	-	0.1693	-
N	-	-	10°	-	-	10°
O	-	1.2	-	-	0.0472	-
Q	-	0.8	-	-	0.0315	-
S	-	2.9	-	-	0.1142	-
T	-	3.65	-	-	0.1437	-
U	-	1.0	-	-	0.0394	-
X	See VARIATIONS					
Y	See VARIATIONS					
VARIATIONS						
Option A						
X	4.1	-	4.7	0.1614	-	0.1850
Y	6.5	-	7.1	0.2559	-	0.2795
Option B						
X	4.1	-	4.7	0.1614	-	0.1850
Y	4.9	-	5.5	0.1929	-	0.2165
Option C						
X	4.3	-	5.2	0.1693	-	0.2047
Y	6.9	-	7.5	0.2717	-	0.2953

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. "D" and “E" do not include mold flash or protrusions Mold flash or protrusions shall not exceed 0.15 mm per side (0.006”)

9.4 VFQFPN-48 (7x7x1.0 - opt. D) package information

Figure 18. VFQFPN-48 (7x7x1.0 - opt. D) package outline



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. REFER JEDEC MO-220.

7446345_G_V0 (Opt. C)

GAPGPS03449

Table 13. VFQFPN-48 (7x7x1.0 - opt. D) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.85	0.95	1.05	0.0335	0.0374	0.0413
A1	-	-	0.05	-	-	0.0020
A2	-	0.75	-	-	0.0295	-
A3	-	0.200	-	-	0.0079	-
b	0.15	0.25	0.35	0.0059	0.0098	0.0138
D	6.80	7.00	7.15	0.2697	0.2756	0.2815
D2	5.15	5.30	5.45	0.2028	0.2087	0.2146
E	6.85	7.00	7.15	0.2697	0.2756	0.2815
E2	5.15	5.30	5.45	0.2028	0.2087	0.2146
e	0.45	0.50	0.55	0.0177	0.0197	0.0217
L	0.45	0.50	0.55	0.0177	0.0197	0.0217
ddd	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

9.5 Package marking information

Figure 19. PowerSSO-36 (exp. pad) marking information

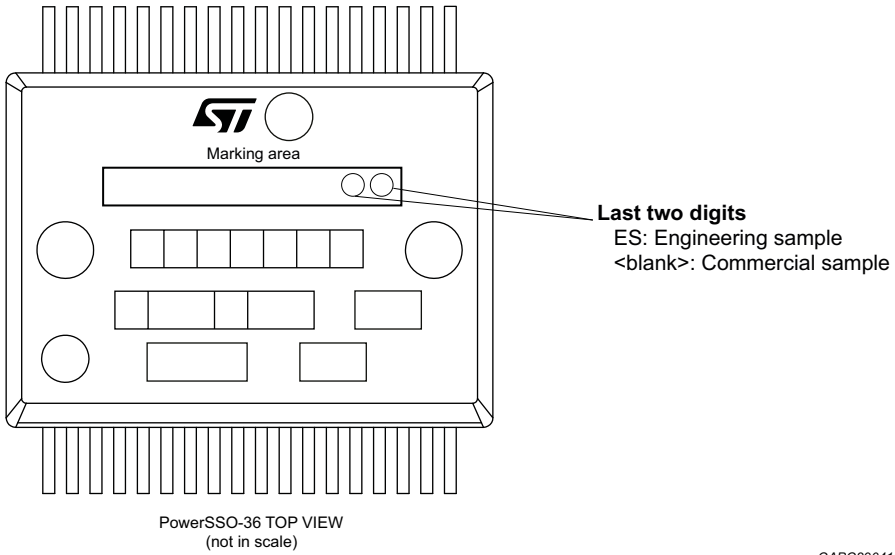


Figure 20. PowerSSO-36 (slug up) marking information

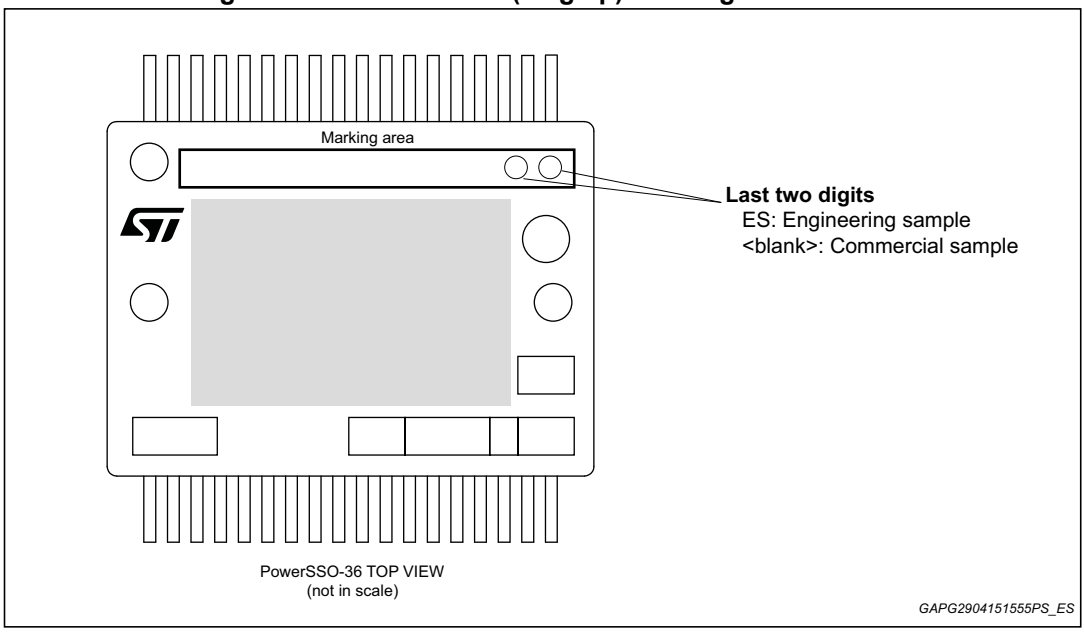
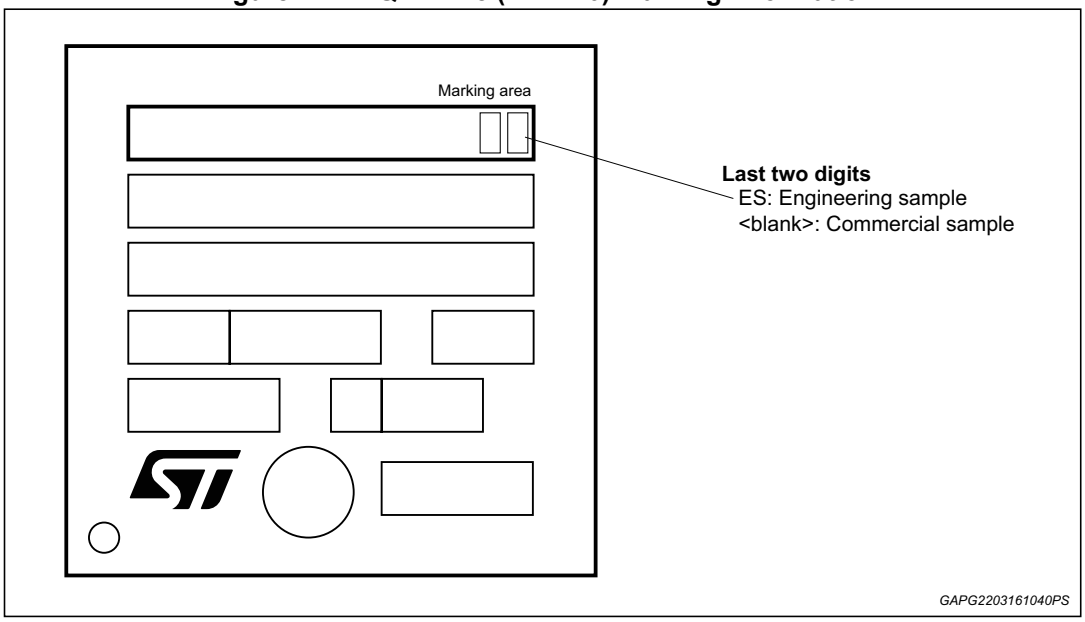


Figure 21. VFQFPN-48 (7x7x1.0) marking information



Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted to run a qualification activity prior to any decision to use these engineering samples.

10 Revision history

Table 14. Document revision history

Date	Revision	Changes
29-Oct-2015	1	Initial release.
21-Nov-2016	2	Added: – “Automotive” in the title, AEC-Q100 qualifed in the feature and car icon, in cover page, – Two order codes in *Table 1: Device summary on page 1*. – *Figure 5: VQFPN-48 pinout configuration on page 12*, – *Table 3: VQFPN-48 pins description on page 12*, – *Table 6: Thermal data (VQFPN-48) on page 14* – *Chapter 9.4: VFQFPN-48 (7x7x1.0 - opt. D) package information on page 45* – *Figure 21: VFQFPN-48 (7x7x1.0) marking information on page 47*. Updated: – *Section 1: Overview on page 6*, – *Section 3: Application diagrams*,*Table 2: PowerSSO-36 pins description*, – *Table 7: Electrical characteristics* – *Section 6.2.2 on page 19*, – *Section 6.2.5 on page 20*, – *Pulse-by-pulse current limiting (OCP) on page 27*, – *Figure 8: Thermal design on page 37*, – *Section 8: Thermal design*.