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# 1 Block and pin connections diagrams

Figure 1. Block diagram

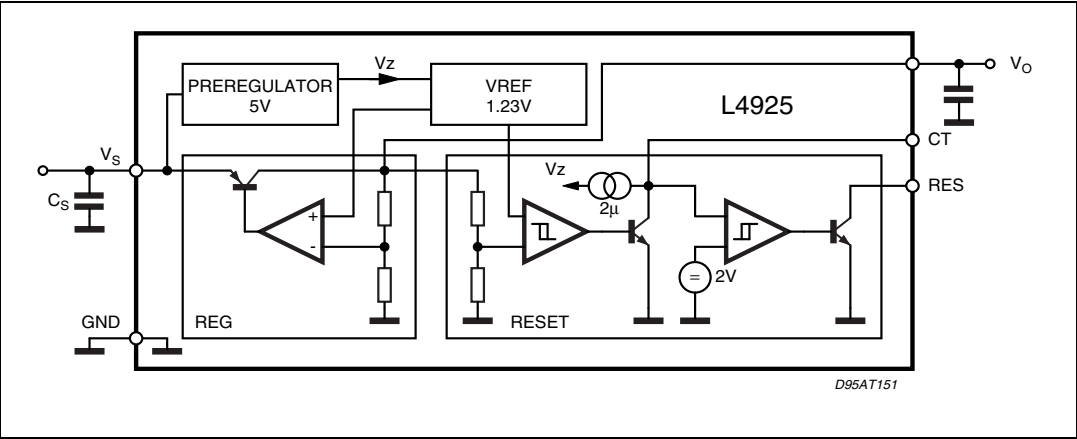
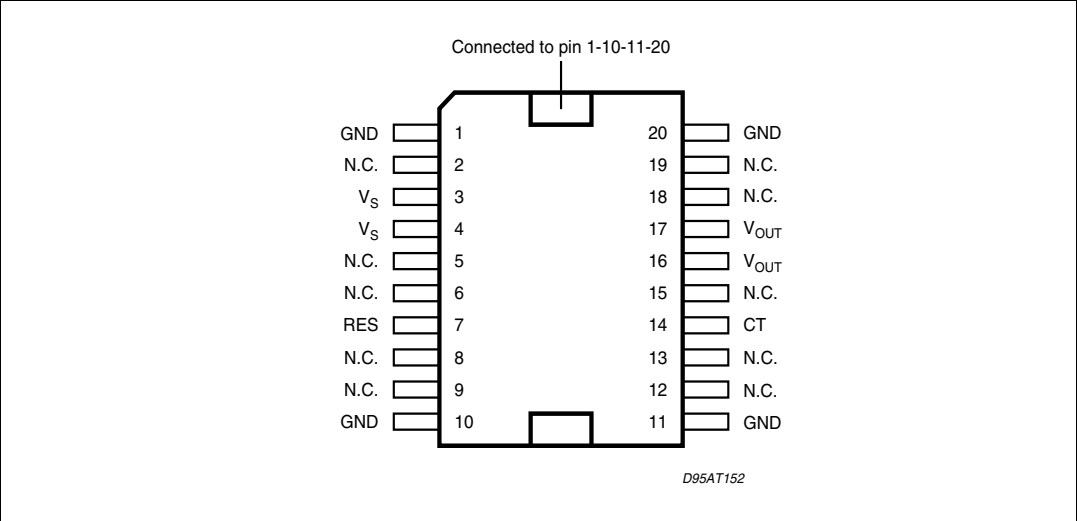


Figure 2. PowerSO-20 pin connections (top view)



## 1.1 Thermal data

Table 2. Thermal data

Symbol	Parameter	PowerSO-20	Unit
$R_{th(j-amb)}$	Thermal resistance junction to ambient	15 to 60	$^{\circ}C/W$
$R_{th(j-c)}$	Thermal resistance junction to case (max)	3.5	$^{\circ}C/W$

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{SDC}$	DC operating supply voltage	28	V
$V_{STR}$	Transient supply voltage ( $t < 1s$ )	40	V
$I_O$	Output current	internally limited	
$V_O$	Output voltage	20	V
$V_{RES}$	Output voltage	20	V
$I_{RES}$	Output current	5	mA
$T_{stg}$	Storage temperature	-55 to 150	°C
$T_j$	Operating junction temperature	-40 to 150	°C
$T_{j-SD}$	Thermal shutdown-junction temperature	165	°C

*Note:* The circuit is ESD protected according to MIL-STD-883C. According to ISO/DIS 7637 the transients must be clamped with external circuitry (see Application Circuit).

### 2.2 Electrical characteristics

$V_S = 14\text{ V}$ ;  $T_j = -40$  to  $125\text{ °C}$  unless otherwise specified.

**Table 4. Electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_O$	Output voltage	$V_I = 6$ to $28\text{ V}$ ; $I_O = 1$ to $500\text{ mA}$	4.90	5	5.10	V
$V_O$	Output voltage	$V_I = 35\text{ V}$ ; $T < 1\text{ s}$ ; $I_O = 1$ to $500\text{ mA}$			5.50	V
$V_{DP}$	Dropout voltage	$I_O = 100\text{ mA}$		0.2	0.3	V
		$I_O = 500\text{ mA}$		0.3	0.6	V
$V_{IO}$	Input to output voltage difference in undervoltage condition	$V_I = 4\text{ V}$ ; $I_O = 100\text{ mA}$			0.5	V
$V_{OL}$	Line regulation	$V_I = 6$ to $28\text{ V}$ ; $I_O = 1$ to $1\text{ mA}$			10	mV
$V_{OLO}$	Load regulation	$I_O = 1$ to $500\text{ mA}$			50	mV
$I_{LIM}$	Current limit	$V_O = 4.5\text{ V}$ ;	550	1000	1500	mA
		$V_O = 0$ ; Foldback characteristic		250		mA
$I_{QSE}$	Quiescent current	$I_O = 0.3\text{ mA}$		190	360	μA
$I_Q$	Quiescent current	$I_O = 500\text{ mA}$			20	mA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Reset</b>						
$V_{RT}$	Reset threshold voltage		4.2		4.8	V
$V_{RTH}$	Reset threshold		50	100	200	mV
$t_{RD}$	Reset pulse delay	$C_T = 100 \text{ nF}$ ; $t_R \geq 100 \text{ } \mu\text{s}$	60	100	140	ms
$t_{RR}$	Reset reaction time	$C_T = 100 \text{ nF}$ ;		5	30	$\mu\text{s}$
$V_{RL}$	Reset output low voltage	$R_{RES} = 10 \text{ K}\Omega$ to $V_O$ ; $V_S = \geq 3 \text{ V}$			0.4	V
$I_{RH}$	Reset output high leakage current	$V_{RES} = 5 \text{ V}$			1	$\mu\text{A}$
$V_{CTth}$	Delay comparator threshold			2		V
$V_{CTth \text{ hy}}$	Delay comparator threshold hysteresis			200		mV

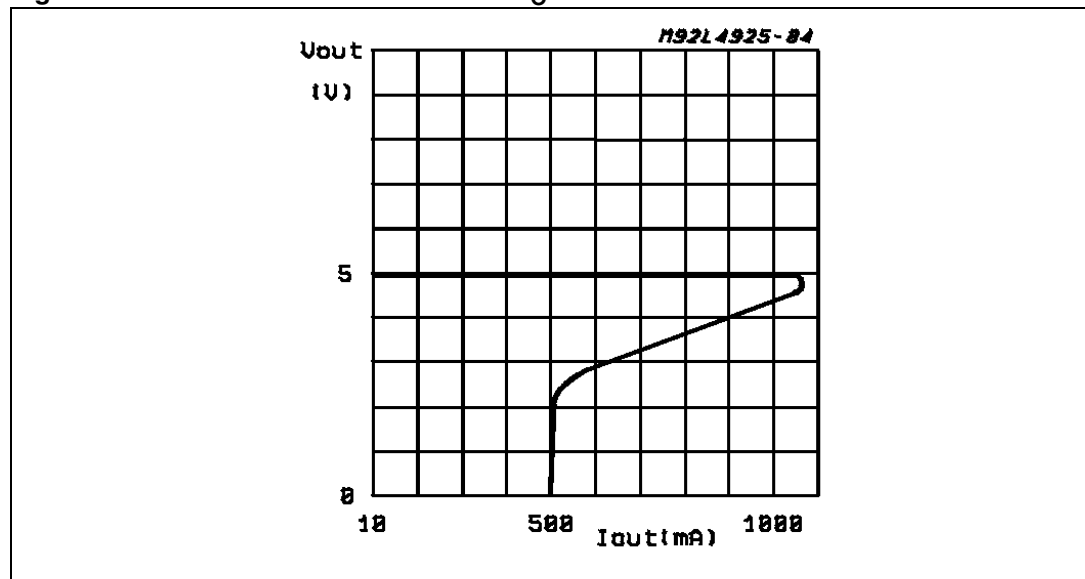
### 3 Functional description

The L4925 is a monolithic integrated voltage regulator, based on the STM modular voltage regulator approach. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

#### 3.1 Voltage regulator

The voltage regulator uses an Isolated Collector Vertical PNP transistor as a regulating element. With this structure very low dropout voltage at currents up to 500 mA is obtained.

**Figure 3. Foldback characteristics of  $V_O$**



The dropout operation of the standby regulator is maintained down to 3 V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 35 V. With this feature no functional interruption due to overvoltage pulses is generated.

The typical curve showing the standby output voltage as a function of the input supply voltage is shown in [Figure 4](#).

The current consumption of the device (quiescent current) is less than 250  $\mu$ A. To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled.

The quiescent current as a function of the supply input voltage is shown in [Figure 5](#).

Figure 4. Output voltage vs input voltage

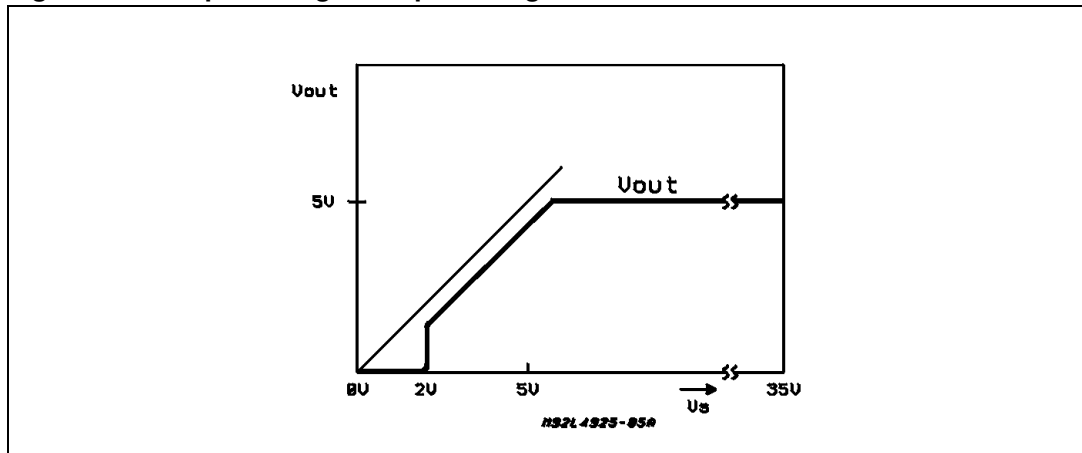
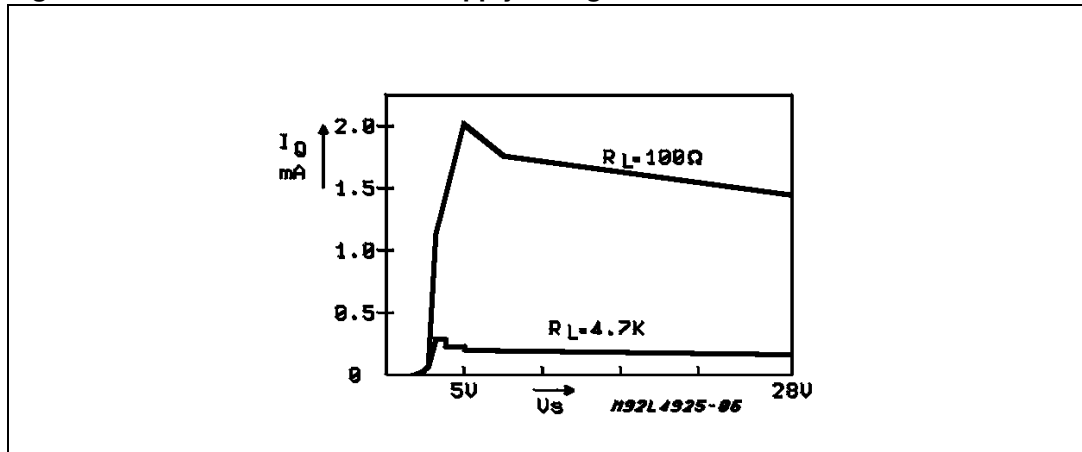


Figure 5. Quiescent current vs supply voltage



### 3.2 Reset circuit

The block circuit diagram of the reset circuit is shown in [Figure 6](#). The reset circuit supervises the output voltage. The reset threshold of 4.5 V is defined with the internal reference voltage and standby output divider. The reset pulse delay time  $t_{RD}$  is defined with the charge time of an external capacitor  $C_T$ :

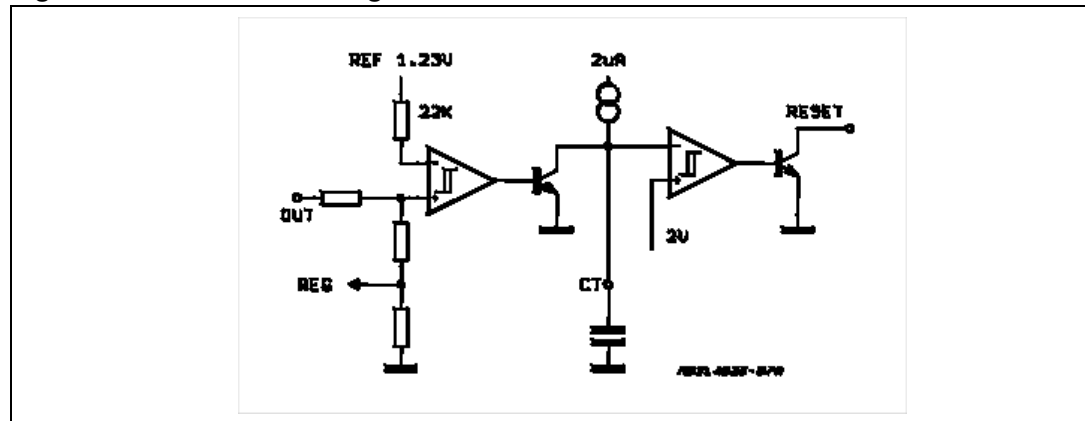
$$t_{RD} = \frac{C_T \cdot 2V}{2\mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor  $C_T$  and it is proportional to the value of  $C_T$ . The reaction time of the reset circuit increases the noise immunity. Standby output voltage drops below the reset threshold only a bit longer than the reaction time results in a shorter reset delay time.

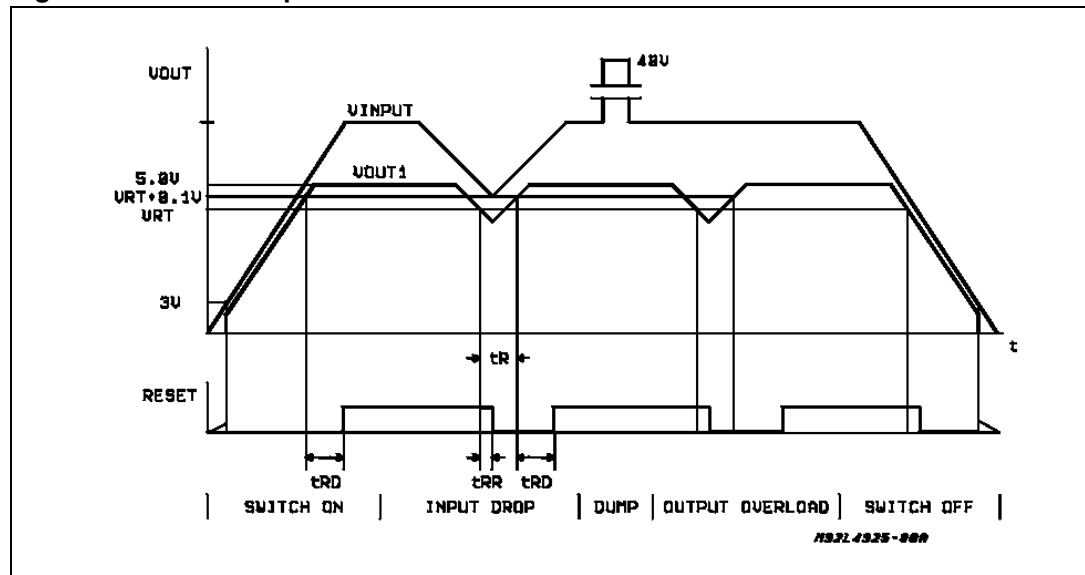
The nominal reset delay time is generated for standby output voltage drops longer than approximately 50 ms. The typical reset output waveforms are shown in [Figure 7](#).



**Figure 6. Block circuit diagram**



**Figure 7. Reset output waveforms**



## 4 Application information

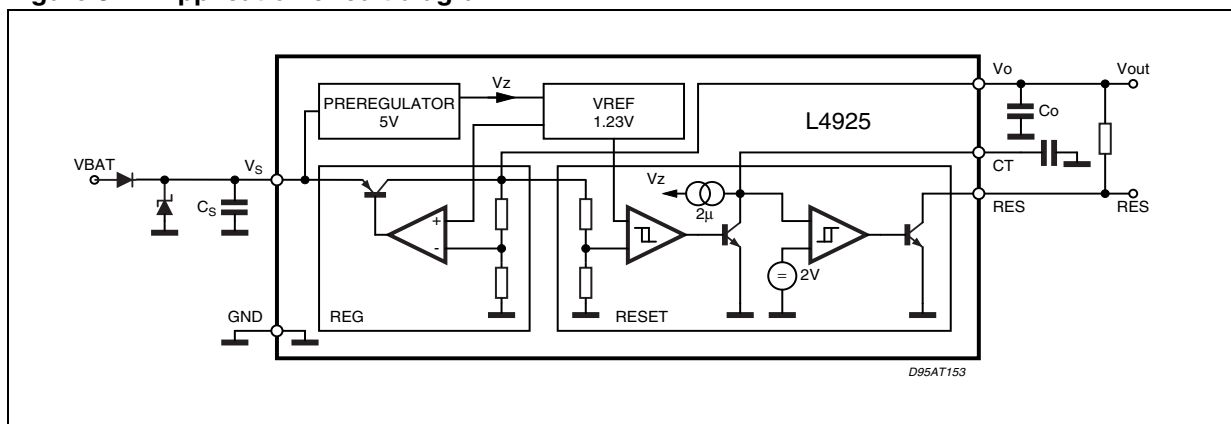
### 4.1 Supply voltage transients

High supply voltage transients can cause a reset output signal disturbance.

For supply voltage greater than 8 V the circuit shows a high immunity of the reset output against supply transients of more than 100 V/ms. For supply voltage lower than 8 V, supply transients of more than 0.4 V/ms. can cause a reset signal disturbance.

### 4.2 Application circuit

Figure 8. Application circuit diagram



For stability:  $C_S \geq 1 \mu\text{F}$ ;  $C_O \geq 10 \mu\text{F}$ ;  $\text{ESR} \leq 2.5 \Omega$  at 10 KHz

Recommended for application:  $C_S = C_O = 10 \mu\text{F}$  to  $100 \mu\text{F}$

## 5 Package Informations

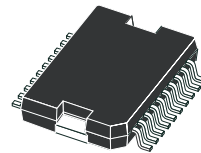
Figure 9. PowerSO-20 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8° (typ.)					
S	8° (max. )					
T		10			0.394	

- (1) "D and E1" do not include mold flash or protrusions.  
 - Mold flash or protrusions shall not exceed 0.15mm (0.006")  
 - Critical dimensions: "E", "G" and "a3".  
 (2) For subcontractors, the limit is the one quoted in JEDEC MO-166

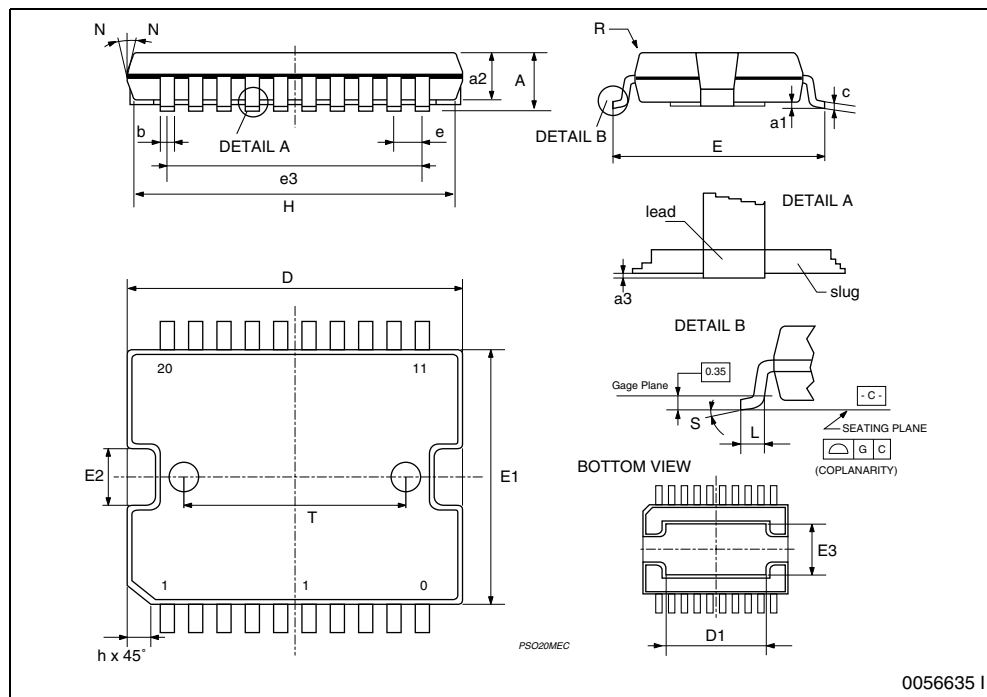
### OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO-20



## 6 Revision history

**Table 5. Document revision history**

Date	Revision	Changes
01-Oct-2003	4	First issue in EDOCD DMS
18-Nov-2005	5	Added GND pins to fig. 4 Added order code and changed the formatting style in compliance with the new template
03-Feb-2006	6	Reset Threshold Voltage changed from 4.5V / 5.2V (min/max) to 4.2V / 4.8V on <a href="#">Table 4</a> .
09-Feb-2010	7	Reformatted entire document. Removed PENTAWATT package Updated <a href="#">Table 2: Thermal data</a>
20-Sep-2013	8	Updated disclaimer.

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