Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	0.25	–––	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.082	Ω	V_{GS} = 10V, I_D = 18A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	–––	5.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	25	µA	V_{DS} = 200V, V_{GS} = 0V
		–––	–––	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	17	–––	–––	S	V_{DS} = 50V, I_D = 18A
Q_g	Total Gate Charge	–––	70	107	nC	I_D = 18A
Q_{gs}	Gate-to-Source Charge	–––	18	23		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	33	65		V_{GS} = 10V ④
$t_{d(on)}$	Turn-On Delay Time	–––	16	–––	ns	V_{DD} = 100V
t_r	Rise Time	–––	38	–––		I_D = 18A
$t_{d(off)}$	Turn-Off Delay Time	–––	26	–––		R_G = 2.5Ω
t_f	Fall Time	–––	10	–––		R_D = 5.4Ω, ④
C_{iss}	Input Capacitance	–––	2370	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	390	–––		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	–––	78	–––		f = 1.0MHz
C_{oss}	Output Capacitance	–––	2860	–––		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	–––	150	–––		V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	–––	170	–––		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤

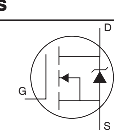
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	–––	420	mJ
I_{AR}	Avalanche Current①	–––	18	A
E_{AR}	Repetitive Avalanche Energy①	–––	20	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface ⑥	0.50	–––	
$R_{\theta JA}$	Junction-to-Ambient⑥	–––	62	
$R_{\theta JA}$	Junction-to-Ambient⑦	–––	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	31	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	124		
V_{SD}	Diode Forward Voltage	–––	–––	1.3	V	T_J = 25°C, I_S = 18A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	200	300	ns	T_J = 25°C, I_F = 18A
Q_{rr}	Reverse RecoveryCharge	–––	1.7	2.6	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

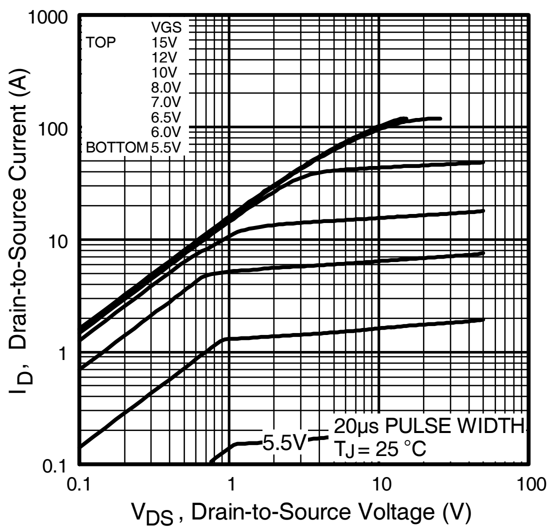


Fig 1. Typical Output Characteristics

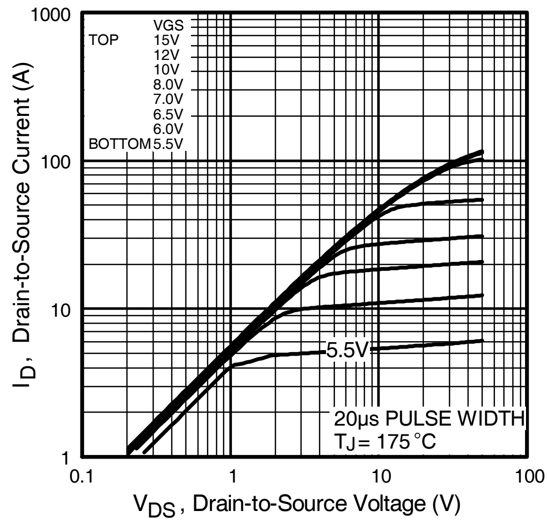


Fig 2. Typical Output Characteristics

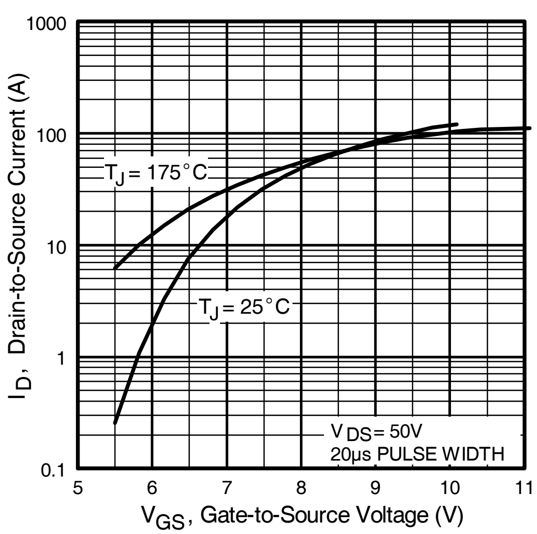


Fig 3. Typical Transfer Characteristics

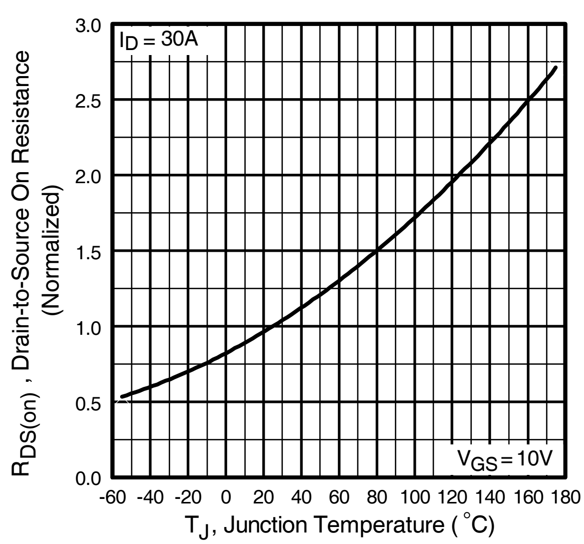


Fig 4. Normalized On-Resistance
Vs. Temperature

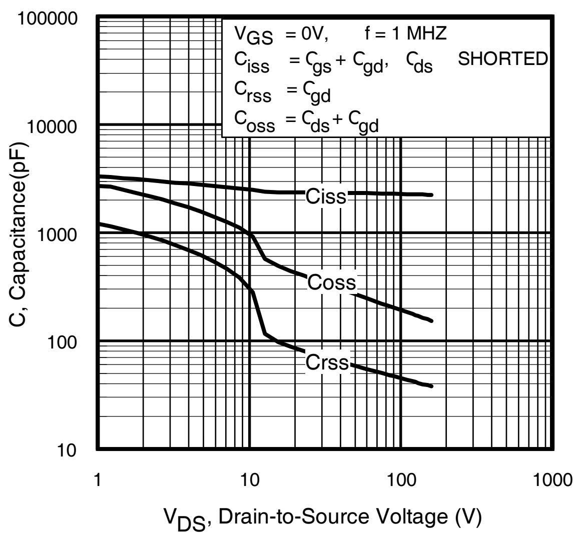


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

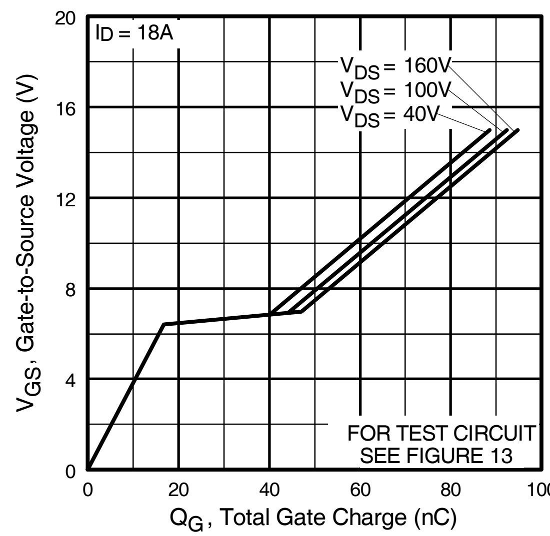


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

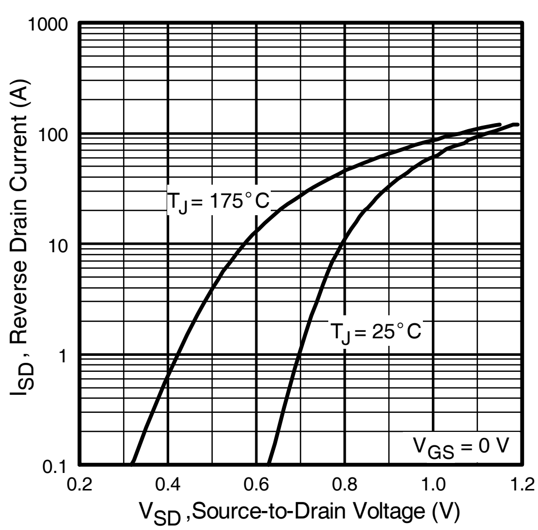


Fig 7. Typical Source-Drain Diode Forward Voltage

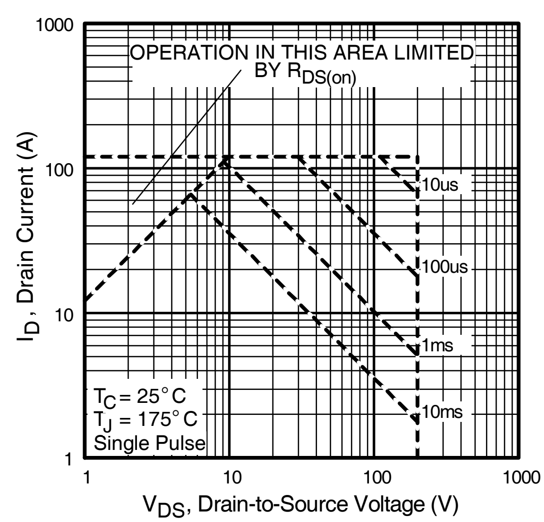


Fig 8. Maximum Safe Operating Area

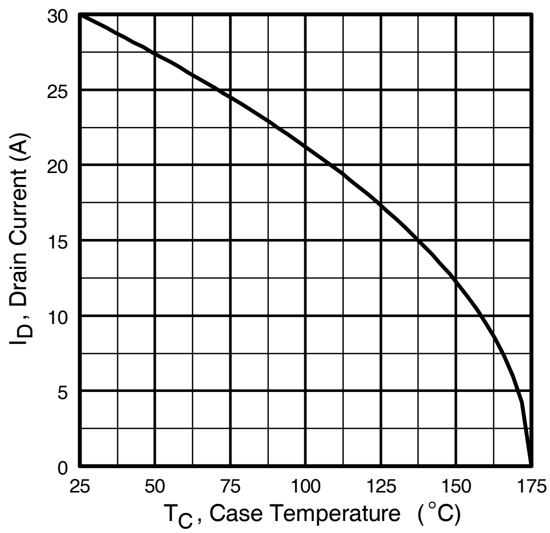


Fig 9. Maximum Drain Current Vs. Case Temperature

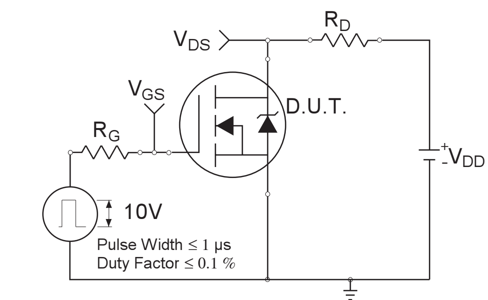


Fig 10a. Switching Time Test Circuit

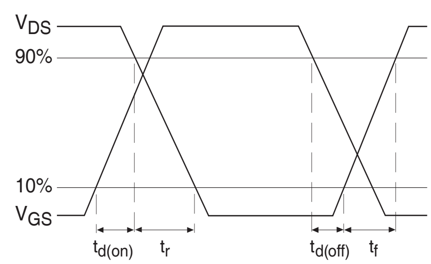


Fig 10b. Switching Time Waveforms

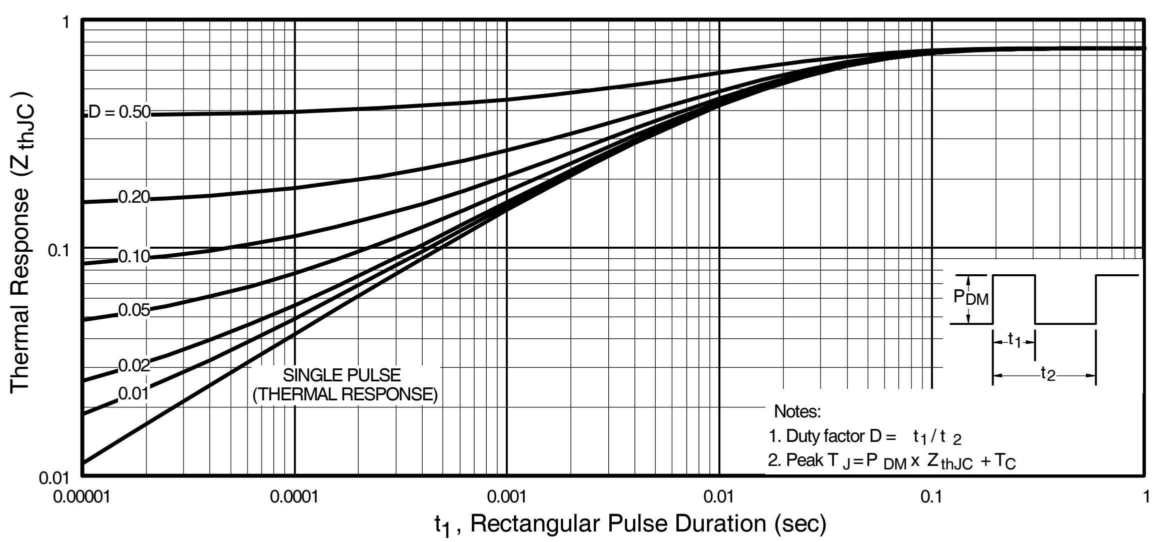


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

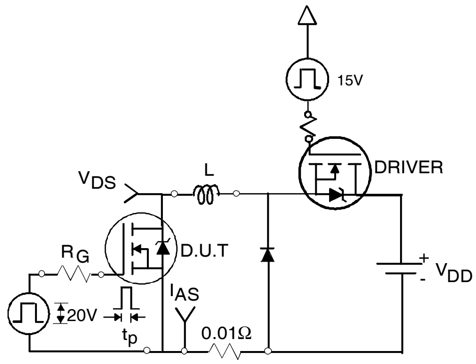


Fig 12a. Unclamped Inductive Test Circuit

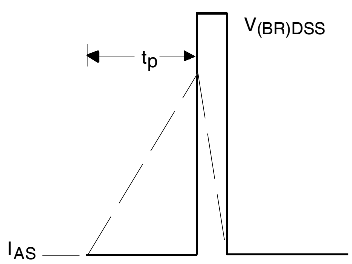


Fig 12b. Unclamped Inductive Waveforms

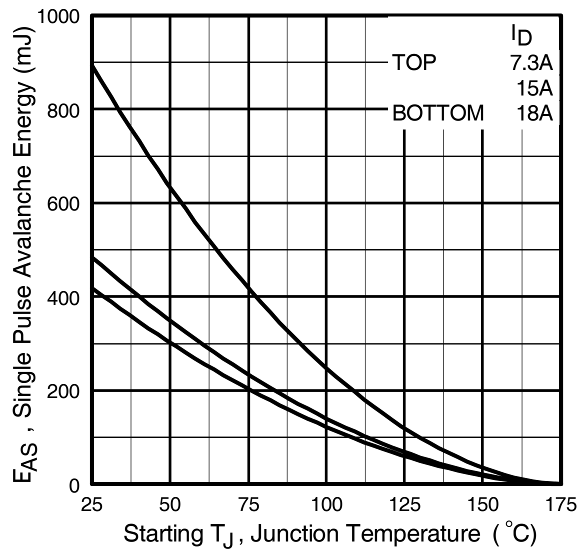


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

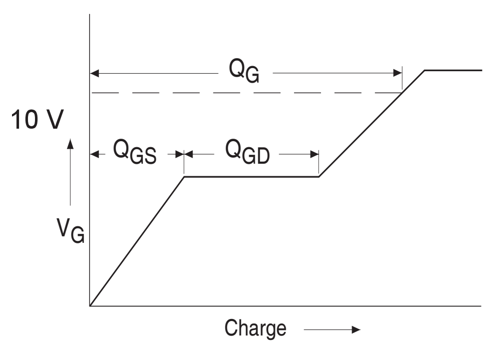


Fig 13a. Basic Gate Charge Waveform

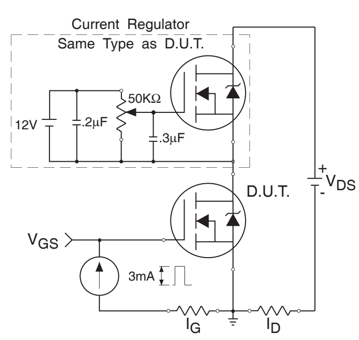
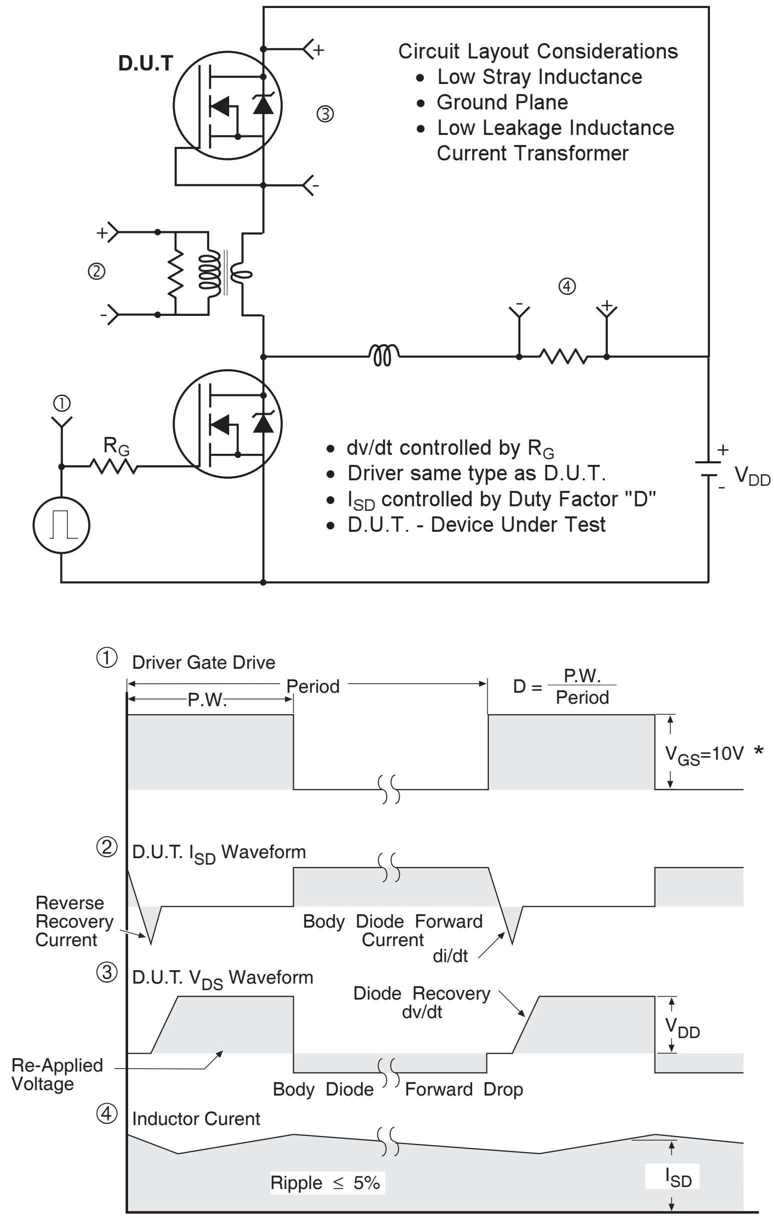


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

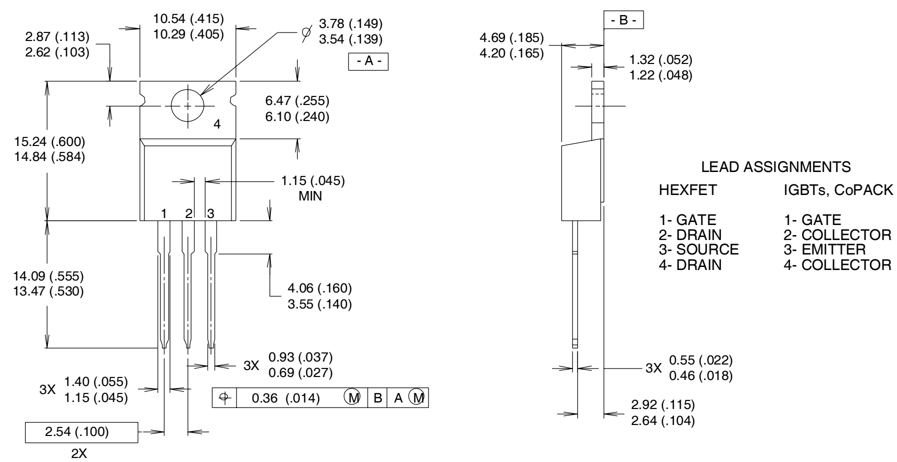


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

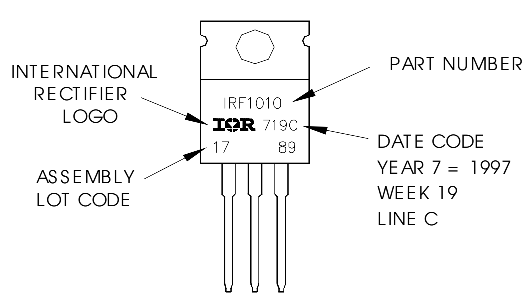
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information

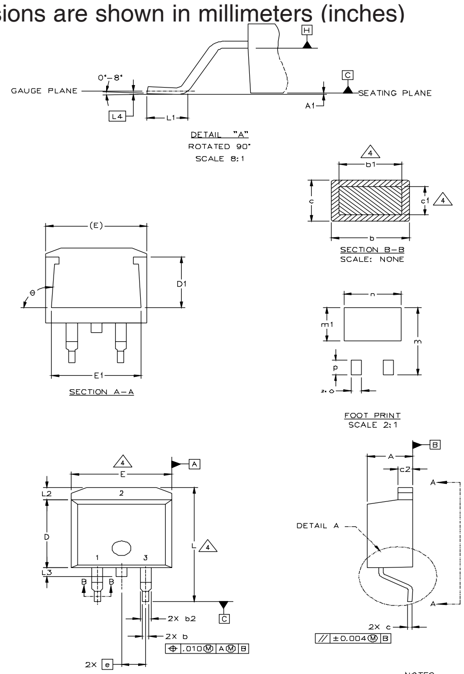
EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

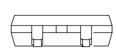
Note: "P" in assembly line position indicates "Lead-Free"



D^{2}Pak Package Outline

Dimensions are shown in millimeters (inches)





SYMBOL	DIMENSIONS MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.	NOTES
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.– GATE	1.– GATE	1.– ANODE *
2.– DRAIN	2.– COLLECTOR	2.– CATHODE
3.– SOURCE	3.– EMITTER	3.– ANODE

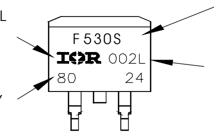
* PART DEPENDENT.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

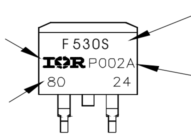
D^{2}Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

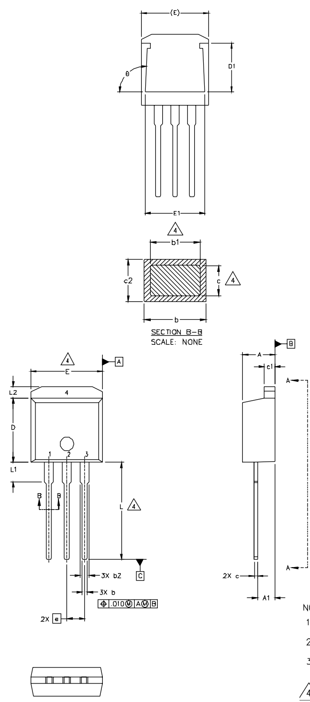
Note: "P" in assembly line position indicates "Lead-Free"



OR



TO-262 Package Outline



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET	IGBT
1.– GATE	1- GATE
2.– DRAIN	2- COLLECTOR
3.– SOURCE	3- EMITTER
4.– DRAIN	

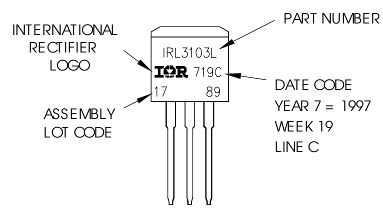
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

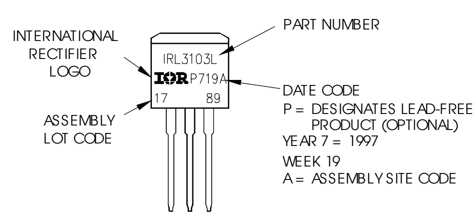
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"

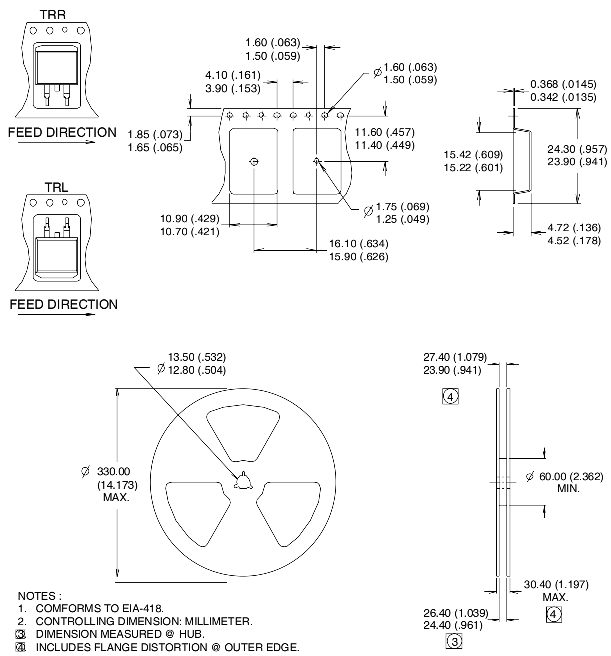


OR



D^2Pak Tape & Reel Infomation

Dimensions are shown in millimeters (inches)



Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, $L = 3.8mH$ $R_G = 25\Omega$, $I_{AS} = 18A$.

③ $I_{SD} \leq 18A$, $di/dt \leq 110A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ This is only applied to TO-220AB package

⑦ This is applied to D^2Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

International
IOR Rectifier

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

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