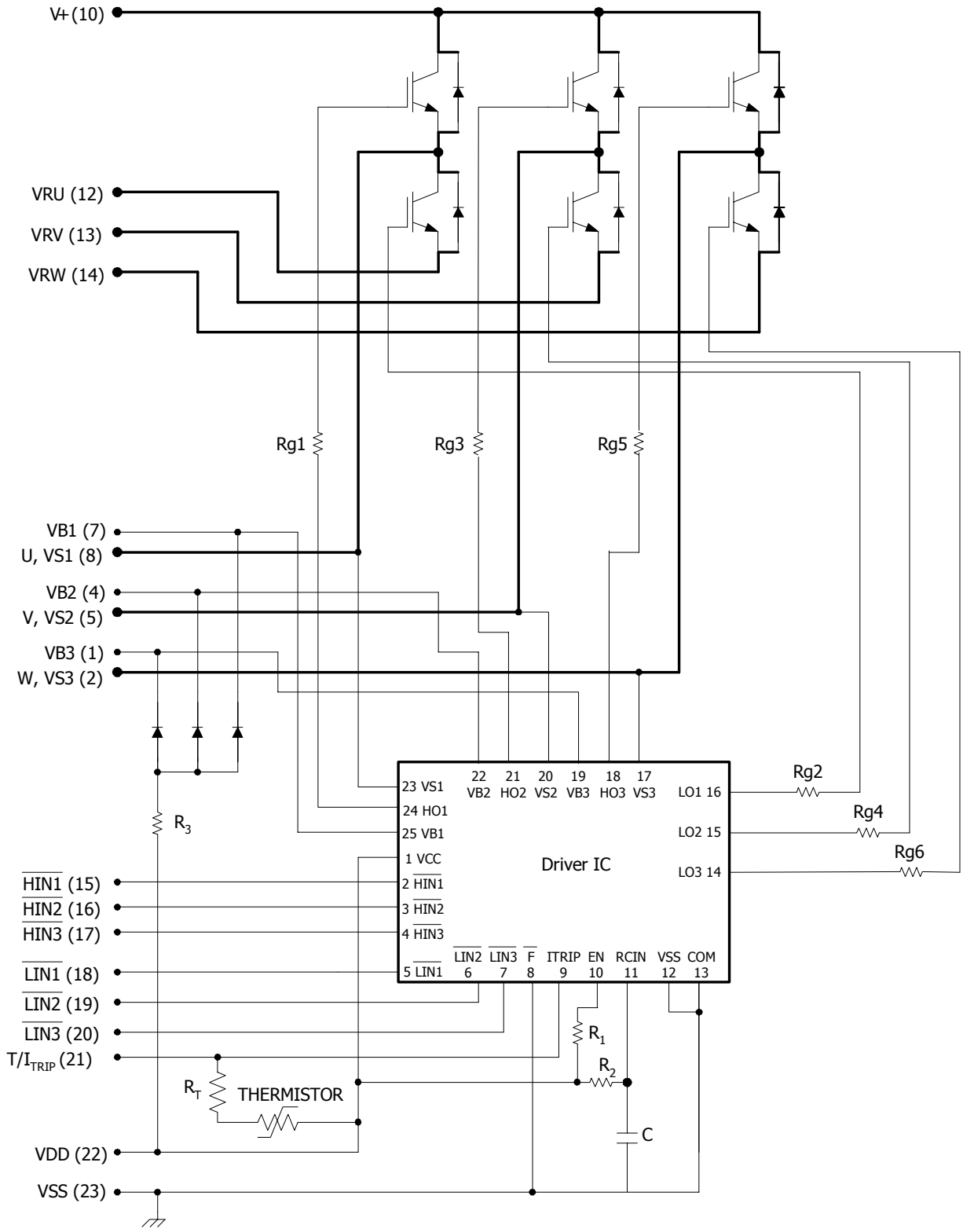
Internal Electrical Schematic - IRAMS10UP60A



Inverter Section Electrical Characteristics @ T_J = 25°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	---	---	V	V_{IN}=0V, I_C=20µA
$\Delta V_{(BR)CES}$ / ΔT	Temperature Coeff. Of Breakdown Voltage	---	0.57	---	V/°C	V_{IN}=0V, I_C=1.0mA (25°C - 150°C)
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	---	1.7	2.0	V	I_C=5A T_J=25°C, V_{DD}=15V
		---	2.0	2.4		I_C=5A T_J=150°C
I_{CES}	Zero Gate Voltage Collector Current-to-Emitter	---	5	15	µA	V_{IN}=5V, V^+=600V
		---	10	40		V_{IN}=5V, V^+=600V, T_J=150°C
I_{lk_module}	Zero Gate Phase-to-Phase Current	--	--	50	µA	V_{IN}=5V, V^+=600V
V_{FM}	Diode Forward Voltage Drop	---	1.8	2.35	V	I_C=5A
		---	1.3	1.7		I_C=5A, T_J=150°C

Inverter Section Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
E_{on}	Turn-On Switching Loss	---	200	235		I_C=5A, V^+=400V
E_{off}	Turn-Off Switching Loss	---	75	100	µJ	V_{DD}=15V, L=1mH
E_{tot}	Total Switching Loss	---	275	335		See CT1 T_J=25°C
E_{on}	Turn-on Swtiching Loss	---	300	360		T_J=150°C
E_{off}	Turn-off Switching Loss	---	135	165	µJ	Energy losses include "tail" and diode reverse recovery
E_{tot}	Total Switching Loss	---	435	525		
Erec	Diode Reverse Recovery energy	---	30	40	µJ	T_J=150°C, V^+ =400V V_{DD}=15V, I_F=5A, L=1mH
t_{rr}	Diode Reverse Recovery time	---	100	145	ns	
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J=150°C, I_C=5A, V_P=600V V^+=480V, V_{DD}=+15V to 0V See CT3
SCSOA	Short Circuit Safe Operating Area	10	---	---	µs	T_J=150°C, V_P=600V, V^+=360V, V_{DD}=+15V to 0V See CT2

Thermal Resistance

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$R_{th(J-C)}$	Junction to case thermal resistance, each IGBT under inverter operation.	---	4.2	4.7	°C/W	Flat, greased surface. Heatsink compound thermal conductivity - 1W/mK
$R_{th(J-C)}$	Junction to case thermal resistance, each Diode under inverter operation.	---	5.5	6.5	°C/W	
$R_{th(C-S)}$	Thermal Resistance case to sink	---	0.1	---	°C/W	

Absolute Maximum Ratings Driver Function

Absolute Maximum Ratings indicate substaines limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS} (Note 1)

Symbol	Definition	Min	Max	Units
$V_{S1,2,3}$	High Side offset voltage	-0.3	600	V
$V_{B1,2,3}$	High Side floating supply voltage	-0.3	20	V
V_{DD}	Low Side and logic fixed supply voltage	-0.3	20	V
V_{IN}	Input voltage LIN, HIN, T/I_{TRIP}	-0.3	7	V
T_J	Juction Temperature	-40	150	°C

Recommended Operating Conditions Driver Function

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to V_{SS}. The V_S offset is tested with all supplies biased at 15V differential (Note 1). All input pin (V_{IN}) and I_{TRIP} are clamped with a 5.2V zener diode and pull-up resistor to V_{DD}

Symbol	Definition	Min	Max	Units
$V_{B1,2,3}$	High side floating supply voltage	V_S+12	V_S+20	V
$V_{S1,2,3}$	High side floating supply offset voltage	Note 2	450	
V_{DD}	Low side and logic fixed supply voltage	12	20	V
V_{ITRIP}	T/I_{TRIP} input voltage	V_{SS}	V_{SS}+5	
V_{IN}	Logic input voltage LIN, HIN	V_{SS}	V_{SS}+5	V

Static Electrical Characteristics Driver Function

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$)=15V, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels. (Note 1)

Symbol	Definition	Min	Typ	Max	Units
$V_{IN,th+}$	Positive going input threshold	3.0	---	---	V
$V_{IN,th-}$	Negative going input threshold	---	---	0.8	V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage Positive going threshold	10.6	11.1	11.6	V
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage Negative going threshold	10.4	10.9	11.4	V
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage $I_{lockout}$ hysteresis	---	0.2	---	V
I_{QBS}	Quiescent V_{BS} supply current	---	70	120	µA
I_{QCC}	Quiscent V_{CC} supply current	---	1.6	2.3	mA
I_{LK}	Offset Supply Leakage Current	---	---	50	µA
I_{IN+}	Input bias current (OUT=LO)	---	100	220	µA
I_{IN+}	Input bias current (OUT=HI)	---	200	300	µA
V(I_{TRIP})	I_{TRIP} threshold Voltage (OUT=HI or OUT=LO)	3.85	4.3	4.75	V

Dynamic Electrical Characteristics

$V_{DD}=V_{BS}=V_{BIAS}=15V$, $I_o=1A$, $V_D=9V$, $PWM_{IN}=2kHz$, $V_{IN\_ON}=V_{IN\_th+}$, $V_{IN\_OFF}=V_{IN\_th-}$
$T_A=25°C$, unless otherwise specified

Symbol	Definition	Min	Typ	Max	Units
T_{ON}	Input to output propagation turn-on delay time (see fig.11)	-	470	-	ns
T_{OFF}	Input to output propagation turn-off delay time (see fig. 11)	-	615	-	ns
D_T	Dead Time	-	300	-	ns
I/T_{Trip}	T/I_{Trip} to six switch to turn-off propagation delay (see fig. 2)	-	750	-	ns
T_{FCLTRL}	Post I_{Trip} to six switch to turn-off clear time (see fig. 2)	-	9	-	ms

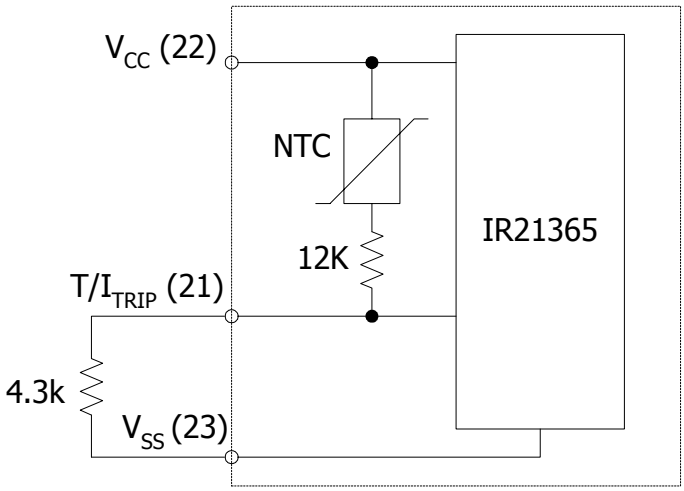
Internal NTC - Thermistor Characteristics

Parameter		Typ	Units	Conditions
R_{25}	Resistance	100 +/- 5%	kΩ	T_C = 25°C
R_{125}	Resistance	2.522 + 17.3 % /- 14.9%	kΩ	T_C = 125°C
B	B-Constant (25-50°C)	4250 +/- 3%	k	$R_2 = R_1 e^{[B(1/T2 - 1/T1)]}$
Temperature Range		-40 / 125	°C	
Typ. Dissipation constant		1	mW/°C	T_C = 25°C

Note 1: For more details, see IR21365 data sheet

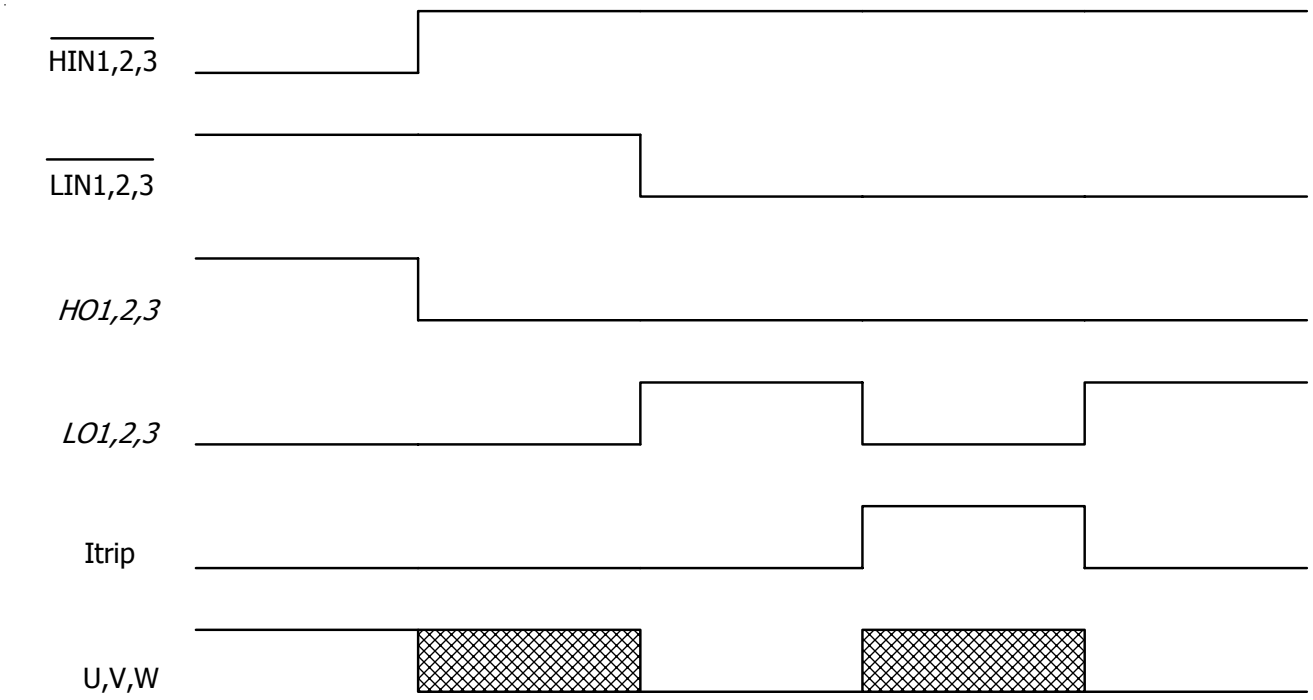
Note 2: Logic operational for V_S from V^--5V to V^-+600V. Logic stata held for V_S from V^--5V to V^--V_{BS}. (Please refer to DT97-3 for more details)

Thermistor Built-in IRAMS10UP60A

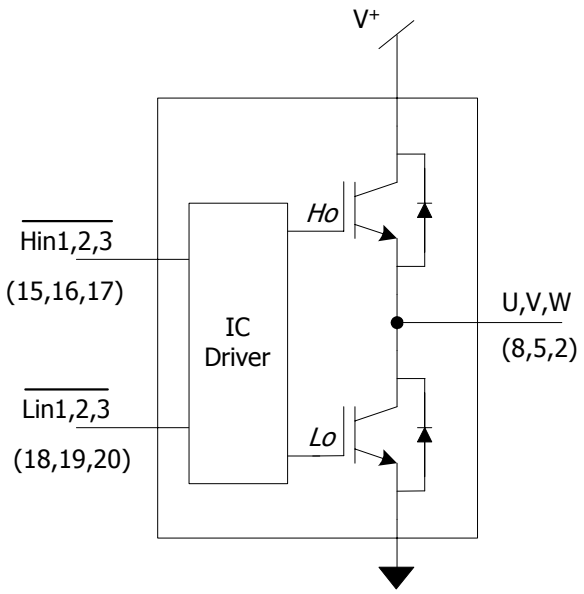


Note 3: The Maximum recommended sense voltage at the T/I_{TRIP} terminal under normal operating conditions is 3.3V.

Figure1. Input/Output Timing Diagram

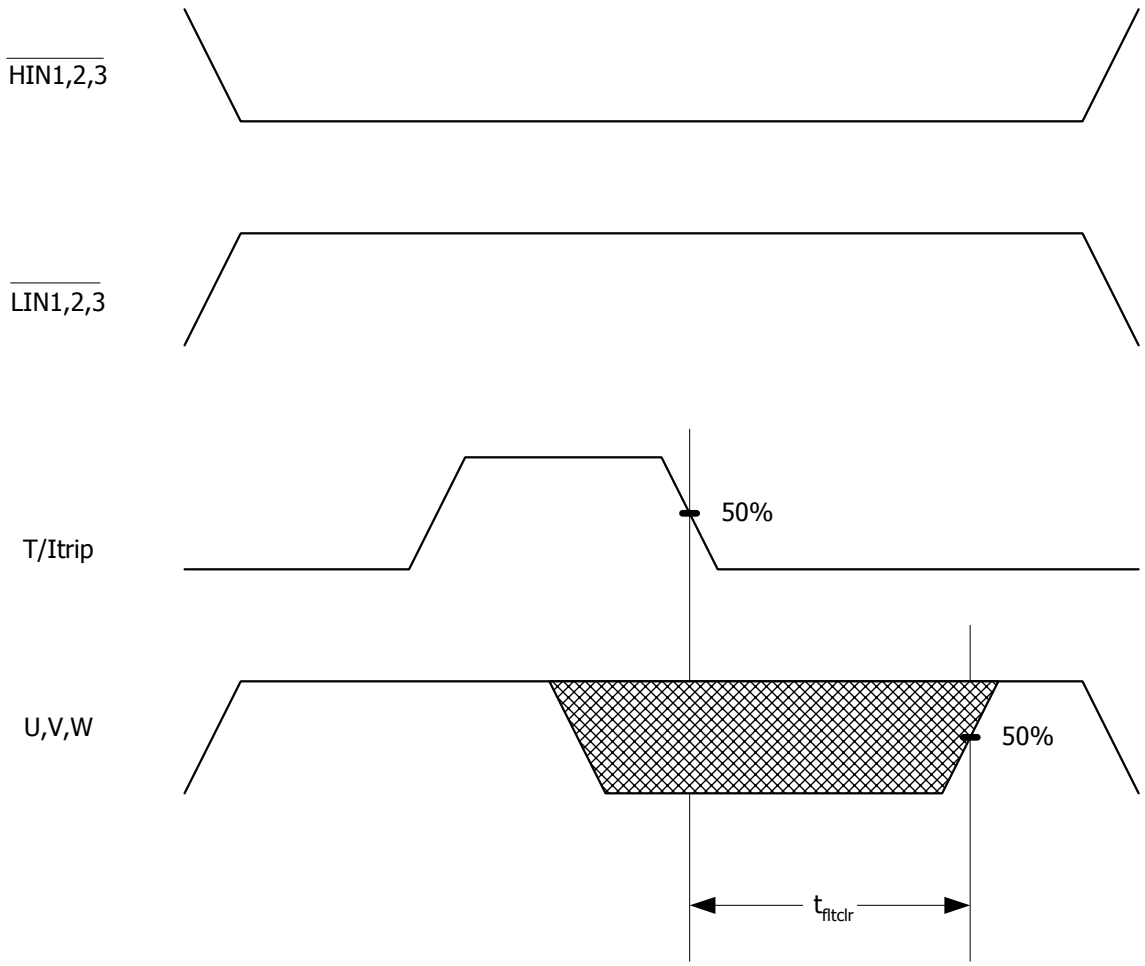


Note 4: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.



Itrip	$\overline{HIN1,2,3}$	$\overline{LIN1,2,3}$	U,V,W
0	0	1	Vbus
0	1	0	0
0	1	1	X
1	X	X	X

Figure 2. T/I_{Trip} Timing Waveform

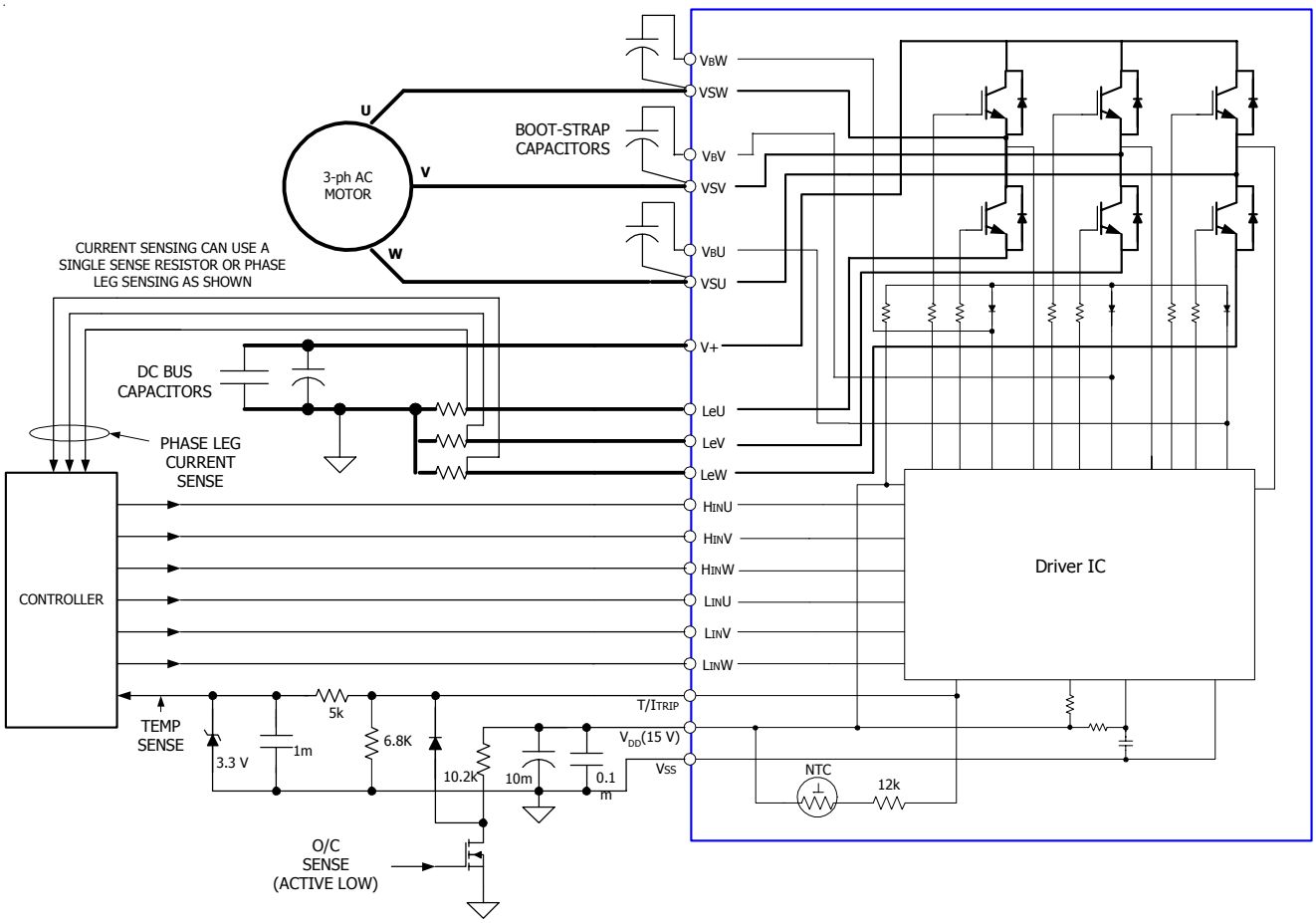


Note 5: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.

Module Pin-Out Description

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W,VS3	Output 3 - High Side Floating Supply Offset Voltage
3	na	none
4	VB2	High Side Floating Supply voltage 2
5	V,VS2	Output 2 - High Side Floating Supply Offset Voltage
6	na	none
7	VB1	High Side Floating Supply voltage 1
8	U,VS1	Output 1 - High Side Floating Supply Offset Voltage
9	na	none
10	V+	Positive Bus Input Voltage
11	na	none
12	LE1	Low Side Emitter Connection - Phase 1
13	LE2	Low Side Emitter Connection - Phase 2
14	LE3	Low Side Emitter Connection - Phase 3
15	HIN1	Logic Input High Side Gate Driver - Phase 1
16	HIN2	Logic Input High Side Gate Driver - Phase 2
17	HIN3	Logic Input High Side Gate Driver - Phase 3
18	LIN1	Logic Input Low Side Gate Driver - Phase 1
19	LIN2	Logic Input Low Side Gate Driver - Phase 2
20	LIN3	Logic Input Low Side Gate Driver - Phase 3
21	T/Itrip	Temperature Monitor and Shut-down Pin
22	VCC	+15V Main Supply
23	VSS	Negative Main Supply

Typical Application Connection IRAMS10UP60A



1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.

2. In order to provide good decoupling between V_{CC}-Gnd and V_B-V_{SS} terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically 0.1µF, are strongly recommended.

3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR design tip DN 98-2a, application note AN-1044 or Figure 9.

4. Low inductance shunt resistors shuld be used for phase leg current sensing. Similarly, the length of the traces between pins 12, 13 and 14 to the corrisponding shunt resistors should be kept as small as possible.

5. Over-current sense signal can be obtained from external hardware detecting excessive instantaneous current in inverter.

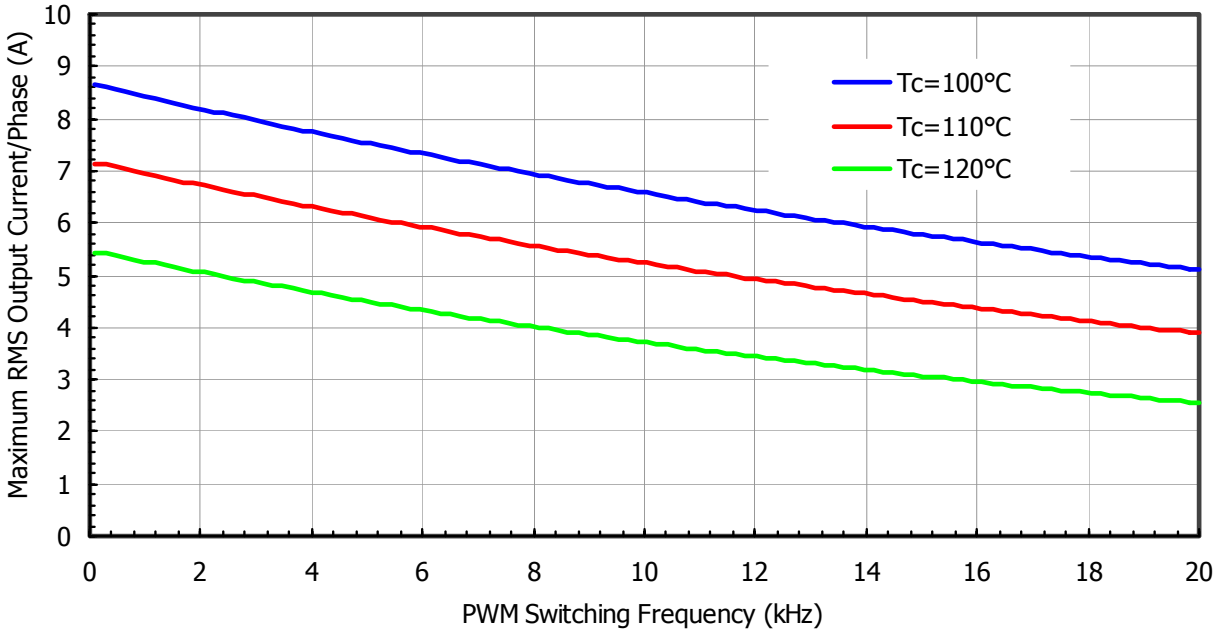


Figure 3. Maximum sinusoidal phase current as function of switching frequency
V_{BUS}=400V, T_j=150°C, Modulation Depth=0.8, PF=0.6

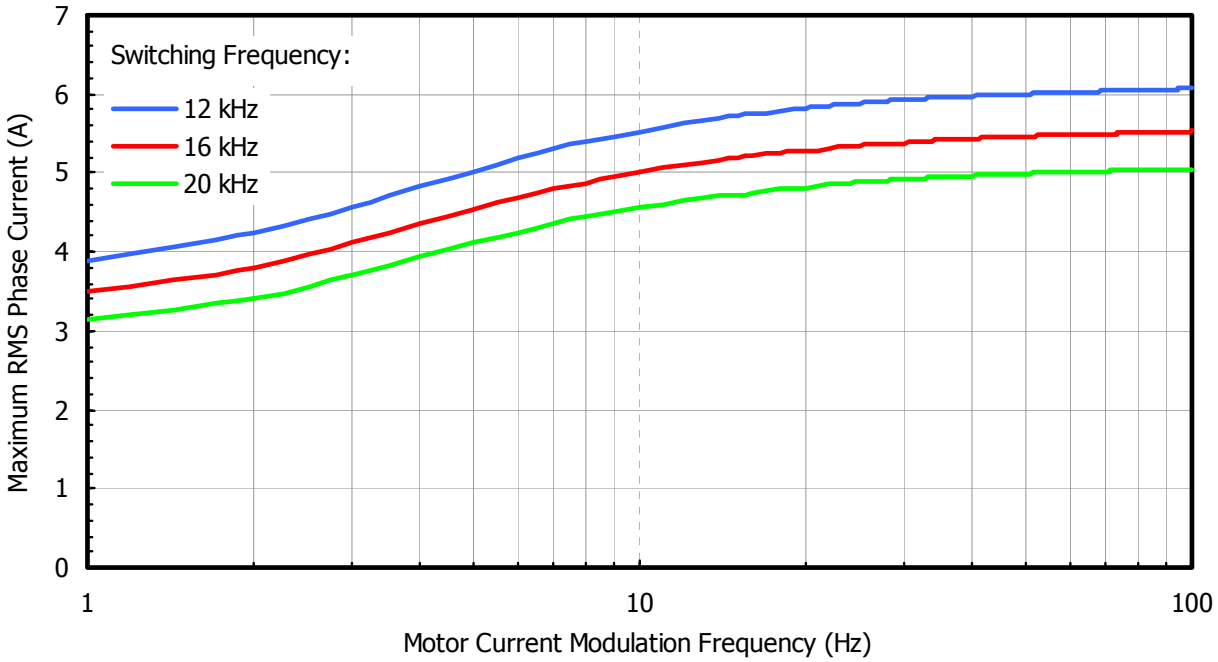


Figure 4. Maximum sinusoidal phase current as function of modulation frequency
V_{BUS}=400V, T_j=150°C, T_c=100°C, Modulation Depth=0.8, PF=0.6

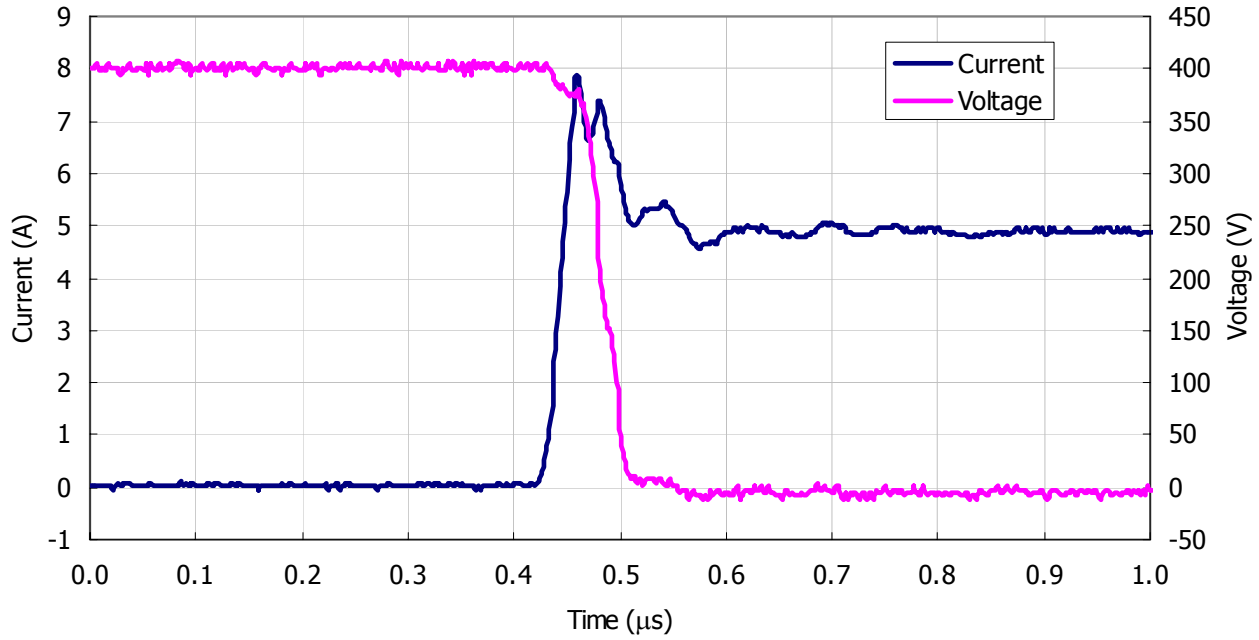


Figure 5. IGBT Turn-on. Typical turn-on waveform @T_j=125°C, V_{BUS}=400V

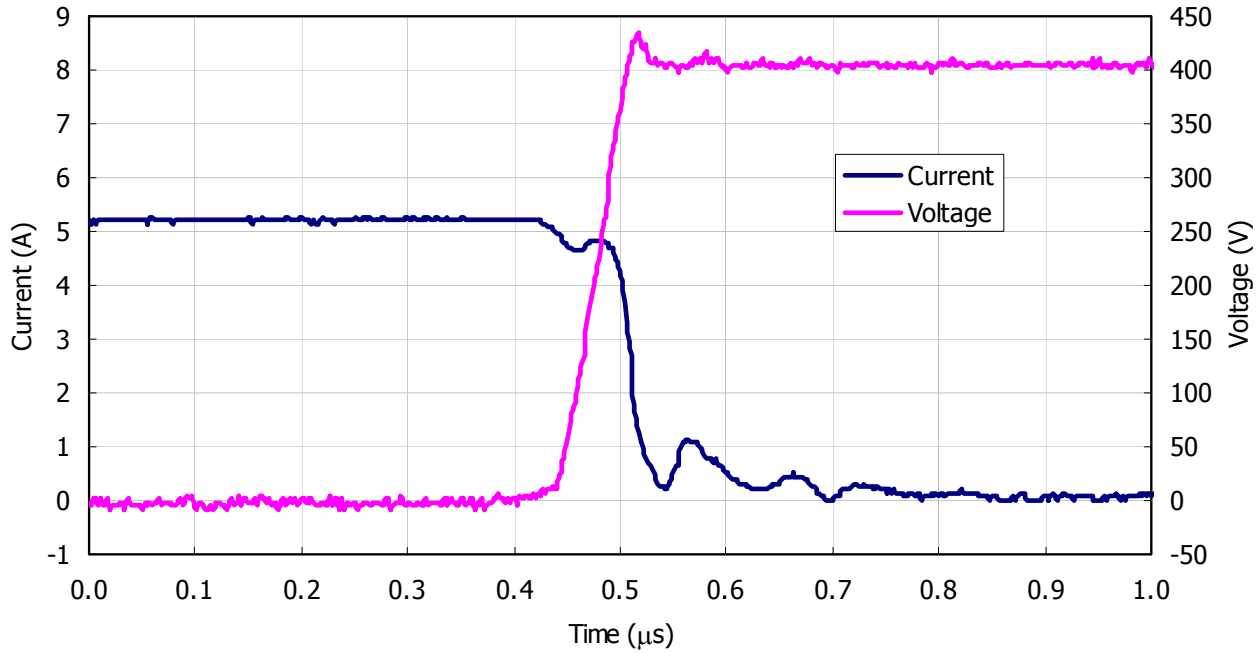


Figure 6. IGBT Turn-off. Typical turn-off waveform @T_j=125°C, V_{BUS}=400V

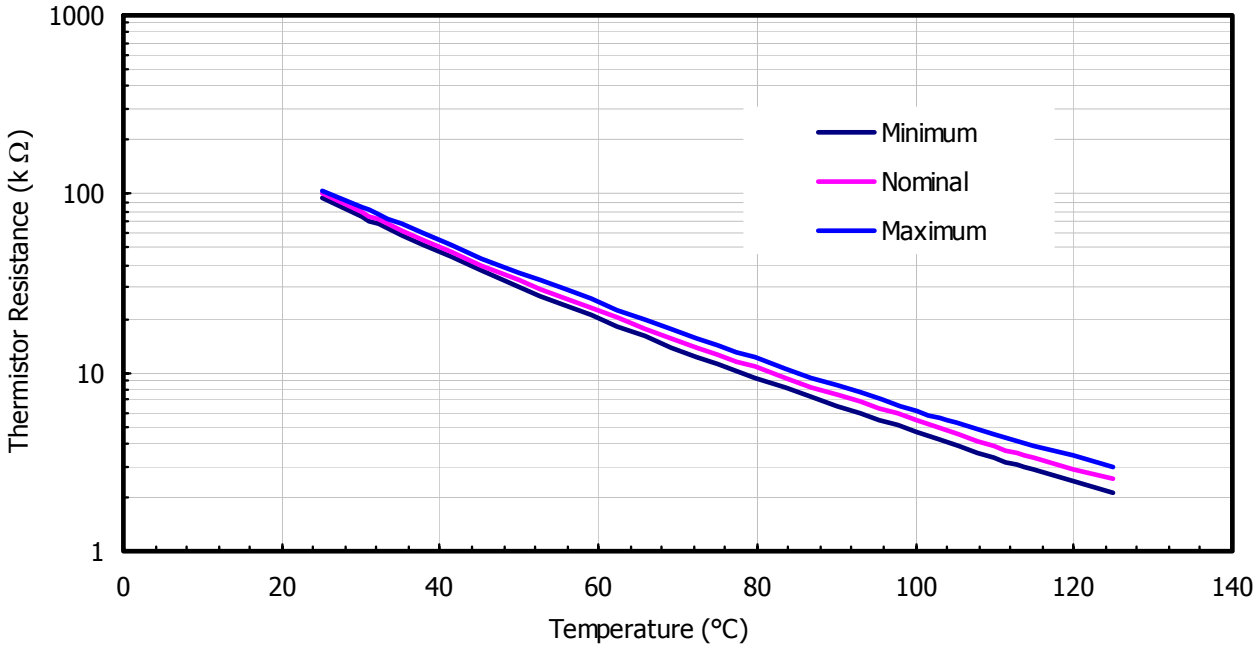


Figure 7. Variation of thermistor resistance with temperature

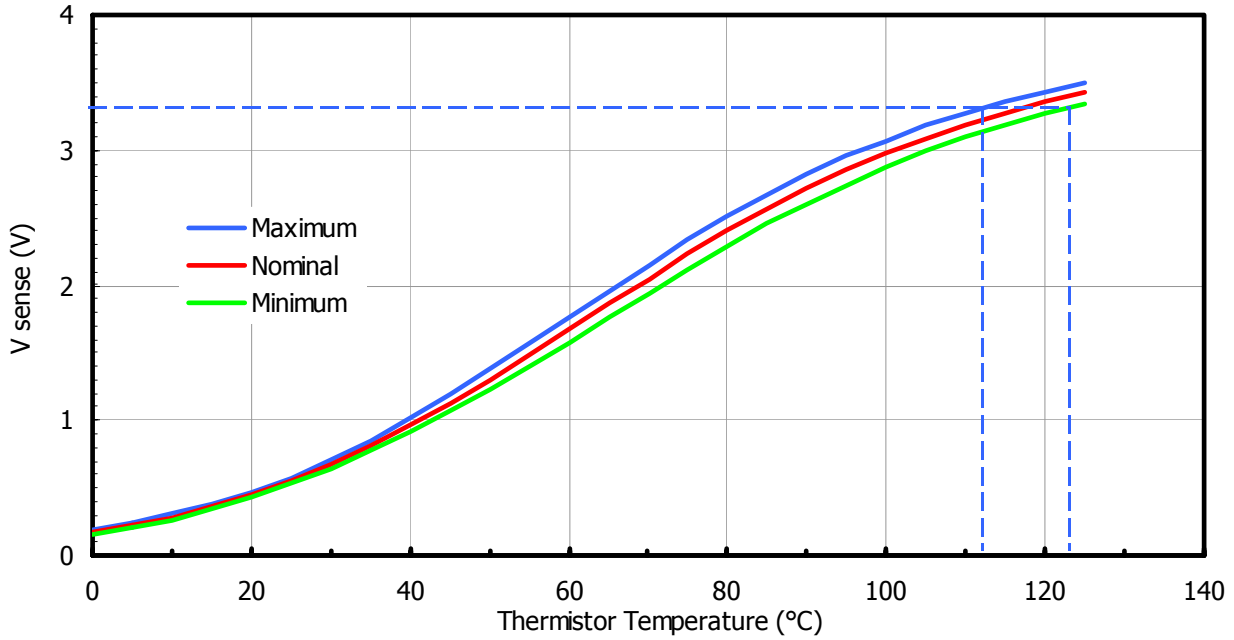


Figure 8. Variation of temperature sense voltage with thermistor temperature using external bias resistance of 4.3KΩ, V_{CC}=15V

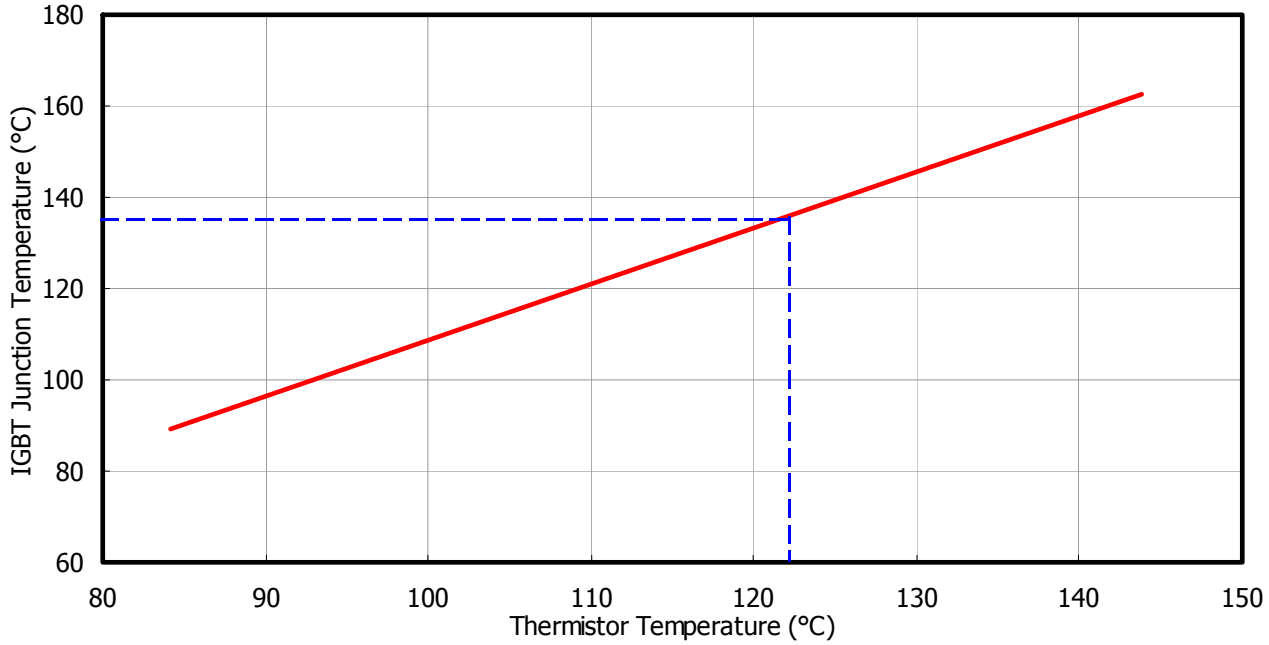


Figure 9. Estimated maximum IGBT junction temperature with thermistor temperature

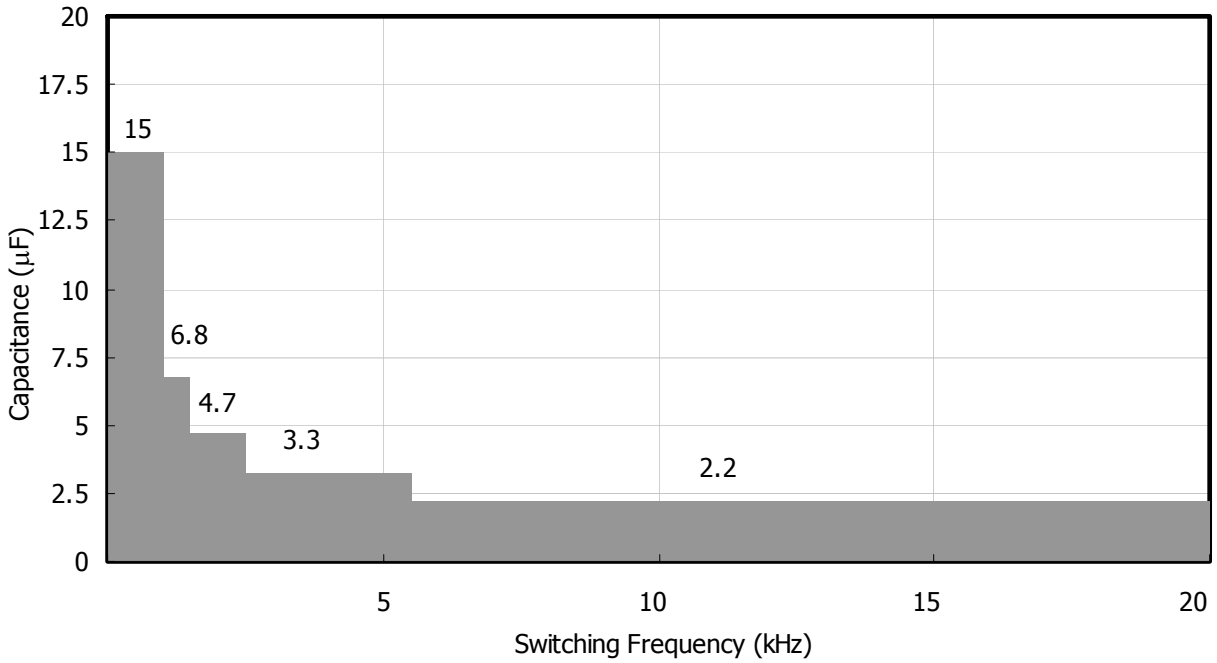


Figure 10. Recommended minimum Bootstrap Capacitor value Vs Switching Frequency

Figure 11. Switching Parameter Definitions

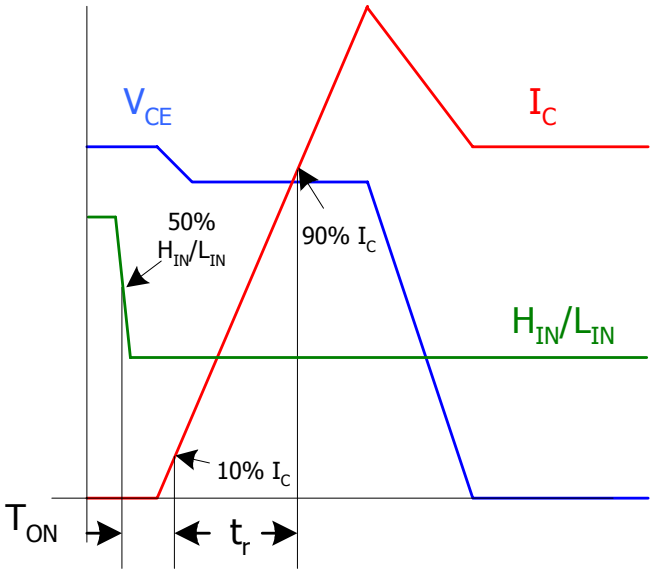


Figure 11a. Input to Output propagation turn-on delay time

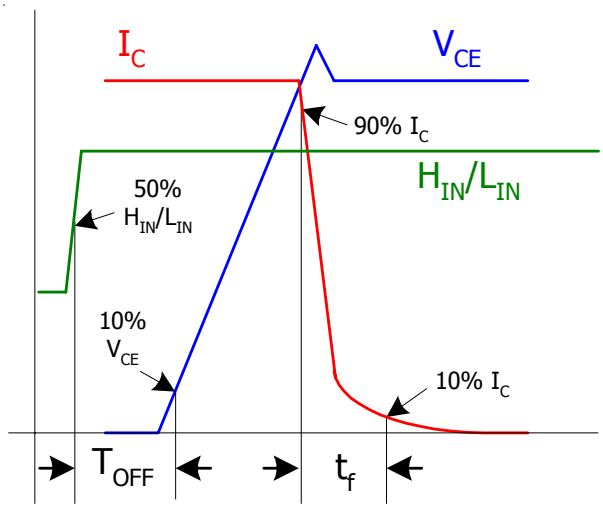


Figure 11b. Input to Output propagation turn-off delay timet

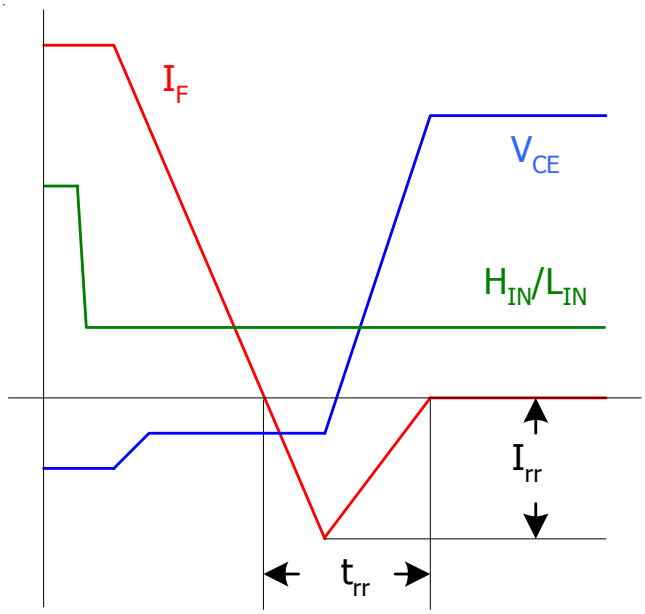


Figure 11c. Diode Reverse Recovery

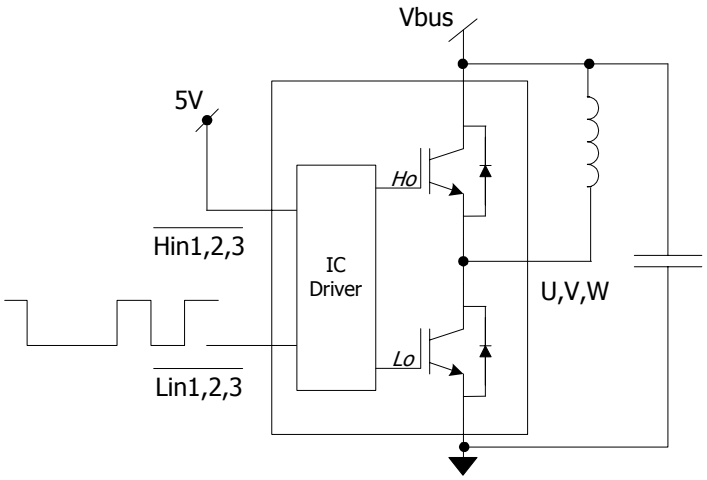


Figure CT1. Switching Loss Circuit

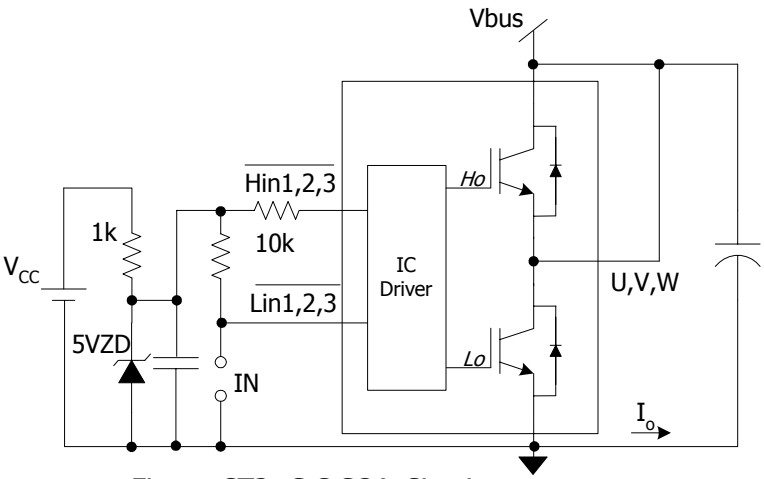
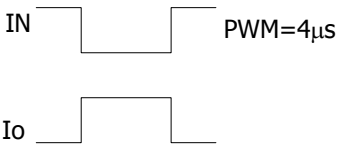


Figure CT2. S.C.SOA Circuit



V_P=Peak Voltage on the IGBT die

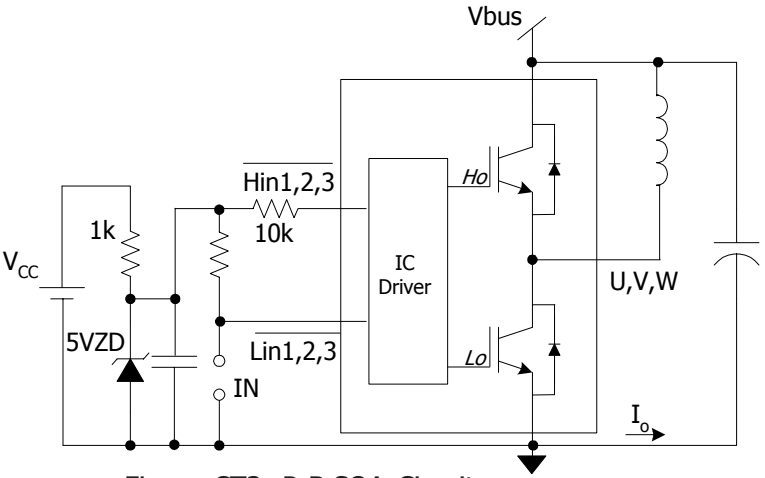
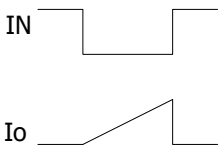


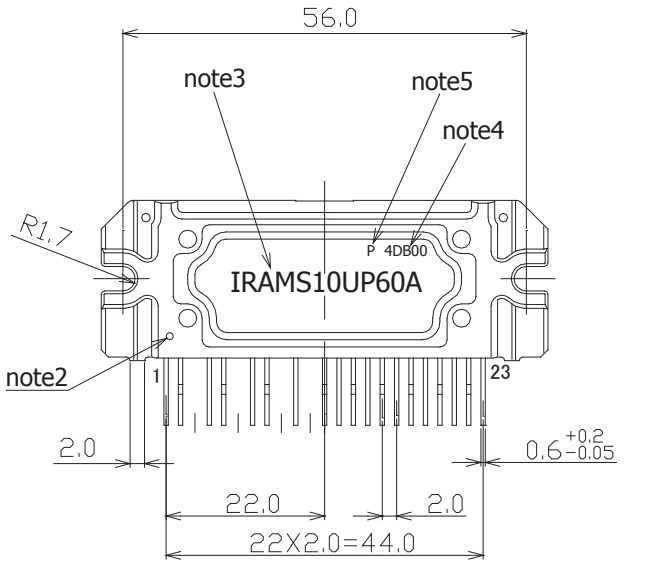
Figure CT3. R.B.SOA Circuit

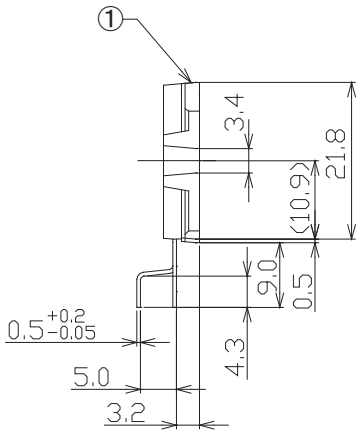


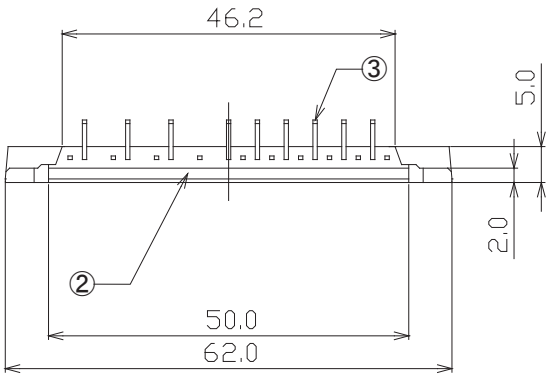
V_P=Peak Voltage on the IGBT die

Package Outline IRAMS10UP60A

missing pin : 3,6,9,11







note1: Unit Tolerance is ±0.5mm,
Unless Otherwise Specified.

note2: Mirror Surface Mark indicates Pin1 Identification.

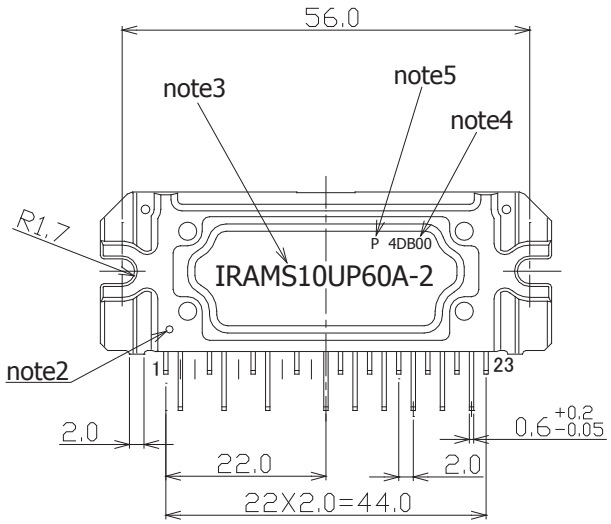
note3: Part Number Marking.
Characters Font in this drawing differs from
Font shown on Module.

note4: Lot Code Marking.
Characters Font in this drawing differs from
Font shown on Module.

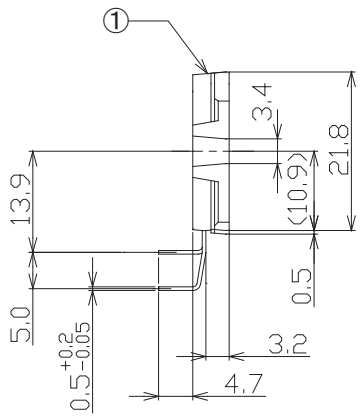
note5: "P" Character denotes Lead Free.
Characters Font in this drawing differs from
Font shown on Module.

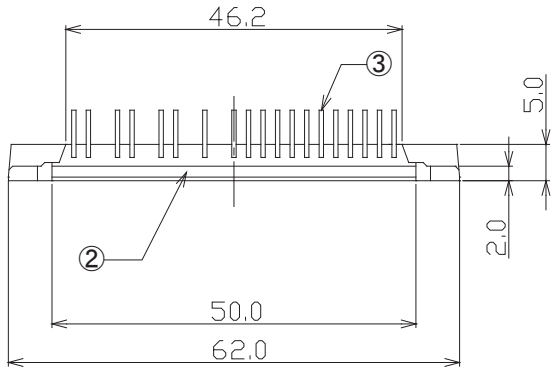
Dimensions in mm
For mounting instruction see AN-1049

Package Outline IRAMS10UP60A-2



missing pin : 3,6,9,11





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note2: Mirror Surface Mark indicates Pin1 Identification.

note3: Part Number Marking.
Characters Font in this drawing differs from Font shown on Module.

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Characters Font in this drawing differs from Font shown on Module.

Dimensions in mm
For mounting instruction see AN-1049

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2012-12-19