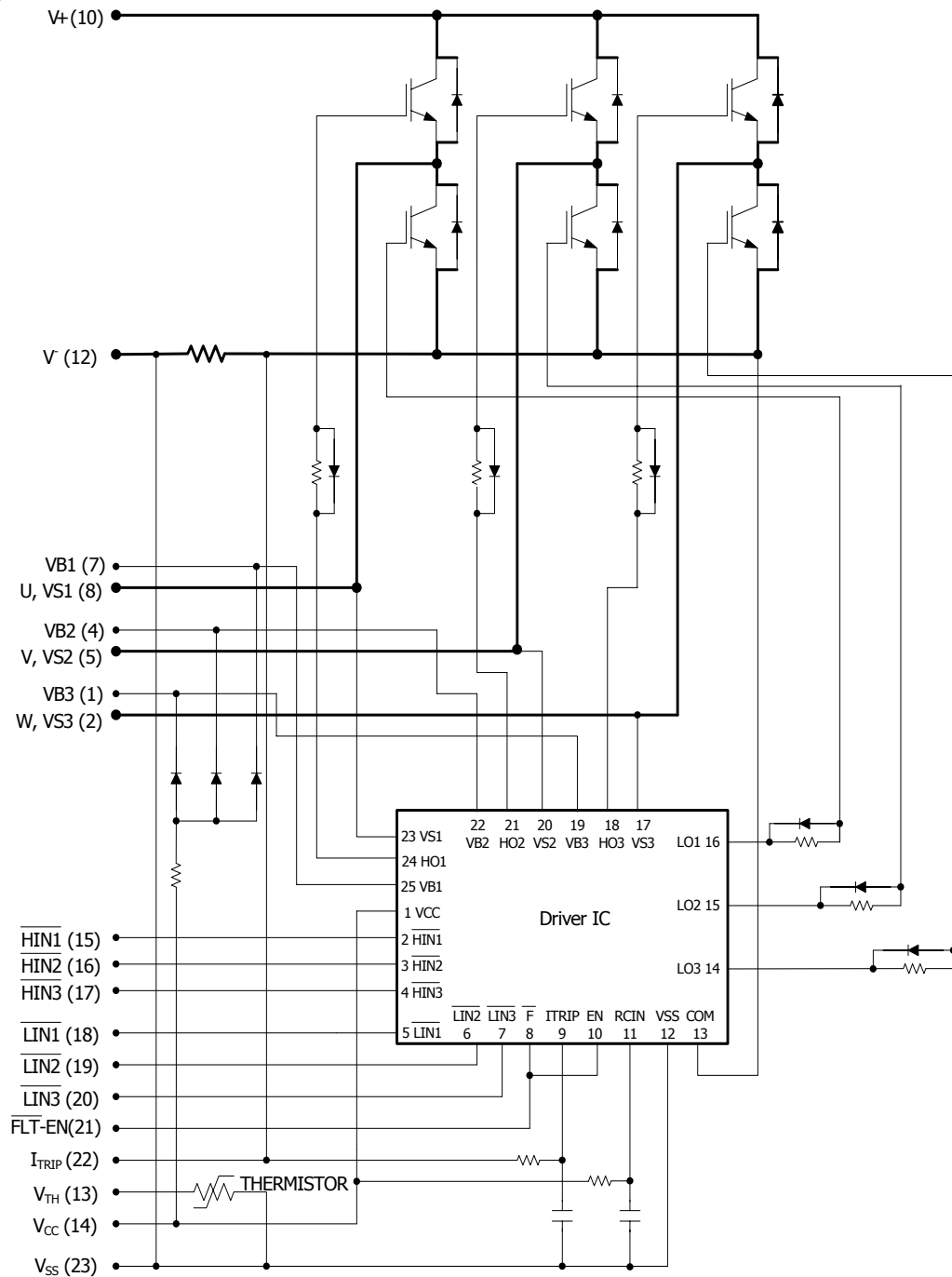


IRAMS10UP60B

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Internal Electrical Schematic - IRAMS10UP60B



Absolute Maximum Ratings (Continued)

Symbol	Parameter	Min	Max	Units	Conditions
I_{BDF}	Bootstrap Diode Peak Forward Current	---	4.5	A	$t_p = 10\text{ms}$, $T_J = 150^\circ\text{C}$, $T_C = 100^\circ\text{C}$
$P_{BR \text{ Peak}}$	Bootstrap Resistor Peak Power (Single Pulse)	---	80	W	$t_p = 100\mu\text{s}$, $T_C = 100^\circ\text{C}$ ESR / ERJ series
$V_{S1,2,3}$	High side floating supply offset voltage	$V_{B1,2,3} - 25$	$V_{B1,2,3} + 0.3$	V	
$V_{B1,2,3}$	High side floating supply voltage	-0.3	600	V	
V_{CC}	Low Side and logic fixed supply voltage	-0.3	20	V	
$V_{IN}, V_{EN}, V_{ITRIP}$	Input voltage LIN, HIN, EN, I_{Trip}	-0.3	Lower of ($V_{SS} + 15\text{V}$) or $V_{CC} + 0.3\text{V}$	V	

Inverter Section Electrical Characteristics @ $T_J = 25^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	---	---	V	$V_{IN} = 5\text{V}$, $I_C = 250\mu\text{A}$
$\Delta V_{(BR)CES} / \Delta T$	Temperature Coefficient of Breakdown Voltage	---	0.57	---	V/ $^\circ\text{C}$	$V_{IN} = 5\text{V}$, $I_C = 1.0\text{mA}$ ($25^\circ\text{C} - 150^\circ\text{C}$)
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	---	1.70	2.00	V	$I_C = 5\text{A}$, $V_{CC} = 15\text{V}$
		---	2.00	2.40		$I_C = 5\text{A}$, $V_{CC} = 15\text{V}$, $T_J = 150^\circ\text{C}$
I_{CES}	Zero Gate Voltage Collector Current	---	5	80	μA	$V_{IN} = 5\text{V}$, $V^+ = 600\text{V}$
		---	10	---		$V_{IN} = 5\text{V}$, $V^+ = 600\text{V}$, $T_J = 150^\circ\text{C}$
V_{FM}	Diode Forward Voltage Drop	---	1.80	2.35	V	$I_C = 5\text{A}$
		---	1.30	1.70		$I_C = 5\text{A}$, $T_J = 150^\circ\text{C}$
V_{BDFM}	Bootstrap Diode Forward Voltage Drop	--	--	1.25	V	$I_F = 1\text{A}$
		---	---	1.10		$I_F = 1\text{A}$, $T_J = 150^\circ\text{C}$
R_{BR}	Bootstrap Resistor Value	---	2	---	Ω	$T_J = 25^\circ\text{C}$
$\Delta R_{BR}/R_{BR}$	Bootstrap Resistor Tolerance	---	---	± 5	%	$T_J = 25^\circ\text{C}$
I_{BUS_TRIP}	Current Protection Threshold (positive going)	13.1	---	16.4	A	$T_J = -40^\circ\text{C}$ to 125°C See fig. 2

Inverter Section Switching Characteristics @ $T_J = 25^\circ\text{C}$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
E_{ON}	Turn-On Switching Loss	---	200	235	μJ	$I_C = 5\text{A}$, $V^+ = 400\text{V}$ $V_{CC} = 15\text{V}$, $L = 2\text{mH}$ Energy losses include "tail" and diode reverse recovery See CT1
E_{OFF}	Turn-Off Switching Loss	---	75	100		
E_{TOT}	Total Switching Loss	---	275	335		
E_{REC}	Diode Reverse Recovery energy	---	15	25		
t_{RR}	Diode Reverse Recovery time	---	70	100	ns	See CT1
E_{ON}	Turn-On Switching Loss	---	300	360	μJ	$I_C = 5\text{A}$, $V^+ = 400\text{V}$ $V_{CC} = 15\text{V}$, $L = 2\text{mH}$, $T_J = 150^\circ\text{C}$ Energy losses include "tail" and diode reverse recovery See CT1
E_{OFF}	Turn-off Switching Loss	---	135	165		
E_{TOT}	Total Switching Loss	---	435	525		
E_{REC}	Diode Reverse Recovery energy	---	30	40		
t_{RR}	Diode Reverse Recovery time	---	100	145	ns	See CT1
Q_G	Turn-On IGBT Gate Charge	---	29	44	nC	$I_C = 15\text{A}$, $V^+ = 400\text{V}$, $V_{GE} = 15\text{V}$
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 150^\circ\text{C}$, $I_C = 5\text{A}$, $V_P = 600\text{V}$ $V^+ = 450\text{V}$ $V_{CC} = +15\text{V}$ to 0V See CT3
SCSOA	Short Circuit Safe Operating Area	10	---	---	μs	$T_J = 150^\circ\text{C}$, $V_P = 600\text{V}$, $V^+ = 360\text{V}$, $V_{CC} = +15\text{V}$ to 0V See CT2
I_{CSC}	Short Circuit Collector Current	---	47	---	A	$T_J = 150^\circ\text{C}$, $V_P = 600\text{V}$, $t_{SC} < 10\mu\text{s}$ $V^+ = 360\text{V}$, $V_{GE} = 15\text{V}$ $V_{CC} = +15\text{V}$ to 0V See CT2

Recommended Operating Conditions Driver Function

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltages are absolute referenced to COM/ I_{TRIP} . The V_S offset is tested with all supplies biased at 15V differential (Note 3)

Symbol	Definition	Min	Max	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_S + 12$	$V_S + 20$	V
$V_{S1,2,3}$	High side floating supply offset voltage	Note 4	450	
V_{CC}	Low side and logic fixed supply voltage	12	20	V
V_{ITRIP}	I_{TRIP} input voltage	V_{SS}	$V_{SS} + 5$	
V_{IN}	Logic input voltage LIN, HIN	V_{SS}	$V_{SS} + 5$	V
V_{EN}	Logic input voltage EN	V_{SS}	$V_{SS} + 5$	V

Note 3: For more details, see IR21363 data sheet

Note 4: Logic operational for V_S from COM-5V to COM+600V. Logic state held for V_S from COM-5V to COM- V_{BS} . (please refer to DT97-3 for more details)

Static Electrical Characteristics Driver Function

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$)=15V, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM/ I_{TRIP} and are applicable to all six channels. (Note 3)

Symbol	Definition	Min	Typ	Max	Units
V_{INH} / V_{ENH}	Logic "0" input voltage	3.0	---	---	V
V_{INL} / V_{ENL}	Logic "1" input voltage	---	---	0.8	V
V_{CCUV+} , V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage Positive going threshold	10.6	11.1	11.6	V
V_{CCUV-} , V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage Negative going threshold	10.4	10.9	11.4	V
V_{CCUVH} , V_{BSUVH}	V_{CC} and V_{BS} supply undervoltage lock-out hysteresis	---	0.2	---	V
$V_{IN,Clamp}$	Input Clamp Voltage (HIN , LIN , I_{TRIP}) $I_{IN}=10\mu A$	4.9	5.2	5.5	V
I_{QBS}	Quiescent V_{BS} supply current $V_{IN}=0V$	---	---	165	μA
I_{QCC}	Quiescent V_{CC} supply current $V_{IN}=0V$	---	---	3.35	mA
I_{LK}	Offset Supply Leakage Current	---	---	60	μA
I_{IN+} , I_{EN+}	Input bias current $V_{IN}=5V$	---	200	300	μA
I_{IN-} , I_{EN-}	Input bias current $V_{IN}=0V$	---	100	220	μA
I_{TRIP+}	I_{TRIP} bias current $V_{ITRIP}=5V$	---	30	100	μA
I_{TRIP-}	I_{TRIP} bias current $V_{ITRIP}=0V$	---	0	1	μA
$V(I_{TRIP})$	I_{TRIP} threshold Voltage	440	490	540	mV
$V(I_{TRIP}, HYS)$	I_{TRIP} Input Hysteresis	---	70	---	mV
$R_{ON/FLT}$	Fault Output ON Resistance	---	50	100	ohm

Dynamic Electrical Characteristics

Driver only timing unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
T_{ON}	Input to Output propagation turn-on delay time (see fig.11)	---	590	---	ns	$V_{CC}=V_{BS}= 15V$, $I_C=10A$, $V^+=400V$
T_{OFF}	Input to Output propagation turn-off delay time (see fig. 11)	---	700	---	ns	
T_{FLIN}	Input Filter time (HIN , LIN)	100	200	---	ns	$V_{IN}=0$ & $V_{IN}=5V$
$T_{BLT-Trip}$	I_{TRIP} Blanking Time	100	150	---	ns	$V_{IN}=0$ & $V_{IN}=5V$
D_T	Dead Time ($V_{BS}=V_{DD}=15V$)	220	290	360	ns	$V_{BS}=V_{CC}=15V$
M_T	Matching Propagation Delay Time (On & Off)	---	40	75	ns	$V_{CC}= V_{BS}= 15V$, external dead time> 400ns
T_{ITrip}	I_{Trip} to six switch to turn-off propagation delay (see fig. 2)	---	---	1.75	μs	$V_{CC}=V_{BS}= 15V$, $I_C=10A$, $V^+=400V$
$T_{FLT-CLR}$	Post I_{Trip} to six switch to turn-off clear time (see fig. 2)	---	7.7	---	ms	$T_C = 25^\circ C$
		---	6.7	---		$T_C = 100^\circ C$

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Thermal and Mechanical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$R_{th(J-C)}$	Thermal resistance, per IGBT	---	4.2	4.7	°C/W	Flat, greased surface. Heatsink compound thermal conductivity 1W/mK
$R_{th(J-C)}$	Thermal resistance, per Diode	---	5.5	6.5		
$R_{th(C-S)}$	Thermal resistance, C-S	---	0.1	---		
C_D	Creepage Distance	3.2	---	---	mm	See outline Drawings

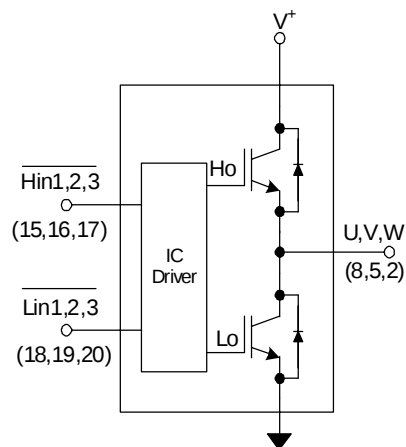
Internal Current Sensing Resistor - Shunt Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
R_{shunt}	Resistance	33.0	33.3	33.7	mΩ	$T_C = 25^\circ\text{C}$
T_{coeff}	Temperature Coefficient	0	---	200	ppm/°C	
P_{shunt}	Power Dissipation	---	---	2.2	W	$-40^\circ\text{C} < T_C < 100^\circ\text{C}$
T_{Range}	Temperature Range	-40	---	125	°C	

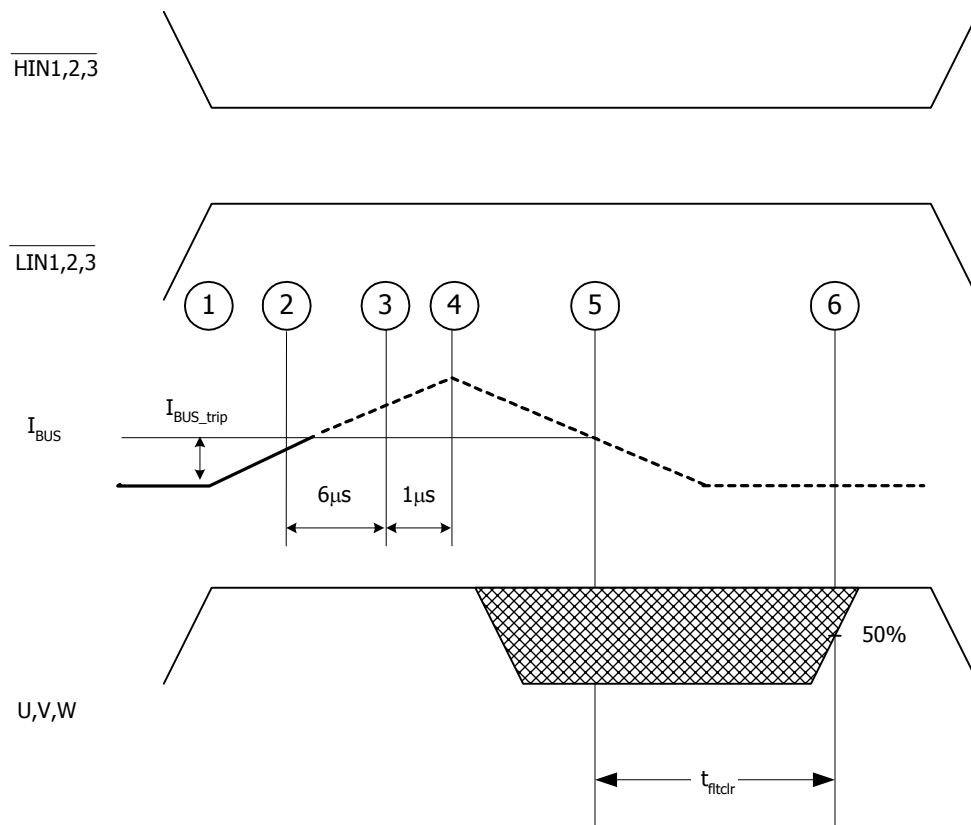
Internal NTC - Thermistor Characteristics

Parameter	Definition	Min	Typ	Max	Units	Conditions
R_{25}	Resistance	97	100	103	kΩ	$T_C = 25^\circ\text{C}$
R_{125}	Resistance	2.25	2.52	2.80	kΩ	$T_C = 125^\circ\text{C}$
B	B-constant (25-50°C)	4165	4250	4335	k	$R_2 = R_1 e^{[B(1/T_2 - 1/T_1)]}$
Temperature Range		-40		125	°C	
Typ. Dissipation constant			1		mW/°C	$T_C = 25^\circ\text{C}$

Input-Output Logic Level Table



FLT- EN	I_{TRIP}	$\overline{HIN1,2,3}$	$\overline{LIN1,2,3}$	U,V,W
1	0	0	1	V^+
1	0	1	0	0
1	0	1	1	Off
1	1	X	X	Off
0	X	X	X	Off



Sequence of events:

- 1-2) Current begins to rise
- 2) Current reaches $\text{I}_{\text{BUS_Trip}}$ level
- 2-3) Current is higher than $\text{I}_{\text{BUS_Trip}}$ for at least $6\mu\text{s}$. This value is the worst-case condition with very low over-current. In case of high current (short circuit), the actual delay will be smaller.
- 3-4) Delay between driver identification of over-current condition and disabling of all outputs
- 4) Current starts decreasing, eventually reaching 0
- 5) Current goes below $\text{I}_{\text{BUS_trip}}$, the driver starts its auto-reset sequence
- 6) Driver is automatically reset and normal operation can resume (over-current condition must be removed by the time the drivers automatically resets itself)

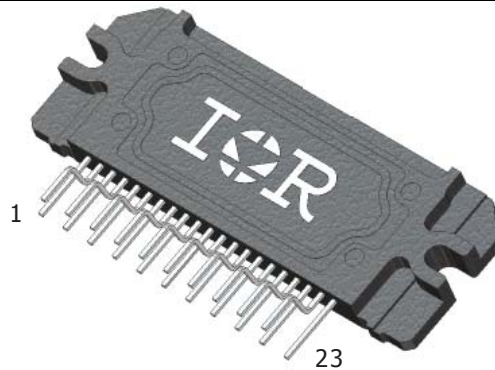
Figure 2. I_{Trip} Timing Waveform

Note 5: The shaded area indicates that both high-side and low-side switches are off and therefore the half-bridge output voltage would be determined by the direction of current flow in the load.

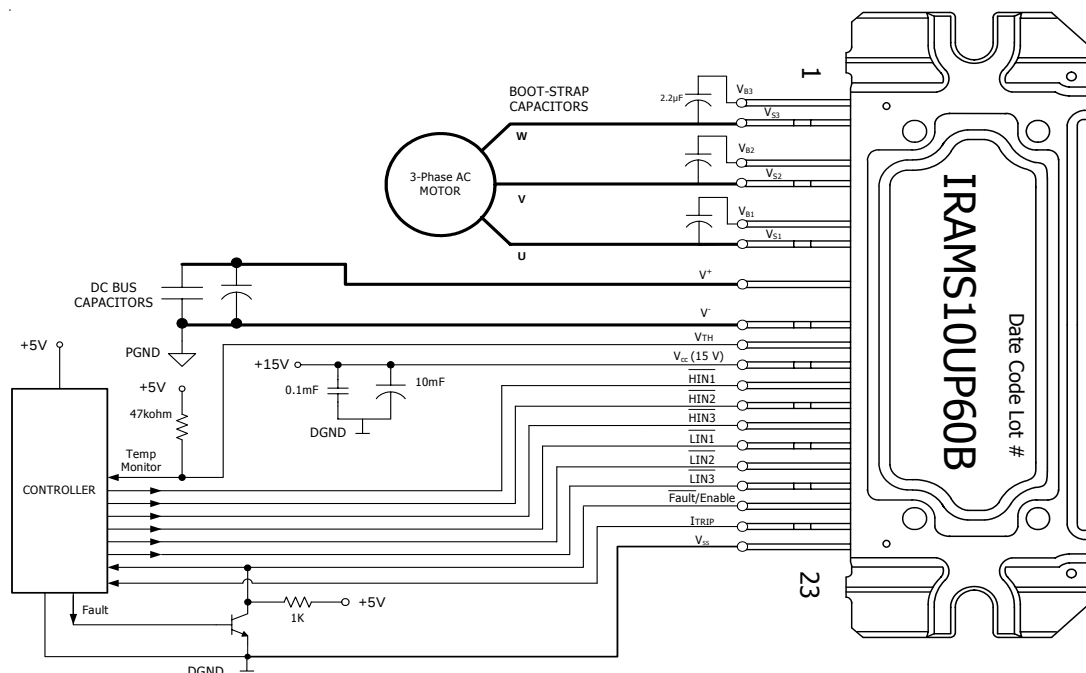
IRAMS10UP60B

Module Pin-Out Description

Pin	Name	Description
1	V_{B3}	High Side Floating Supply Voltage 3
2	W, V_{S3}	Output 3 - High Side Floating Supply Offset Voltage
3	NA	none
4	V_{B2}	High Side Floating Supply voltage 2
5	V, V_{S2}	Output 2 - High Side Floating Supply Offset Voltage
6	NA	none
7	V_{B1}	High Side Floating Supply voltage 1
8	U, V_{S1}	Output 1 - High Side Floating Supply Offset Voltage
9	NA	none
10	V^+	Positive Bus Input Voltage
11	NA	none
12	V^-	Negative Bus Input Voltage
13	V_{TH}	Temperature Feedback
14	V_{CC}	+15V Main Supply
15	$\overline{H_{IN1}}$	Logic Input High Side Gate Driver - Phase 1
16	$\overline{H_{IN2}}$	Logic Input High Side Gate Driver - Phase 2
17	$\overline{H_{IN3}}$	Logic Input High Side Gate Driver - Phase 3
18	$\overline{L_{IN1}}$	Logic Input Low Side Gate Driver - Phase 1
19	$\overline{L_{IN2}}$	Logic Input Low Side Gate Driver - Phase 2
20	$\overline{L_{IN3}}$	Logic Input Low Side Gate Driver - Phase 3
21	$\overline{FLT}/\text{Enable}$	Fault Output and Enable Pin
22	I_{TRIP}	Current Sense and Itrip Pin
23	V_{SS}	Negative Main Supply



Typical Application Connection IRAMS10UP60B



1. Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible to reduce ringing and EMI problems. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
2. In order to provide good decoupling between $V_{CC}-V_{SS}$ and $V_{B1,2,3}-V_{S1,2,3}$ terminals, the capacitors shown connected between these terminals should be located very close to the module pins. Additional high frequency capacitors, typically $0.1\mu F$, are strongly recommended.
3. Value of the boot-strap capacitors depends upon the switching frequency. Their selection should be made based on IR design tip DN 98-2a, application note AN-1044 or Figure 9. Bootstrap capacitor value must be selected to limit the power dissipation of the internal resistor in series with the V_{CC} . (see maximum ratings Table on page 3).
4. Current sense signal can be obtained from pin 22 and pin 23. Care should be taken to avoid having inverter current flowing through pin 22 to maintain required current measurement accuracy.
5. After approx. 8ms the FAULT is reset. (see Dynamic Characteristics Table on page 5).
6. PWM generator must be disabled within Fault duration to guarantee shutdown of the system, overcurrent condition must be cleared before resuming operation.
7. Fault/Enable pin must be pulled-up to +5V.

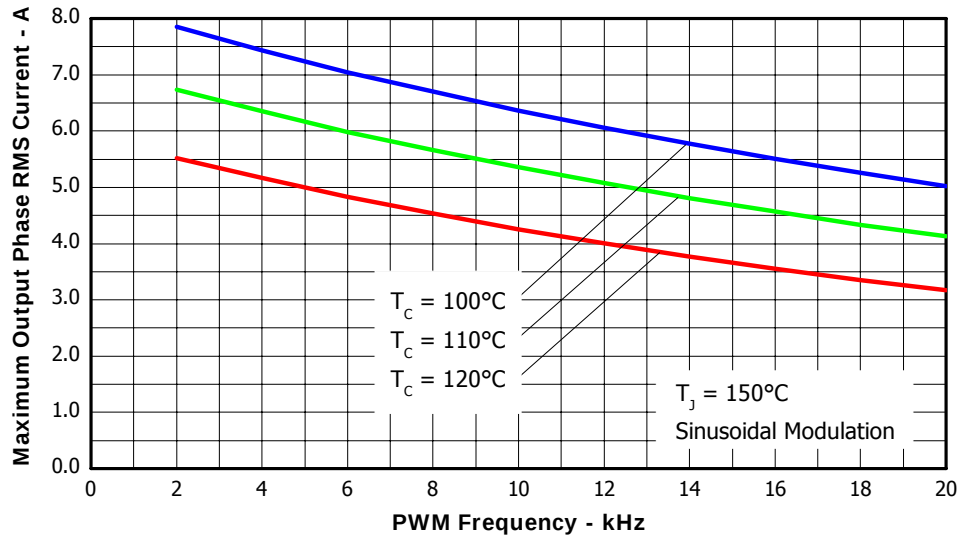


Figure 3. Maximum Sinusoidal Phase Current vs. PWM Switching Frequency
 $V^+ = 400\text{V}$, $T_j = 150^\circ\text{C}$, Modulation Depth=0.8, PF=0.6

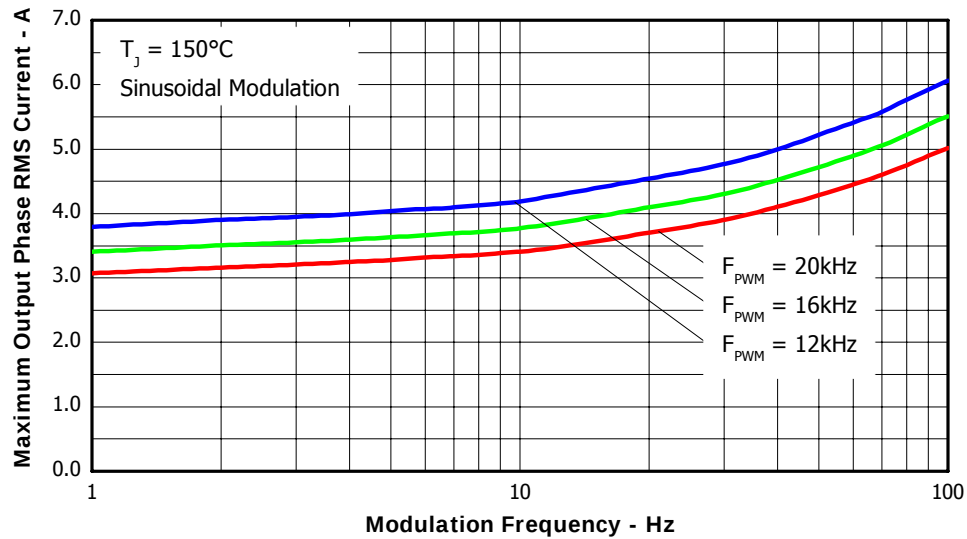


Figure 4. Maximum Sinusoidal Phase Current vs. Modulation Frequency
 $V^+ = 400\text{V}$, $T_j = 150^\circ\text{C}$, $T_c = 100^\circ\text{C}$, Modulation Depth=0.8, PF=0.6

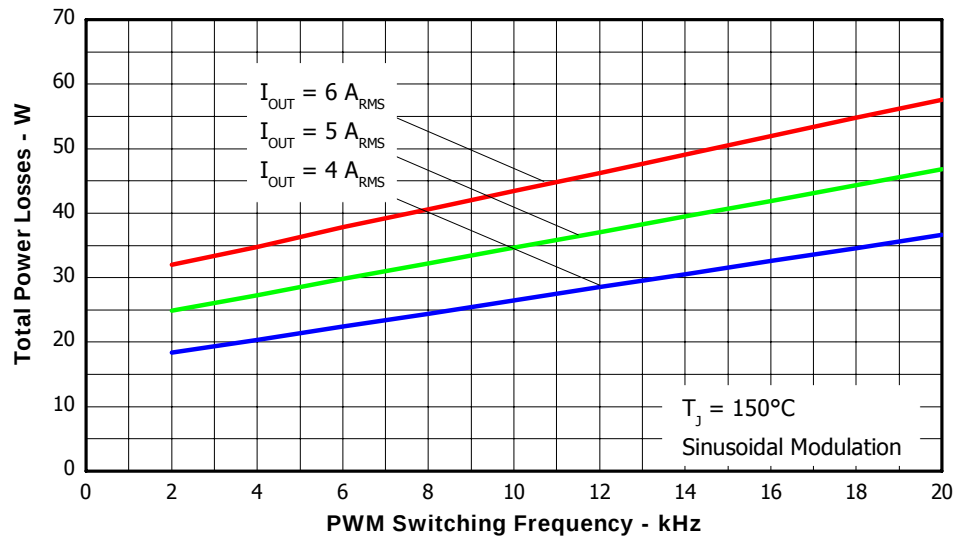


Figure 5. Total Power Losses vs. PWM Switching Frequency, Sinusoidal modulation
 $V^+=400V$, $T_J=150^\circ C$, Modulation Depth=0.8, PF=0.6

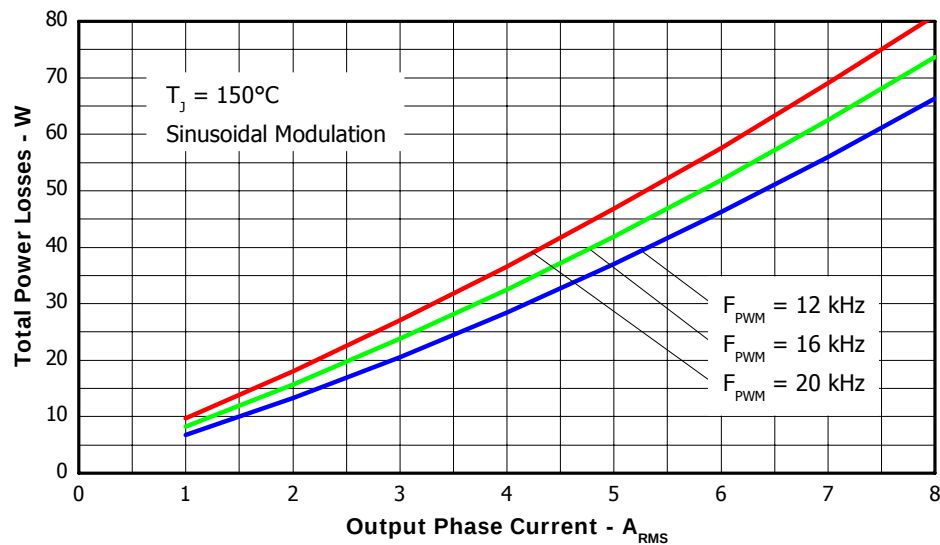


Figure 6. Total Power Losses vs. Output Phase Current, Sinusoidal modulation
 $V_{BUS}=400V$, $T_J=150^\circ C$, Modulation Depth=0.8, PF=0.6

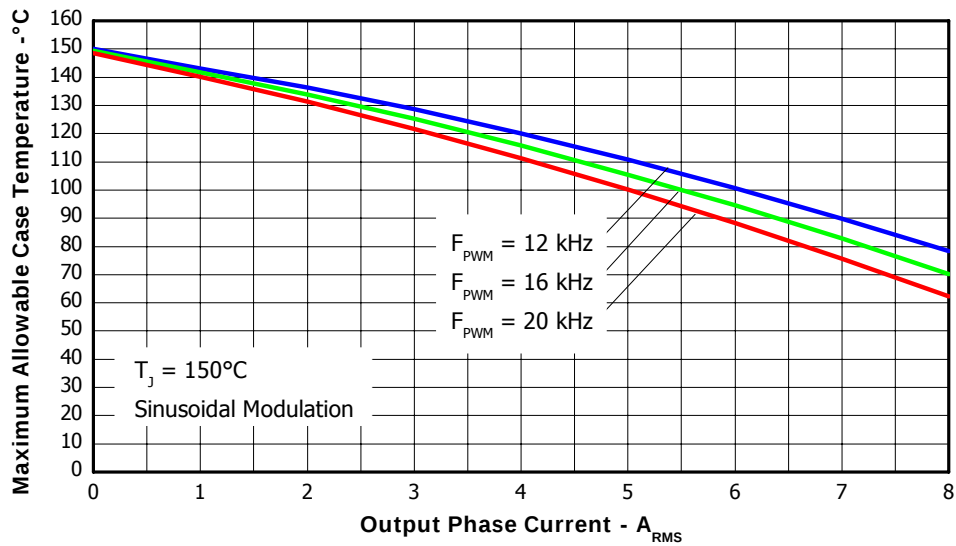


Figure 7. Maximum Allowable Case temperature vs. Output RMS Current per Phase

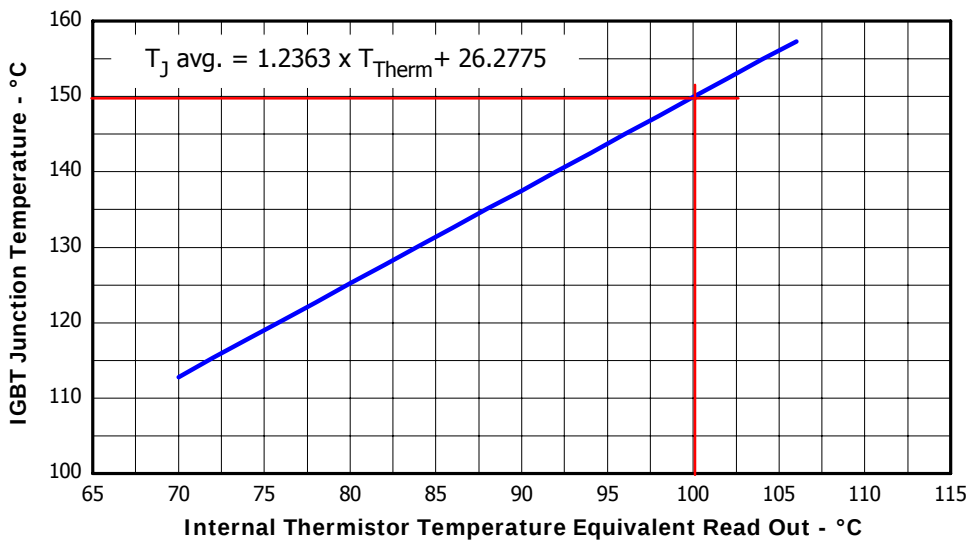


Figure 8. Estimated Maximum IGBT Junction Temperature vs. Thermistor Temperature

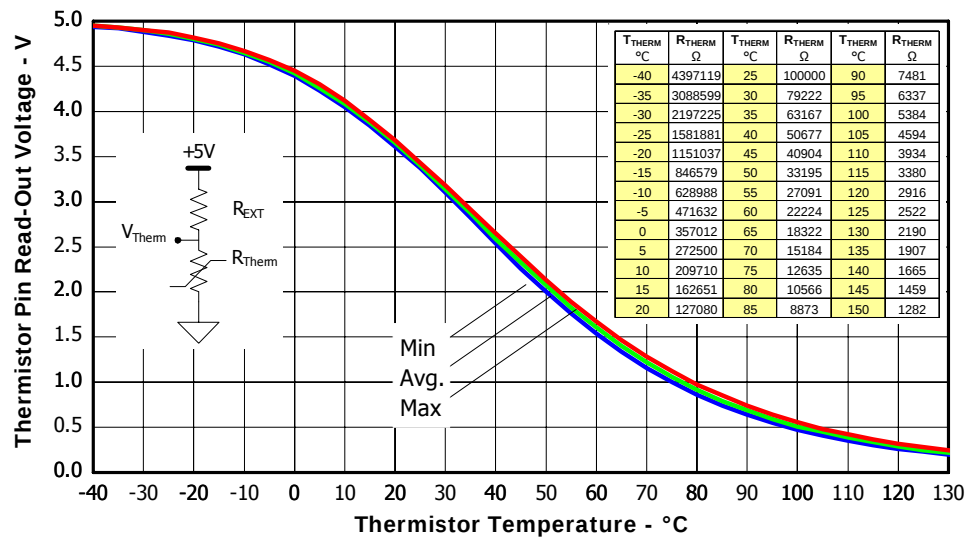


Figure 9. Thermistor Readout vs. Temperature (47kohm pull-up resistor, 5V) and Nominal Thermistor Resistance values vs. Temperature Table.

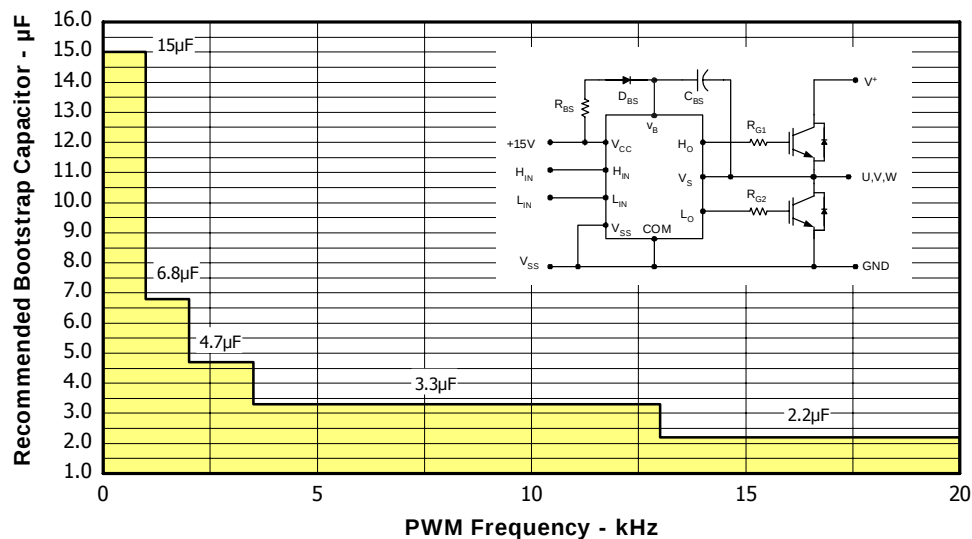


Figure 10. Recommended Bootstrap Capacitor Value vs. Switching Frequency

Figure 11. Switching Parameter Definitions

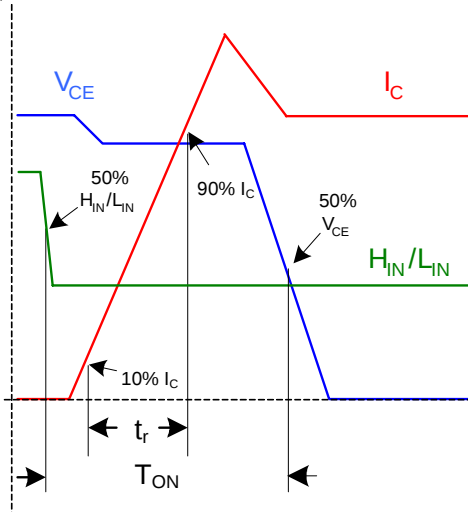


Figure 11a. Input to Output Propagation turn-on Delay Time

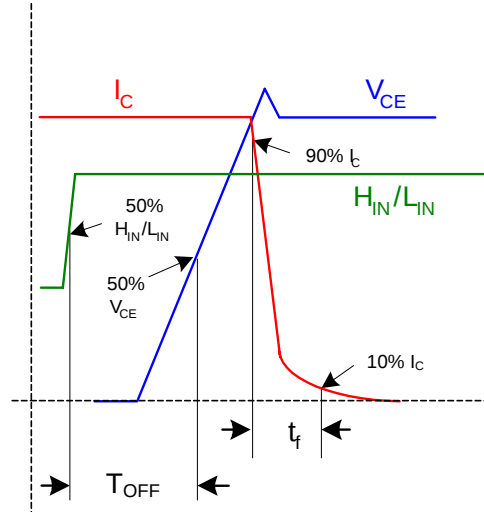


Figure 11b. Input to Output Propagation turn-off Delay Time

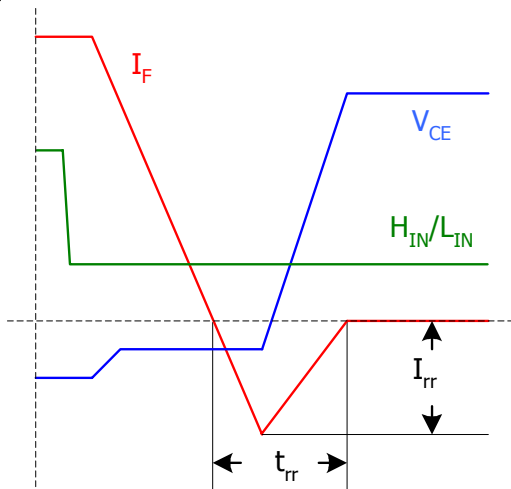


Figure 11c. Diode Reverse Recovery

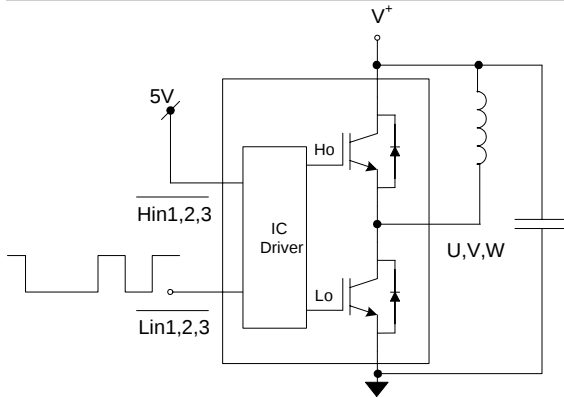


Figure CT1. Switching Loss Circuit

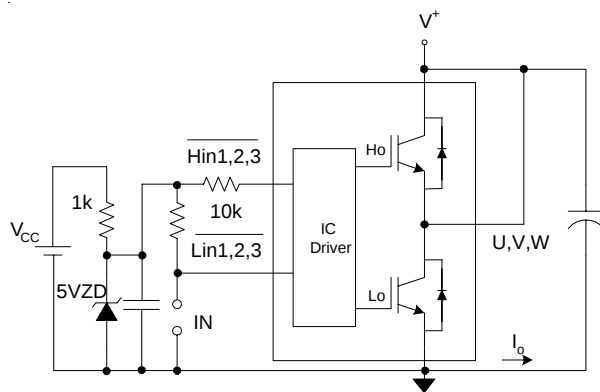
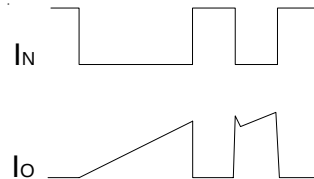


Figure CT2. S.C.SOA Circuit

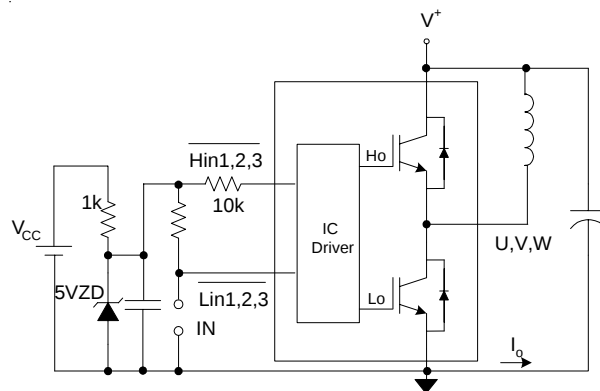
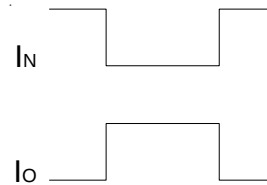
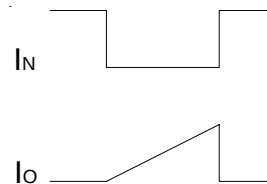
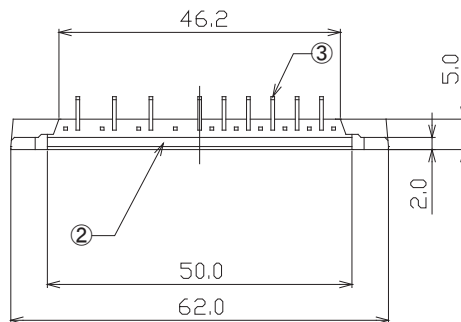
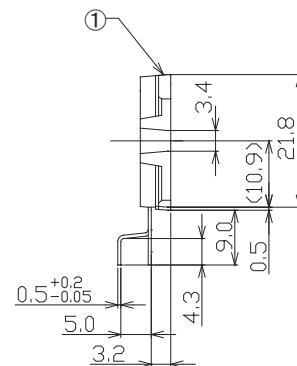


Figure CT3. R.B.SOA Circuit



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missing pin : 3,6,9,11



note1: Unit Tolerance is $\pm 0.5\text{mm}$,
Unless Otherwise Specified.

note2: Mirror Surface Mark indicates Pin1 Identification.

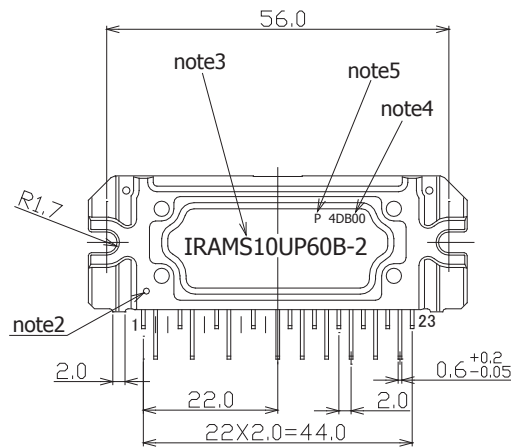
note3: Part Number Marking.
Characters Font in this drawing differs from
Font shown on Module.

note4: Lot Code Marking.
Characters Font in this drawing differs from
Font shown on Module.

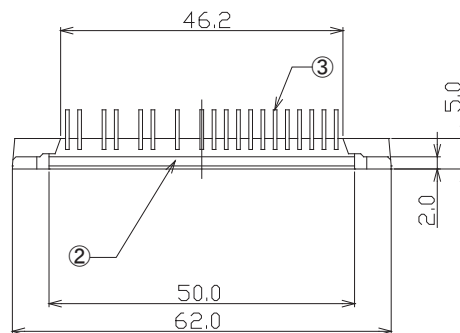
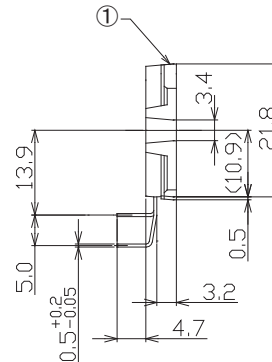
note5: "P" Character denotes Lead Free.
Characters Font in this drawing differs from
Font shown on Module.

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Package Outline IRAMS10UP60B-2



missing pin : 3,6,9,11



- note1: Unit Tolerance is +0.5mm, Unless Otherwise Specified.
- note2: Mirror Surface Mark indicates Pin1 Identification.
- note3: Part Number Marking. Characters Font in this drawing differs from Font shown on Module.
- note4: Lot Code Marking. Characters Font in this drawing differs from Font shown on Module.
- note5: "P" Character denotes Lead Free. Characters Font in this drawing differs from Font shown on Module.

Dimensions in mm
For mounting instruction see AN-1049