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1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	10.1 6.4	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	18	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	142	mJ	I_D=1.3A; V_{DD}=50V; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	0.21	mJ	I_D=1.3A; V_{DD}=50V; see table 11
Avalanche current, repetitive	I_{AR}	-	-	1.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS}=0...480V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation (Non FullPAK) TO-252	P_{tot}	-	-	86	W	T_C=25°C
Storage temperature	T_{stg}	-40	-	150	°C	-
Operating junction temperature	T_j	-40	-	150	°C	-
Continuous diode forward current	I_S	-	-	7.1	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	18	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 9
Maximum diode commutation speed	di_f/dt	-	-	500	A/µs	V_{DS}=0...400V, I_{SD}<=I_S, T_j=25°C see table 9
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	28	W	T_C=25°C
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$.TO252 equivalent, Maximum duty cycle D=0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.5	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	V_{DS}=V_{GS}, I_D=0.21mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=650, V_{GS}=0V, T_j=25°C V_{DS}=650, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.54 1.40	0.65 -	Ω	V_{GS}=10V, I_D=2.1A, T_j=25°C V_{GS}=10V, I_D=2.1A, T_j=150°C
Gate resistance	R_G	-	10.5	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	440	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	30	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	21	-	pF	V_{GS}=0V, V_{DS}=0...480V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	88	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...480V
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=3.2A, R_G=6.8Ω; see table 10
Rise time	t_r	-	8	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=3.2A, R_G=6.8Ω; see table 10
Turn-off delay time	$t_{d(off)}$	-	64	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=3.2A, R_G=6.8Ω; see table 10
Fall time	t_f	-	11	-	ns	V_{DD}=400V, V_{GS}=13 V, I_D=3.2A, R_G=6.8Ω; see table 10

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.75	-	nC	V_{DD}=480V, I_D=3.2A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	12	-	nC	V_{DD}=480V, I_D=3.2A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	23	-	nC	V_{DD}=480V, I_D=3.2A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.5	-	V	V_{DD}=480V, I_D=3.2A, V_{GS}=0 to 10V

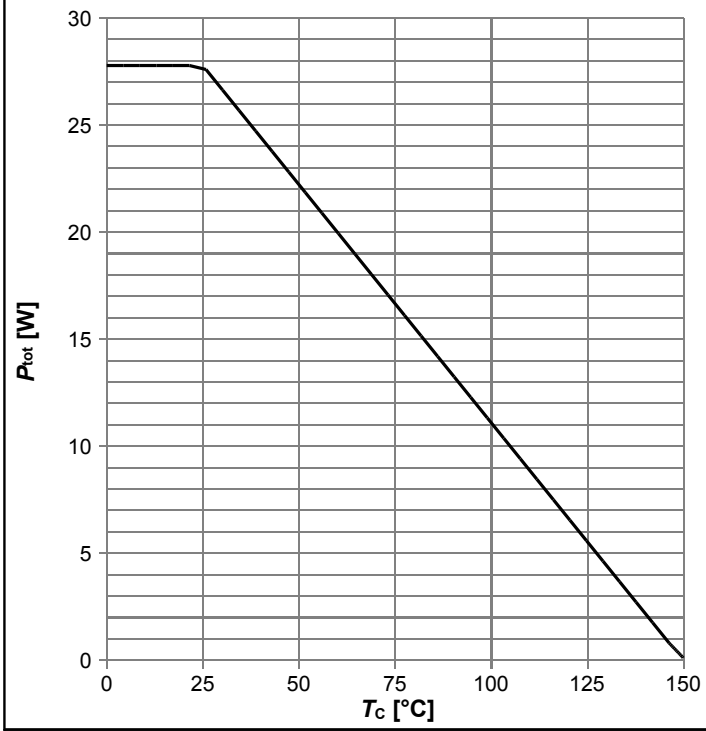
[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{o(BR)DSS}$
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{o(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=3.2A, T_j=25°C
Reverse recovery time	t_{rr}	-	270	-	ns	V_R=400V, I_F=3.2A, di_F/dt=100A/µs; see table 9
Reverse recovery charge	Q_{rr}	-	2	-	µC	V_R=400V, I_F=3.2A, di_F/dt=100A/µs; see table 9
Peak reverse recovery current	I_{rrm}	-	13	-	A	V_R=400V, I_F=3.2A, di_F/dt=100A/µs; see table 9

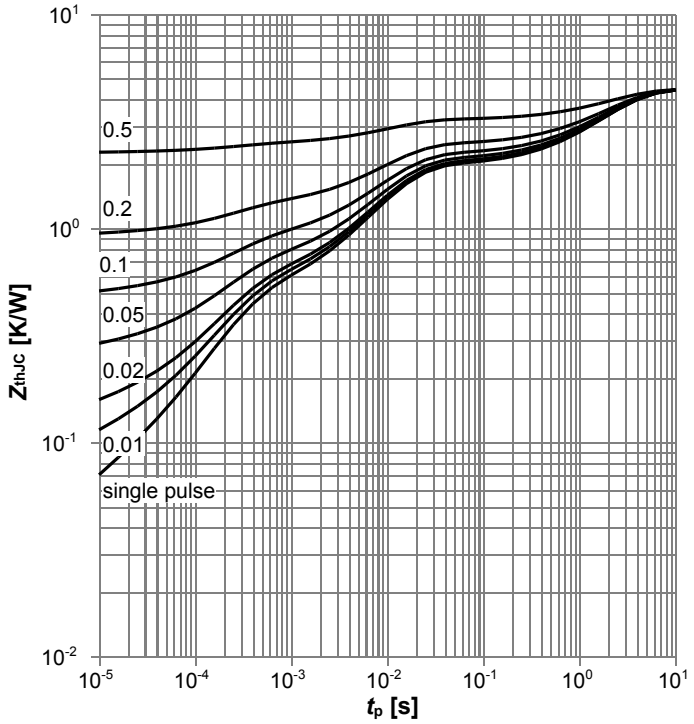
4 Electrical characteristics diagrams

Diagram 2: Power dissipation (FullPAK)



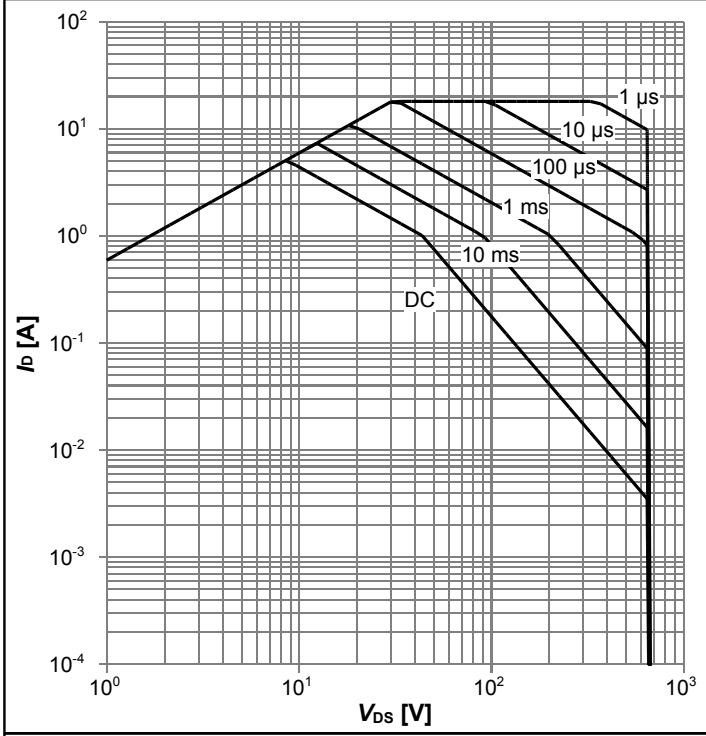
$P_{tot}=f(T_C)$

Diagram 4: Max. transient thermal impedance (FullPAK)



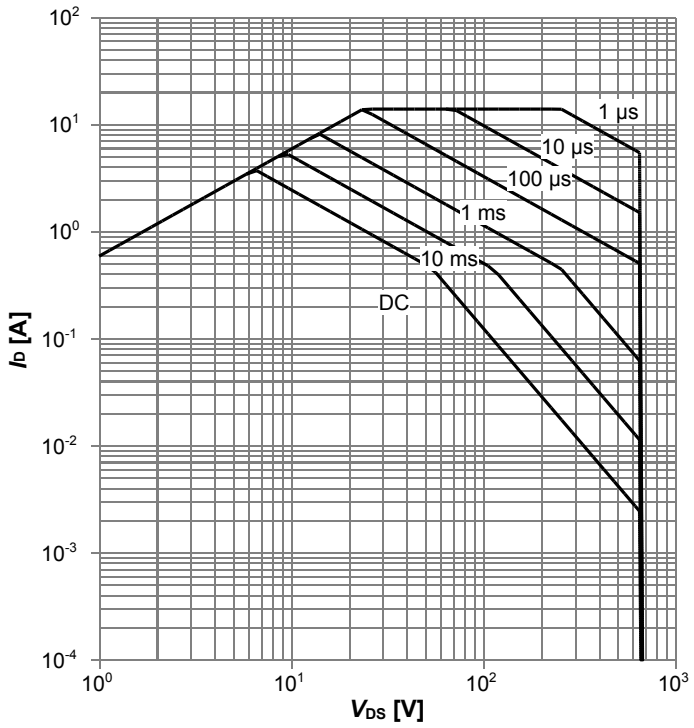
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 6: Safe operating area (FullPAK)



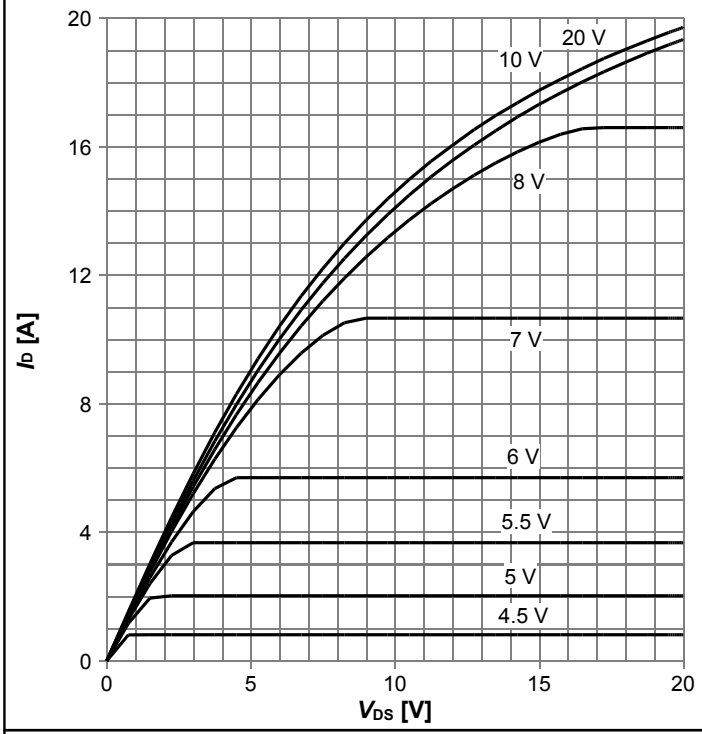
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 8: Safe operating area (FullPAK)



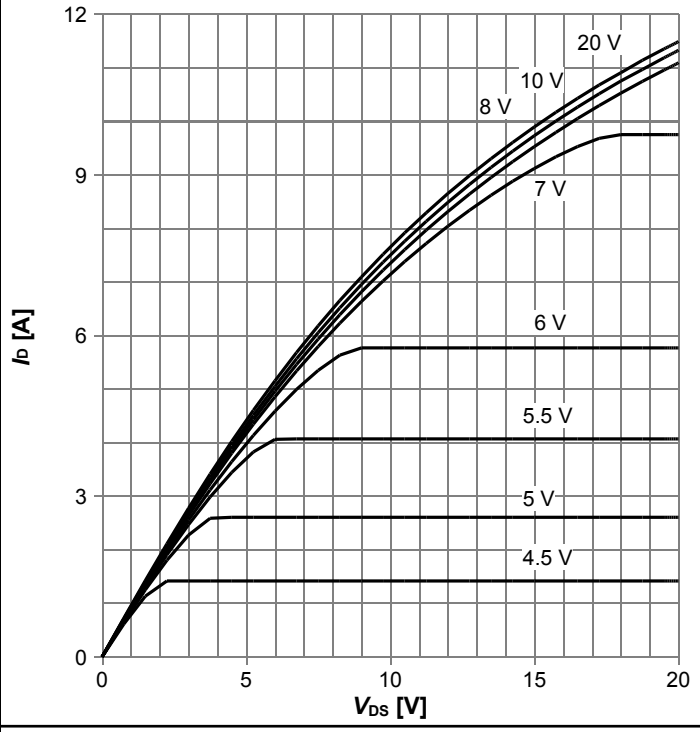
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Diagram 9: Typ. output characteristics



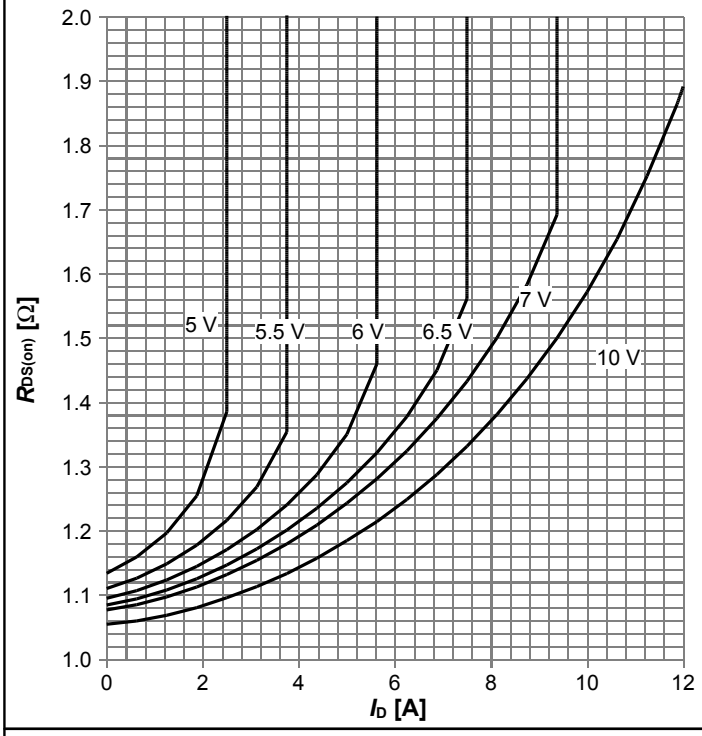
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 10: Typ. output characteristics



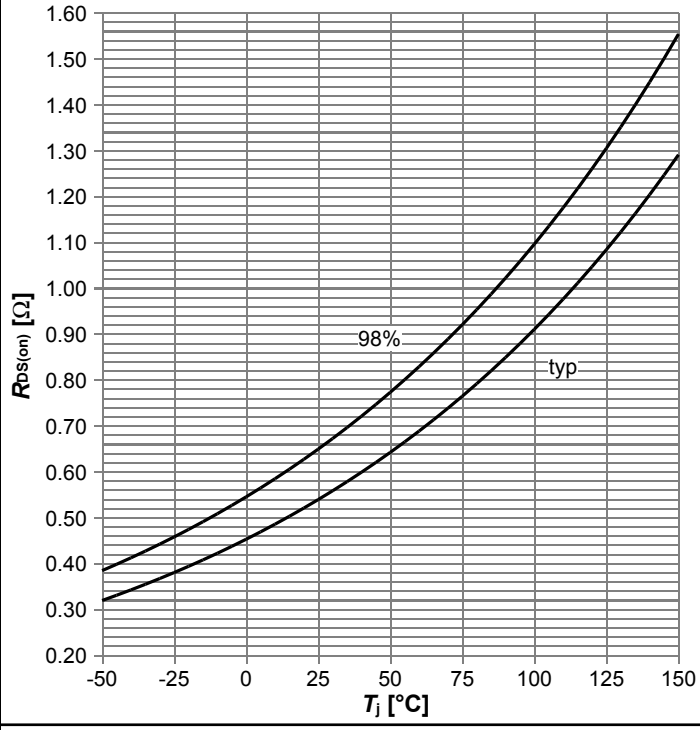
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



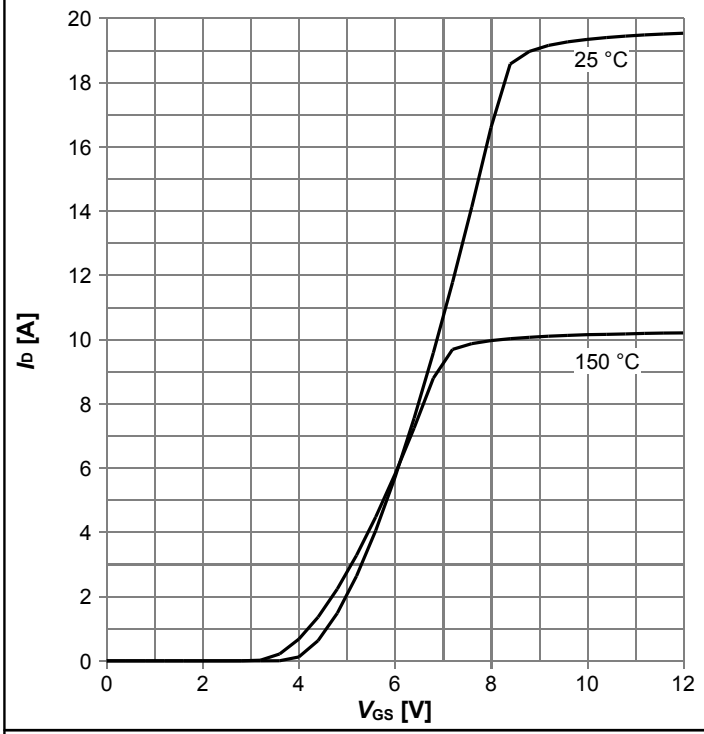
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Diagram 12: Drain-source on-state resistance



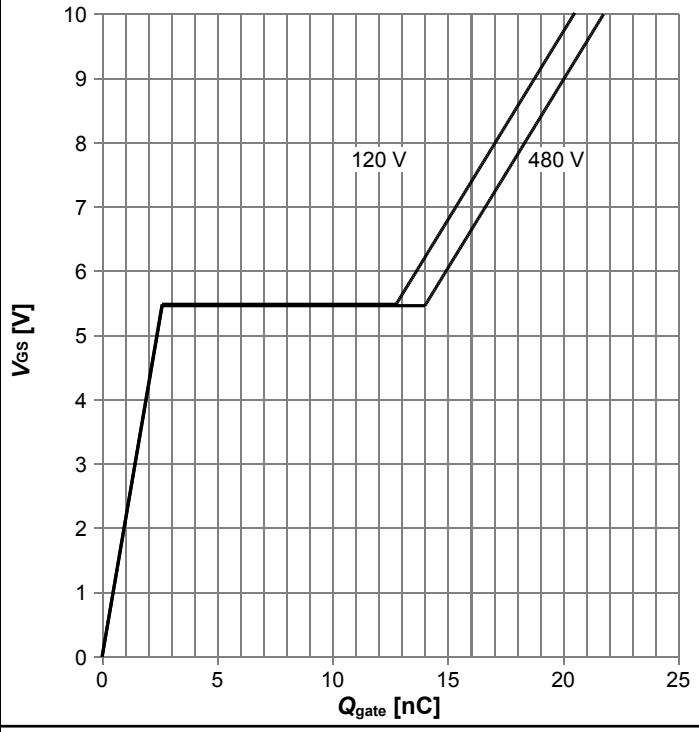
$R_{DS(on)}=f(T_j)$; $I_D=2.1$ A; $V_{GS}=10$ V

Diagram 13: Typ. transfer characteristics



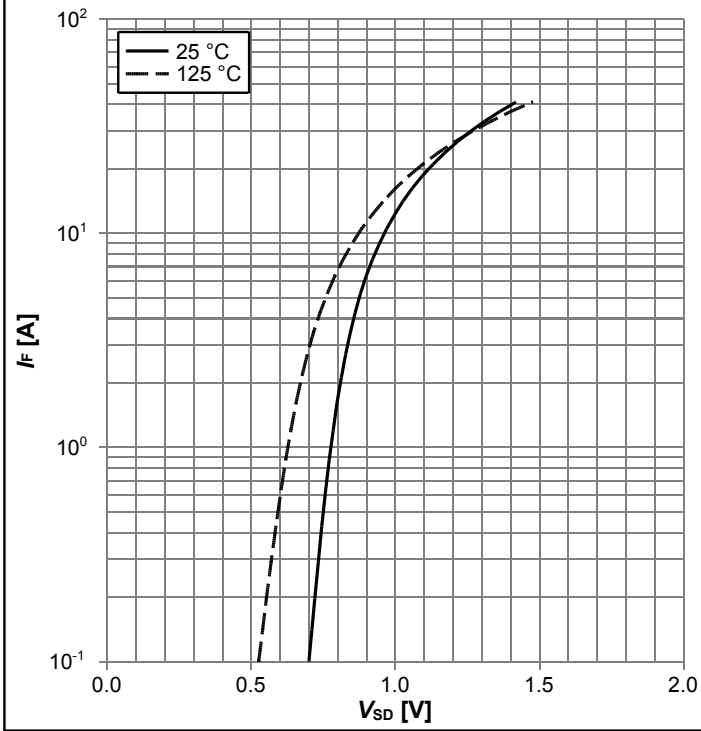
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j

Diagram 14: Typ. gate charge



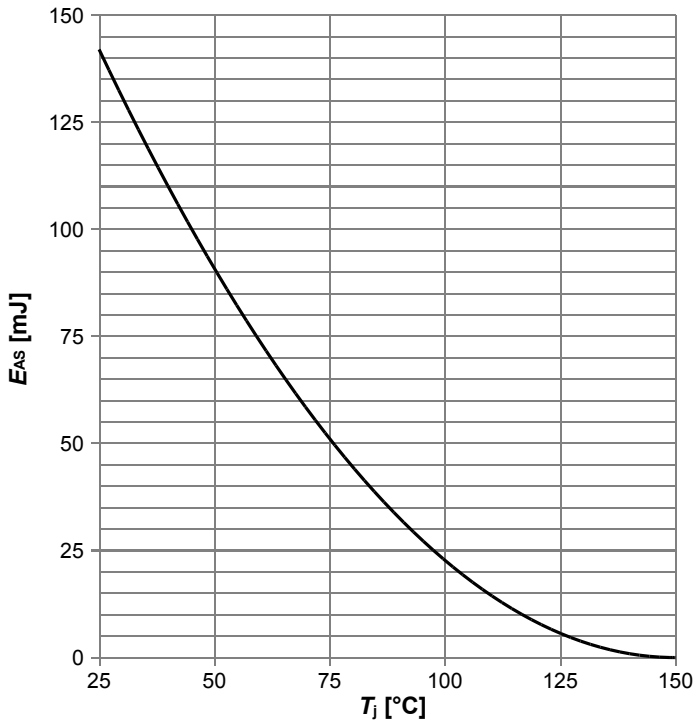
$V_{GS}=f(Q_{gate})$; I_D=3.2 A pulsed; parameter: V_{DD}

Diagram 15: Forward characteristics of reverse diode



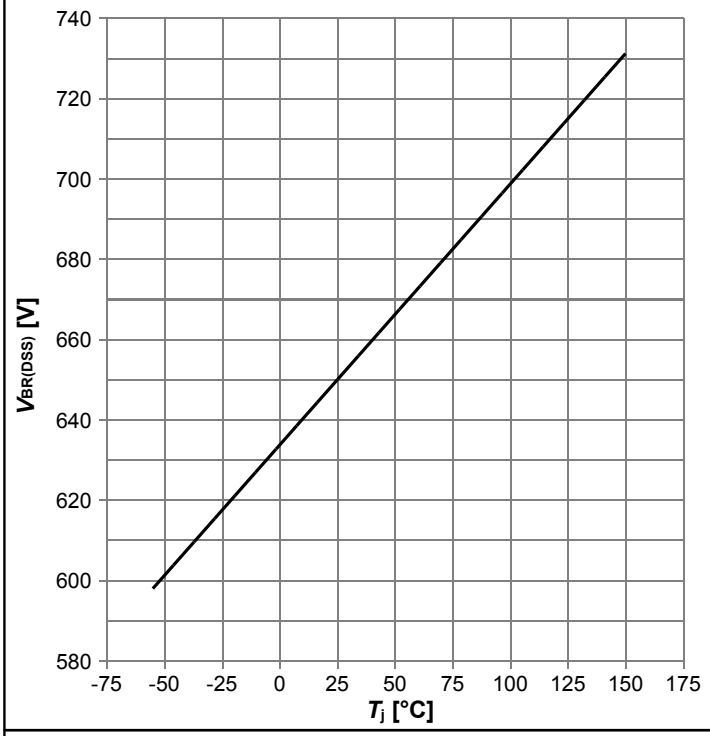
$I_F=f(V_{SD})$; parameter: T_j

Diagram 16: Avalanche energy



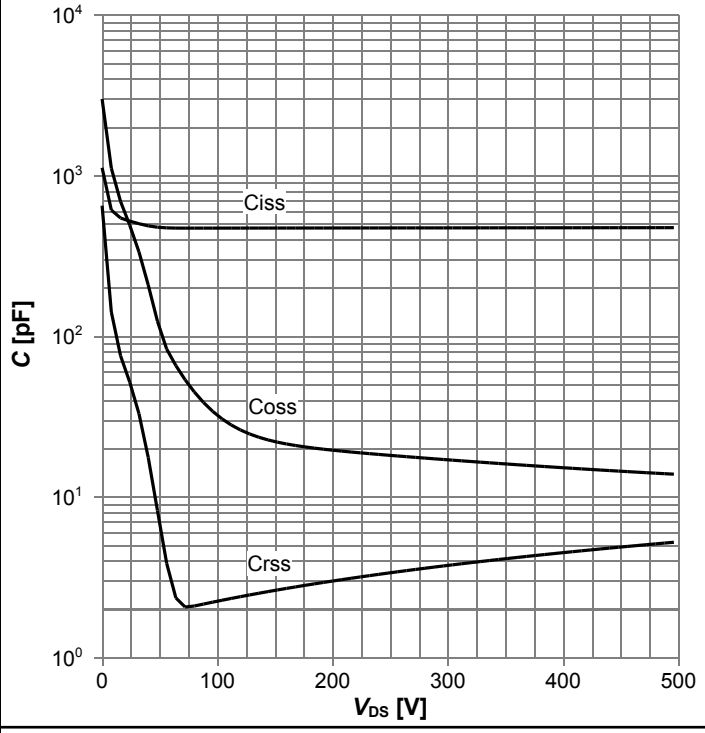
$E_{AS}=f(T_j)$; I_D=1.3 A; V_{DD}=50 V

Diagram 17: Drain-source breakdown voltage



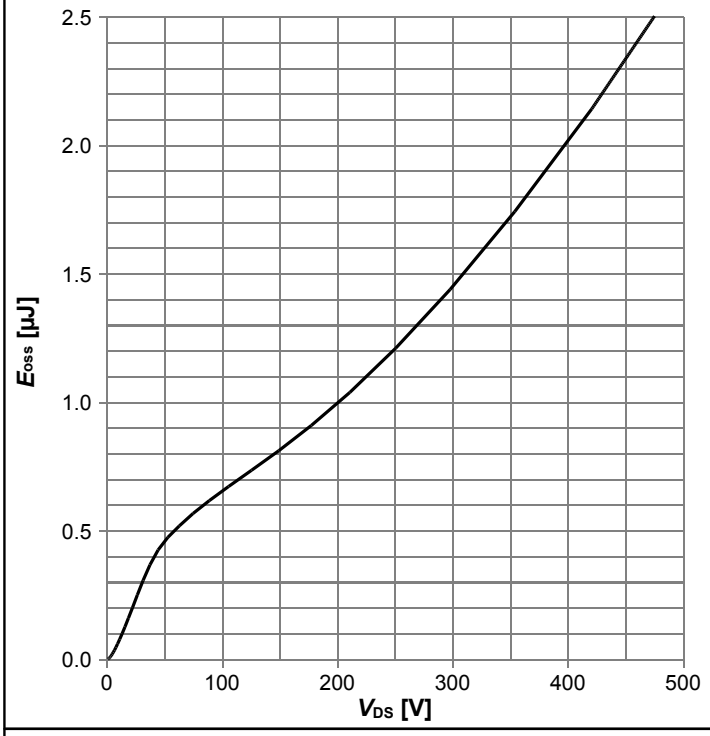
$V_{BR(DSS)}$=f(T_j); I_D=1.0 mA

Diagram 18: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 19: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

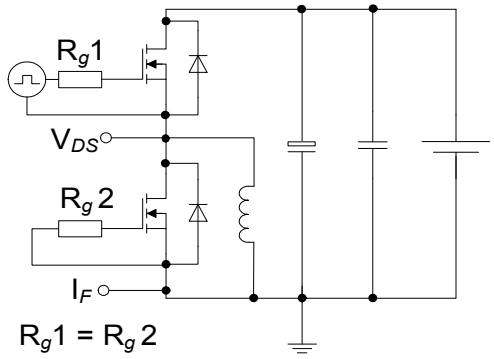
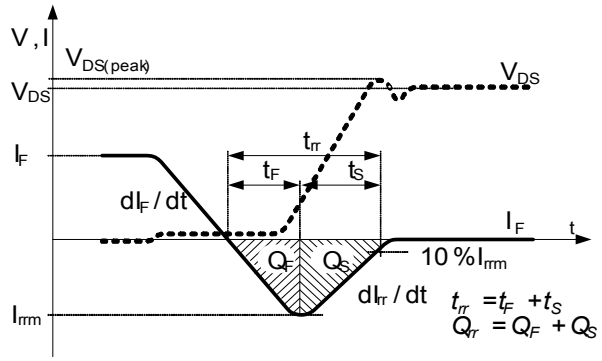
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

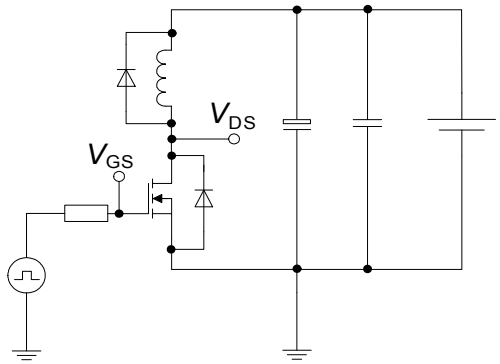
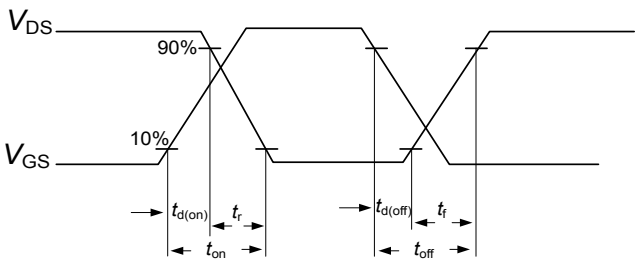
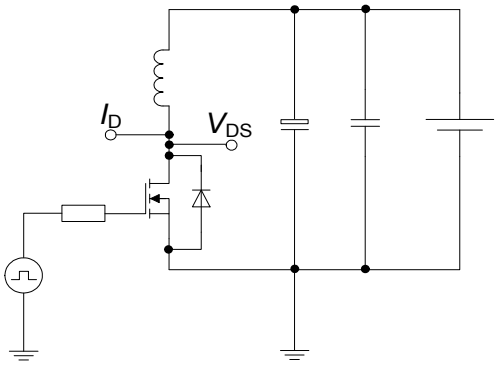
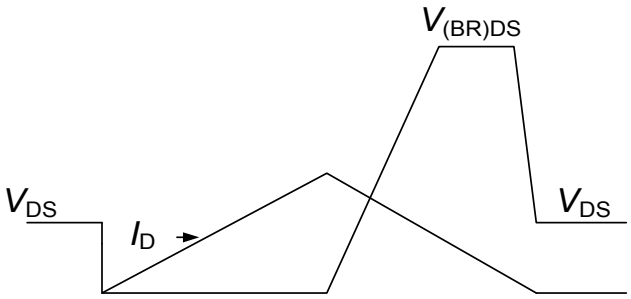
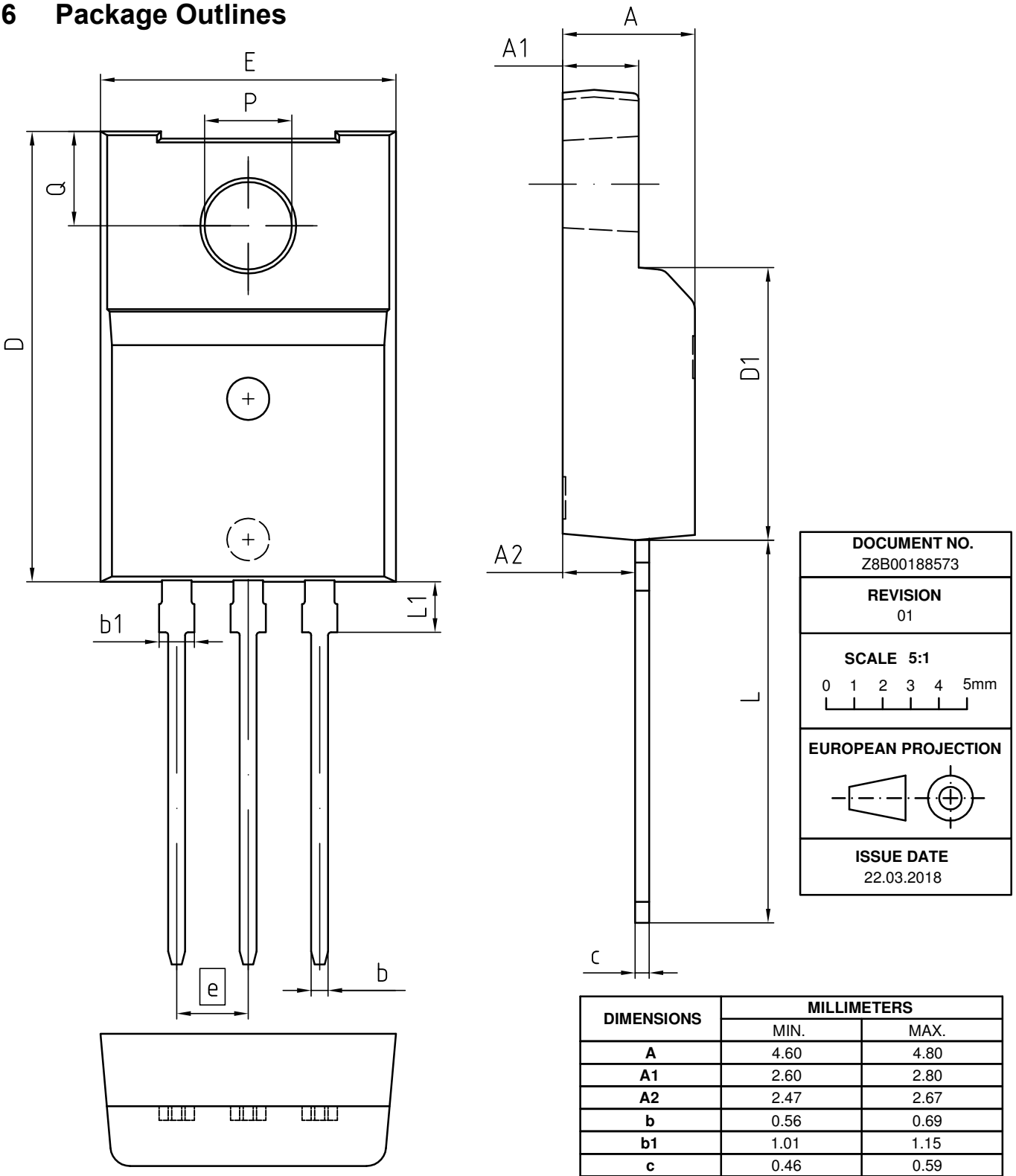
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.60	4.80
A1	2.60	2.80
A2	2.47	2.67
b	0.56	0.69
b1	1.01	1.15
c	0.46	0.59
D	15.90	16.10
D1	9.58	9.78
E	10.40	10.60
e	2.54	
N	3	
L	13.45	13.75
L1	1.70	1.91
øP	3.00	3.20
Q	3.25	3.45

Figure 1 Outline PG-TO 220 FullPAK - Narrow Lead, dimensions in mm

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPAN65R650CE

Revision: 2018-04-30, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-04-27	Release of final version
2.1	2016-11-28	Revised package drawing on page 11
2.2	2018-04-30	Revised package drawing

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