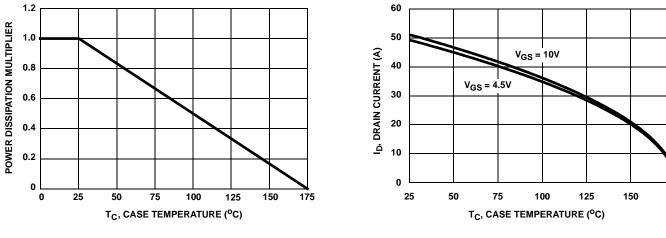
PARAMETER	SYMBOL	TES	T CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS	•	+		+	+	+	
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)		100	-	-	V
		$I_D = 250 \mu A, V_{GS} = 0$	0V , T _C = -40 ^o C (Figure 12)	90	-	-	V
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 95V, V_{GS} = 0$	V	-	-	1	μΑ
		$V_{DS} = 90V, V_{GS} = 0$	DV, T _C = 150 ^o C	-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	$V_{GS} = \pm 16V$		-	-	±100	nA
ON STATE SPECIFICATIONS						1	
Gate to Source Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_D = 25$	1	-	3	V	
Drain to Source On Resistance	rDS(ON)	I _D = 51A, V _{GS} = 10	V (Figures 9, 10)	-	0.023	0.026	Ω
THERMAL SPECIFICATIONS		TO 202			1	0.00	90.04
Thermal Resistance Junction to Case	R _{0JC}	TO-263		-	-	0.83	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	62	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} =	= 4.5V)						
Turn-On Time	tON	$V_{DD} = 50V, I_D = 34$		-	-	336	ns
Turn-On Delay Time	^t d(ON)	V _{GS} = 4.5V, R _{GS} = 12Ω _ (Figures 15, 21, 22) _		-	17	-	ns
Rise Time	t _r			-	207	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	83	-	ns
Fall Time	t _f			-	136	-	ns
Turn-Off Time	^t OFF		-	-	328	ns	
SWITCHING SPECIFICATIONS (V _{GS} =	= 10V)						
Turn-On Time	tON	$V_{DD} = 50V, I_D = 51A V_{GS} = 10V, R_{GS} = 12\Omega (Figures 16, 21, 22)$		-	-	96	ns
Turn-On Delay Time	t _{d(ON)}			-	10	-	ns
Rise Time	t _r			-	55	-	ns
Turn-Off Delay Time	t _{d(OFF)}	_		-	151	-	ns
Fall Time	t _f	1		-	110	-	ns
Turn-Off Time	tOFF		-	-	392	ns	
GATE CHARGE SPECIFICATIONS	1	1		<u> </u>	1	1	1
Total Gate Charge	Q _{g(TOT)}	$V_{GS} = 0V$ to 10V	V _{DD} = 50V,	-	71	86	nC
Gate Charge at 5V	Q _{g(5)}	$V_{GS} = 0V \text{ to } 5V$	I _D = 35A, I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	39	47	nC
Threshold Gate Charge	Q _{g(TH)}	$V_{GS} = 0V$ to 1V		-	2.0	2.4	nC
Gate to Source Gate Charge	Q _{gs}	(,,,,	-	6	-	nC	
Gate to Drain "Miller" Charge	Q _{gd}	1		-	19	-	nC
CAPACITANCE SPECIFICATIONS	. <u> </u>	1	1	L	1	1	ı
Input Capacitance	C _{ISS}	$V_{DS} = 25V, V_{GS} = 0$	-	2400	-	pF	
Output Capacitance	C _{OSS}	f = 1MHz	-	520	-	pF	
Reverse Transfer Capacitance	C _{RSS}	(Figure 13)		140		pF	

Electrical Specifications $T_C = 25^{\circ}C$, Unless Otherwise Specified

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V _{SD}	I _{SD} = 35A	-	-	1.25	V
		I _{SD} = 15A	-	-	1.0	V
Reverse Recovery Time	t _{rr}	I _{SD} = 35A, dI _{SD} /dt = 100A/μs	-	-	137	ns
Reverse Recovered Charge	Q _{RR}	I _{SD} = 35A, dI _{SD} /dt = 100A/μs	-	-	503	nC

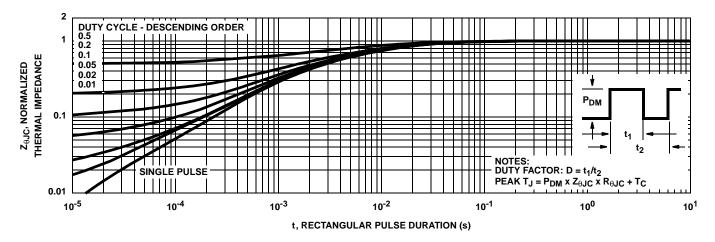
Typical Performance Curves

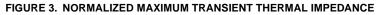


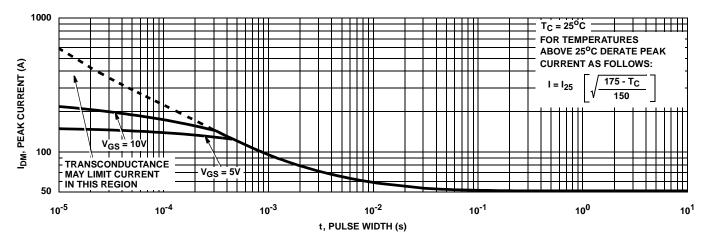




175









www.onsemi.com 3

Typical Performance Curves (Continued)

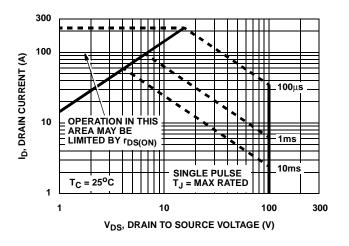


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

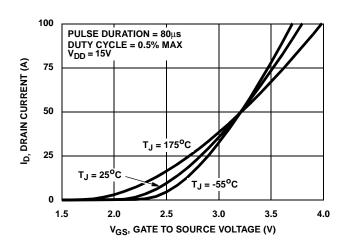


FIGURE 7. TRANSFER CHARACTERISTICS

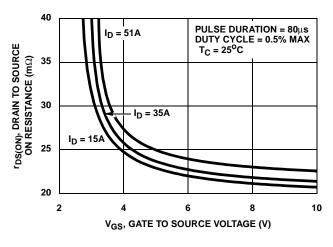


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

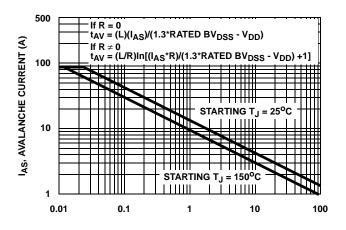


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

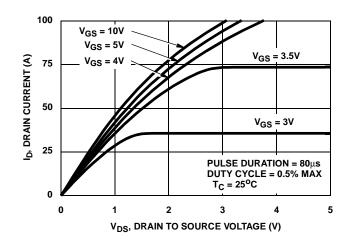
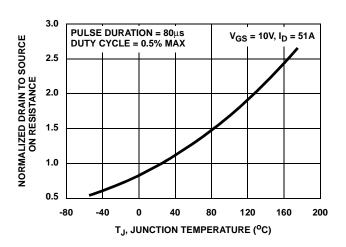
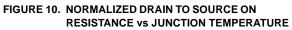


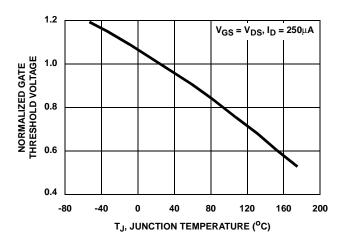
FIGURE 8. SATURATION CHARACTERISTICS





www.onsemi.com 4

Typical Performance Curves (Continued)





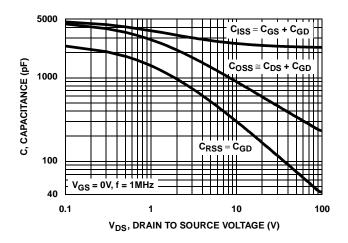


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

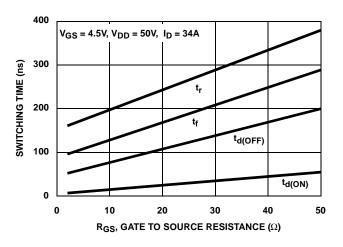


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

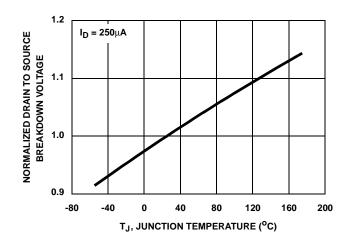


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

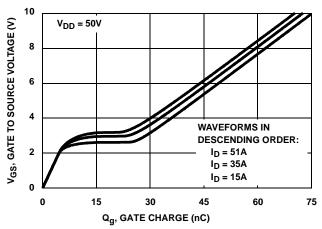
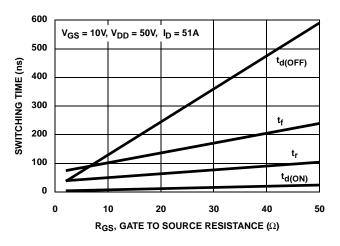


FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT

GATE CURRENT





www.onsemi.com 5

Test Circuits and Waveforms

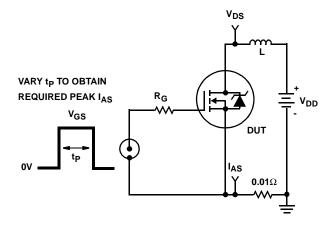


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

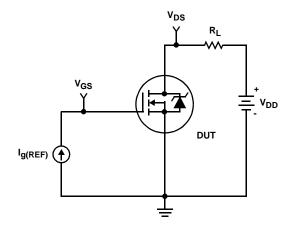


FIGURE 19. GATE CHARGE TEST CIRCUIT

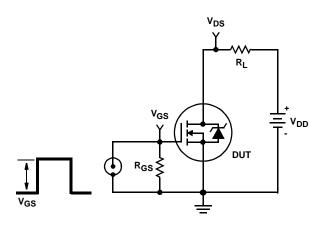


FIGURE 21. SWITCHING TIME TEST CIRCUIT

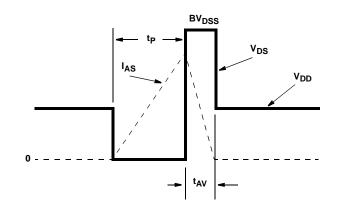


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

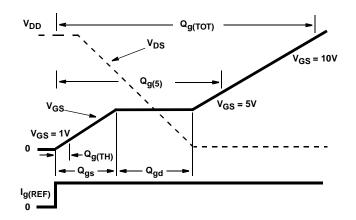


FIGURE 20. GATE CHARGE WAVEFORMS

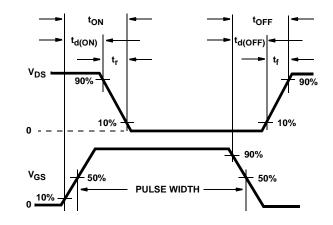


FIGURE 22. SWITCHING TIME WAVEFORM

6

SOURCE

<u>ი</u> 3

PSPICE Electrical Model

.SUBCKT HUF76639 2 1 3 ; rev 26 July 1999

CA 12 8 4.2e-9 CB 15 14 4.2e-9 CIN 6 8 2.27e-9 DBODY 7 5 DBODYMOD DBREAK 5 11 DBREAKMOD LDRAIN **DPLCAP 10 5 DPLCAPMOD** DPLCAP 5 EBREAK 11 7 17 18 118.2 10 EDS 148581 RLDRAIN **≷RSLC**1 EGS 138681 DBREAK ESG 6 10 6 8 1 51 RSLC2 EVTHRES 6 21 19 8 1 5 EVTEMP 20 6 18 22 1 ESLC 11 IT 8 17 1 50 17 18 DBODY RDRAIN LDRAIN 2 5 1.0e-9 <u>6</u> 8 EBREAK ESG LGATE 1 9 5.1e-9 EVTHRES 16 LSOURCE 3 7 3.1e-9 21 19 8 MWEAK i∢ LGATE EVTEMP MMED 16 6 8 8 MMEDMOD RGATE GATE 1[₹ 18 MSTRO 16 6 8 8 MSTROMOD MMED 1 22 9 $\mathbf{\mathcal{M}}$ 20 MWEAK 16 21 8 8 MWEAKMOD MSTRC RLGATE RBREAK 17 18 RBREAKMOD 1 LSOURCE CIN RDRAIN 50 16 RDRAINMOD 15.8e-3 8 RGATE 9 20 1.94 RSOURCE RLDRAIN 2 5 10 RLSOURCE RLGATE 1 9 51 RLSOURCE 3 7 31 S1A 5 S2A RBREAK 121 RSI C1 5 51 RSI CMOD 1e-6 <u>13</u> 8 <u>14</u> 13 15 17 18 RSLC2 5 50 1e3 RSOURCE 8 7 RSOURCEMOD 3.6e-3 S1B ∩ S2B RVTFMP **RVTHRES 22 8 RVTHRESMOD 1** 13 СВ **RVTEMP 18 19 RVTEMPMOD 1** 19 CA IT 14 **↑** S1A 6 12 13 8 S1AMOD VBAT 5 6 S1B 13 12 13 8 S1BMOD EGS EDS 8 S2A 6 15 14 13 S2AMOD 8 S2B 13 15 14 13 S2BMOD 22 RVTHRES

VBAT 22 19 DC 1

ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*99),3.5))}

.MODEL DBODYMOD D (IS = 2.6e-12 RS = 2.65e-3 IKF = 6 TRS1 = 1.5e-3 TRS2 = 3.5e-6 CJO = 2.1e-9 TT = 5.6e-8 M = 0.52) .MODEL DBREAKMOD D (RS = 2.5e-1 TRS1 = 1e-4 TRS2 = -1e-6) .MODEL DPLCAPMOD D (CJO = 2.6e-9 IS = 1e-30 M = 0.89 N = 10) .MODEL MMEDMOD NMOS (VTO = 1.77 KP = 7 IS = 1e-30 N = 10 TOX = 1 L = 1U W = 1U RG = 1.94) .MODEL MSTROMOD NMOS (VTO = 2.06 KP = 95 IS = 1e-30 N = 10 TOX = 1 L = 1U W = 1U) MODEL MWEAKMOD NMOS (VTO = 1.48 KP = 0.12 IS = 1e-30 N = 10 TOX = 1 L = 1U W = 1U RG = 19.4 RS = .1) .MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = -5e-7) .MODEL RDRAINMOD RES (TC1 = 8.5e-3 TC2 = 2.3e-5) .MODEL RSLCMOD RES (TC1 = 3.4e-3 TC2 = 2.5e-6) MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6) .MODEL RVTHRESMOD RES (TC1 = -1.9e-3 TC2 = -4.5e-6) .MODEL RVTEMPMOD RES (TC1 = -1.7e-3 TC2 = 1.5e-6) .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.5 VOFF = -2.0) .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF = -4.5) .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF = 0.3) .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.3 VOFF = -0.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 26 July 1999 template huf76639 n2,n1,n3 electrical n2,n1,n3 var i iscl d..model dbodymod = (is = 2.6e-12, cjo = 2.1e-9, tt = 5.6e-8, m = 0.52, n=10) d..model dbreakmod = () d..model dplcapmod = (cjo = 2.6e-9, is = 1e-30, m = 0.89)m..model mmedmod = (type=_n, vto = 1.77, kp = 7, is = 1e-30, tox = 1) m..model mstrongmod = (type=_n, vto = 2.06,kp = 95, is = 1e-30, tox = 1) m..model mweakmod = (type=_n, vto = 1.48, kp = 0.12, is = 1e-30, tox = 1) LDRAIN sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -4.5, voff = -2.0) DPLCAP 5 DRAIN sw vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -2.0, voff = -4.5) o 2 10 $sw_vcsp...model s2amod = (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0.3)$ RLDRAIN sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.3, voff = -0.5) RSLC1 RDBREAK 51 c.ca n12 n8 = 4.2e-9 RSLC2 ₹ 72 c.cb n15 n14 = 4.2e-9 RDBODY ISCL c.cin n6 n8 = 2.27e-9 DBREAK 50 d.dbody n7 n71 = model = dbodymod 71 d.dbreak n72 n11 = model = dbreakmod 6 8 ESG 11 d.dplcap n10 n5 = model = dplcapmod EVTHRES 16 21 19 8 MWEAK i.it n8 n17 = 1 i∙ LGATE EVTEMP DBODY RGATE GATE 6 18 22 EBREAK I.Idrain n2 n5 = 1.0e-9 MMED i∙ 1 0 9 \sim 20 1.10ate n1 n9 = 5.1e-9MSTR RLGATE l.lsource n3 n7 = 3.1e-9 LSOURCE CIN SOURCE 8 m.mmed n16 n6 n8 n8 = model = mmedmod, I = 1u, w = 1u 3 m.mstrong n16 n6 n8 n8 = model = mstrongmod, I = 1u, w = 1u RSOURCE m.mweak n16 n21 n8 n8 = model = mweakmod, I = 1u, w = 1u RLSOURCE os2A S1A res.rbreak n17 n18 = 1, tc1 = 1.05e-3, tc2 = -5e-7 RBREAK <u>13</u> 8 <u>14</u> 13 15 res.rdbody n71 n5 = 2.65e-3, tc1 = 1.5e-3, tc2 = 3.5e-6 17 18 res.rdbreak n72 n5 = 2.5e-1, tc1 = 1e-4, tc2 = -1e-6 RVTEMP res.rdrain n50 n16 = 15.8e-3, tc1 = 8.5e-3, tc2 = 2.3e-5 o S2B S1B res.rgate n9 n20 = 1.94 13 СВ 19 CA res.rldrain n2 n5 = 10 IT (♠ 14 res.rlgate n1 n9 = 51 VBAT <u>6</u> 8 res.rlsource n3 n7 = 31 5 EGS EDS res.rslc1 n5 n51 = 1e-6, tc1 = 3.4e-3, tc2 = 2.5e-6 8 res.rslc2 n5 n50 = 1e3 22 res.rsource n8 n7 = 3.6e-3, tc1 = 1e-3, tc2 = 1e-6 RVTHRES res.rvtemp n18 n19 = 1, tc1 = -1.7e-3, tc2 = 1.5e-6 res.rvthres n22 n8 = 1, tc1 = -1.9e-3, tc2 = -4.5e-6 spe.ebreak n11 n7 n17 n18 = 118.2 spe.eds n14 n8 n5 n8 = 1 spe.eqs n13 n8 n6 n8 = 1 spe.esg n6 n10 n6 n8 = 1 spe.evtemp n20 n6 n18 n22 = 1 spe.evthres n6 n21 n19 n8 = 1 sw_vcsp.s1a n6 n12 n13 n8 = model = s1amod sw_vcsp.s1b n13 n12 n13 n8 = model = s1bmod sw_vcsp.s2a n6 n15 n14 n13 = model = s2amod sw_vcsp.s2b n13 n15 n14 n13 = model = s2bmod v.vbat n22 n19 = dc = 1 equations { i(n51 - n50) + = iscliscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/99))** 3.5))

SPICE Thermal Model

REV 26 July 1999

HUF76639T

CTHERM1 th 6 3.2e-3 CTHERM2 6 5 8.5e-3 CTHERM3 5 4 1.2e-2 CTHERM4 4 3 1.6e-2 CTHERM5 3 2 5.5e-2 CTHERM6 2 tl 1.5

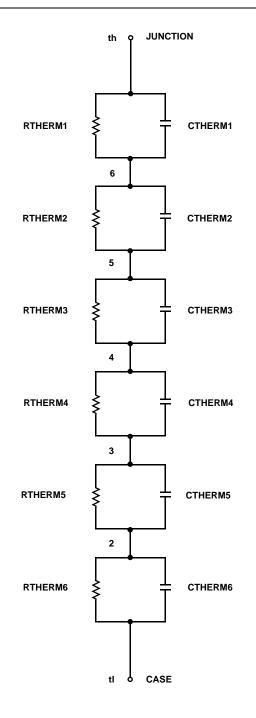
RTHERM1 th 6 8.0e-3 RTHERM2 6 5 6.8e-2 RTHERM3 5 4 9.2e-2 RTHERM4 4 3 2.0e-1 RTHERM5 3 2 2.4e-1 RTHERM6 2 tl 5.2e-2

SABER Thermal Model

SABER thermal model HUF76639T

template thermal_model th tl thermal_c th, tl { ctherm.ctherm1 th 6 = 3.2e-3 ctherm.ctherm2 6 5 = 8.5e-3 ctherm.ctherm3 5 4 = 1.2e-2 ctherm.ctherm4 4 3 = 1.6e-2 ctherm.ctherm5 3 2 = 5.5e-2 ctherm.ctherm6 2 tl = 1.5 rtherm.rtherm1 th 6 = 8.0e-3 rtherm.rtherm2 6 5 = 6.8e-2

rtherm.rtherm2 6 5 = 6.8e-2 rtherm.rtherm3 5 4 = 9.2e-2 rtherm.rtherm4 4 3 = 2.0e-1 rtherm.rtherm5 3 2 = 2.4e-1 rtherm.rtherm6 2 tl = 5.2e-2 }



ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at <u>www.onsemi.com/site/pdf/Patent-Marking.pdf</u>. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor haves against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death a

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com N. American Technical Support: 800–282–9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910

Japan Customer Focus Center Phone: 81-3-5817-1050 ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

Semiconductor Components Industries, LLC