


**54 dB, LOGARITHMIC
DETECTOR / CONTROLLER, 50 - 8000 MHz**
Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Down (EN) Input					
Voltage Range for Normal Mode		0.8 x Vcc	Vcc/2		V
Voltage Range for Powerdown Mode			Vcc/2	0.2 x Vcc	V
Power Supply (Vcc)					
Operating Voltage Range			2.7 - 5.5		V
Supply Current in Normal Mode	EN Input at Vcc		17		mA
Supply Current in Power Down Mode	EN Input at GND		0.4		mA
OUTP Output					
Rise Time	CLPF= 0, No Power to -10 dBm, 10% - 90%		24		ns
Fall Time	CLPF= 0, -10 dBm to No Power, 90% - 10%		36		ns
Output Video BW	50mV reduction in output voltage swing (3 dB referred to the input) ^[1]		16		MHz
Voltage Range	Closed Loop (Eval Board Setup)		0.2 - 1.2		V
Voltage Range	Open Loop		0.1 to (Vcc -0.1)		V
Current Drive Source / Sink			4.2 / 0.48		mA
OUTN Output					
Current Drive Source / Sink			4.0 / 0.43		mA
Output Voltage Range			0.2 - 2.1		V
RF Input					
Input Return Loss (S11)	F= 50 MHz to 8 GHz Z ₀ = 50Ω, See plot		10		dB
VSET Input					
Input Impedance			1		MΩ
Input Voltage Range	Eval Board		0.2 - 1.2		V
Low Frequency Gain	VSET to OUTP		64		dB
Open Loop Corner Frequency			11		kHz

[1] Two tone test: Frequency = 900 MHz, Tone 1 Power = -20 dBm, Tone 2 Power = -28 dBm

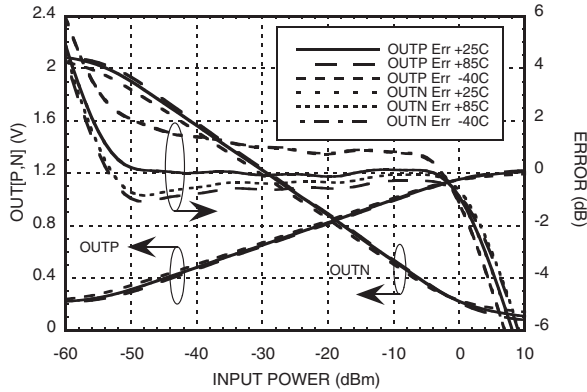
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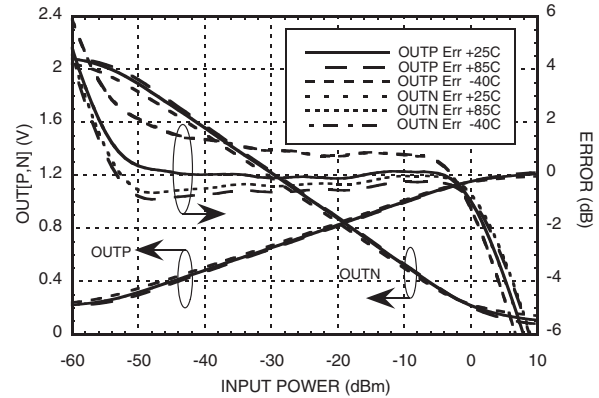


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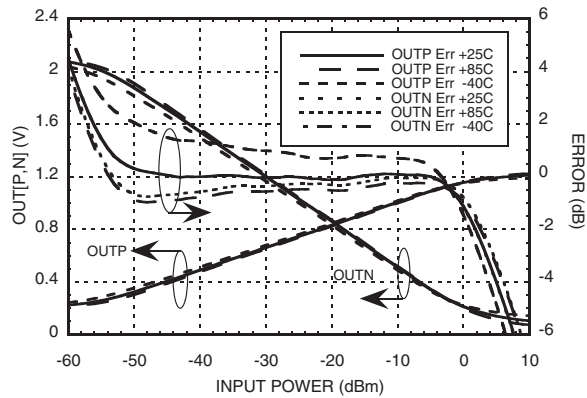
**Output Voltage & Error
vs. Input Power, $f_{in} = 50$ MHz**



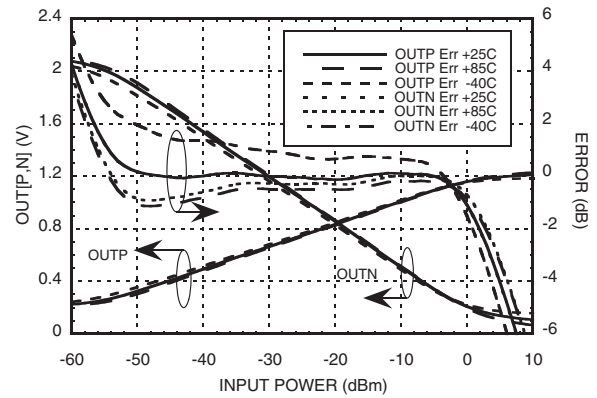
**Output Voltage & Error
vs. Input Power, $f_{in} = 100$ MHz**



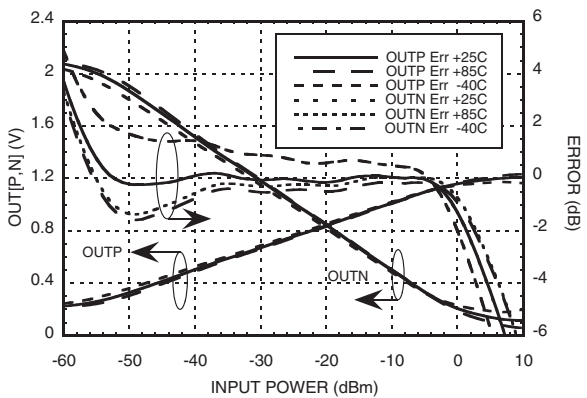
**Output Voltage & Error
vs. Input Power, $f_{in} = 500$ MHz**



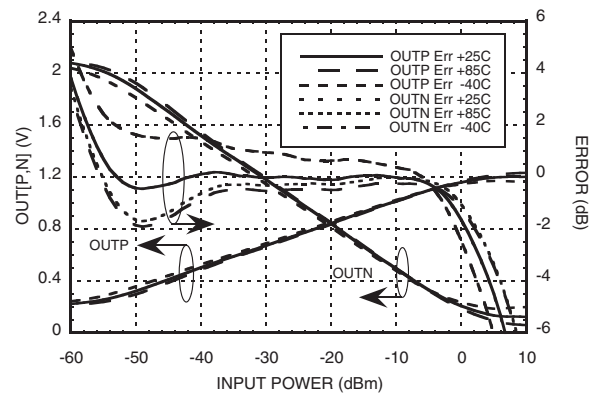
**Output Voltage & Error
vs. Input Power, $f_{in} = 900$ MHz**



**Output Voltage & Error
vs. Input Power, $f_{in} = 1900$ MHz**



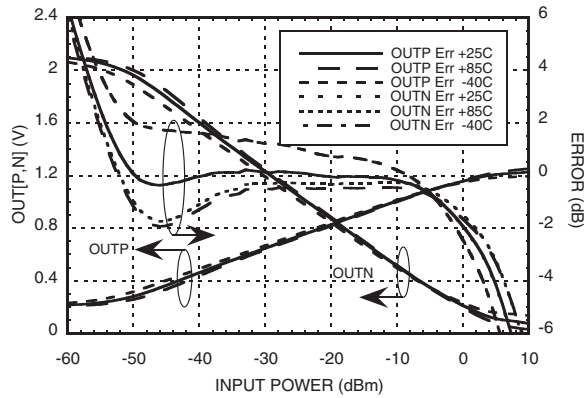
**Output Voltage & Error
vs. Input Power, $f_{in} = 2700$ MHz**



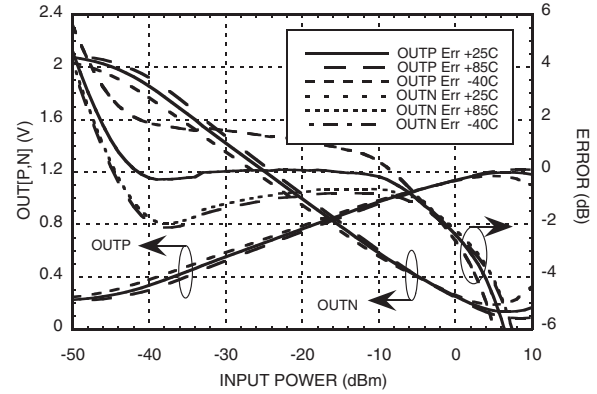


**54 dB, LOGARITHMIC
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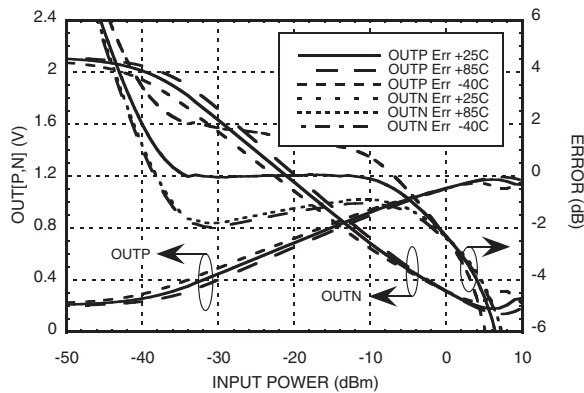
**Output Voltage & Error
vs. Input Power, $F_{in} = 3900$ MHz**



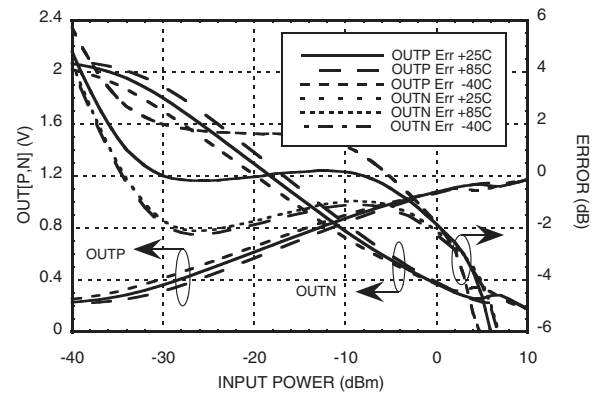
**Output Voltage & Error
vs. Input Power, $F_{in} = 5800$ MHz**



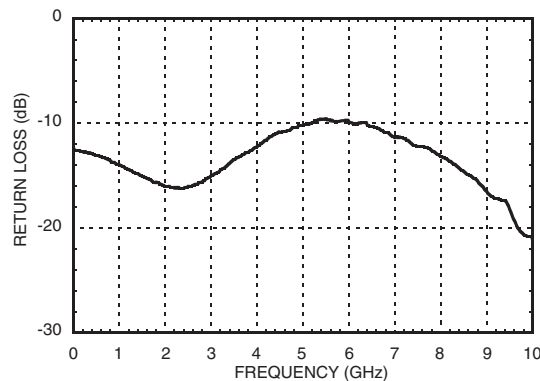
**Output Voltage & Error
vs. Input Power, $F_{in} = 7000$ MHz**

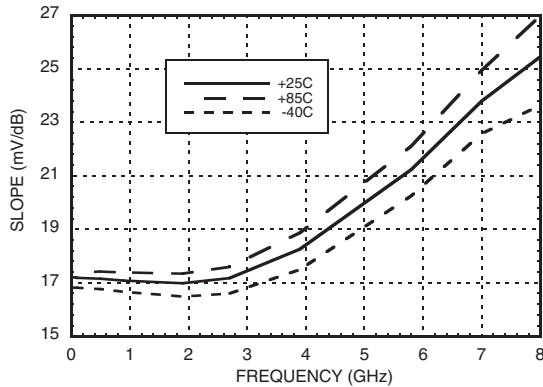
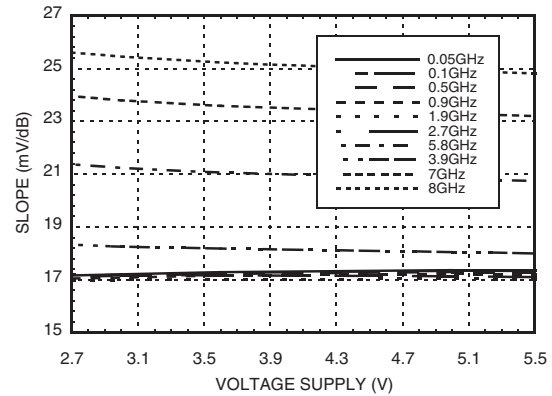
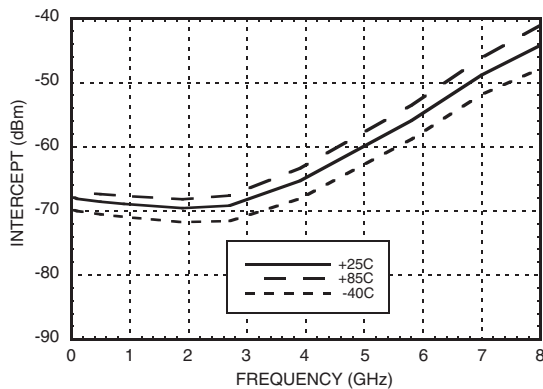
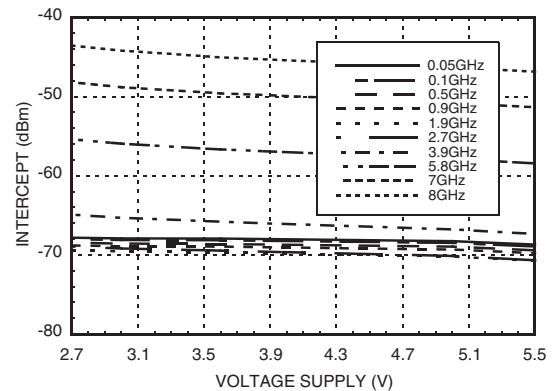
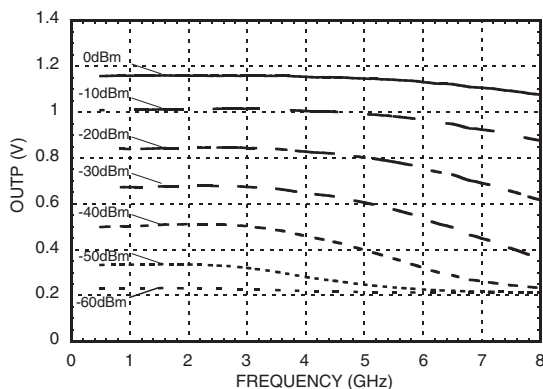
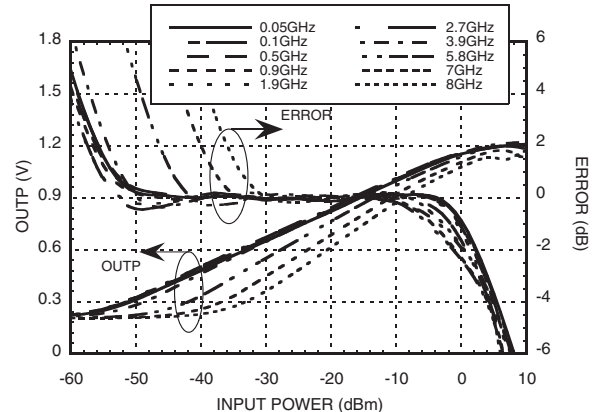


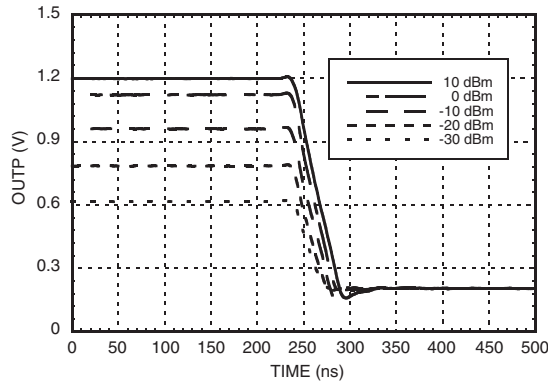
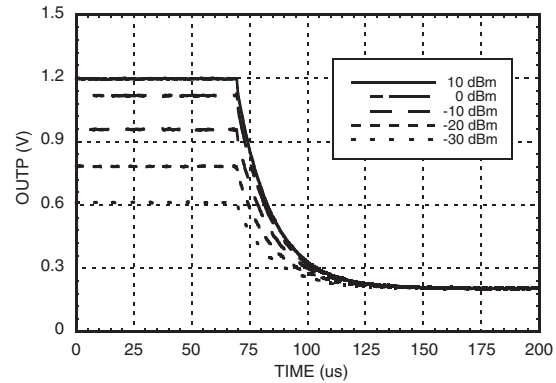
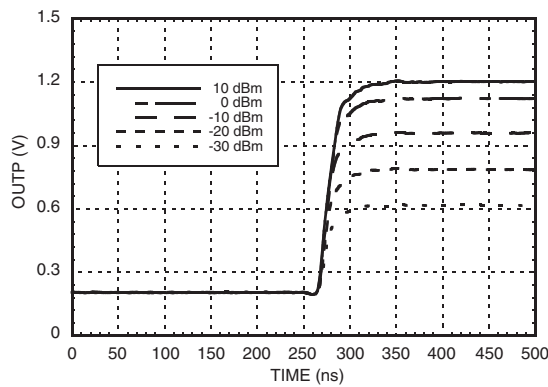
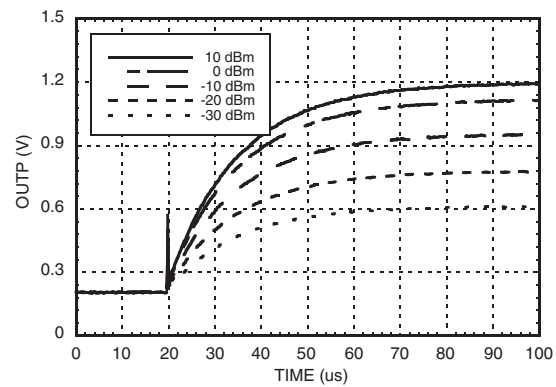
**Output Voltage & Error
vs. Input Power, $F_{in} = 8000$ MHz**



Input Return Loss



**54 dB, LOGARITHMIC
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OUTP Slope vs. Frequency

OUTP Slope vs. Supply Voltage

OUTP Intercept vs. Frequency

OUTP Intercept vs. Supply Voltage

OUTP vs. Frequency & Input Power

OUTP Voltage & Error vs. Frequency


Output Response ^[1] Fall Time C1 = Open

Output Response Fall Time ^[1] C1 = 10nF

Output Response Rise Time ^[1] C1 = Open

Output Response Rise Time ^[1] C1 = 10nF


[1] 900 MHz, Switched CW-Tone

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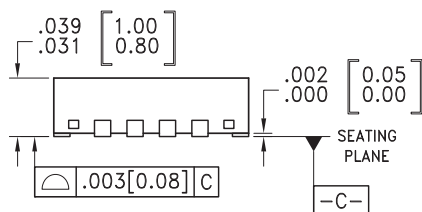
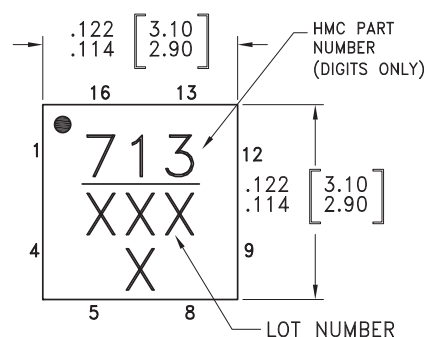
Absolute Maximum Ratings

Vcc	0 to +5.6V
EN Input Voltage	0 to +5.6V
VSET Input Voltage	0 to +5.6V
OUTP Output Current	5 mA
OUTN Output Current	5 mA
RF Input Power	12 dBm
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 5.43 mW/°C above 85°C)	0.22 Watts
Thermal Resistance (R _{th}) (junction to lead)	184 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1C

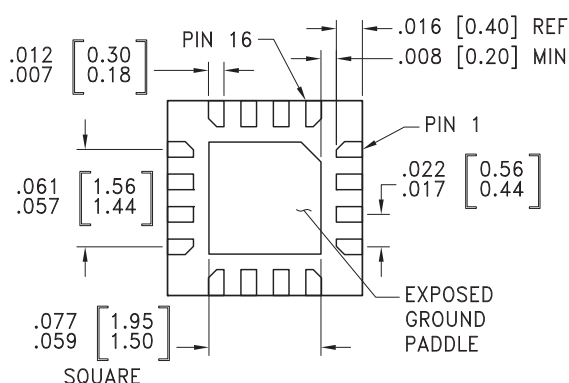


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



BOTTOM VIEW



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE
MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[1]
HMC713LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	713 XXXX

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C


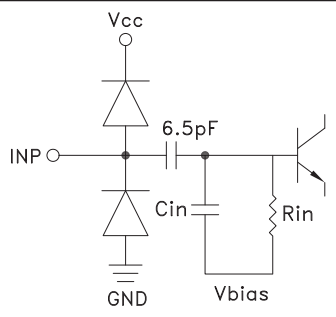
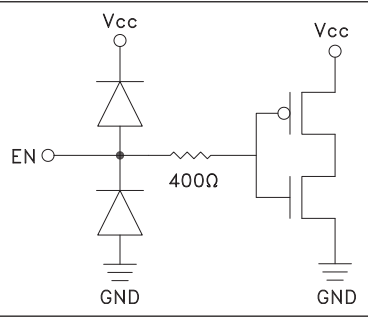
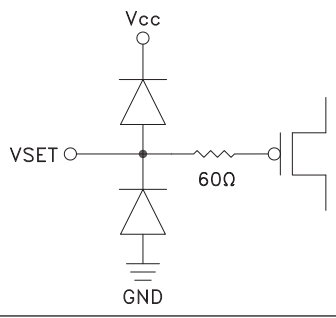
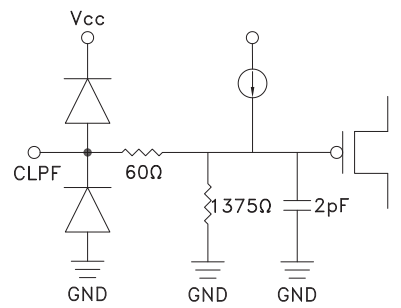
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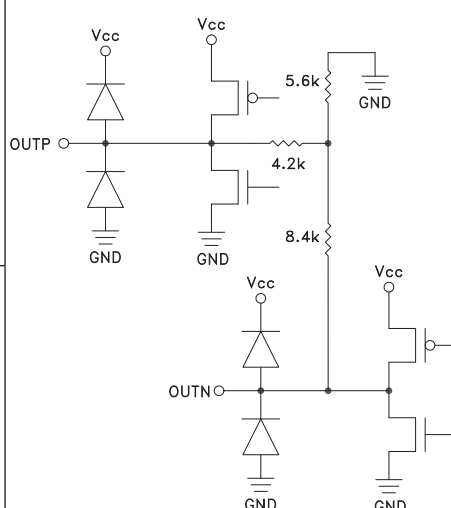
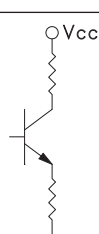


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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4	N/C	These pins are not connected internally.	
2, 5, 9 - 12	GND	These pins and package bottom must be connected to RF/DC ground.	
3	RFIN	RF input pin.	
6	EN	Enable pin. Apply VEN > 0.8 x Vcc for normal operation. Apply VEN < 0.2xVcc to disable the HMC713LP3E and reduce supply current to 0.4mA.	
7	VSET	Set point input for controller mode. Connect to OUTP with the resistor network shown in evaluation board drawing for detector mode.	
8	CLPF	Connection for ground referenced external lowpass filter capacitor.	

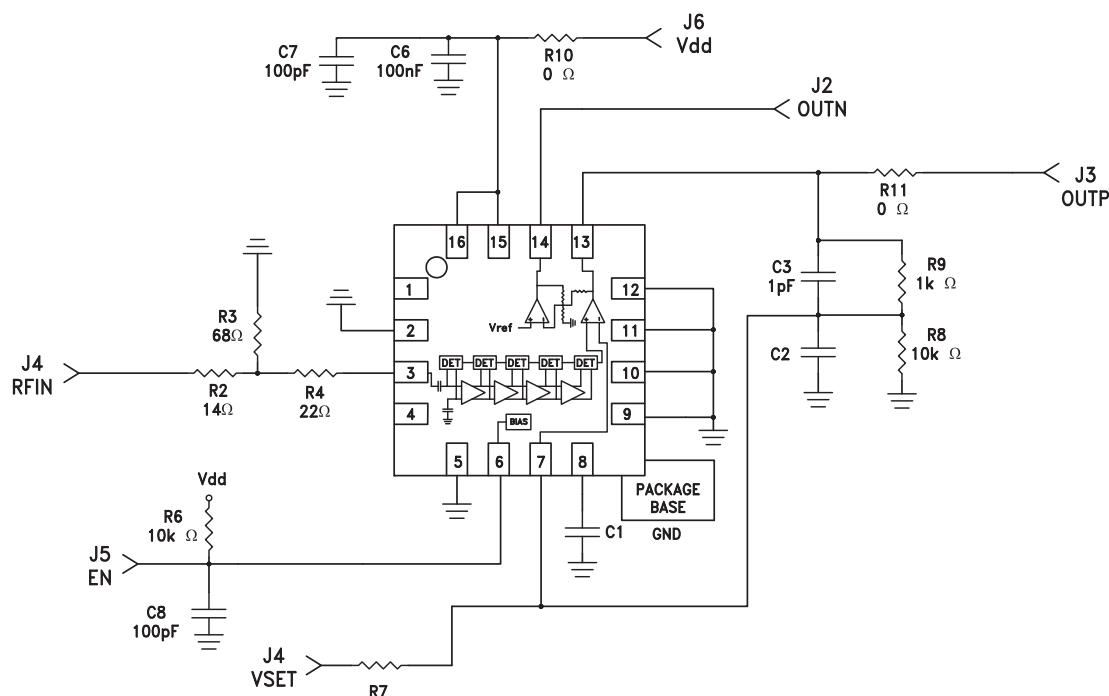

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Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
13	OUTP	Logarithmic output that converts the input power to a DC level in controller mode. Output voltage increases with increasing amplitude	
14	OUTN	Inverted logarithmic output. $OUTN = 2.55 - 2 \times OUTP$	
15, 16	Vcc	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	



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Application & Evaluation PCB Schematic



Notes

Note 1: The HMC713LP3E evaluation board is pre-assembled for single-ended input, and detector/RSSI mode.

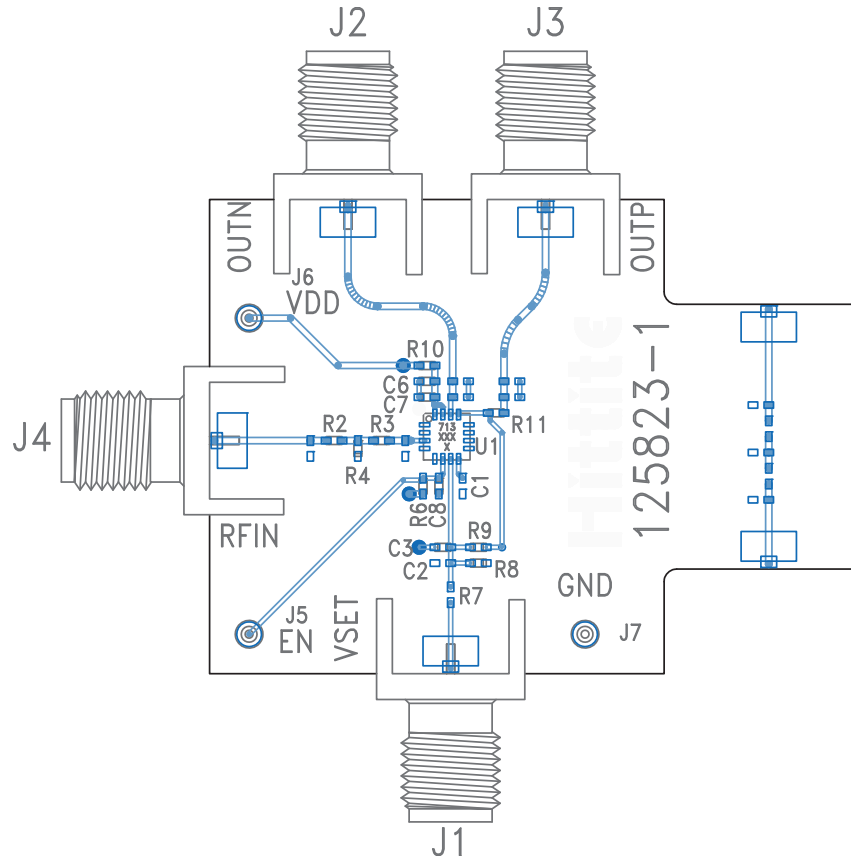
Note 2: For detector mode, connect high impedance volt meter to the OUTP / OUTN port.

Note 3: For controller mode, remove R9 & C3 and install 1k Ω resistor (R7, not included) and 100pF capacitor (C2, not included), then make appropriate connection to OUTP and VSET. In controller mode, the OUTP / OUTN output can be used to drive a variable gain amplifier, or a variable attenuator, either directly or through a buffer or microcontroller. VSET should be connected to an external supply, typically between +0.2 and +1.2V.

Note 4: An external capacitance C1 can be connected to CLPF port for additional filtering of OUTP and OUTN outputs..



Evaluation PCB



List of Materials for Evaluation PCB 125825 ^[1]

Item	Description
J1 - J4	PC Mount SMA Connector
J5 - J7	DC Pin
C3	1 pF Capacitor, 0402 Pkg.
C6	0.1 μ F Capacitor, 0402 Pkg.
C7, C8	100 pF Capacitor, 0402 Pkg.
R2	14 Ω Resistor, 0402 Pkg.
R3	68 Ω Resistor, 0402 Pkg.
R4	22 Ω Resistor, 0402 Pkg.
R6, R8	10k Ω Resistor, 0402 Pkg.
R9	1k Ω Resistor, 0402 Pkg.
R10, R11	0 Ω Resistor, 0402 Pkg.
U1	HMC713LP3E Logarithmic Amplifier
PCB ^[2]	125823 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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