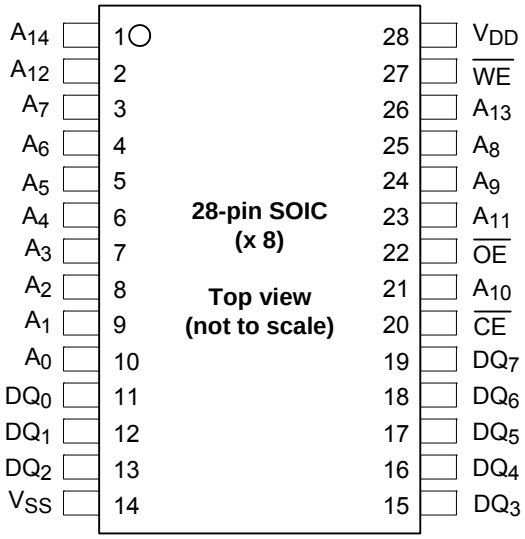
Contents

Pinout

Figure 1. 28-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
A_{14}–A_0	Input	**Address inputs**: The 15 address lines select one of 32,768 bytes in the F-RAM array.
DQ_7–DQ_0	Input/Output	**Data I/O Lines**: 8-bit bidirectional data bus for accessing the F-RAM array.
$\overline{WE}$	Input	**Write Enable**: A write cycle begins when $\overline{WE}$ is asserted. Asserting $\overline{WE}$ LOW causes the FM18W08 to write the contents of the data bus to the address location latched by the falling edge of $\overline{CE}$.
$\overline{CE}$	Input	**Chip Enable**: The device is selected when $\overline{CE}$ is LOW. Asserting $\overline{CE}$ LOW causes the address to be latched internally. Address changes that occur after $\overline{CE}$ goes LOW will be ignored until the next falling edge occurs.
$\overline{OE}$	Input	**Output Enable**: When $\overline{OE}$ is LOW, the FM18W08 drives the data bus when the valid read data is available. Deasserting $\overline{OE}$ HIGH tristates the DQ pins.
V_{SS}	Ground	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.
NC	No connect	No connect. This pin is not connected to the die.

Device Operation

The FM18W08 is a bytewide F-RAM memory logically organized as 32,768 × 8 and accessed using an industry-standard parallel interface. All data written to the part is immediately nonvolatile with no delay. Functional operation of the F-RAM memory is the same as SRAM type devices, except the FM18W08 requires a falling edge of $\overline{CE}$ to start each memory cycle. See the Functional Truth Table on page 13 for a complete description of read and write modes.

Memory Architecture

Users access 32,768 memory locations, each with 8 data bits through a parallel interface. The complete 15-bit address specifies each of the 8,192 bytes uniquely. The F-RAM array is organized as 4092 rows of 8-bytes each. This row segmentation has no effect on operation, however the user can group data into blocks by its endurance characteristics as explained in the Endurance section.

The cycle time is the same for read and write memory operations. This simplifies memory controller logic and timing circuits. Likewise the access time is the same for read and write memory operations. When $\overline{CE}$ is deasserted HIGH, a pre-charge operation begins, and is required of every memory cycle. Thus unlike SRAM, the access and cycle times are not equal. Writes occur immediately at the end of the access with no delay. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed.

It is the user's responsibility to ensure that V_{DD} remains within datasheet tolerances to prevent incorrect operation. Also proper voltage level and timing relationships between V_{DD} and $\overline{CE}$ must be maintained during power-up and power-down events. See "Power Cycle Timing" on page 12.

Memory Operation

The FM18W08 is designed to operate in a manner similar to other bytewide memory products. For users familiar with BBSRAM, the performance is comparable but the bytewide interface operates in a slightly different manner as described below. For users familiar with EEPROM, the differences result from the higher write performance of F-RAM technology including NoDelay writes and much higher write endurance.

Read Operation

A read operation begins on the falling edge of $\overline{CE}$. At this time, the address bits are latched and a memory cycle is initiated. Once started, a full memory cycle must be completed internally even if $\overline{CE}$ goes inactive. Data becomes available on the bus after the access time is met.

After the address has been latched, the address value may be changed upon satisfying the hold time parameter. Unlike an SRAM, changing address values will have no effect on the memory operation after the address is latched.

The FM18W08 will drive the data bus when $\overline{OE}$ is asserted LOW and the memory access time is met. If $\overline{OE}$ is asserted after the memory access time is met, the data bus will be driven with valid data. If $\overline{OE}$ is asserted before completing the memory access, the data bus will not be driven until valid data is available. This feature minimizes supply current in the system by eliminating transients caused by invalid data being driven to the bus. When $\overline{OE}$ is deasserted HIGH, the data bus will remain in a HI-Z state.

Write Operation

In the FM18W08, writes occur in the same interval as reads. The FM18W08 supports both $\overline{CE}$ and $\overline{WE}$ controlled write cycles. In both cases, the address is latched on the falling edge of $\overline{CE}$.

In a $\overline{CE}$-controlled write, the $\overline{WE}$ signal is asserted before beginning the memory cycle. That is, $\overline{WE}$ is LOW when the device is activated with the chip enable. In this case, the device begins the memory cycle as a write. The FM18W08 will not drive the data bus regardless of the state of $\overline{OE}$.

In a $\overline{WE}$-controlled write, the memory cycle begins on the falling edge of $\overline{CE}$. The $\overline{WE}$ signal falls after the falling edge of $\overline{CE}$. Therefore, the memory cycle begins as a read. The data bus will be driven according to the state of $\overline{OE}$ until $\overline{WE}$ falls. The $\overline{CE}$ and $\overline{WE}$ controlled write timing cases are shown in the page 12.

Write access to the array begins asynchronously after the memory cycle is initiated. The write access terminates on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever comes first. A valid write operation requires the user to meet the access time specification before deasserting $\overline{WE}$ or $\overline{CE}$. The data setup time indicates the interval during which data cannot change before the end of the write access.

Unlike other nonvolatile memory technologies, there is no write delay with F-RAM. Because the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data polling, a technique used with EEPROMs to determine if a write is complete, is unnecessary.

Pre-charge Operation

The pre-charge operation is an internal condition in which the memory state is prepared for a new access. All memory cycles consist of a memory access and a pre-charge. Pre-charge is user-initiated by driving the $\overline{CE}$ signal HIGH. It must remain HIGH for at least the minimum pre-charge time, t_{PC}.

The user determines the beginning of this operation since a pre-charge will not begin until $\overline{CE}$ rises. However, the device has a maximum $\overline{CE}$ LOW time specification that must be satisfied.

Endurance

Internally, a F-RAM operates with a read and restore mechanism. Therefore, each read and write cycle involves a change of state. The memory architecture is based on an array of rows and columns. Each read or write access causes an endurance cycle for an entire row. In the FM18W08, a row is 64 bits wide. Every 8-byte boundary marks the beginning of a new row. Endurance can be optimized by ensuring frequently accessed data is located in different rows. Regardless, F-RAM

offers substantially higher write endurance than other nonvolatile memories. The rated endurance limit of 10^{14} cycles will allow 150,000 accesses per second to the same row for over 20 years.

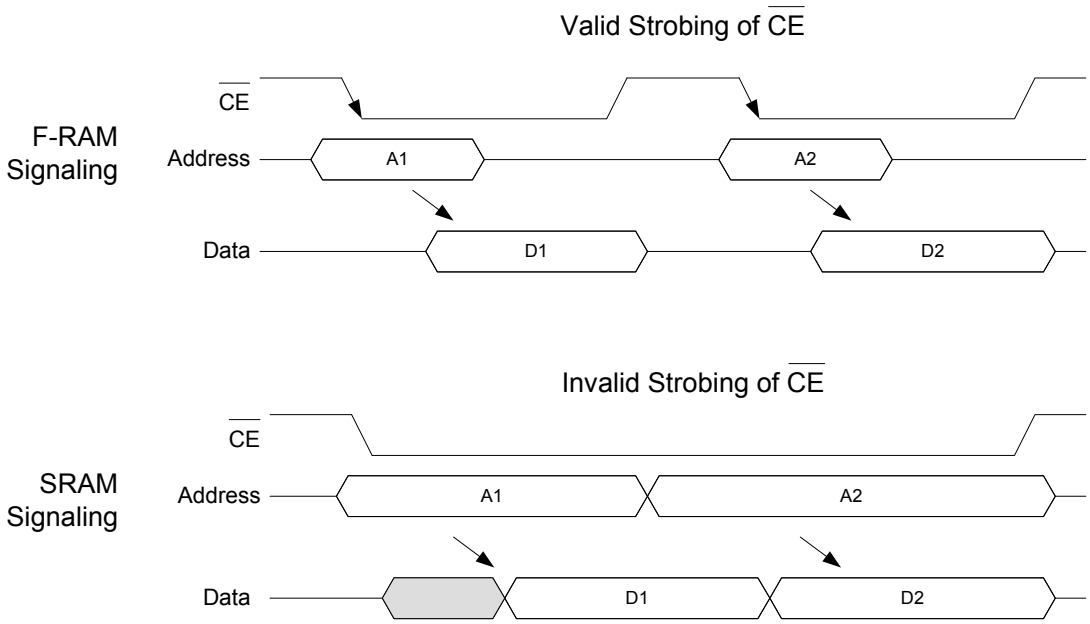
F-RAM Design Considerations

When designing with F-RAM for the first time, users of SRAM will recognize a few minor differences. First, bytewide F-RAM memories latch each address on the falling edge of chip enable. This allows the address bus to change after starting the memory access. Since every access latches the memory address on the falling edge of $\overline{CE}$, users cannot ground it as they might with SRAM.

Users who are modifying existing designs to use F-RAM should examine the memory controller for timing compatibility of address and control pins. Each memory access must be qualified with a LOW transition of $\overline{CE}$. In many cases, this is the only change required. An example of the signal relationships is shown in Figure 2 below. Also shown is a common SRAM signal relationship that will not work for the FM18W08.

The reason for $\overline{CE}$ to strobe for each address is twofold: it latches the new address and creates the necessary pre-charge period while $\overline{CE}$ is HIGH.

Figure 2. Chip Enable and Memory Address Relationships

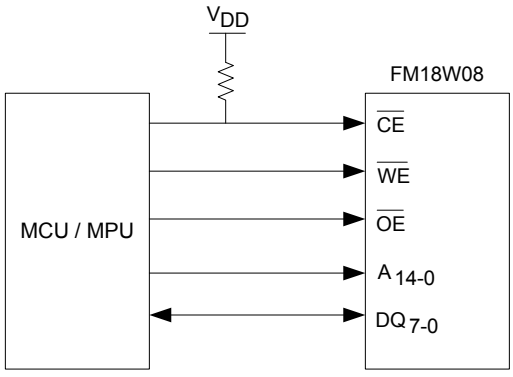


A second design consideration relates to the level of V_{DD} during operation. Battery-backed SRAMs are forced to monitor V_{DD} in order to switch to battery backup. They typically block user access below a certain V_{DD} level in order to prevent loading the battery with current demand from an active SRAM. The user can be abruptly cut off from access to the nonvolatile memory in a power down situation with no warning or indication.

F-RAM memories do not need this system overhead. The memory will not block access at any V_{DD} level that complies with the specified operating range. The user should take measures to prevent the processor from accessing memory when V_{DD} is out-of-tolerance. The common design practice of holding a processor in reset during power-down may be sufficient. It is recommended that chip enable is pulled HIGH and allowed to track V_{DD} during power-up and power-down cycles. It is the user's responsibility to ensure that chip enable is HIGH to prevent accesses below V_{DD} min. (2.7 V).

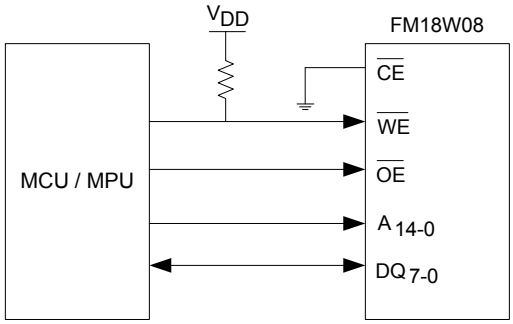
Figure 3 shows a pull-up resistor on $\overline{CE}$, which will keep the pin HIGH during power cycles, assuming the MCU / MPU pin tristates during the reset condition. The pull-up resistor value should be chosen to ensure the $\overline{CE}$ pin tracks V_{DD} to a high enough value, so that the current drawn when $\overline{CE}$ is LOW is not an issue.

Figure 3. Use of Pull-up Resistor on $\overline{CE}$



Note that if $\overline{CE}$ is tied to ground, the user must be sure $\overline{WE}$ is not LOW at power-up or power-down events. If the chip is enabled and $\overline{WE}$ is LOW during power cycles, data will be corrupted. Figure 4 shows a pull-up resistor on $\overline{WE}$, which will keep the pin HIGH during power cycles, assuming the MCU / MPU pin tristates during the reset condition. The pull-up resistor value should be chosen to ensure the $\overline{WE}$ pin tracks V_{DD} to a high enough value, so that the current drawn when $\overline{WE}$ is LOW is not an issue.

Figure 4. Use of Pull-up Resistor on $\overline{WE}$



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Maximum accumulated storage time
At 125 °C ambient temperature ..... 1000 h
At 85 °C ambient temperature ..... 10 Years

Ambient temperature
with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to + 7.0 V

Voltage applied to outputs
in High Z state ..... –0.5 V to V_{DD} + 0.5 V

Input voltage ..... –1.0 V to + 7.0 V and $V_{IN} < V_{DD}$ + 1.0 V

Transient voltage (< 20 ns) on
any pin to ground potential ..... –2.0 V to V_{CC} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) ..... 1.0 W

Surface mount Pb soldering
temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) .... 15 mA

Static discharge voltage
Human Body Model (AEC-Q100-002 Rev. E) ..... 4 kV

Charged Device Model (AEC-Q100-011 Rev. B) .. 1.25 kV

Machine Model (AEC-Q100-003 Rev. E) ..... 300 V

Latch-up current ..... > 140 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.7 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [1]	Max	Unit
V_{DD}	Power supply voltage		2.7	3.3	5.5	V
I_{DD}	V_{DD} supply current	V_{DD} = 5.5 V, $\overline{CE}$ cycling at min. cycle time. All inputs toggling at CMOS levels (0.2 V or V_{DD} – 0.2 V), all DQ pins unloaded.	–	–	12	mA
I_{SB}	Standby current	V_{DD} = 5.5 V, $\overline{CE}$ at V_{IH}, All other pins are static and at CMOS levels (0.2 V or V_{DD} – 0.2 V)	–	20	50	µA
I_{LI}	Input leakage current	V_{IN} between V_{DD} and V_{SS}	–	–	±1	µA
I_{LO}	Output leakage current	V_{OUT} between V_{DD} and V_{SS}	–	–	±1	µA
V_{IH}	Input HIGH voltage		0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage		– 0.3	–	0.3 × V_{DD}	V
V_{OH1}	Output HIGH voltage	I_{OH} = –1.0 mA, V_{DD} > 2.7 V	2.4	–	–	V
V_{OH2}	Output HIGH voltage	I_{OH} = –100 µA	V_{DD} – 0.2	–	–	V
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, V_{DD} > 2.7 V	–	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 150 µA	–	–	0.2	V

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	At +85 °C	10	–	Years
		At +75 °C	38	–	
		At +65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Note
1. Typical values are at 25 °C, V_{DD} = V_{DD} (typ). Not 100% tested.

Capacitance

Parameter	Description	Test Conditions	Max	Unit
$C_{I/O}$	Input/Output capacitance (DQ)	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(Typ)	8	pF
C_{IN}	Input capacitance		6	pF

Thermal Resistance

Parameter	Description	Test Conditions	28-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	58	°C/W
Θ_{JC}	Thermal resistance (junction to case)		26	°C/W

AC Test Conditions

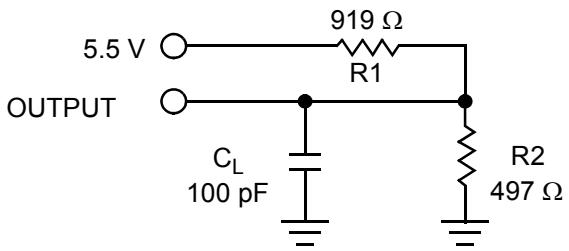
Input pulse levels .....10% and 90% of V_{DD}

Input rise and fall times (10%–90%) ..... ≤ 5 ns

Input and output timing reference levels .....0.5 V_{DD}

Output load capacitance..... 100 pF

Figure 5. AC Test Loads



AC Switching Characteristics

Over the Operating Range

Parameters [2]		Description	V_{DD} = 2.7 V to 3.0 V		V_{DD} = 3.0 V to 5.5 V		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Read Cycle							
t_{CE}	t_{ACE}	Chip enable access time	–	80	–	70	ns
t_{CA}	–	Chip enable active time	80	–	70	–	ns
t_{RC}	–	Read cycle time	145	–	130	–	ns
t_{PC}	–	Pre-charge time	65	–	60	–	ns
t_{AS}	t_{SA}	Address setup time	0	–	0	–	ns
t_{AH}	t_{HA}	Address hold time	15	–	15	–	ns
t_{OE}	t_{DOE}	Output enable access time	–	15	–	12	ns
t_{HZ}[3, 4]	t_{HZCE}	Chip Enable to output HI-Z	–	15	–	15	ns
t_{OHZ}[3, 4]	t_{HZOE}	Output enable HIGH to output HI-Z	–	15	–	15	ns

Notes
2. Test conditions assume a signal transition time of 5 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% and 90% of V_{DD}, output loading of the specified I_{OL}/I_{OH} and load capacitance shown in AC Test Conditions on page 8.
3. t_{HZ} and t_{OHZ} are specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
4. This parameter is characterized but not 100% tested.

AC Switching Characteristics (continued)

Over the Operating Range

Parameters [2]		Description	V_{DD} = 2.7 V to 3.0 V		V_{DD} = 3.0 V to 5.5 V		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	
SRAM Write Cycle							
t_{WC}	t_{WC}	Write cycle time	145	–	130	–	ns
t_{CA}	–	Chip enable active time	80	–	70	–	ns
t_{CW}	t_{SCE}	Chip enable to write enable HIGH	80	–	70	–	ns
t_{PC}	–	Pre-charge time	65	–	60	–	ns
t_{WP}	t_{PWE}	Write enable pulse width	50	–	40	–	ns
t_{AS}	t_{SA}	Address setup time	0	–	0	–	ns
t_{AH}	t_{HA}	Address hold time	15	–	15	–	ns
t_{DS}	t_{SD}	Data input setup time	40	–	30	–	ns
t_{DH}	t_{HD}	Data input hold time	0	–	0	–	ns
t_{WZ}[5, 6]	t_{HZWE}	Write enable LOW to output HI-Z	–	15	–	15	ns
t_{WX}[6]	–	Write enable HIGH to output driven	10	–	10	–	ns
t_{HZ}[5]	–	Chip enable to output HI-Z	–	15	–	15	ns
t_{WS}[7]	–	Write enable to $\overline{CE}$ LOW setup time	0	–	0	–	ns
t_{WH}[7]	–	Write enable to $\overline{CE}$ HIGH hold time	0	–	0	–	ns

Notes
5. t_{WZ} and t_{HZ} is specified with a load capacitance of 5 pF. Transition is measured when the outputs enter a high impedance state.
6. This parameter is characterized but not 100% tested.
7. The relationship between $\overline{CE}$ and $\overline{WE}$ determines if a $\overline{CE}$ or $\overline{WE}$ controlled write occurs.

Figure 6. Read Cycle Timing

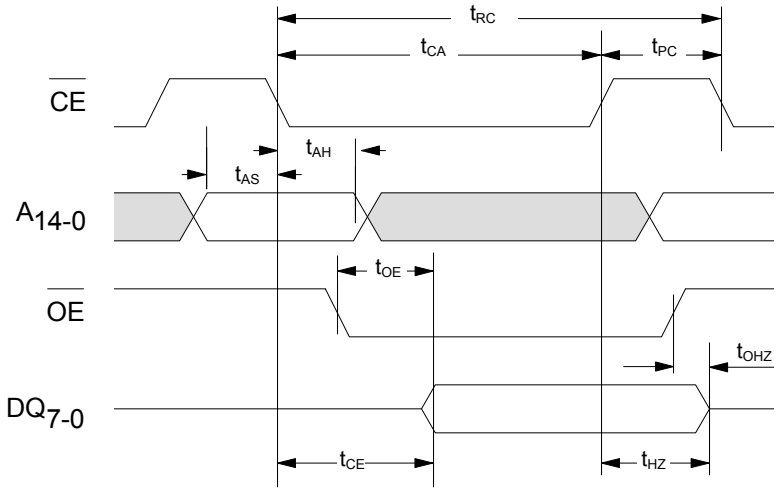


Figure 7. Write Cycle Timing 1 ($\overline{CE}$ Controlled)

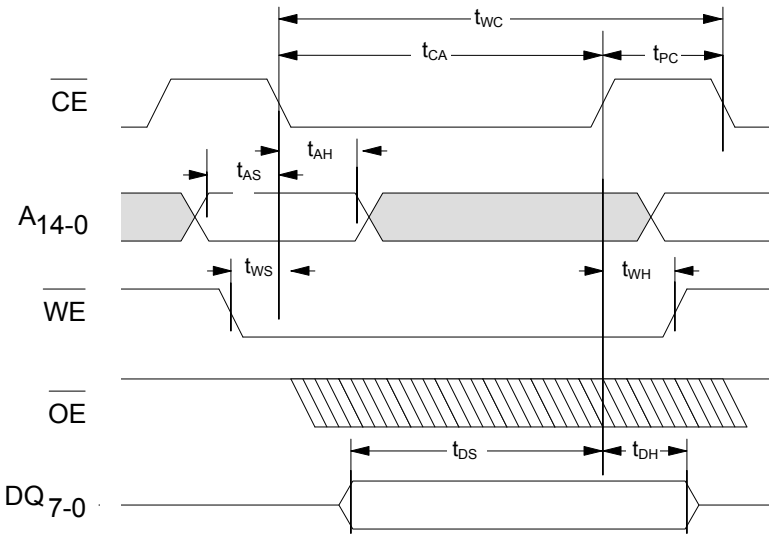
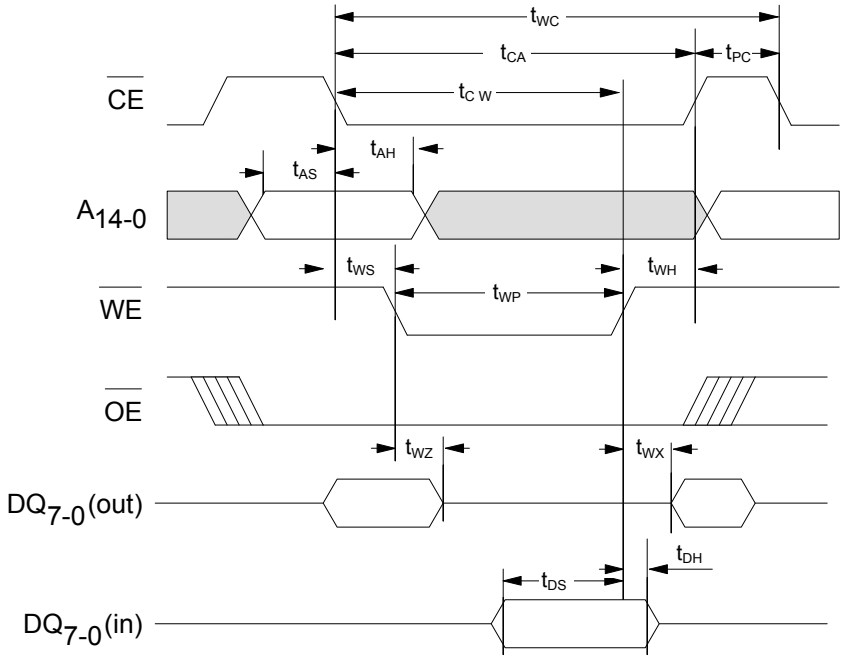


Figure 8. Write Cycle Timing 2 ($\overline{WE}$ Controlled)

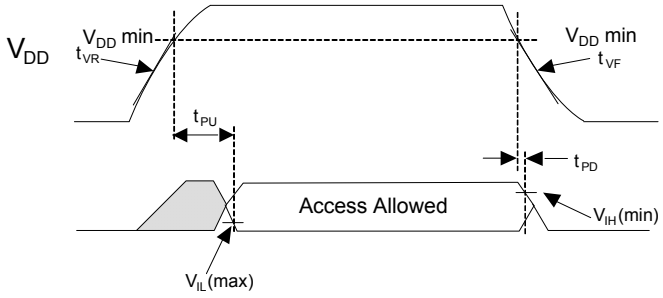


Power Cycle Timing

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up (after V_{DD} min. is reached) to first access time	10	–	ms
t_{PD}	Last write ($\overline{WE}$ HIGH) to power down time	0	–	µs
t_{VR}[8]	V_{DD} power-up ramp rate	30	–	µs/V
t_{VF}[8]	V_{DD} power-down ramp rate	30	–	µs/V

Figure 9. Power Cycle Timing



Note
8. Slope measured at any point on the V_{DD} waveform.

Functional Truth Table

$\overline{CE}$	$\overline{WE}$	Operation [9, 10]
H	X	Standby/Pre-charge
↓	X	Latch Address (and begin write if $\overline{WE}$ = LOW)
L	H	Read
L	↓	Write

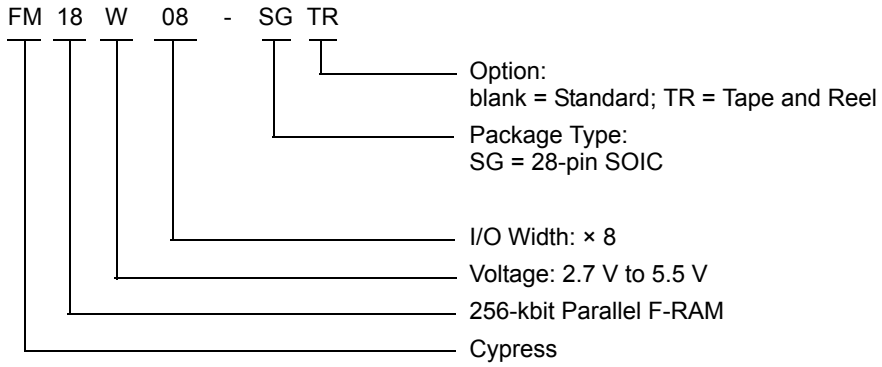
Notes
9. H = Logic HIGH, L = Logic LOW, V = Valid Data, X = Don't Care, ↓ = toggle LOW, ↑ = toggle HIGH.
10. The $\overline{OE}$ pin controls only the DQ output buffers.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM18W08-SG	51-85026	28-pin SOIC	Industrial
FM18W08-SGTR	51-85026	28-pin SOIC	

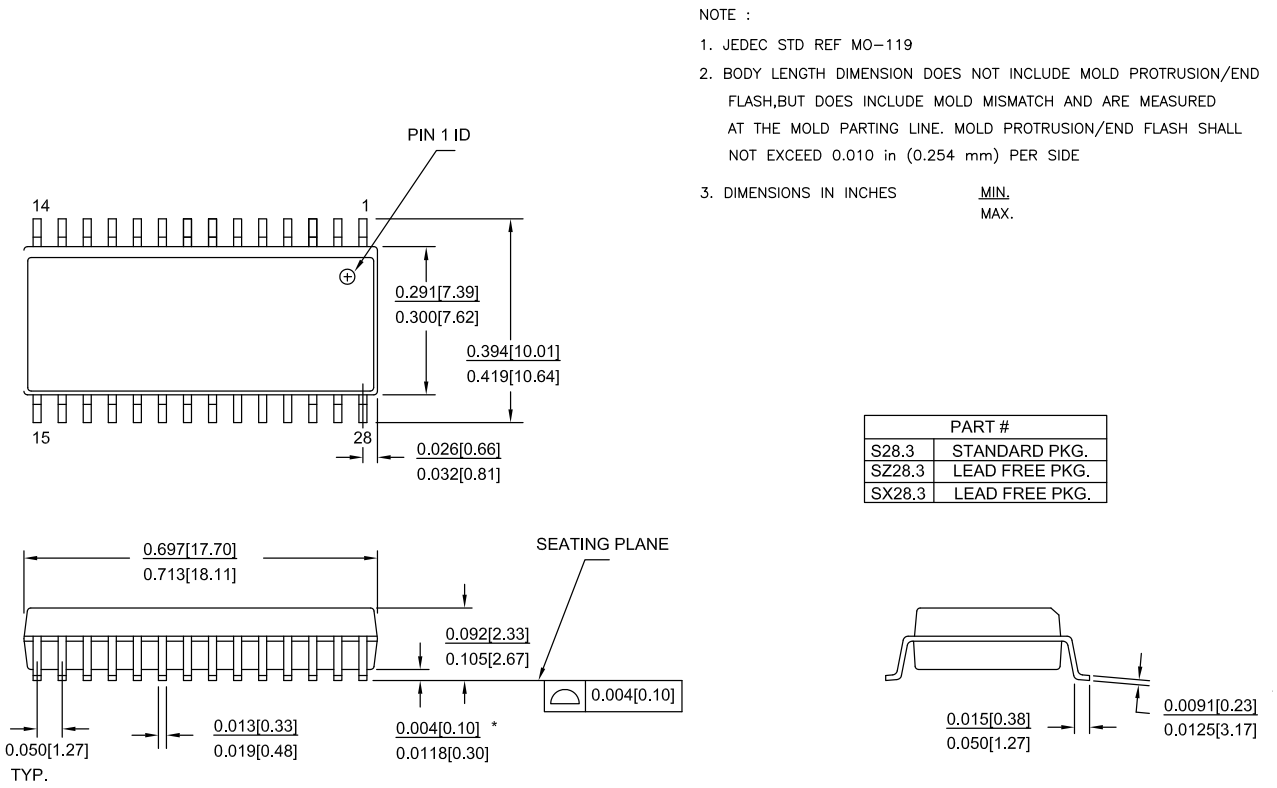
All the above parts are Pb-free.

Ordering Code Definitions



Package Diagram

Figure 10. 28-pin SOIC Package Outline, 51-85026



Acronyms

Acronym	Description
CPU	Central Processing Unit
CMOS	Complementary Metal Oxide Semiconductor
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I/O	Input/Output
MCU	Microcontroller Unit
MPU	Microprocessor Unit
RoHS	Restriction of Hazardous Substances
R/W	Read and Write
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
MΩ	megaohm
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM18W08, 256-Kbit (32 K × 8) Wide Voltage Bytewide F-RAM Memory Document Number: 001-86207				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3912933	GVCH	02/25/2013	New spec
*A	4000965	GVCH	05/15/2013	Added Appendix A - Errata for FM18W08
*B	4045491	GVCH	06/30/2013	All errata items are fixed and the errata is removed.
*C	4274813	GVCH	03/10/2014	Converted to Cypress standard format Changed datasheet status from “Preliminary to Final” Updated Maximum Ratings table - Removed Moisture Sensitivity Level (MSL) - Added junction temperature and latch up current Updated Data Retention and Endurance table Added Thermal Resistance table Removed Package Marking Scheme (top mark)
*D	4569028	GVCH	11/13/2014	Added related documentation hyperlink in page 1. Updated package diagram to most current revision.
*E	4881950	ZSK / PSR	09/04/2015	Updated Maximum Ratings: Removed “Maximum junction temperature”. Added “Maximum accumulated storage time”. Added “Ambient temperature with power applied”. Updated to new template.

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