August 2016

FCB110N65F

N-Channel SuperFET® II FRFET® MOSFET

650 V, 35 A, 110 mΩ

Features

- 700 V @T_J = 150°C
- Typ. $R_{DS(on)}$ = 96 mΩ (Typ.)
- Ultra Low Gate Charge (Typ. Q_g = 98 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 464 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

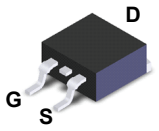
- Telecom/Server Power Supplies
- Solar Inverters
- Computing Power Supplies
- FPD TV Power/Lighting

Description

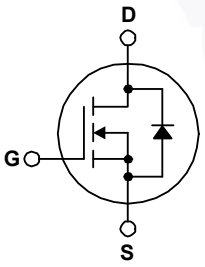
SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance.

SuperFET® II FRFET® MOSFET combines a faster and more rugged intrinsic body diode performance with fast switching, aimed at achieving better reliability and efficiency especially in resonant switching applications.

SuperFET® II FRFET® is very suitable for the switching power applications such as server/telecom power, Solar inverter, FPD TV power, computing power, lighting and industrial power applications.



D²-PAK



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FCB110N65F	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	- DC	±20	V
		- AC	±30	
I_D	Drain Current	- Continuous (T_C = 25°C)	35	A
		- Continuous (T_C = 100°C)	24	
I_{DM}	Drain Current	- Pulsed (Note 1)	105	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	809	mJ
I_{AR}	Avalanche Current	(Note 1)	8	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.57	mJ
dv/dt	MOSFET dv/dt	(Note 3)	100	V/ns
	Peak Diode Recovery dv/dt		50	
P_D	Power Dissipation	(T_C = 25°C)	357	W
		- Derate Above 25°C	2.86	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCB110N65F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Mimimum Pad of 2-oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in^2 Pad of 2-oz copper), Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Tape Width
FCB110N65F	FCB110N65F	D^2-PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 10 mA, V_{GS} = 0 V, T_J = 25°C	650	-	-	V
		I_D = 10 mA, V_{GS} = 0 V, T_J = 150°C	700	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	-	0.72	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	-	-	10	μA
		V_{DS} = 520 V, V_{GS} = 0 V, T_C = 125°C	-	110	-	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 3.5 mA	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 17.5 A	-	96	110	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 17.5 A	-	30	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	-	3680	4895	pF
C_{oss}	Output Capacitance		-	110	145	pF
C_{rss}	Reverse Transfer Capacitance		-	0.65	-	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	-	65	-	pF
C_{oss} eff.	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	464	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 380 V, I_D = 17.5 A, V_{GS} = 10 V (Note 4)	-	98	145	nC
Q_{gs}	Gate to Source Gate Charge		-	20	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	43	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.7	-	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 17.5 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	-	31	72	ns
t_r	Turn-On Rise Time		-	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		-	89	188	ns
t_f	Turn-Off Fall Time		-	5.7	21	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	35	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	100	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 17.5 A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 17.5 A, dI_F/dt = 100 A/μs	-	133	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.67	-	μC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. I_{AS} = 8 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 17.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 380 V, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

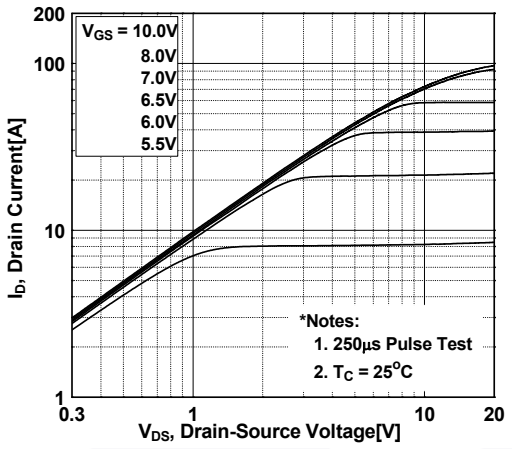


Figure 2. Transfer Characteristics

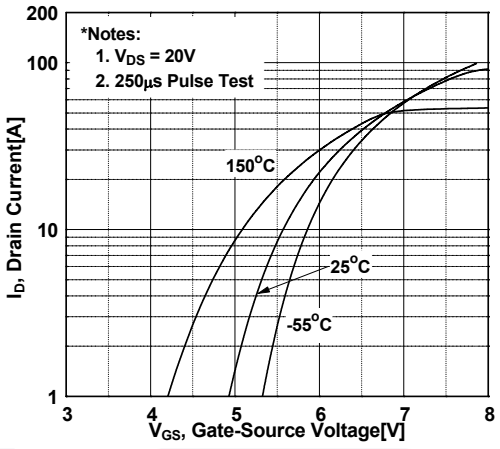


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

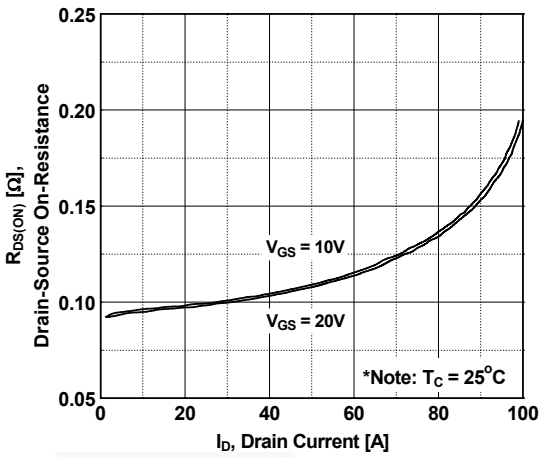


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

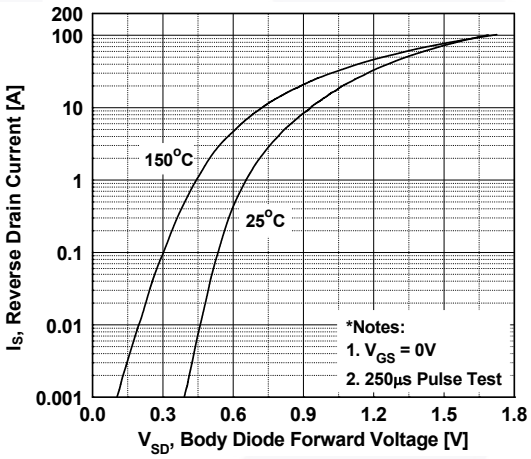


Figure 5. Capacitance Characteristics

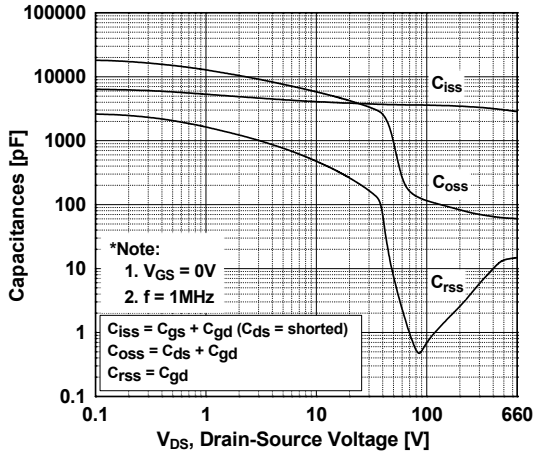
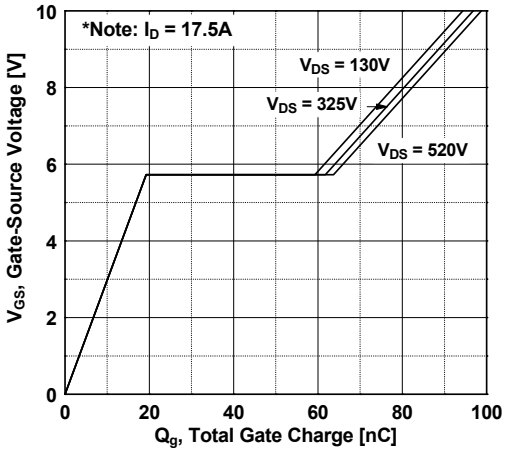


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

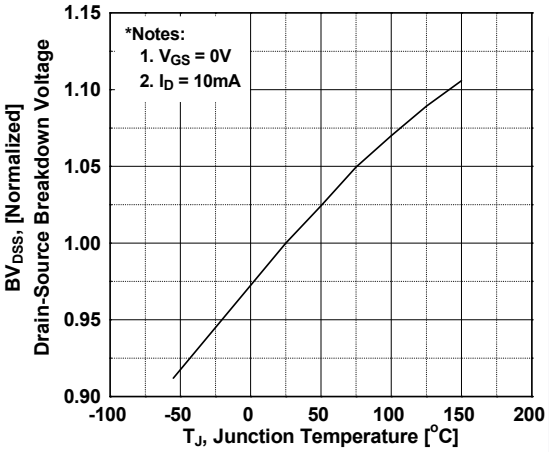


Figure 8. On-Resistance Variation vs. Temperature

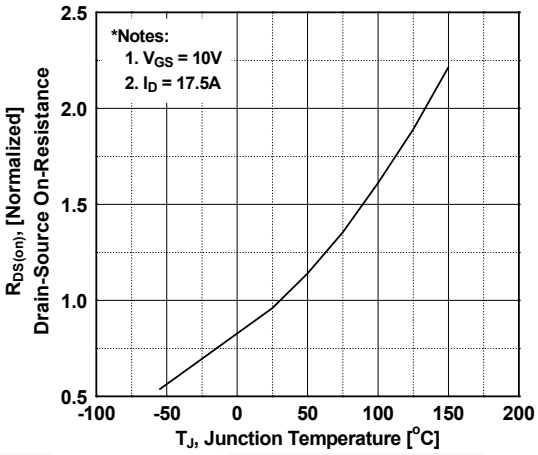


Figure 9. Maximum Safe Operating Area

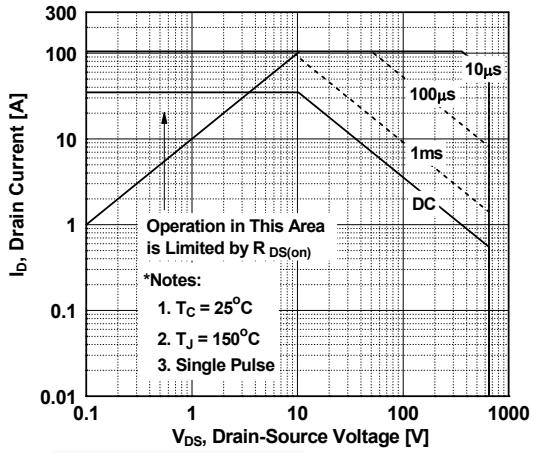


Figure 10. Maximum Drain Current vs. Case Temperature

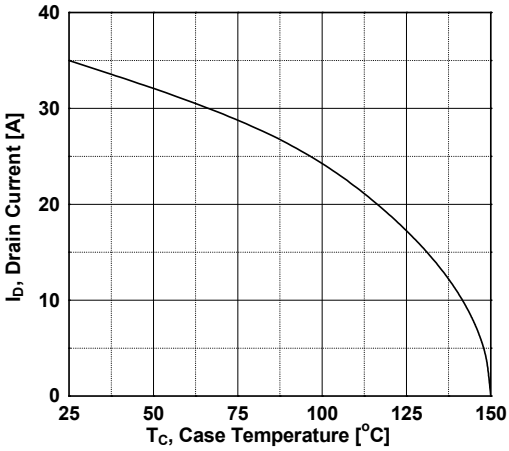
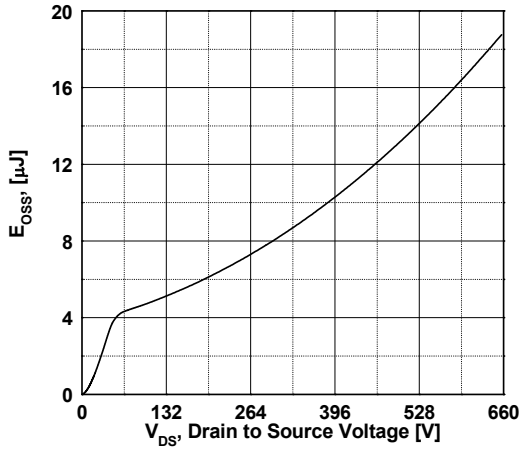
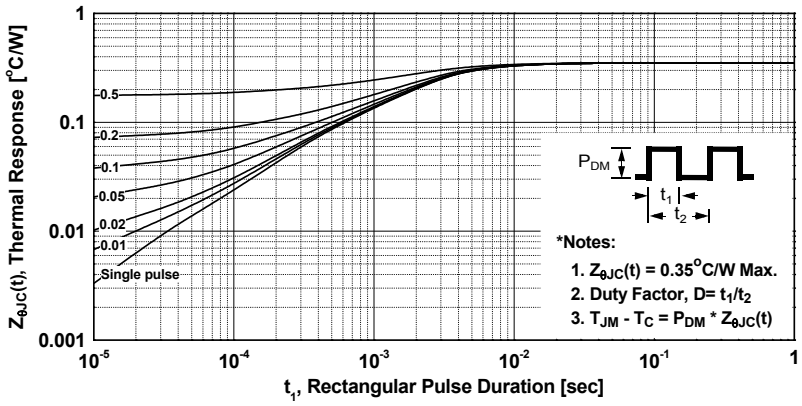


Figure 11. Eoss vs. Drain to Source Voltage Switching Capability



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



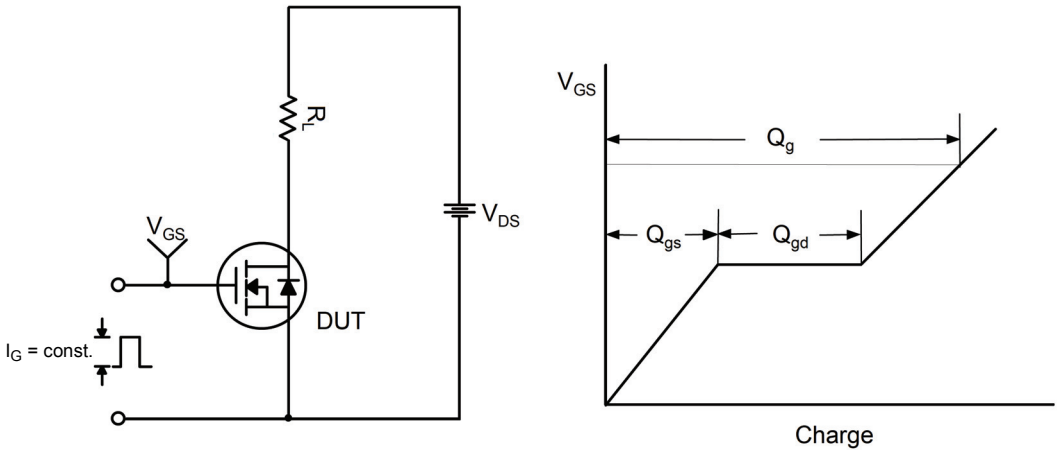


Figure 13. Gate Charge Test Circuit & Waveform

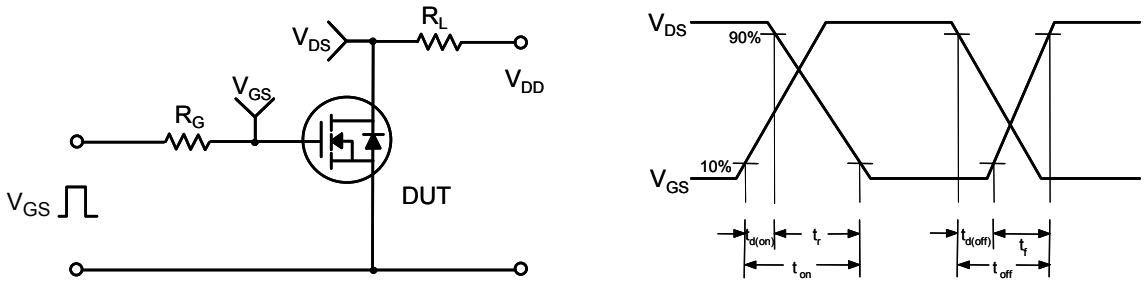


Figure 14. Resistive Switching Test Circuit & Waveforms

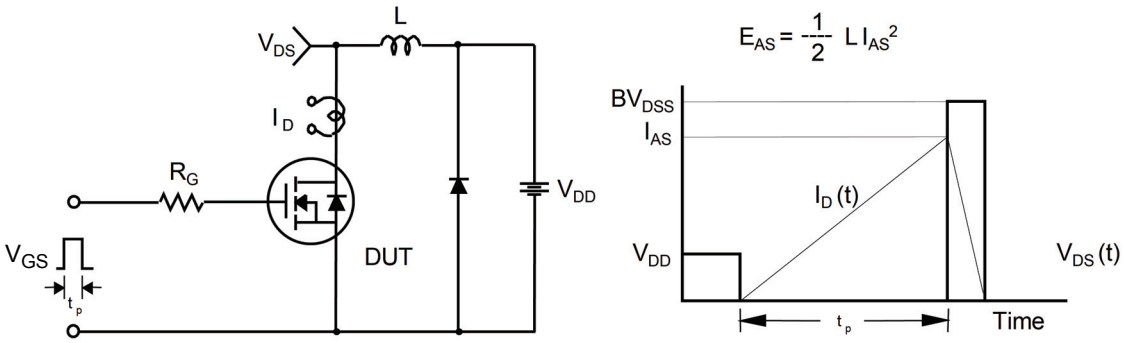


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

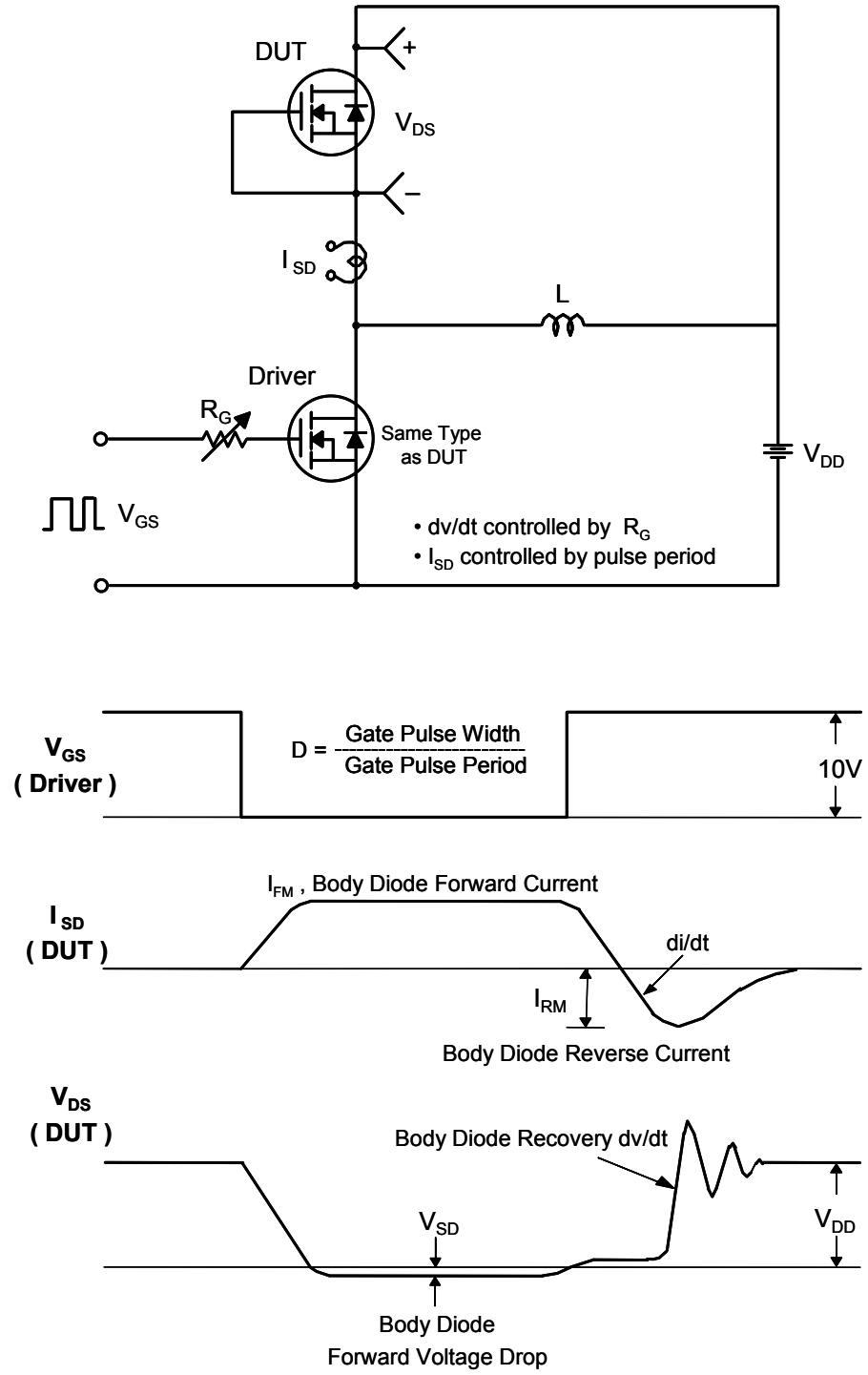
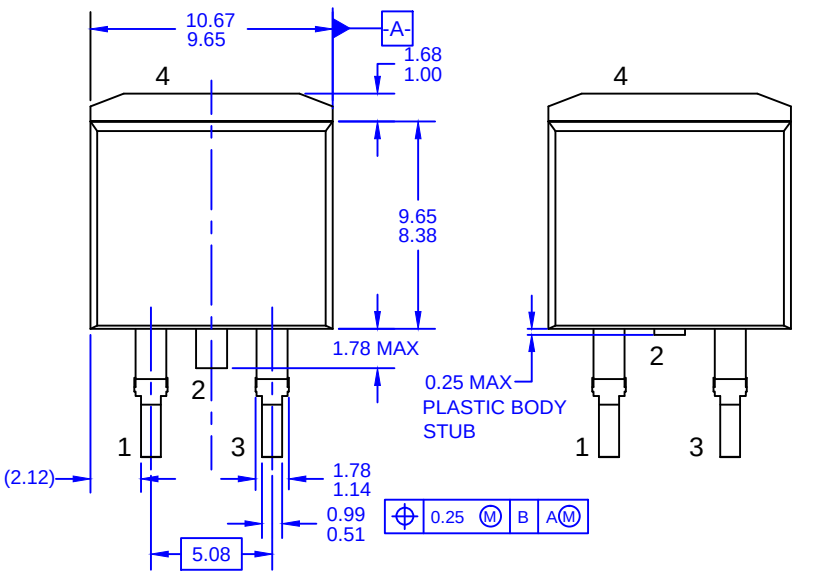
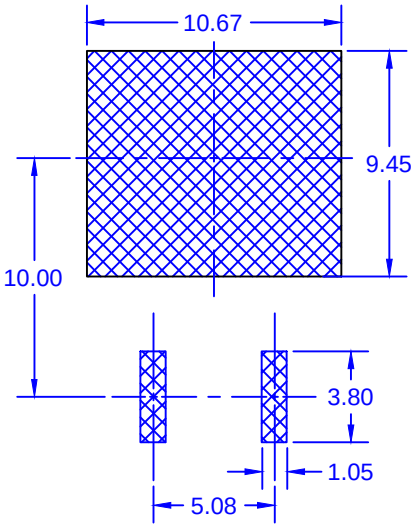


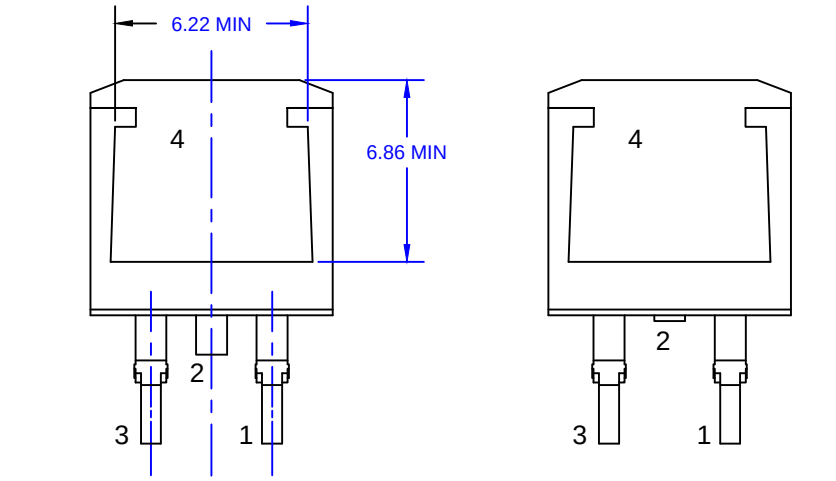
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



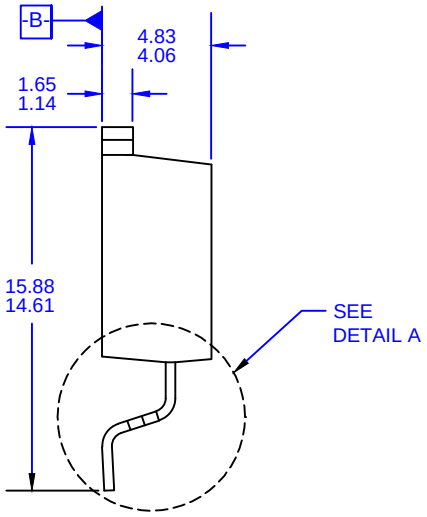
FRONT VIEW - DIODE PRODUCTS VERSION
ALTERNATIVE SUPPLIER DETAIL



LAND PATTERN RECOMMENDATION
UNLESS NOTED, ALL DIMS TYPICAL

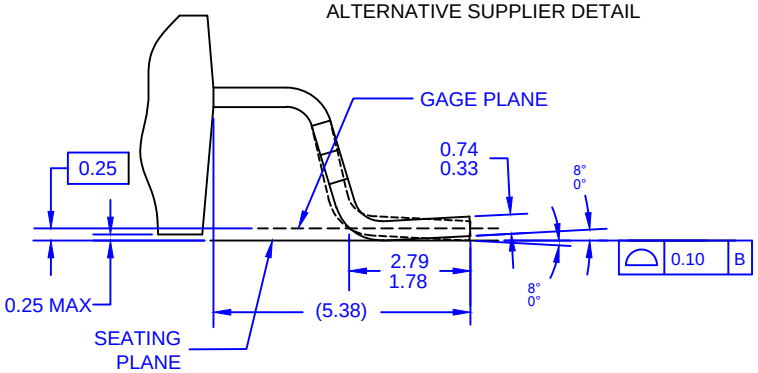


BACK VIEW - DIODE PRODUCTS VERSION
ALTERNATIVE SUPPLIER DETAIL



NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) REFERENCE JEDEC, TO-263, VARIATION AB.
C) DIMENSIONING AND TOLERANCING PER DIMENSIONING AND TOLERANCING PER ASME Y14.5 - 2009.
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
F) FILENAME: TO263A02REV8



DETAIL A, ROTATED 90°
SCALE: 2X

PUBLICATION ORDERING INFORMATION

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