Order Number(s):

EMC1001-AFZQ-TR for 6 pin, SOT 23 Lead-Free RoHS compliant package

(tape and reel)

EMC1001-1-AFZQ-TR for 6 pin, SOT 23 Lead-Free RoHS compliant package

(alternate addresses, tape and reel)

See Table 1.2, "SMBus Address Configuration Information," on page 3

Reel size is 8,000 pieces.

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Chapter 1 Pin Configuration

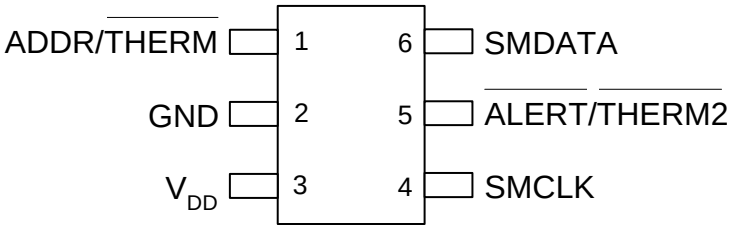

Figure 1.1 EMC1001 Pin Configuration

Table 1.1 Pin Description

PIN	PIN NO.	DESCRIPTION
ADDR/$\overline{\text{THERM}}$	1	Logic output that can be used to turn on/off a fan or throttle a CPU clock in the event of an over-temperature condition. This is an open-drain output. This pin is sampled following power up and the value of the pull up resistor determines the SMBus slave address per Table 1.2.Total capacitance on this pin must not exceed 100 pF, and the pull-up resistor must be connected to the same supply voltage as V_{DD}
GND	2	Ground.
V_{DD}	3	Supply Voltage, 3.0V to 3.6V.
SMCLK	4	SMBus clock input.
$\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$	5	Logic output used as interrupt, SMBus alert or as a second $\overline{\text{THERM}}$ output. This is an open-drain output.
SMDATA	6	SMBus data input/output, open drain output.

Table 1.2 SMBus Address Configuration Information

PART NUMBER	ADDR/THERM PULL-UP RESISTOR	SMBUS ADDRESS	PACKAGE DESCRIPTION
EMC1001	7.5kΩ ±5% Note 1.1, Note 1.2	1001 000b	6-Lead SOT-23
	12kΩ ±5% Note 1.2	1001 001b	6-Lead SOT-23
	20kΩ ±5% Note 1.2	0111 000b	6-Lead SOT-23
	33kΩ ±5% Note 1.2	0111 001b	6-Lead SOT-23
EMC1001-1	7.5kΩ ±5% Note 1.1, Note 1.2	1001 010b	6-Lead SOT-23
	12kΩ ±5% Note 1.2	1001 011b	6-Lead SOT-23
	20kΩ ±5% Note 1.2	0111 010b	6-Lead SOT-23
	33kΩ ±5% Note 1.2	0111 011b	6-Lead SOT-23

Note 1.1 This value must be greater than 1kΩ ±5% and less than or equal to 7.5kΩ ±5%.

Note 1.2 The pull-up resistor must be connected to V_{DD} (pin 1), and the total capacitance on this pin must be less than 100pF.

Table 1.3 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage V_{DD}	-0.3 to 5.0	V
Voltage on $\overline{ALERT}$/$\overline{THERM2}$, SMDATA and SMCLK pins	-0.3 to 5.5	V
Voltage on any other pin	-0.3 to V_{DD}+0.3	V
Operating Temperature Range	-25 to +125	°C
Storage Temperature Range	-55 to +150	°C
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020	
Package Thermal Characteristics for SOT23-6		
Power Dissipation	TBD	mW @ 70°C
Thermal Resistance	111.5	°C/W
ESD Rating, All Pins (Human Body Model)	2000	V

Note: Stresses above those listed could cause damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

Chapter 2 Electrical Characteristics

Table 2.1 Electrical Characteristics

V_{DD}=3.0V to 3.6V, T_A= -25°C to +125°C, Typical values at T_A = 27°C unless otherwise noted						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
DC Power						
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Average Operating Current	I_{DD}		47	TBD	µA	0.0625 conversion/s See Table 4.6, "Conversion Rates," on page 14
	I_{PD}		4.8	10	µA	Standby mode
Temperature Measurement						
Accuracy			±0.5	±1.5	°C	40°C≤T_A≤85°C
			±1	±3	°C	-25°C≤T_A≤125°C
Resolution			0.25		°C	
Conversion Time			26		ms	
Voltage Tolerance						
Voltage at pin (ADDR/$\overline{\text{THERM}}$,)	V_{TOL}	-0.3		3.6	V	
Voltage at pin ($\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$, SMDATA,SMCLK)	V_{TOL}	-0.3		5.5	V	
Digital Outputs (ADDR/$\overline{\text{THERM}}$, $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$)						
Output Low Voltage	V_{OL}			0.4	V	I_{OUT}=-4mA
High Level Leakage Current	I_{OH}		0.1	1	µA	V_{OUT}=V_{DD}
SMBus Interface (SMDATA,SMCLK)						
Input High Level	V_{IH}	2.0			V	
Input Low Level	V_{IL}			0.8	V	
Input High/Low Current	I_{IH}/I_{IL}	-1		1	µA	
Hysteresis			500		mV	
Input Capacitance			5		pF	
Output Low Sink Current		6			mA	SMDATA = 0.6V
SMBus Timing						
Clock Frequency	F_{SMB}	10		400	kHz	
Spike Suppression				50	ns	

Table 2.1 Electrical Characteristics (continued)

V_{DD}=3.0V to 3.6V, T_A= -25°C to +125°C, Typical values at T_A = 27°C unless otherwise noted						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Bus free time Start to Stop	T_{BUF}	1.3			µS	
Hold time Start	$T_{HD:STA}$	0.6			µS	
Setup time Start	$T_{SU:STA}$	0.6			µS	
Setup time Stop	$T_{SU:STO}$	0.6			µS	
Data Hold Time	$T_{HD:DAT}$	0.3			µS	
Data Setup Time	$T_{SU:DAT}$	100			ns	
Clock Low Period	T_{LOW}	1.3			µS	
Clock High Period	T_{HIGH}	0.6			µS	
Clock/Data Fall Time	T_F	*		300	ns	*Min = 20+0.1C_b ns
Clock/Data Rise Time	T_R	*		300 Note 2.1	ns	*Min = 20+0.1C_b ns
Capacitive Load (each bus line)	C_b	0.6		400	pF	

Note 2.1 300nS rise time max is required for 400kHz bus operation. For lower clock frequencies, the maximum rise time is (0.1/F_{SMB})+50nS

Chapter 3 System Management Bus Interface Protocol

A host controller, such as an SMSC I/O controller, communicates with the EMC1001 via the two wire serial interface named SMBus. The SMBus interface is used to read and write registers in the EMC1001, which is a slave-only device. A detailed timing diagram is shown in Figure 3.1.

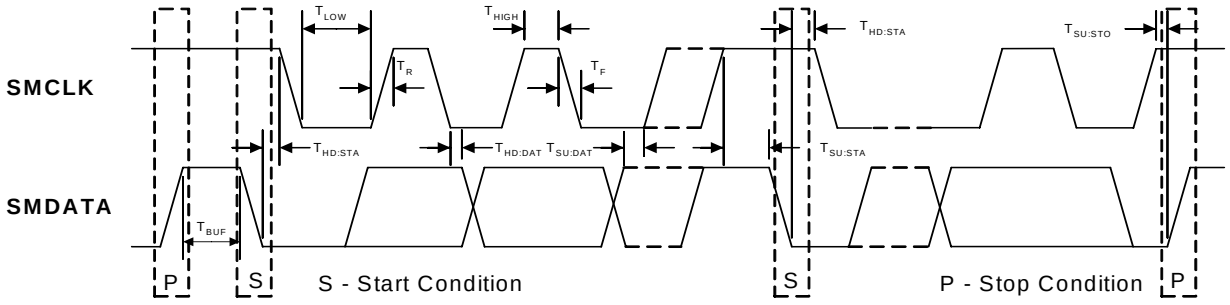

Figure 3.1 System Management Bus Timing Diagram

The EMC1001 implements a subset of the SMBus specification and supports Write Byte, Read Byte, Send Byte, Receive Byte, and Alert Response Address protocols. as shown. In the tables that describe the protocol, the “gray” columns indicate that the slave is driving the bus.

3.1 Write Byte

The Write Byte protocol is used to write one byte of data to the registers as shown below:

Table 3.1 SMBus Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	STOP
1	7	1	1	8	1	8	1	1

3.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown below:

Table 3.2 SMBus Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	START	SLAVE ADDRESS	RD	ACK	DATA	NACK	STOP
1	7	1	1	8	1	1	7	1	1	8	1	1

3.3 Send Byte

The Send Byte protocol is used to set the Internal Address Register to the correct Address. The Send Byte can be followed by the Receive Byte protocol described below in order to read data from the register. The send byte protocol cannot be used to write data - if data is to be written to a register then the write byte protocol must be used as described in subsection above. The send byte protocol is shown in Table 3.3.

Table 3.3 SMBus Send Byte Protocol

FIELD:	START	SLAVE ADDR	WR	ACK	REG. ADDR	ACK	STOP
Bits:	1	7	1	1	8	1	1

3.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This can be used for consecutive reads of the same register as shown below:

Table 3.4 SMBus Receive Byte Protocol

FIELD:	START	SLAVE ADDR	RD	ACK	REG. DATA	NACK	STOP
Bits:	1	7	1	1	8	1	1

3.5 Alert Response Address

The $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ output can be used as an SMBALERT# as described in 4.3, "ALERT/THERM2 Output," on page 11. The Alert Response Address is polled by the Host whenever it detects an SMBALERT#, i.e. when the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin is asserted. The EMC1001 will acknowlege the Alert Response Address and respond with its device address as shown below.

Table 3.5 Modified SMBus Receive Byte Protocol Response to ARA

FIELD:	START	ALERT RESPONSE ADDRESS	RD	ACK	EMC1001 SLAVE ADDRESS	NACK	STOP
Bits:	1	7	1	1	8	1	1

3.6 SMBus Addresses

The EMC1001 is available in two versions, each of which has four 7-bit slave addresses that are enabled based on the pull-up resistor on the ADDR/$\overline{\text{THERM}}$ pin. The value of this pull up resistor determines the slave address per Table 1.2 on page 3. Attempting to communicate with the EMC1001 SMBus interface with an invalid slave address or invalid protocol results in no response from the device and does not affect its register contents. The EMC1001 supports stretching of the SMCLK signal by other devices on the SMBus but will not perform this operation itself. The EMC1001 has an SMBus timeout feature. Bit 7 of the SMBus Timeout Enable register enables this function when set to 1 (the default setting is 0). When this feature is enabled, the SMBus will timeout after approximately 25ms of inactivity.

Chapter 4 Product Description

The EMC1001 is an SMBus temperature that monitors a single temperature zone. Thermal management is performed in cooperation with a host device. The host reads the temperature data from the EMC1001 and takes appropriate action such as controlling fan speed or processor clock frequency. The EMC1001 has programmable temperature limit registers that define a safe operating window. After the host has configured the temperature limits, the EMC1001 can operate as a free-running independent watchdog to warn the host of temperature hot spots without requiring the host to poll the device. The ADDR/$\overline{\text{THERM}}$ output can be used to control a fan without host intervention.

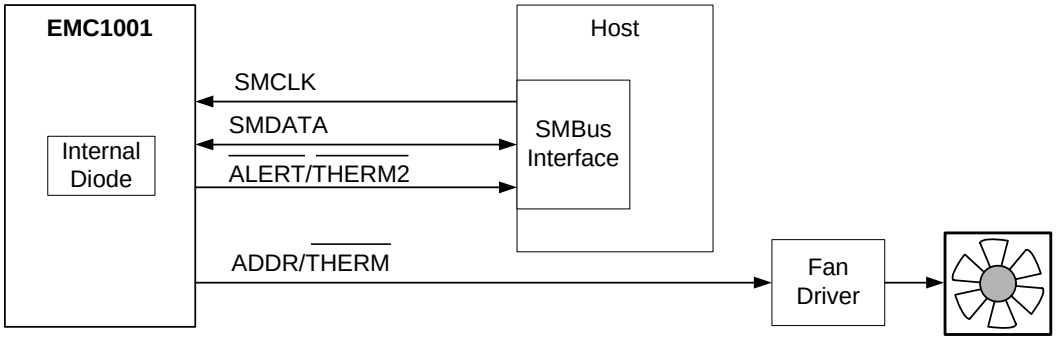

Figure 4.1 Controlling a fan without host intervention.

The EMC1001 has two basic modes of operation:

- Run Mode: In this mode, the EMC1001 continuously converts temperature data and updates its registers. The rate of temperature conversion is configured as shown in Section 4.9 on page 14.
- Standby Mode: In this mode, the EMC1001 is placed in standby to conserve power as described in Section 4.5 on page 12.

4.1 Temperature Monitors

Thermal diode temperature measurements are based on the change in forward bias voltage (ΔV_{BE}) of a diode when operated at two different currents:

$$\Delta V_{BE} = V_{BE\_HIGH} - V_{BE\_LOW} = \frac{\eta kT}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right)$$

where:

k = Boltzmann's constant

T = absolute temperature in Kelvin

q = electron charge

η = diode ideality factor

The change in ΔV_{BE} voltage is proportional to absolute temperature T.

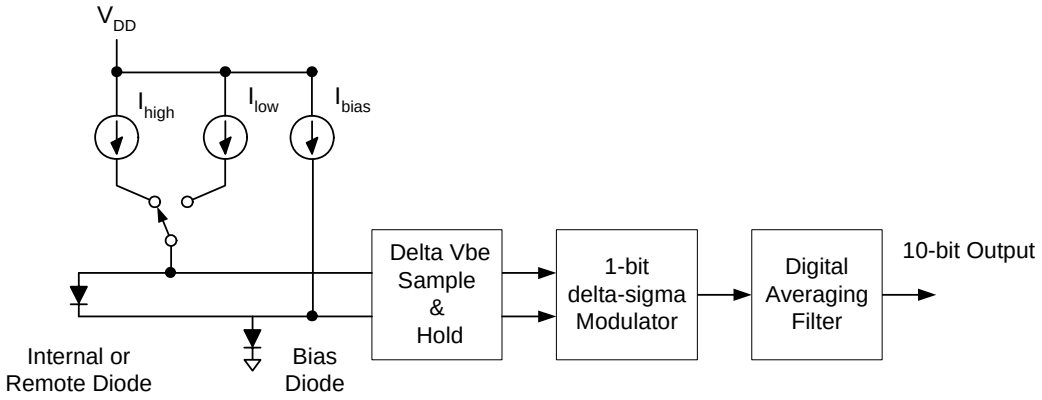

Figure 4.2 Detailed Block Diagram

Figure 4.2 shows a detailed block diagram of the temperature measurement circuit. The EMC1001 incorporates switched capacitor technology that integrates the temperature diode ΔV_{BE} from different bias currents. The negative terminal, DN, for the temperature diode is internally biased with a forward diode voltage referenced to ground.

The advantages of this architecture over Nyquist rate FLASH or SAR converters are superb linearity and inherent noise immunity. The linearity can be directly attributed to the delta-sigma ADC single-bit comparator while the noise immunity is achieved by the ~20ms integration time which translates to 50Hz input noise bandwidth.

4.2 Temperature Measurement Results and Data

The 10-bit temperature measurement results are stored in temperature value registers. Table 4.1 shows the two's complement temperature data format with an LSB equivalent to 0.25°C.

Table 4.1 Temperature Data Format

TEMPERATURE	VALID RANGE –40°C TO 125°C TWO'S COMPLEMENT
-0.25°C	1111 1111 11 Note 4.1
0.0°C	0000 0000 00
+0.25°C	0000 0000 01
+0.50°C	0000 0000 10
+0.75°C	0000 0000 11
+1°C	0000 0001 00
+125°C	0111 1101 00 Note 4.2

Note 4.1 Temperature measurement returns 1100 0000 00 for all temperatures ≤ -64.00°C

Note 4.2 Temperature measurement returns 0111 1111 11 for all temperatures ≥ +127.75°C

The eight most significant bits are stored in the Temperature Value High Byte register and the two least significant bits stored in the Temperature Value Low Byte register as outlined in Table 4.2. The six LSB positions of the Temperature Value Low Byte register always read zero. In Table 4.2, the upper case

"B" shows the bit position of a 16-bit word created by concatenating the High Byte and Low Byte, and the lower case "b" shows the bit position in the 10-bit value.

Table 4.2 Bit Position of Two Byte Values

HIGH BYTE								LOW BYTE							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	0	0	0	0	0	0

4.3 $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ Output

The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ output asserts if an out of limit measurement is detected (TA ≤ low limit or TA > high limit). The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is an open drain output and requires a pull up resistor to V_{DD}.The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin can be used as an SMBALERT#, or may be configured as a second $\overline{\text{THERM}}$ output.

As described in the SMBus specification, an SMBus slave may inform the SMBus master that it wants to talk by asserting the SMBALERT# signal. One or more $\overline{\text{ALERT}}$ outputs can be hardwired together as a wired-or bus to a common input.

The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin resets when the EMC1001 responds to an alert response address (ARA=0001 100) sent by the host, and if the out of limit condition no longer exists, but it does not reset if the error condition remains. The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin can be masked so that it will not assert in the event of an out of limit temperature measurement, except when it is configured as a second $\overline{\text{THERM}}$ pin.

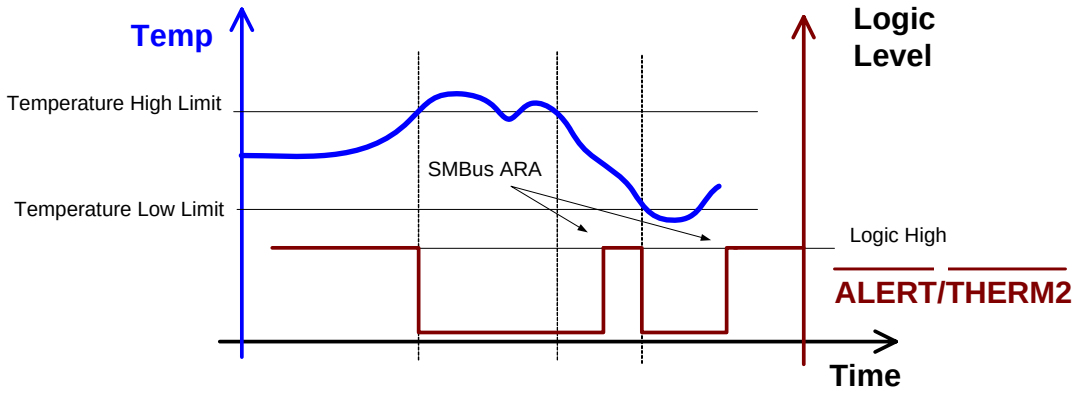

Figure 4.3 $\overline{\text{ALERT}}$ Response to Temperature Limits Exceeded

The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin can be configured as a second $\overline{\text{THERM}}$ pin that asserts when the temperature measurement exceeds the Temperature High Limit value. In this mode, the output will not de-assert until the temerature drops below the Temperature High Limit minus the THERM Hysteresis value.

4.4 ADDR/$\overline{\text{THERM}}$ Output

The ADDR/$\overline{\text{THERM}}$ output asserts if the temperature measurement exceeds the programmable THERM limit. It can be used to drive a fan or other failsafe devices. The ADDR/$\overline{\text{THERM}}$ pin is open drain and requires a pull up resistor to V_{DD}. The value of this pull up resistor determines the slave address per Table 1.2 on page 3. The ADDR/$\overline{\text{THERM}}$ pin cannot be masked.

When the ADDR/$\overline{\text{THERM}}$ pin is asserted, it will not de-assert until the temperature drops below the THERM limit minus the THERM hysteresis value.

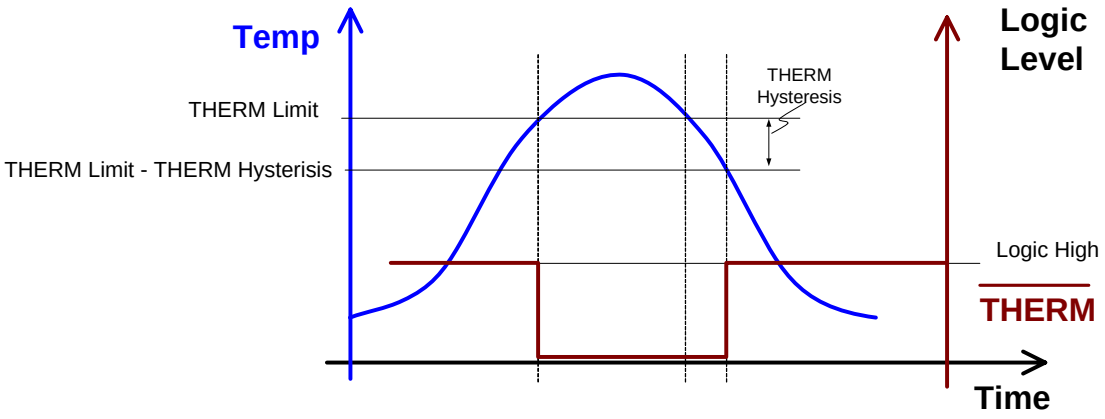

Figure 4.4 $\overline{\text{THERM}}$ Response to THERM Limit Exceeded

4.5 Standby Mode

The EMC1001 can be set to standby mode (low power) by setting a bit in the Configuration Register as described in Section 4.8 on page 13. This shuts down all internal analog functions while the SMBus remains enabled. When the EMC1001 is in standby mode, a One-Shot command measurement can be initiated. The user may also write new values to the limit registers described in Section 4.10 on page 15 while in standby. If the previously stored temperature is outside any of the new limits, the ALERT/$\overline{\text{THERM2}}$ output will respond as described in Section 4.3 and the ADDR/$\overline{\text{THERM}}$ output will respond as described in Section 4.4.

4.6 Register Allocation

The following registers shown in Table 4.3 are accessible through the SMBus:

Table 4.3 Register Map

REGISTER ADDRESS (HEX)	R/W	REGISTER NAME	POWER-ON DEFAULT
00	R	Temperature Value High Byte	0000 0000
01	R	Status	undefined
02	R	Temperature Value Low Byte	0000 0000
03	R/W	Configuration	0000 0000
04	R/W	Conversion Rate	0000 0100
05	R/W	Temperature High Limit High Byte	0101 0101 (85°C)
06	R/W	Temperature High Limit Low Byte	0000 0000
07	R/W	Temperature Low Limit High Byte	0000 0000 (0°C)
08	R/W	Temperature Low Limit Low Byte	0000 0000
0F	W	One-Shot	N/A
20	R/W	THERM Limit	0101 0101 (85°C)
21	R/W	THERM Hysteresis	0000 1010 (10°C)
22	R/W	SMBus Timeout Enable	0000 0001
FD	R	Product ID Register	0000 0000 (EMC1001) 0000 0001 (EMC1001-1)
FE	R	Manufacture ID	0101 1101
FF	R	Revision Number	0000 0011 Note 4.3

Note 4.3 Revision number may change. Please obtain the latest version of this document from the SMSC web site.

At device power-up, the default values are stored in all registers. A power-on-reset is initiated when power is first applied to the part and the V_{DD} supply exceeds the POR threshold. Reads of undefined registers will return 00h and writes to undefined registers will be ignored.

The EMC1001 uses an interlock mechanism that locks the low byte value when the high byte register is read. This prevents updates to the low byte register between high byte and low byte reads. This interlock mechanism requires that the high byte register always be read prior to reading the low byte register.

4.7 Status Register

The status register is a read only register that stores the operational status of the part. When either TLOW or THIGH are set (TA ≤ low limit or TA > high limit) and the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is not masked, the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin will assert. See Section 4.3 on page 11 for more details on the ALERT function.

Table 4.4 Status Register

STATUS REGISTER		
BIT	**NAME**	**FUNCTION**
7	Busy	1 when ADC is converting
6	THIGH	1 when Temperature High Limit is exceeded
5	TLOW	1 when Temperature Low Limit is exceeded
4		Reserved
3		Reserved
2		Reserved
1		Reserved
0	THRM	1 when THERM limit is exceeded

Bit 7 indicates that the ADC is busy converting a value. Bits 6 and 5 indicate that the temperature measurement is above or below the limits respectively. Bit 0 indicates that the measured temperature has exceeded the THERM limit. When bit 0 goes high the $\text{ADDR}/\overline{\text{THERM}}$ output will be asserted.

Each bit is cleared individually when the status register is read, provided that the error condition for that bit no longer exists. The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ output is latched and will not be reset until the host has responded with an alert response address (ARA=0001 100). The $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ output will not reset if the status register has not been cleared.

4.8 Configuration Register

The configuration register controls the functionality of the temperature measurements.

Table 4.5 Configuration Register

CONFIGURATION REGISTER			
BIT	**NAME**	**FUNCTION**	**DEFAULT**
7	MASK1	0 = $\overline{\text{ALERT}}$ enabled 1 = $\overline{\text{ALERT}}$ disabled	0
6	RUN/STOP	0 = Active mode (continuously running) 1 = Standby mode	0
5	$\overline{\text{ALERT}}$ or $\overline{\text{THERM2}}$	0 = $\overline{\text{ALERT}}$ 1 = $\overline{\text{THERM2}}$	0
4 – 0	Reserved		0

Bit 7 is used to mask the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ signal. When this bit is set to 0, any out of limit condition will assert $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$. This bit is ignored if the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin is configured as $\overline{\text{THERM2}}$ signal by bit 5.

Bit 6 initiates ADC conversions. When this bit is low, the ADC will convert temperatures in a continuous mode. When this bit is high, the ADC will be in standby mode, thus reducing supply current significantly though the SMBus will still be active. If bit 6 is 1 and the one-shot register is written to, the ADC will execute a temperature measurement and then return to standby mode.

Bit 5 sets the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin to act as either an SMBALERT# signal or as the $\overline{\text{THERM2}}$ signal. If bit 5 is set to 1 the $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ pin acts as the $\overline{\text{THERM2}}$ signal and bit 7 is ignored.

4.9 Conversion Rate Register

The conversion rate register determines how many times the temperature value will be updated per second. The lowest 4 bits configure a programmable delay that waits between consecutive conversion cycles to obtain the desired conversion rate. Table 4.6 shows the conversion rate and the associated quiescent current.

Table 4.6 Conversion Rates

CONVERSION RATE		
VALUE	**CONVERSIONS/SECOND**	**TYPICAL QUIESCENT CURRENT (μA)**
00h	0.0625	36
01h	0.125	37
02h	0.25	38
03h	0.5	40
04h	1	44
05h	2	54
06h	4	71
07h	8	109
08h	16	182
09h	32	326
0Ah to FFh	Reserved	

4.10 Limit Registers

The user can configure high and low temperature limits and an independent THERM limit. The temperature high limit (T_H) is a 10-bit value that is set by the Temperature High Limit High Byte register and the Temperature High Limit Low Byte register. The Temperature High Limit Low Byte register contains the two least significant bits as shown in Table 4.2 on page 11. The two least significant bits are stored in the upper two bits of the register, and the six LSB positions of this register always read zero.

The temperature low limit (T_L) is a 10-bit value that is set by the Temperature Low Limit High Byte register and the Temperature Low Limit Low Byte register as shown in Table 4.2 on page 11.

The limits are compared to the temperature measurement results (T_{INT}) and have been exceeded if ($T_{INT} \leq T_L$ or $T_{INT} > T_H$). If either limit is exceeded then the appropriate bit is set high in the status register and the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ output will respond as described in Section 4.3 on page 11.

The THERM limit (T_{TH}) is a single byte value set by the THERM Limit register. Exceeding the THERM limit asserts the ADDR/$\overline{\text{THERM}}$ signal as described in Section 4.4 on page 11. When the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is configured as $\overline{\text{THERM2}}$, then exceeding the high limit asserts this pin.

4.11 THERM Hysteresis Register

The THERM hysteresis register holds a hysteresis value that determines the de-assertion of $\overline{\text{THERM}}$ as shown in Figure 4.4 on page 12. It defaults to 10°C and can be set by the user at any time after power up. When the $\overline{\text{ALERT}}/\overline{\text{THERM2}}$ pin is configured as $\overline{\text{THERM2}}$, then the hysteresis value also impacts the de-assertion of $\overline{\text{THERM2}}$.

4.12 One-Shot Register

Writing to the one-shot register while in standby mode initiates a conversion and comparison cycle. The EMC1001 will execute a temperature measurement, compare the data to the limit registers and return to the standby mode. A write to the one-shot register will be ignored if it occurs while the EMC1001 is in run mode.

4.13 SMBus Timeout Enable

The EMC1001 has an SMBus timeout feature. Bit 7 of the SMBus Timeout Enable register enables this function when set to 1 (the default setting is 0). When this feature is enabled, the SMBus will timeout after approximately 25ms of inactivity.

Chapter 5 Package Outline

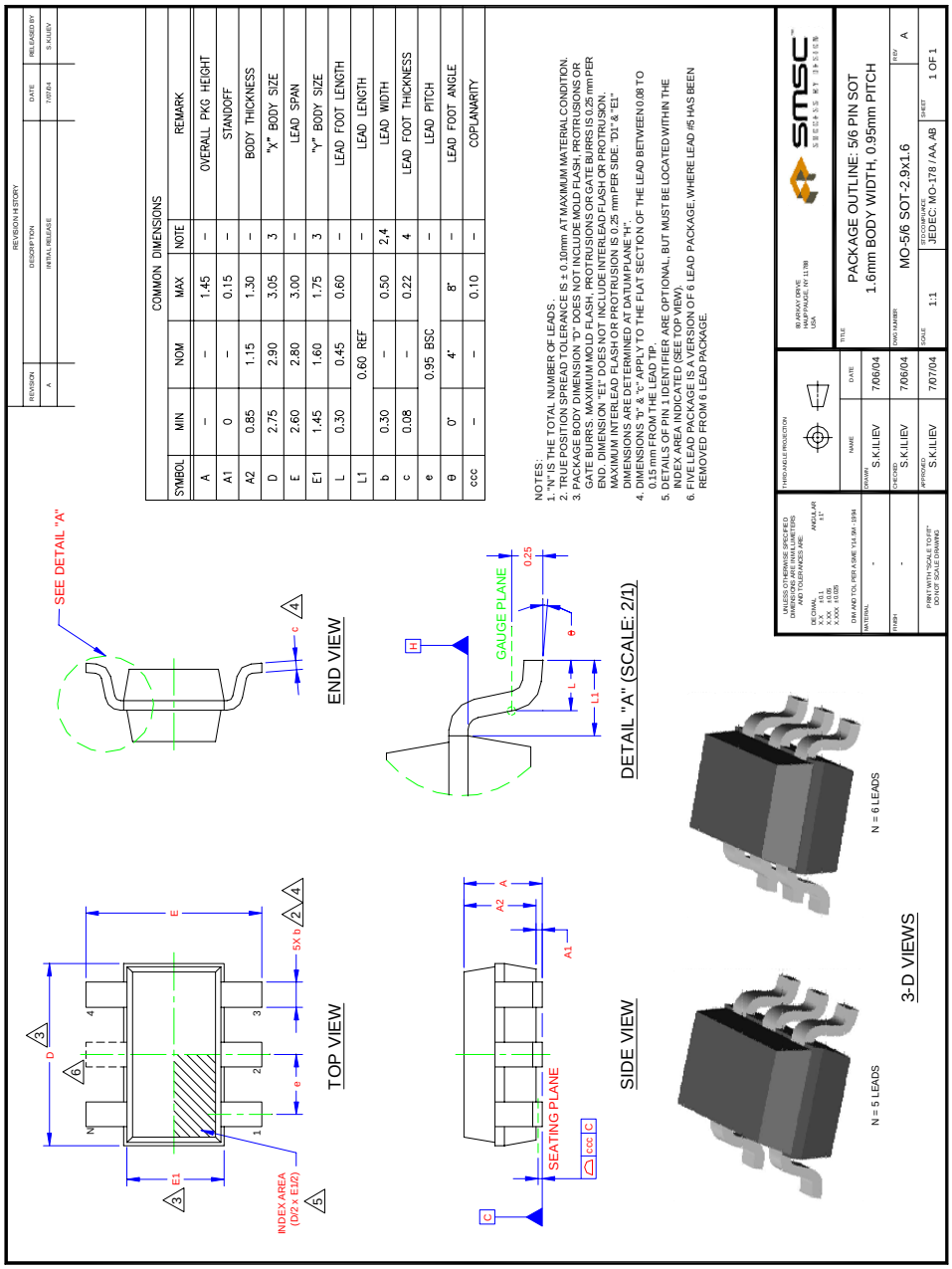

Figure 5.1 EMC1001, 6 Pin SOT Package Outline; 1.6mm Body Width, 0.95mm Pitch