ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-0.5V, +6V
Maximum Current Into Any Pin	±20mA
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See IPC/JEDEC J-STD-020

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

ELECTRICAL CHARACTERISTICS

(-40°C to +85°C, see Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		1.62		5.25	V
Standby Current	I_{CCS}	Bus idle, V_{CC} = 5.25V			3	µA
Operating Current	I_{CCA}	Bus active at 400kHz, V_{CC} = 5.25V			200	µA
SCL, SDA Pins (Note 2) See Figure 5						
LOW Level Input Voltage	V_{IL}	$V_{CC} \geq 2.0V$	-0.3		0.3 × V_{CC}	V
		$V_{CC} < 2.0V$	-0.3		0.25 × V_{CC}	
HIGH Level Input Voltage (Note 3)	V_{IH}	$V_{CC} \geq 2.0V$	0.7 × V_{CC}		V_{CCmax} + 0.3V	V
		$V_{CC} < 2.0V$	0.8 × V_{CC}		V_{CCmax} + 0.3V	
Hysteresis of Schmitt Trigger Inputs (Note 4)	V_{hys}	$V_{CC} \geq 2.0V$	0.05 × V_{CC}			V
		$V_{CC} < 2.0V$	0.1 × V_{CC}			
LOW Level Output Voltage at 4mA Sink Current	V_{OL}				0.4	V
Output Fall Time from V_{Ihmin} to V_{ILmax} with a Bus Capacitance from 10pF to 400pF (Notes 4, 5)	t_{of}	$V_{CC} \geq 2.0V$	20 + 0.1Cb		250	ns
		$V_{CC} < 2.0V$	20 + 0.1Cb		450	
Pulse Width of Spikes that are Suppressed by the Input Filter	t_{SP}	SDA and SCL pins only (Note 4)			50	ns
Input Current with an Input Voltage Between 0.1V_{CC} and 0.9V_{CCmax}	I_i	(Note 6)	-10		10	µA
Input Capacitance	C_i	(Note 4)			10	pF
SCL Clock Frequency (Note 7)	f_{SCL}	$V_{CC} \geq 2.0V$			400	kHz
		$V_{CC} < 2.0V$			344	
Bus Time-out	$t_{TIMEOUT}$	(Note 7)	25		75	ms
Hold Time (Repeated) START Condition. After this Period, the First Clock Pulse is Generated.	$t_{HD:STA}$	(Note 8)	0.6			µs
LOW Period of the SCL Clock (Note 8)	t_{LOW}	$V_{CC} \geq 2.7V$	1.3			µs
		$V_{CC} \geq 2.0V$	1.5			
		$V_{CC} < 2.0V$	2.3			
HIGH Period of the SCL Clock	t_{HIGH}	(Note 8)	0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$	(Note 8)	0.6			µs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time (Notes 9, 10)	$t_{HD:DAT}$	$V_{CC} \geq 2.7V$	0.3		0.9	µs
		$V_{CC} \geq 2.0V$	0.3		1.1	
		$V_{CC} < 2.0V$	0.3		1.7	
Data Setup Time	$t_{SU:DAT}$	(Notes 8, 11)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Note 8)	0.6			µs
Bus Free Time Between a STOP and START Condition	t_{BUF}	(Note 8)	1.3			µs
Capacitive Load for Each Bus Line	C_b	(Notes 4, 8)			400	pF

Note 1: Specifications at -40°C are guaranteed by design and characterization only and not production tested.
Note 2: All values are referred to V_{IHmin} and V_{ILmax} levels.
Note 3: The maximum specification value is guaranteed by design, not production tested.
Note 4: Not production tested. Guaranteed by design or characterization.
Note 5: C_B = total capacitance of one bus line in pF. If mixed with HS-mode devices, faster fall-times according to I^2C-Bus Specification v2.1 are allowed.
Note 6: The DS28CM00 does not obstruct the SDA and SCL lines if V_{CC} is switched off.
Note 7: The minimum SCL clock frequency is limited by the bus timeout feature. If the CM bit is 1 AND SCL stays at the same logic level or SDA stays low for this interval, the DS28CM00 behaves as though it has sensed a STOP condition.
Note 8: System Requirement
Note 9: The DS28CM00 provides a hold time of at least 300ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 10: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 11: A Fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + $t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I²C-bus specification) before the SCL line is released.

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	SCL	Serial interface clock input; must be tied to V_{CC} through a pullup resistor. 5V tolerant input over 1.62V to 5.25V V_{CC} range.
2	GND	Ground supply for the device.
3	SDA	Serial interface bi-directional data line; must be tied to V_{CC} through a pullup resistor. 5V tolerant input/output over 1.62V to 5.25V V_{CC} range.
4	N.C.	Not Connected
5	V_{CC}	Power Supply Input

OVERVIEW

The DS28CM00 consists of a serial interface which provides access to a unique 64-bit Registration number and a Control Register, as shown in the block diagram in Figure 1. The device communicates with a host processor through its SMBus compatible I²C bus interface in standard-mode or in fast-mode. Since the network address of the DS28CM00 is fixed, exactly one device can reside on a bus segment. The Registration Number and Control Register are located in a linear 9-byte address space (Figure 2).

Figure 1. Block Diagram

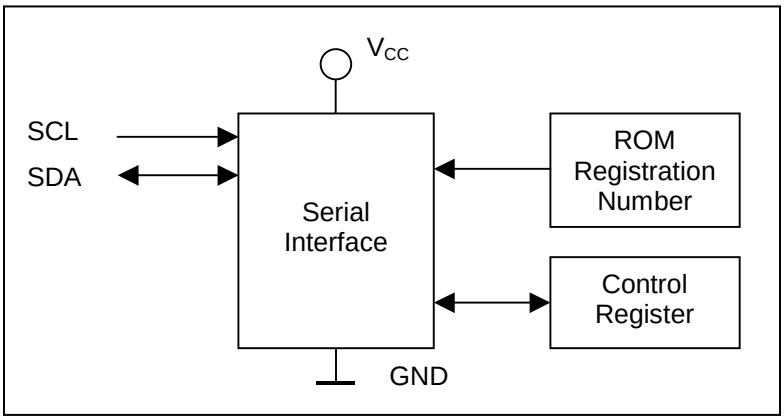


Figure 2. Memory Map

ADDRESS	TYPE	ACCESS	DESCRIPTION
00h	ROM	Read	Device Family Code (70h)
01h	ROM	Read	Serial Number, bits 0 to 7
02h	ROM	Read	Serial Number, bits 8 to 15
03h	ROM	Read	Serial Number, bits 16 to 23
04h	ROM	Read	Serial Number, bits 24 to 31
05h	ROM	Read	Serial Number, bits 32 to 39
06h	ROM	Read	Serial Number, bits 40 to 47
07h	ROM	Read	CRC of Family Code and 48-bit Serial Number
08h	SRAM	R/W	Control Register

Unique Registration Number

Each DS28CM00 has a unique Registration Number that is 64 bits long. The registration number begins with the family code at address 00h followed by the 48-bit serial number (LS-byte at the lower address) and ends at address 07h with the CRC (Cyclic Redundancy Check) of the first 56 bits. This CRC is generated using the polynomial $X^8 + X^5 + X^4 + 1$. Additional information about CRCs is available in *Application Note 27*. The ROM Registration Number is not related to the I²C slave address of the device.

Control Register

The Control Register at address 08h allows switching between I²C mode and SMBus mode. Only the LS bit of this register, referred to as the CM bit, has a function. The other 7 bits always read 0 and cannot be changed. When the CM bit is set to 1 (power-on default), the device is in SMBus mode, which enables the bus timeout function. Setting the CM bit to 0 puts the device in I²C mode, where the timeout function is disabled. In SMBus mode, the serial interface times out and is internally reset if SCL is stuck (high or low) or if SDA is stuck low for the duration of $t_{TIMEOUT}$ or longer. This reset turns the SDA line into an input, ensuring that the device is ready to recognize a communication start condition.

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
08h	0	0	0	0	0	0	0	CM

DEVICE OPERATION

Typically, the DS28CM00 is accessed after power-up to read the 64-bit Registration number, which may serve to identify the object that the device is embedded in. Write access exists only to the Control Register. Read and write access are controlled through the I²C/SMBus serial interface. See section *Read and Write* for details.

Serial Communication Interface

General Characteristics

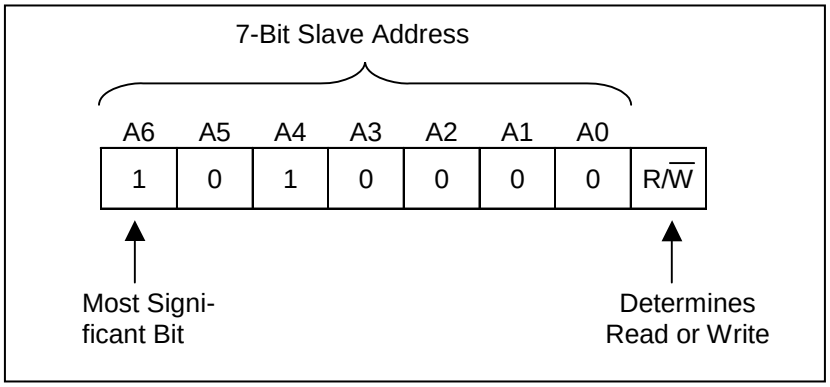
The serial interface uses a data line (SDA) plus a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data can be transferred at rates of up to 100kbps in the Standard-mode, up to 400kbps in the Fast-mode. The DS28CM00 works in both modes.

A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the communication is called a “master.” The devices that are controlled by the master are “slaves.” The DS28CM00 is a slave device.

Slave Address/Direction Byte

To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus. The slave address to which the DS28CM00 responds is shown in Figure 3. The slave address is part of the slave-address/direction byte. The last bit of the slave-address/direction byte (R/$\overline{W}$) defines the data direction. When set to a 0, subsequent data will flow from master to slave (write access mode); when set to a 1, data will flow from slave to master (read access mode).

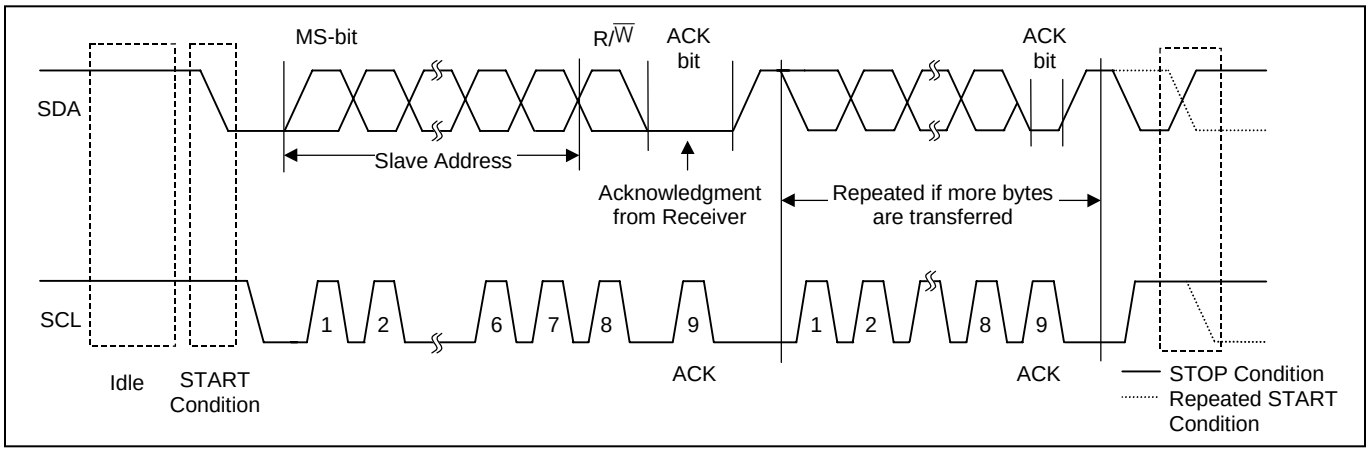
Figure 3. DS28CM00 Slave Address



I²C/SMBus Protocol

Data transfers may be initiated only when the bus is not busy. The master generates the serial clock (SCL), controls the bus access, generates the START and STOP conditions, and determines the number of bytes transferred between START and STOP (Figure 4). Data is transferred in bytes with the most significant bit being transmitted first. After each byte follows an acknowledge bit to allow synchronization between master and slave. During any data transfer, SDA must remain stable whenever the clock line is HIGH. Changes in SDA line while SCL is high will be interpreted as a START or a STOP. The protocol is illustrated in Figure 4. For detailed timing references see Figure 5.

Figure 4. I²C/SMBus Protocol Overview



Bus Idle or Not Busy
Both, SDA and SCL, are inactive, i. e., in their logic HIGH states.

START Condition
To initiate communication with a slave, the master has to generate a START condition. A START condition is defined as a change in state of SDA from HIGH to LOW while SCL remains HIGH.

STOP Condition
To end communication with a slave, the master has to generate a STOP condition. A STOP condition is defined as a change in state of SDA from LOW to HIGH while SCL remains HIGH.

Repeated START Condition
Repeated starts are commonly used for read accesses to select a specific data source or address to read from. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without leaving the bus idle after a STOP condition.

Data Valid
With the exception of the START and STOP condition, transitions of SDA may occur only during the LOW state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL, see Figure 5). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of the SCL pulse.

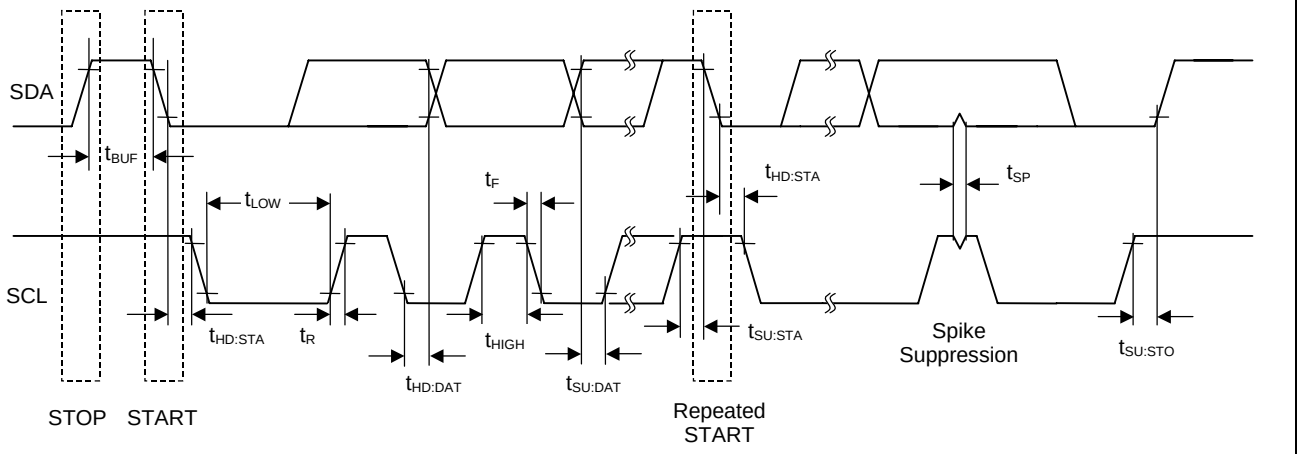
When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum $t_{SU:DAT}$ + t_R in Figure 5) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

Acknowledged
Usually, a receiving device, when addressed, is obliged to generate an acknowledge after the receipt of each byte. The master must generate a clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull SDA LOW during the acknowledge clock pulse in such a way that SDA is stable LOW during the HIGH period of the acknowledge-related clock pulse plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL).

Not Acknowledged by Slave
A slave device may be unable to receive or transmit data, e.g., because it is busy. As a SMBus-compatible device, the DS28CM00 will always acknowledge its slave address. However, some time later the slave may refuse to accept data, e.g., because of an invalid memory address or access mode, e. g. attempting to write to a ROM byte. In this case the slave device will not acknowledge any of the bytes that it refuses and will leave SDA HIGH. After a slave has failed to acknowledge, the master should generate a repeated START condition or a STOP condition followed by a START condition to begin a new data transfer.

Not Acknowledged by Master
At some time when receiving data, the master must signal an end of data to the slave device. To achieve this, the master does not acknowledge the last byte that it has received from the slave. In response, the slave releases SDA, allowing the master to generate the STOP condition.

Figure 5. I²C/SMBus Timing Diagram



NOTE: Timing is referenced to V_{ILMAX} and V_{IHMIN}.

Read and Write

The DS28CM00 behaves like an I²C memory device with an 9-byte memory map (Figure 2). The memory consists of 8 bytes ROM and one byte SRAM, i. e., the Control Register. The ROM data cannot be changed.

To write to the DS28CM00, the master must access the device in write access mode, i.e., the slave address must be sent with the direction bit set to 0. The next byte to be sent in write access mode is an address byte to set the address pointer to a specific location. The DS28CM00 acknowledges any address between 00h and 08h. Write attempts to the ROM are ignored and data received for these addresses is not acknowledged. However, the address pointer increments after every full data byte transmitted by the master and rolls over from 08h to 00h after a full data byte is written to address 08h.

To read from the DS28CM00, the master must access the device in read access mode, i.e., the slave address must be sent with the direction bit set to 1. The address pointer determines the location from which the master will start reading. The pointer is set when the DS28CM00 is accessed in write access mode, as described above. The power-on default of the pointer is 00h. When reading from the device, the address pointer increments with every data byte read. When the end of the memory is reached (address 08h), the address pointer wraps around to 00h. To read from an arbitrary address, the master must first access the DS28CM00 in write access mode and specify a new memory address. The address pointer remains unchanged if the device resets its communication interface due to a bus timeout in SMBus mode.

I²C Communication—Legend

SYMBOL	DESCRIPTION
S	START Condition
AD,0	Select DS28CM00 for Write Access
AD,1	Select DS28CM00 for Read Access
Sr	Repeated START Condition
P	STOP Condition

SYMBOL	DESCRIPTION
A	Acknowledged
A\	Not Acknowledged
<byte>	Transfer of One Byte
VMA	Valid Memory Address (00h to 08h)
IMA	Invalid Memory Address

Command-Specific Communication—Color-Codes

Master-to-Slave	Slave-to-Master

Communication Examples

Write to Control Register (address 08)

S	AD,0	A	08h	A	<byte>	A	P

Write to ROM Address (excludes address 08)

S	AD,0	A	VMA	A	<byte>	A\	P

data is not accepted

Write to invalid address (>08)

S	AD,0	A	IMA	A\	P

address is not accepted

Read

S	AD,0	A	VMA	A	Sr	AD,1	A	<byte>	A	<byte>	A\	P

Set address pointer

one or more bytes

last byte

Application Information

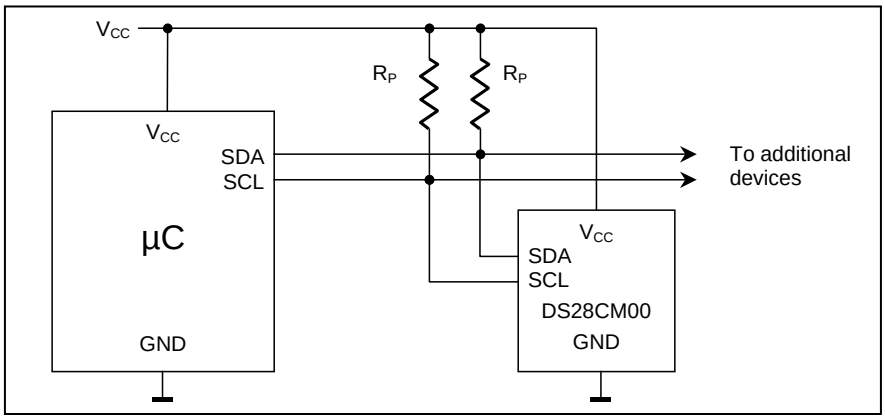
SDA and SCL Pullup Resistors

SDA is an open-drain output on the DS28CM00 that requires a pullup resistor (Figure 6) to realize high logic levels. Because the DS28CM00 uses SCL only as input (no clock stretching) the master can drive SCL either through an open-drain/collector output with a pullup resistor or a push-pull output.

Pullup Resistor R_P Sizing

According to the I²C specification, a slave device must be able to sink at least 3mA at a V_{OL} of 0.4V. The SMBus specification requires a current sink capability of 4mA at 0.4V. The DS28CM00 can sink at least 4mA at 0.4V V_{OL} over its entire operating voltage range. This DC characteristic determines the minimum value of the pullup resistor: **Rpmin = (V_{CC} - 0.4V)/4mA.** With a maximum operating voltage of 5.25V, the minimum value for the pullup resistor is 1.2kΩ. The "Minimum RP" line in Figure 7 shows how the minimum pullup resistor changes with the operating (pullup) voltage.

Figure 6. Application Schematic

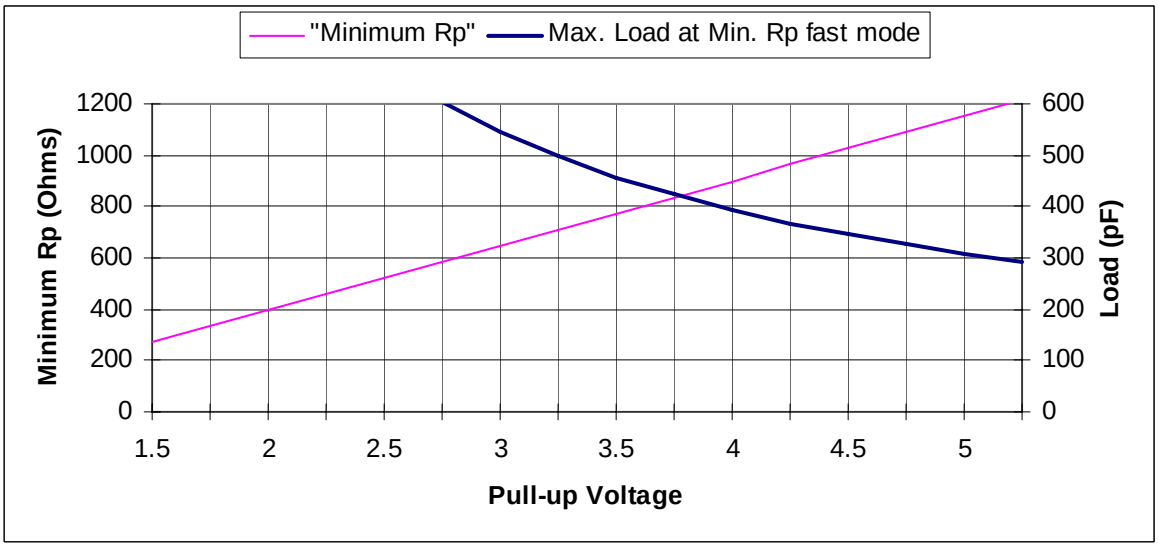


For I²C systems, the rise time and fall time are measured from 30% to 70% of the pullup voltage. The maximum bus capacitance C_B is 400pF. The maximum rise time must not exceed 300ns. Assuming maximum rise time, the maximum resistor value at any given capacitance C_B is calculated as: R_{PMAX} = 300ns/(C_B*ln(7/3)). For a bus capacitance of 400pF the maximum pullup resistor would be 885Ω.

Since a 885Ω pullup resistor, as would be required to meet the rise time specification and 400pF bus capacitance, is lower than R_{PMIN} at 5.25V, a different approach is necessary. The "Max. Load…" line in Figure 7 is generated by first calculating the minimum pullup resistor at any given operating voltage ("Minimum R_P" line) and then calculating the respective bus capacitance that yields a rise time of 300ns.

Only for pullup voltages of 4V and lower can the maximum permissible bus capacitance of 400pF be maintained. A reduced bus capacitance of 300pF is acceptable for the entire operating voltage range. The corresponding pullup resistor value at the voltage is indicated by the "Minimum R_P" line.

Figure 7. I²C Fast Speed Pullup Resistor Selection Chart



PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)