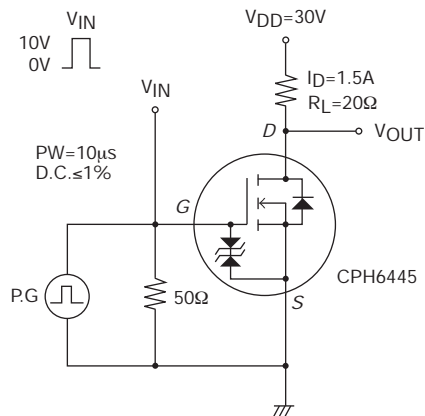


Electrical Characteristics at Ta=25°C

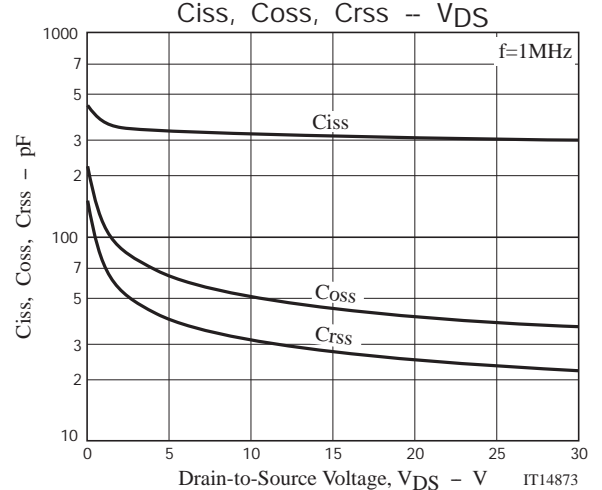
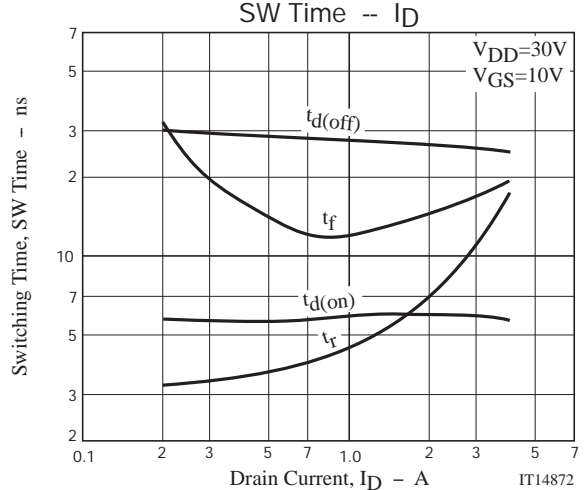
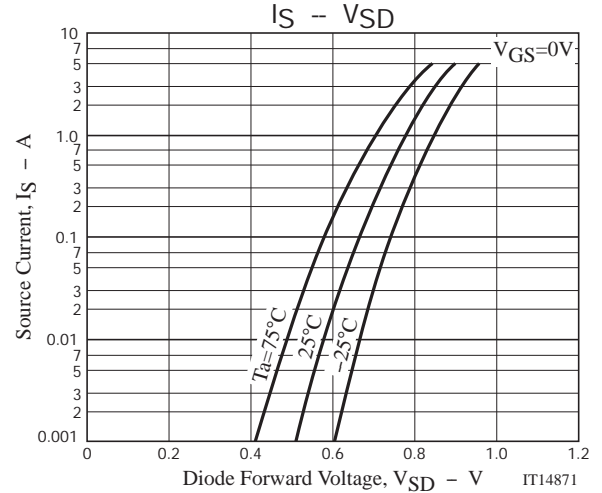
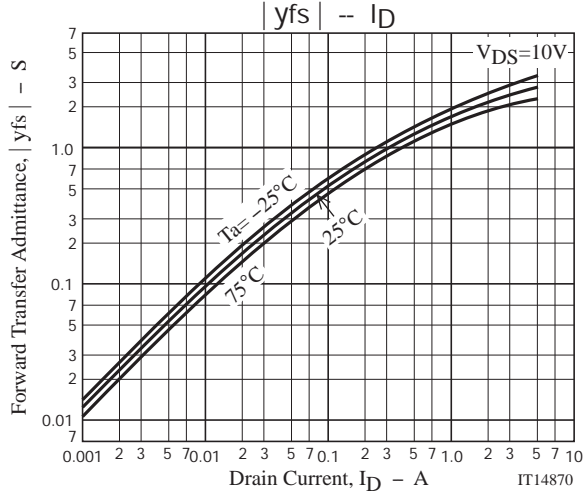
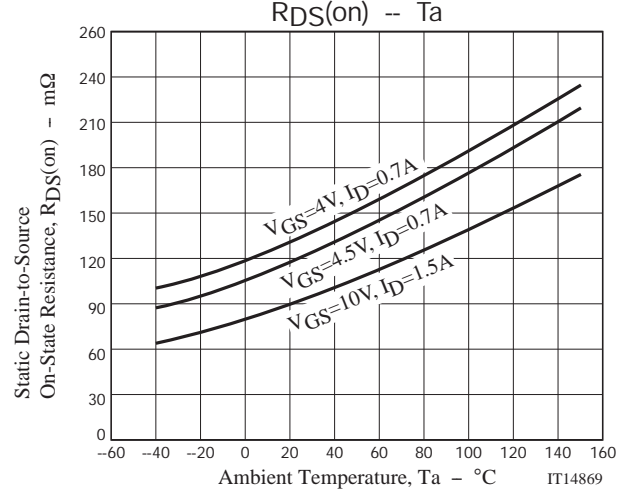
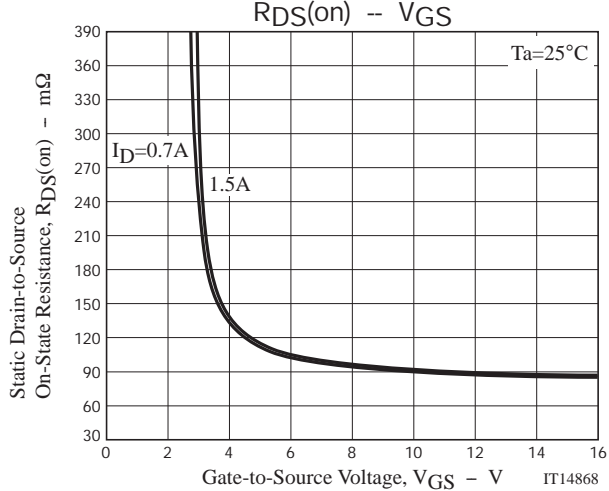
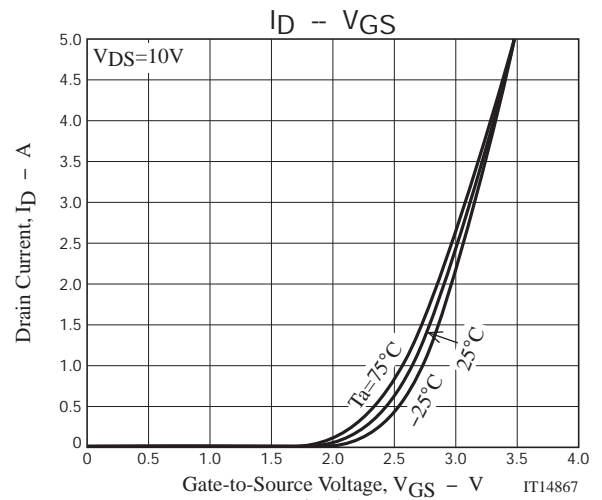
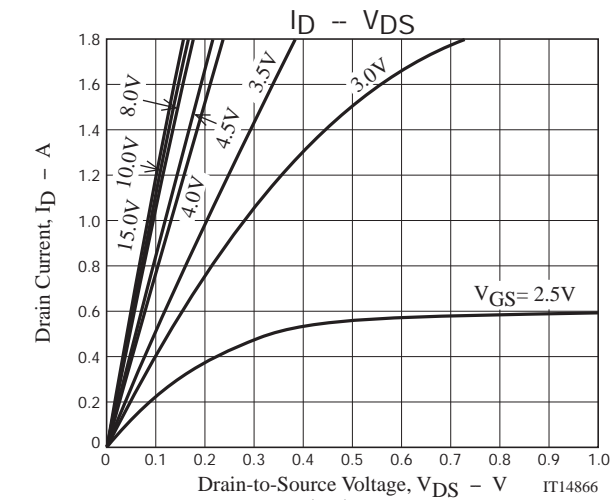
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=1mA, V_{GS}=0V$	60			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$			1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 16V, V_{DS}=0V$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS}=10V, I_D=1mA$	1.2		2.6	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS}=10V, I_D=1.5A$	1.2	2.0		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D=1.5A, V_{GS}=10V$		92	117	$m\Omega$
	$R_{DS(on)2}$	$I_D=0.7A, V_{GS}=4.5V$		120	168	$m\Omega$
	$R_{DS(on)3}$	$I_D=0.7A, V_{GS}=4V$		132	185	$m\Omega$
Input Capacitance	C_{iss}	$V_{DS}=20V, f=1MHz$		310		pF
Output Capacitance	C_{oss}			40		pF
Reverse Transfer Capacitance	C_{rss}			25		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		6.0		ns
Rise Time	t_r			5.5		ns
Turn-OFF Delay Time	$t_{d(off)}$			27		ns
Fall Time	t_f			13		ns
Total Gate Charge	Q_g	$V_{DS}=30V, V_{GS}=10V, I_D=3.5A$		6.8		nC
Gate-to-Source Charge	Q_{gs}			1.1		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			1.4		nC
Diode Forward Voltage	V_{SD}	$I_S=3.5A, V_{GS}=0V$		0.85	1.2	V

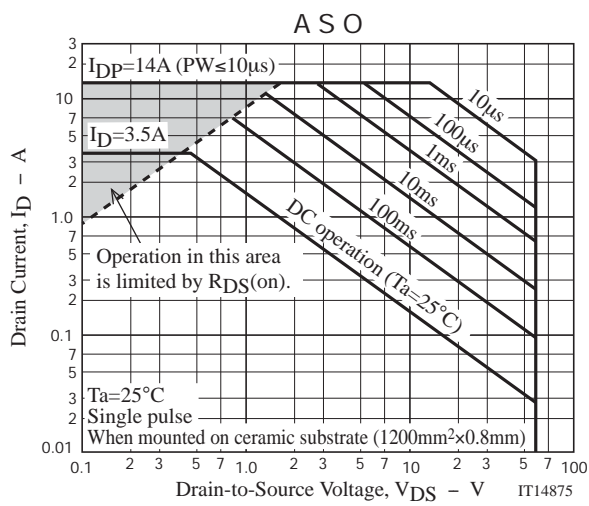
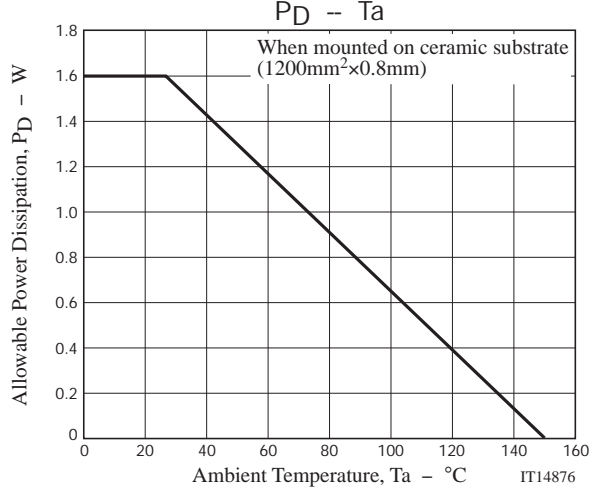
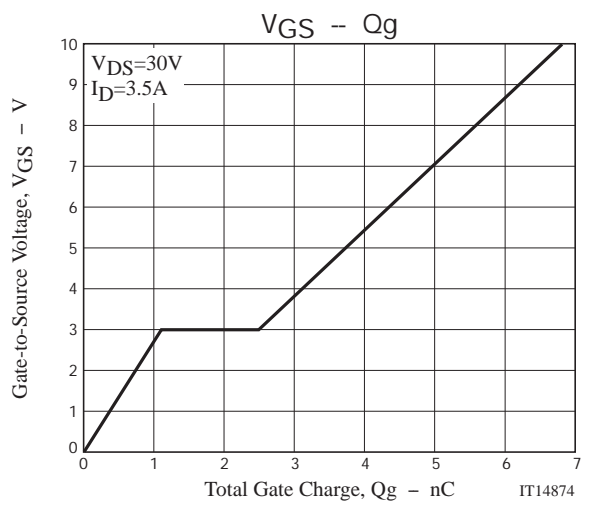
Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
CPH6445-TL-E	CPH6	3,000pcs./reel	Pb Free





Embossed Taping Specification

CPH6445-TL-E

1. Packing Format

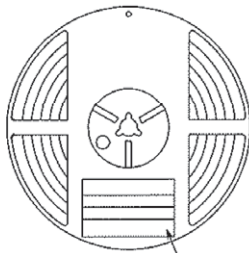
Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
CPH6	CPH6	3,000	15,000	90,000	5 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Reel label, Inner box label
(unit:mm)

Outer box label

It is a label at the time of factory shipments.
The form of a label may change in physical distribution process.

Packing method



Reel label

Type No.
LOT No.
Quantity
Origin

TYPE	000000000
LOT	00
QTY	0,000 (1) LEAD FREE *
SPECIAL	*20722005310C*
ASSEMBLY	**** (DIFFUSION:****)

NOTE (1)

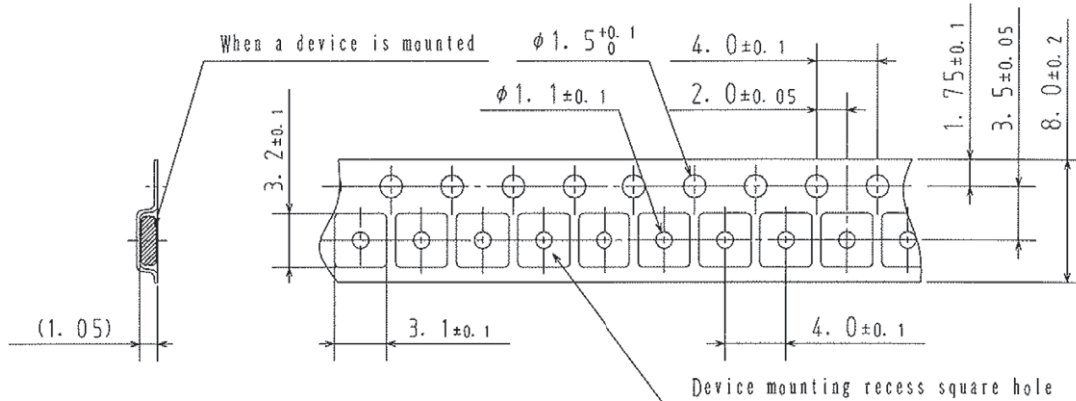
The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

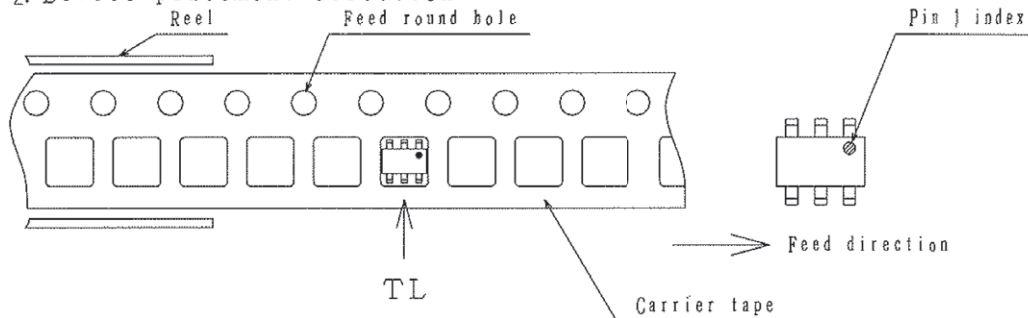
TYPE CODE	*****
TYPE	*****
QTY	0,000 PCS (1) LEAD FREE *
LOT	*****
PACKAGE	*****
SPECIAL	*20722005310C*
ASSEMBLY	**** (DIFFUSION:****)

2. Taping configuration

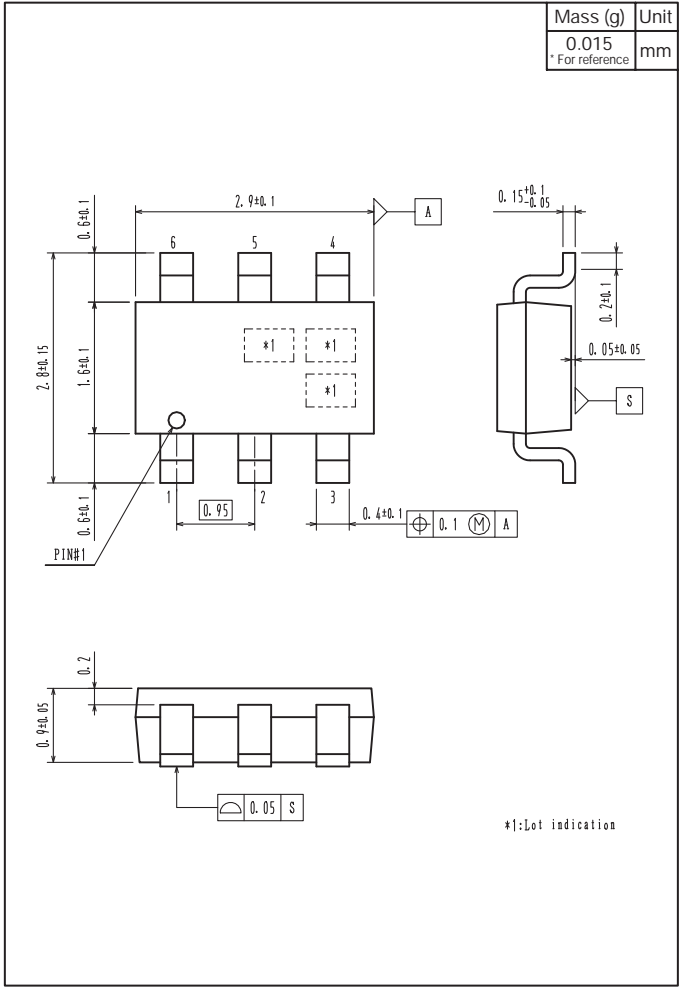
2-1. Carrier tape size (unit:mm)



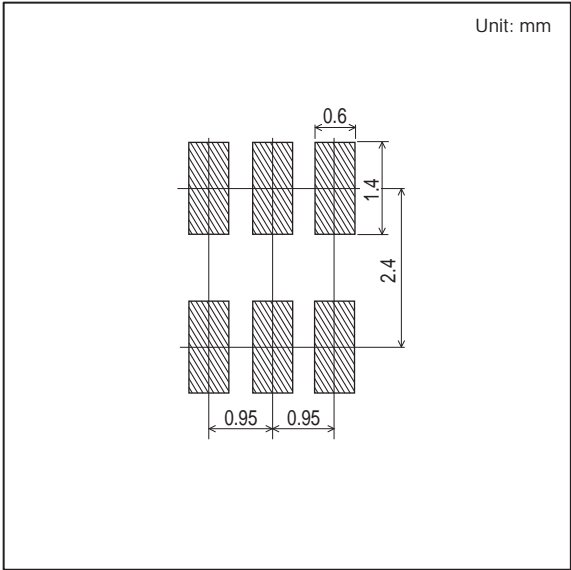
2-2. Device placement direction



Outline Drawing
CPH6445-TL-E



Land Pattern Example



Note on usage : Since the CPH6445 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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