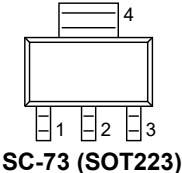
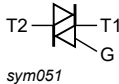


| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------|---------------------------------------|---|-----|-----|-----|------------------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 5 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11 | - | - | 6 | mA |
| V_T | on-state voltage | $I_T = 2\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12 | - | 1.2 | 1.5 | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; (67% of V_{DRM}); exponential waveform; gate open circuit | 20 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 1\text{ A}$; $dV_{com}/dt = 0.1\text{ V}/\mu\text{s}$; gate open circuit | 5 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 1\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit | 1 | - | - | A/ms |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|--------------------------------|---|---|
| 1 | T1 | main terminal 1 |  SC-73 (SOT223) |  sym051 |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| 4 | mb | mounting base; connected to T2 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|---------|--|---------|
| | Name | Description | Version |
| BTA204W-600D | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--------------------------------------|--|-----|-----|------------------|
| V _{DRM} | repetitive peak off-state voltage | | - | 600 | V |
| I _{T(RMS)} | RMS on-state current | full sine wave; T _{sp} ≤ 108 °C; Fig. 1; Fig. 2; Fig. 3 | - | 1 | A |
| I _{TSM} | non-repetitive peak on-state current | full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms | - | 11 | A |
| | | full sine wave; T _{j(init)} = 25 °C; t _p = 20 ms; Fig. 4; Fig. 5 | - | 10 | A |
| I ² t | I ² t for fusing | t _p = 10 ms; SIN | - | 0.5 | A ² s |
| dI _T /dt | rate of rise of on-state current | I _G = 0.2 A | - | 100 | A/μs |
| I _{GM} | peak gate current | | - | 1 | A |
| P _{GM} | peak gate power | | - | 5 | W |
| P _{G(AV)} | average gate power | over any 20ms period | - | 0.5 | W |
| T _{stg} | storage temperature | | -40 | 150 | °C |
| T _j | junction temperature | | - | 125 | °C |

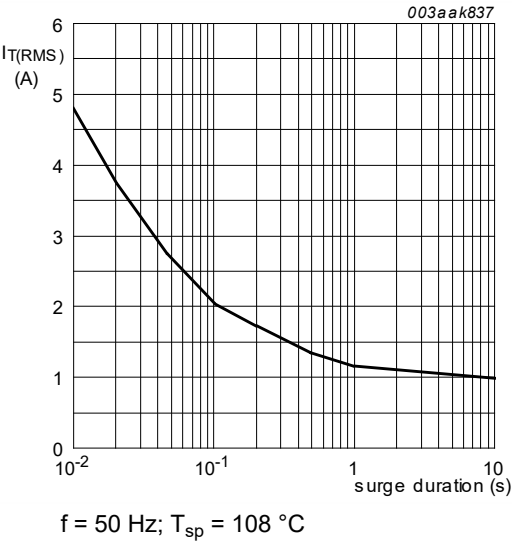


Fig. 1. RMS on-state current as a function of surge duration; maximum values

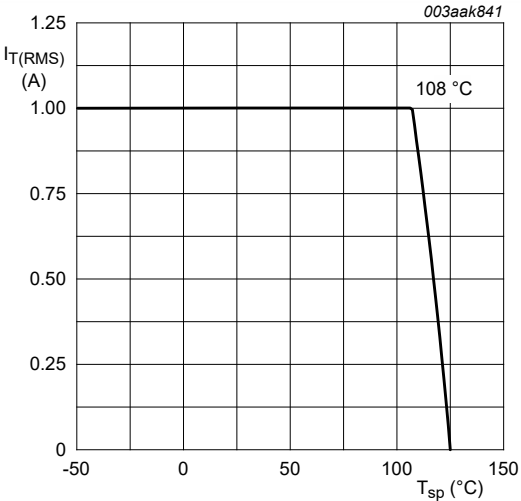
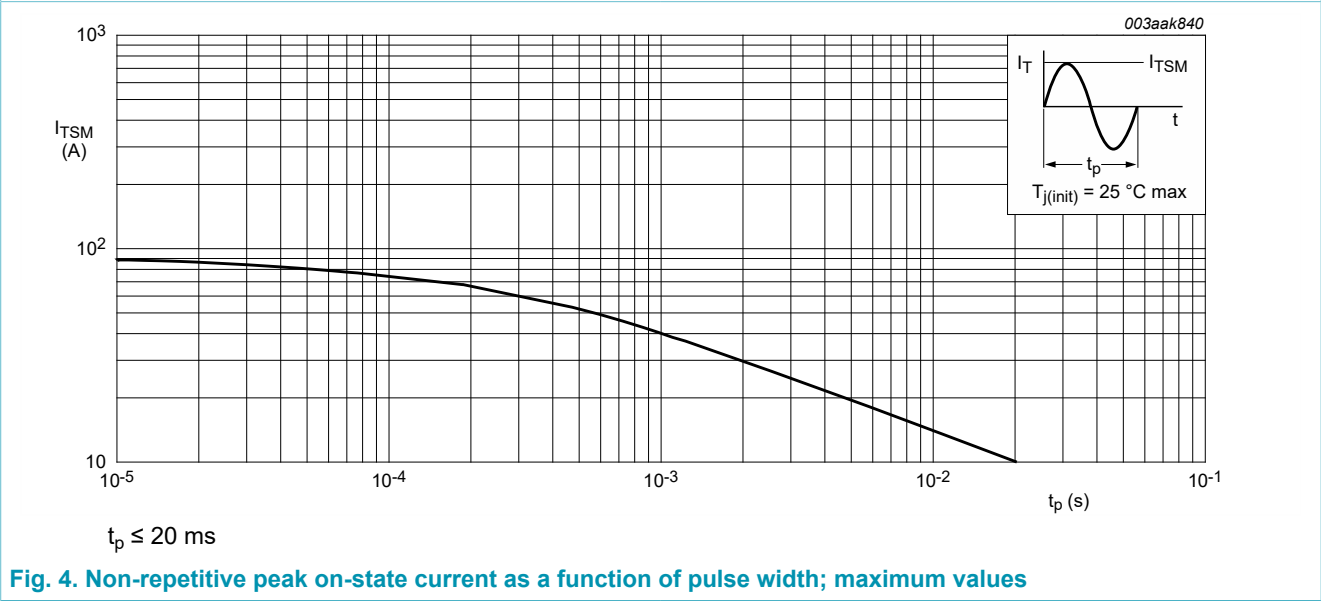
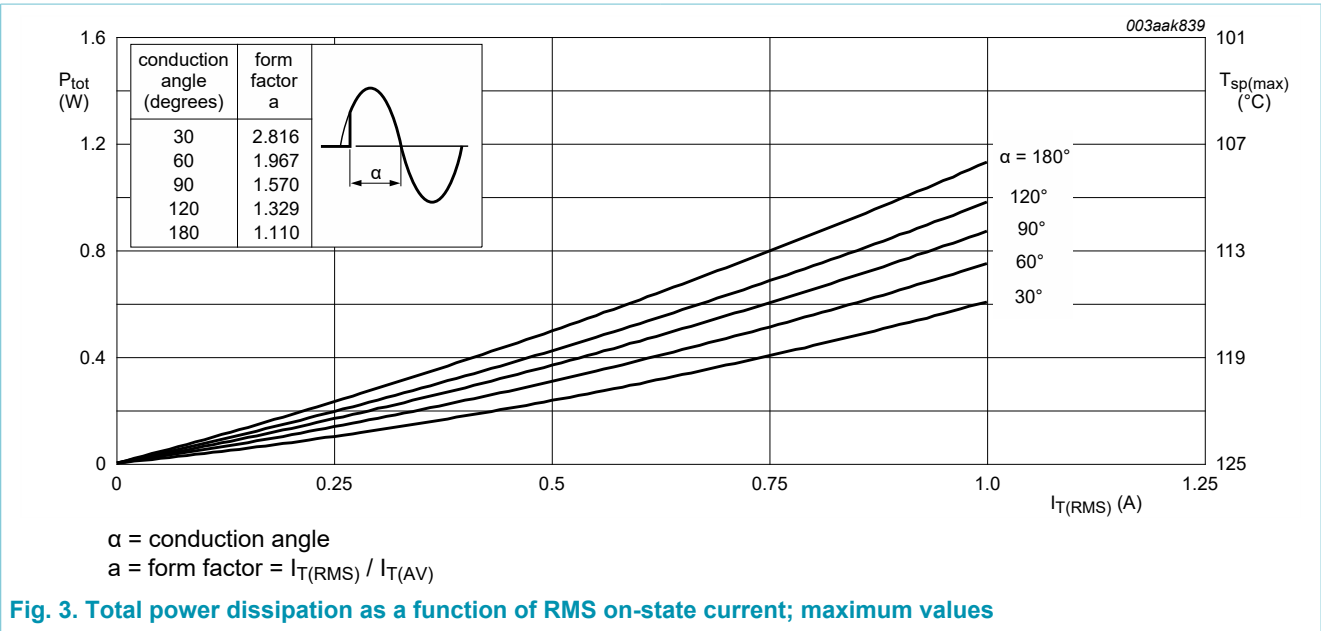
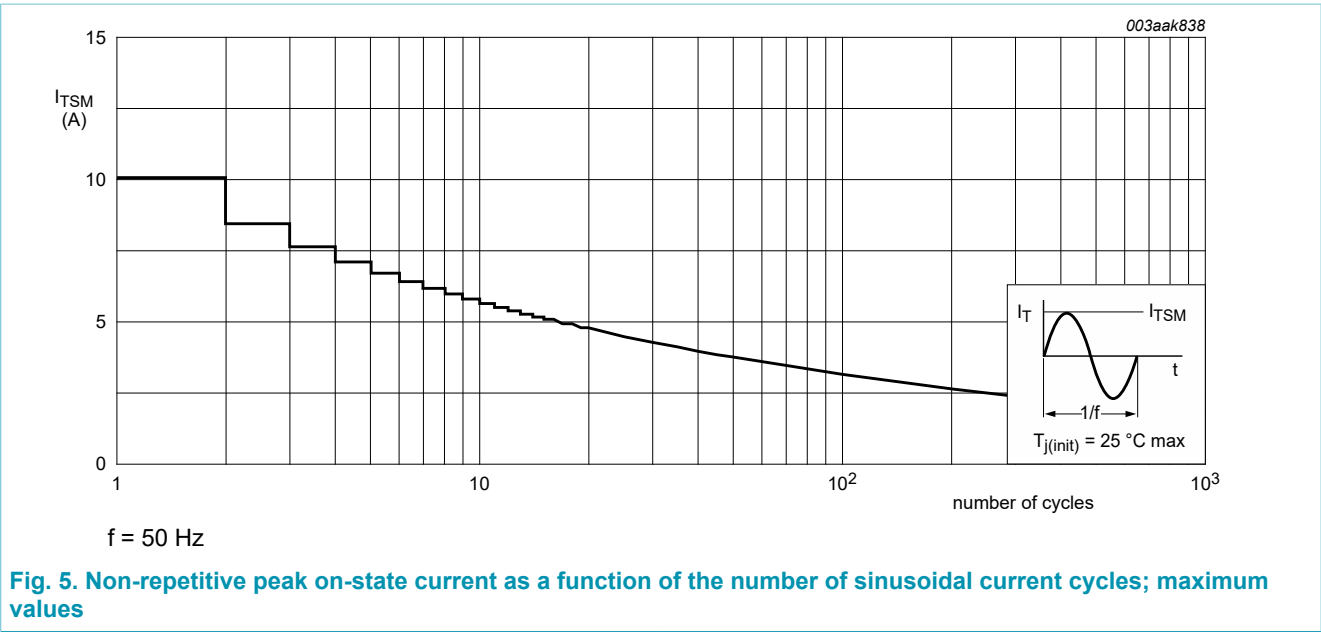


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

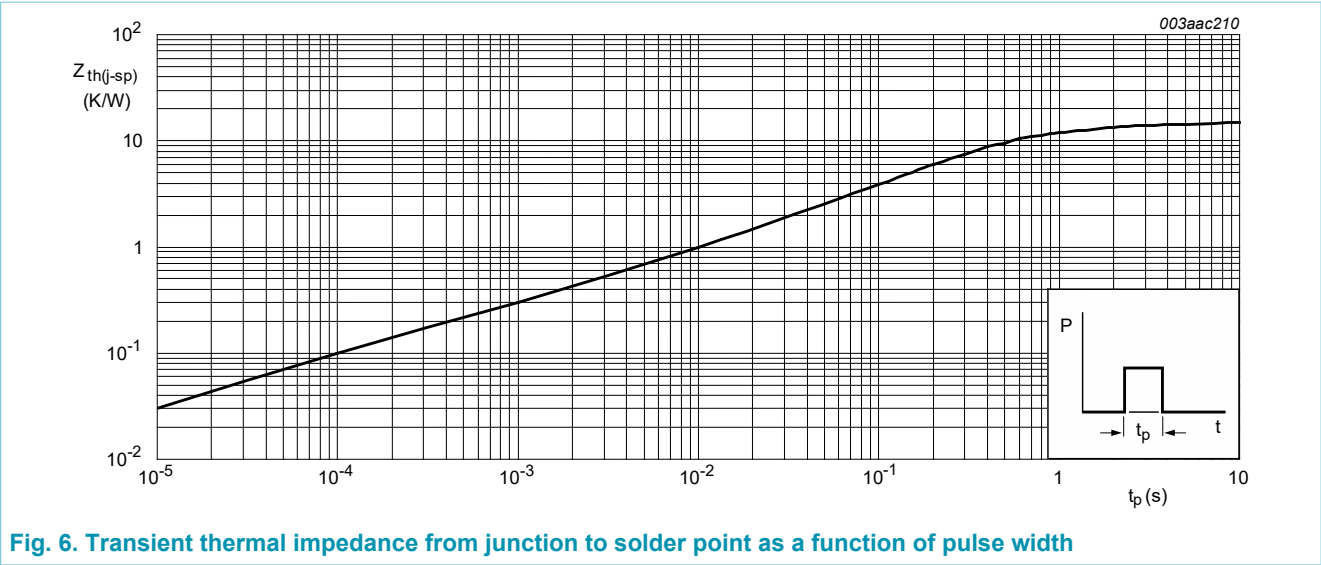


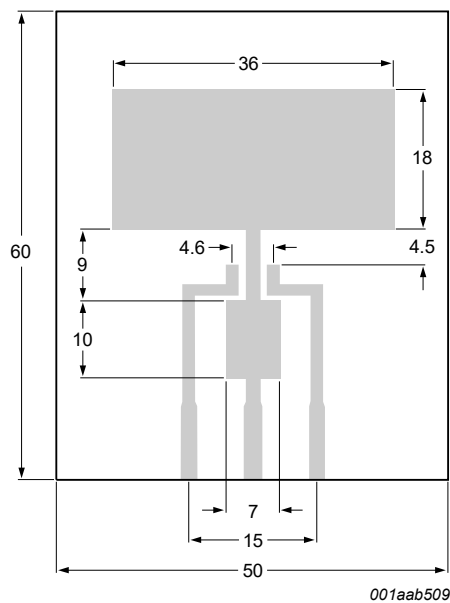


8. Thermal characteristics

Table 5. Thermal characteristics

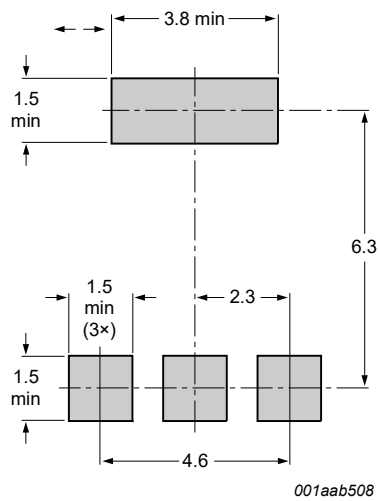
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|--|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | full cycle or half cycle; Fig. 6 | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | printed circuit board mounted: minimum pad area; Fig. 7 | - | 70 | - | K/W |
| | | printed circuit board mounted: minimum footprint; Fig. 8 | - | 156 | - | K/W |





All dimensions are in mm
Printed circuit board:
FR4 epoxy glass (1.6 mm thick), copper laminate
(35 um thick)

Fig. 7. Printed circuit board pad area: SOT223



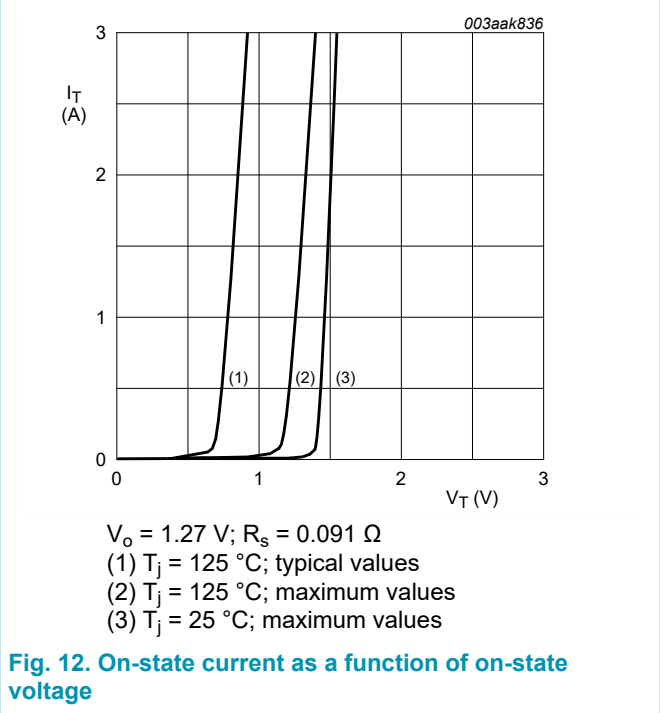
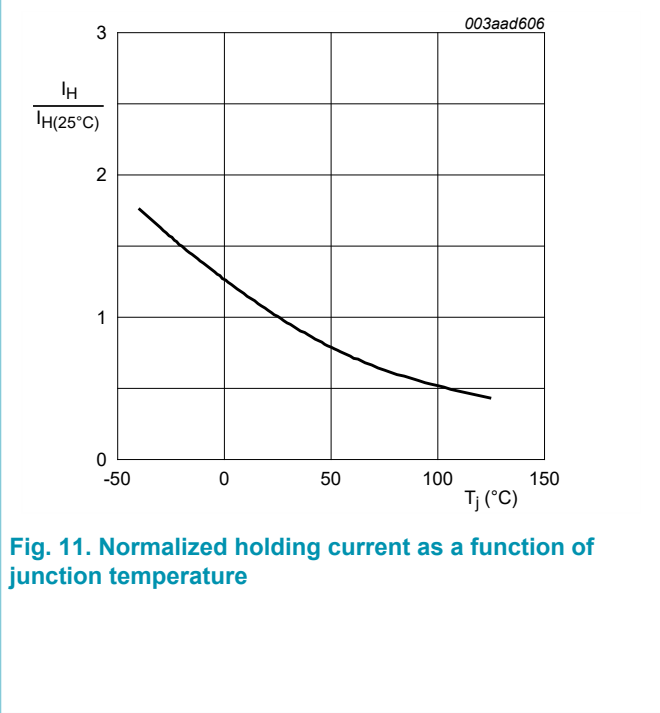
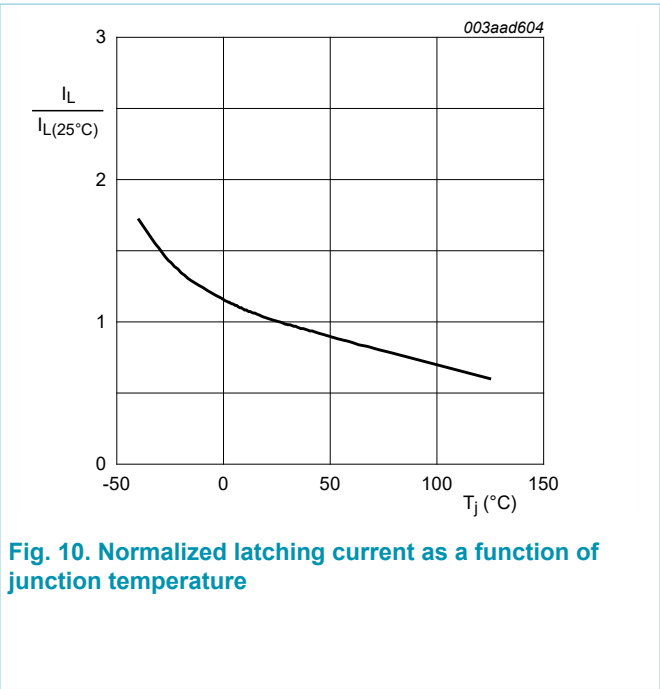
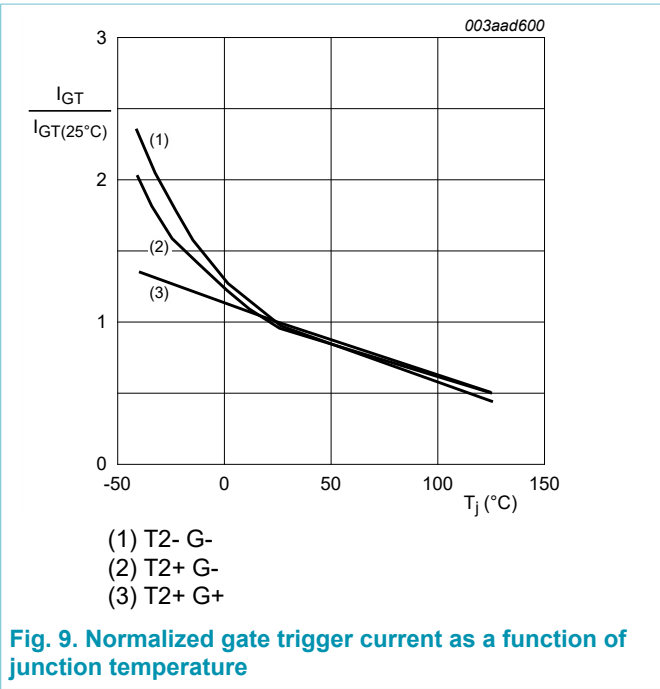
All dimensions are in mm

Fig. 8. Minimum footprint SOT223

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|------|-----|-----|------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 5 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9 | - | - | 5 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | - | 6 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | - | 9 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10 | - | - | 6 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11 | - | - | 6 | mA |
| V_T | on-state voltage | $I_T = 2\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12 | - | 1.2 | 1.5 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 13 | - | 0.7 | 1 | V |
| | | $V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 13 | 0.25 | 0.4 | - | V |
| I_D | off-state current | $V_D = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$ | - | 0.1 | 0.5 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; (67% of V_{DRM}); exponential waveform; gate open circuit | 20 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 1\text{ A}$; $dV_{com}/dt = 0.1\text{ V}/\mu\text{s}$; gate open circuit | 5 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{T(RMS)} = 1\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit | 1 | - | - | A/ms |



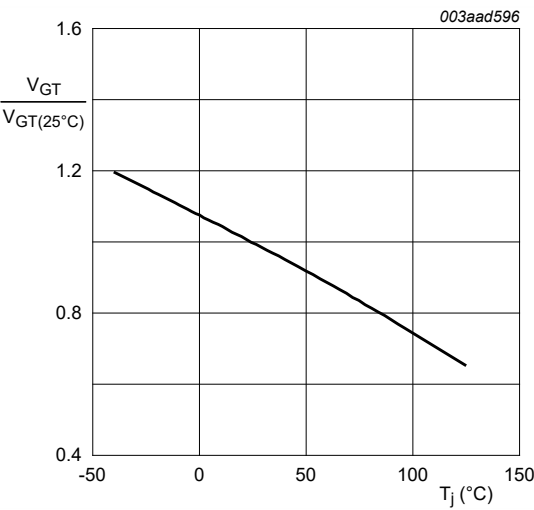
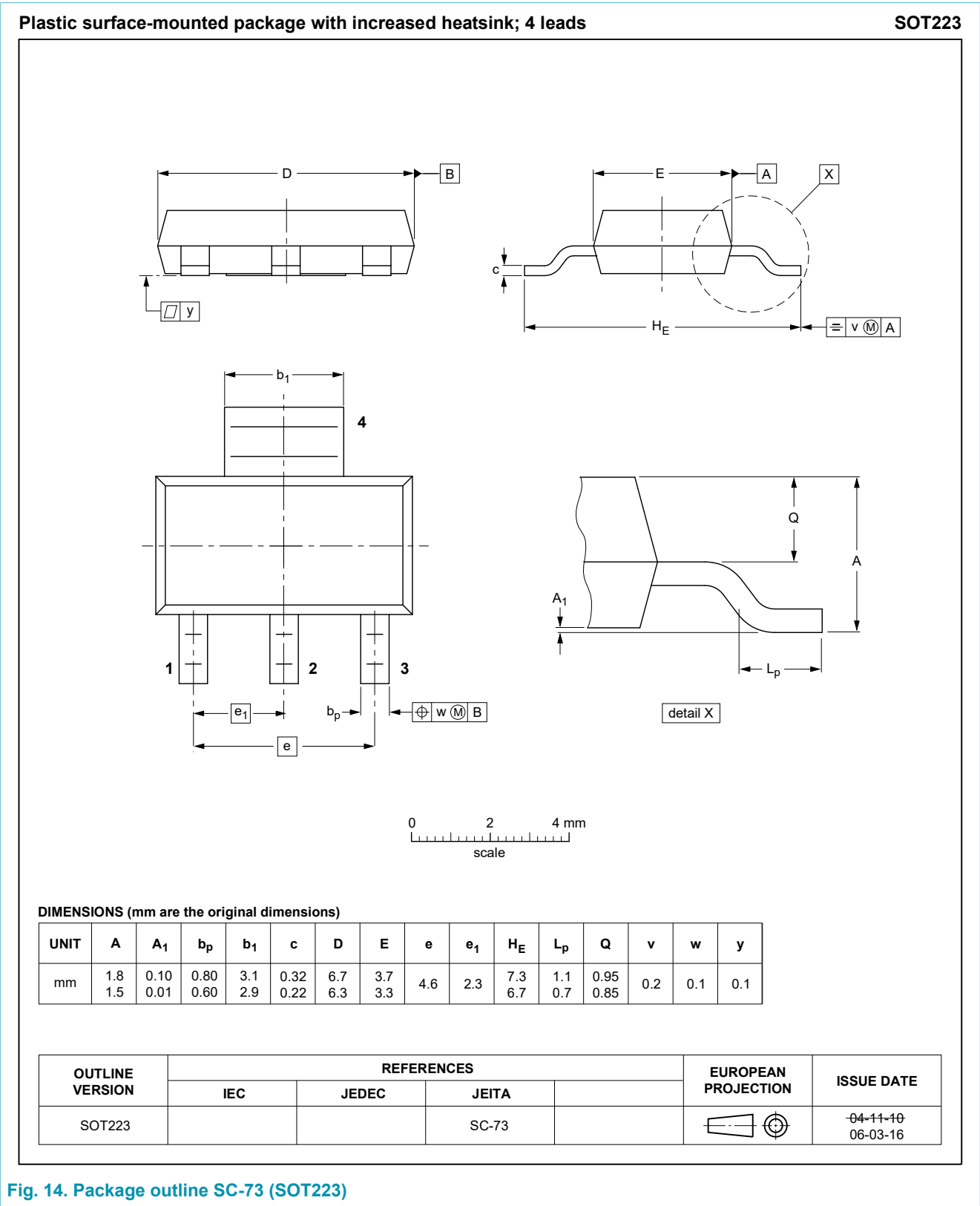


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

10. Package outline



11. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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- [2] The term 'short data sheet' is explained in section "Definitions".
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