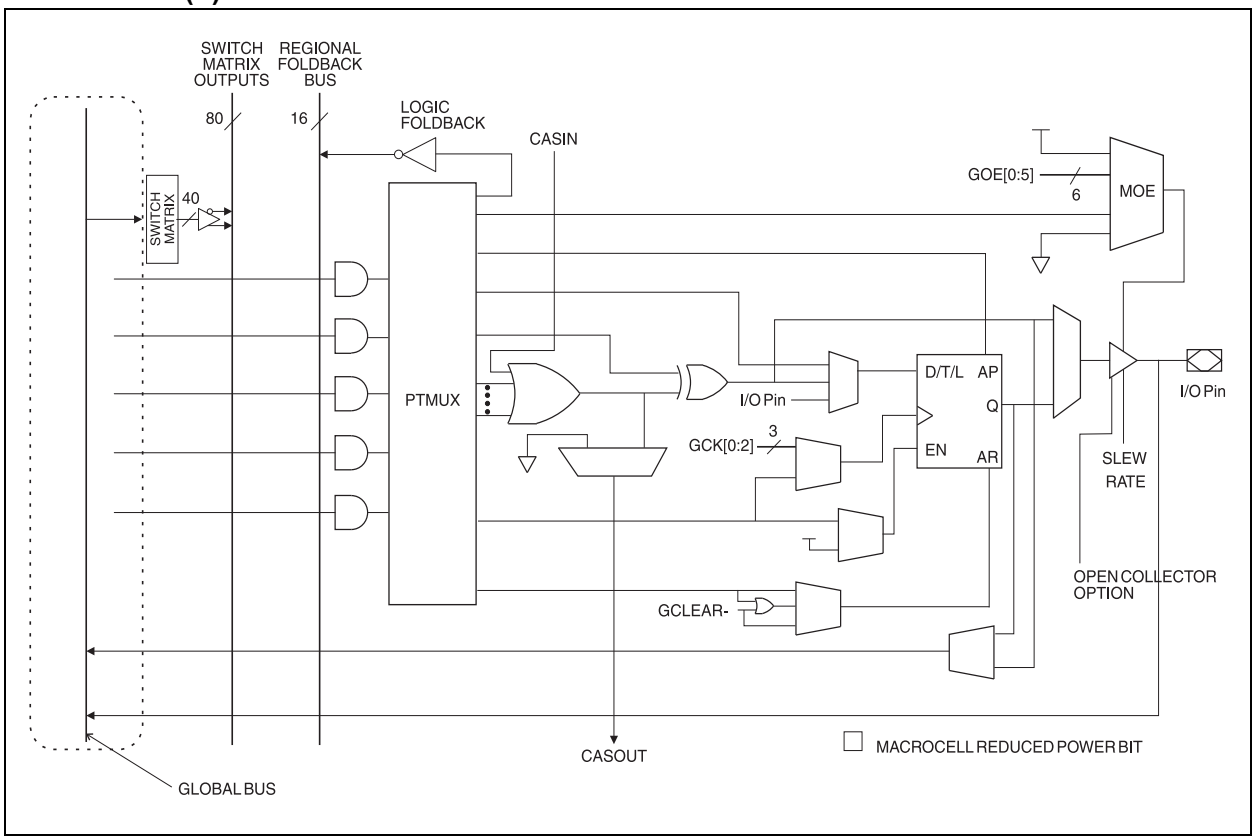
Each of the 64 macrocells generates a buried feedback that goes to the global bus. Each input and I/O pin also feeds into the global bus. The switch matrix in each logic block then selects 40 individual signals from the global bus. Each macrocell also generates a foldback logic term that goes to a regional bus.

Cascade logic between macrocells in the ATF1504-ASV(L) allows fast, efficient generation of complex logic functions. The ATF1504ASV(L) contains four such logic chains, each capable of creating sum term logic with a fan-in of up to 40 product terms.

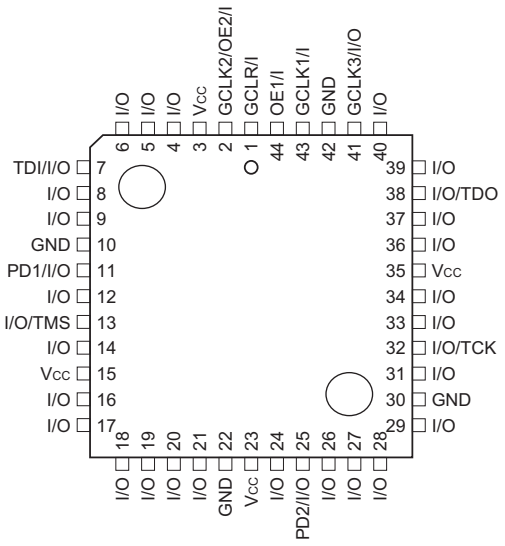
The ATF1504ASV(L) macrocell (see ATF1504ASV(L) Macrocell), is flexible enough to support highly complex logic functions operating at high speed. The macrocell consists of five sections: product terms and product term select multiplexer, OR/XOR/CASCADE logic, a flip-flop, output select and enable, and logic array inputs.

ATF1504ASV(L) Macrocell

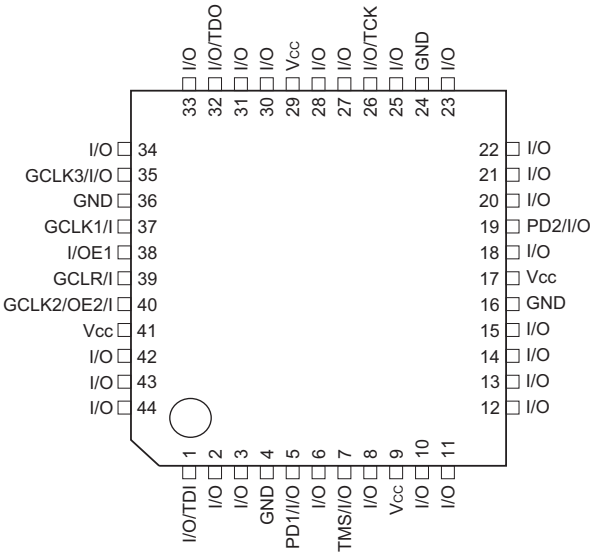


Pin Configurations and Pinouts

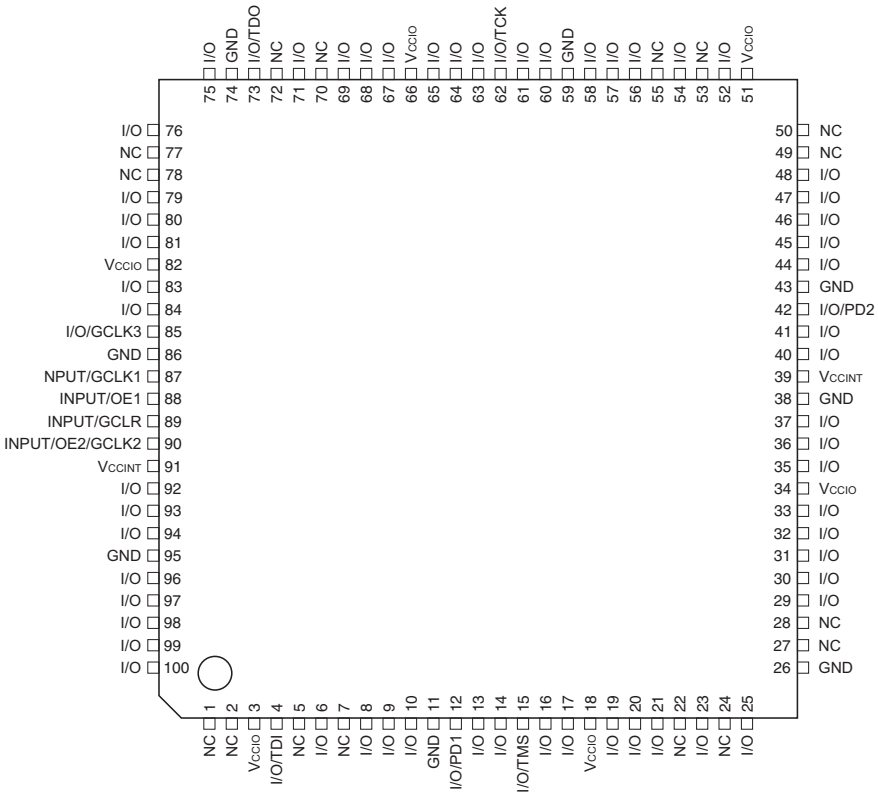
44-Lead PLCC
(Top View)



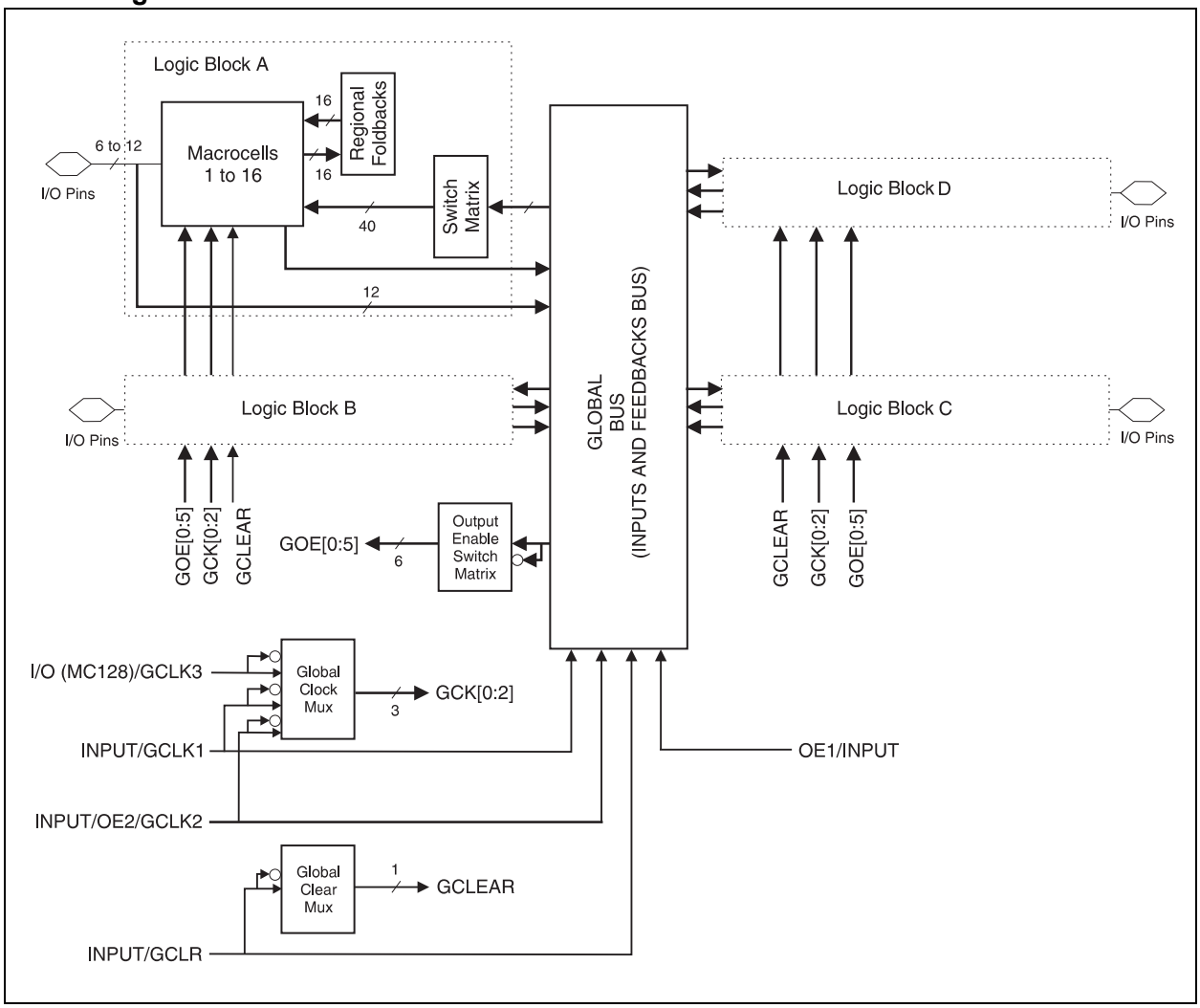
44-Lead TQFP
(Top View)



100-Lead TQFP
(Top View)



Block Diagram



Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF1504ASV(L). Two bytes (16 bits) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

The ATF1504ASV(L) device is an in-system programmable (ISP) device. It uses the industry-standard 4-pin JTAG interface (IEEE Std. 1149.1), and is fully compliant with JTAG's Boundary-scan Description Language (BSDL). ISP allows the device to be programmed without removing it from the printed circuit board. In addition to simplifying the manufacturing flow, ISP also allows design modifications to be made in the field via software.

PRODUCT TERMS AND SELECT MUX

Each ATF1504ASV(L) macrocell has five product terms. Each product term receives as its inputs all signals from both the global bus and regional bus.

The product term select multiplexer (PTMUX) allocates the five product terms as needed to the macrocell logic gates and control signals. The PTMUX programming is determined by the design compiler, which selects the optimum macrocell configuration.

OR/XOR/CASCADE LOGIC

The ATF1504ASV(L)'s logic structure is designed to efficiently support all types of logic. Within a single macrocell, all the product terms can be routed to the OR gate, creating a 5-input AND/OR sum term. With the addition of the CASIN from neighboring macrocells, this can be expanded to as many as 40 product terms with little additional delay.

The macrocell's XOR gate allows efficient implementation of compare and arithmetic functions. One input to the XOR comes from the OR sum term. The other XOR input can be a product term or a fixed high- or low-level. For combinatorial outputs, the fixed level input allows polarity selection. For registered functions, the fixed levels allow DeMorgan minimization of product terms. The XOR gate is also used to emulate T- and JK-type flip-flops.

FLIP-FLOP

The ATF1504ASV(L)'s flip-flop has very flexible data and control functions. The data input can come from either the XOR gate, from a separate product term or directly from the I/O pin. Selecting the separate product term allows creation of a buried registered feedback within a combinatorial output macrocell. (This feature is automatically implemented by the fitter software).

In addition to D, T, JK and SR operation, the flip-flop can also be configured as a flow-through latch. In this mode, data passes through when the clock is high and is latched when the clock is low.

The clock itself can either be one of the Global CLK Signal (GCK[0:2]) or an individual product term. The flip-flop changes state on the clock's rising edge. When the GCK signal is used as the clock, one of the macrocell product terms can be selected as a clock enable. When the clock enable function is active and the enable signal (product term) is low, all clock edges are ignored. The flip-flop's asynchronous Reset signal (AR) can be either the Global Clear (GCLEAR), a product term, or always off. AR can also be a logic OR of GCLEAR with a product term. The asynchronous preset (AP) can be a product term or always off.

EXTRA FEEDBACK

The ATF1504ASV(L) macrocell output can be selected as registered or combinatorial. The extra buried feedback signal can be either combinatorial or a registered signal regardless of whether the output is combinatorial or registered. (This enhancement function is automatically implemented by the fitter software.) Feedback of a buried combinatorial output allows the creation of a second latch within a macrocell.

I/O CONTROL

The output enable multiplexer (MOE) controls the output enable signal. Each I/O can be individually configured as an input, output or for bidirectional operation. The output enable for each macrocell can be selected from the true or compliment of the two output enable pins, a subset of the I/O pins, or a subset of the I/O macrocells. This selection is automatically done by the fitter software when the I/O is configured as an input, all macrocell resources are still available, including the buried feedback, expander and cascade logic.

GLOBAL BUS/SWITCH MATRIX

The global bus contains all input and I/O pin signals as well as the buried feedback signal from all 64 macrocells. The switch matrix in each logic block receives as its inputs all signals from the global bus. Under software control, up to 40 of these signals can be selected as inputs to the logic block.

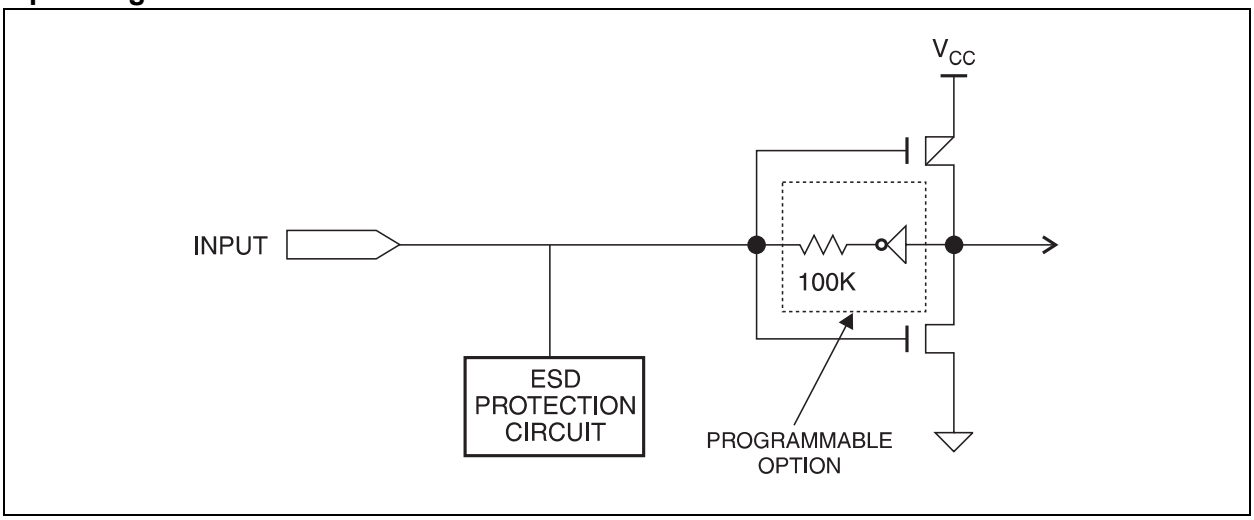
FOLDBACK BUS

Each macrocell also generates a foldback product term. This signal goes to the regional bus and is available to four macrocells. The foldback is an inverse polarity of one of the macrocell's product terms. The four foldback terms in each region allow generation of high fan-in sum terms (up to nine product terms) with little additional delay.

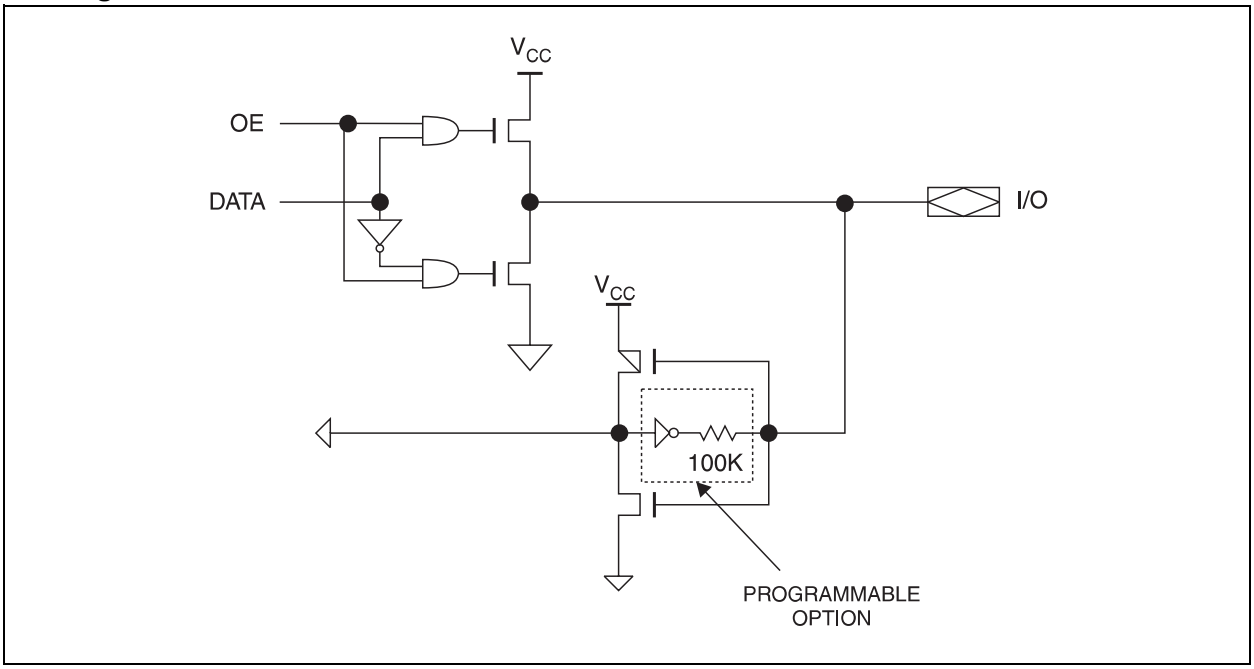
Programmable Pin-Keeper Option for Inputs and I/Os

The ATF1504ASV(L) offers the option of programming all input and I/O pins so that pin-keeper circuits can be utilized. When any pin is driven high or low and then subsequently left floating, it will stay at that previous high or low level. This circuitry prevents unused input and I/O lines from floating to intermediate voltage levels, which causes unnecessary power consumption and system noise. The keeper circuits eliminate the need for external pull-up resistors and eliminate their DC power consumption.

Input Diagram



I/O Diagram



Speed/Power Management

The ATF1504ASV(L) has several built-in speed and power management features. The ATF1504ASVL contains circuitry that automatically puts the device into a low-power Standby mode when no logic transitions are occurring. This not only reduces power consumption during inactive periods, but also provides proportional power savings for most applications running at system speeds below 5 MHz.

To further reduce power, each ATF1504ASV(L) macrocell has a reduced-power bit feature. This feature allows individual macrocells to be configured for maximum power savings. This feature may be selected as a design option.

All ATF1504ASV(L) also have an optional Power-Down mode. In this mode, current drops to below 5 mA. When the power-down option is selected, either PD1 or PD2 pins (or both) can be used to power down the part. The power-down option is selected in the design software or design source file. When enabled, the device goes into power-down when either PD1 or PD2 is high. In the Power-Down mode, all internal logic signals are latched and held, as are any enabled outputs.

All pin transitions are ignored until the PD pin is brought low. When the power-down feature is enabled, the PD1 or PD2 pin cannot be used as a logic input or output. However, the pin's macrocell may still be used to generate buried foldback and cascade logic signals.

All power-down AC characteristic parameters are computed from external input or I/O pins, with reduced-power bit turned on. For macrocells in Reduced-Power mode (reduced-power bit turned on), the reduced-power adder, t_{RPA}, must be added to the AC parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} or t_{ACH}, t_{EN} and t_{SEXP}.

The ATF1504ASV(L) macrocell also has an option whereby the power can be reduced on a per macrocell basis. By enabling this power-down option, macrocells that are not used in an application can be turned down, thereby reducing the overall power consumption of the device. This option is automatically set by the device fitter software.

Each output also has individual slew rate control. This may be used to reduce system noise by slowing down outputs that do not need to operate at maximum speed. Outputs default to slow switching, and may be specified as fast switching in the design software or design file.

Design Software Support

ATF1504ASV(L) designs are supported by Microchip's ProChip Designer and WinCUPL software tools as well as Precision Synthesis from Mentor Graphic as described in the "Programmable Logic Device Design Software Overview".

Power-Up Reset

The ATF1504ASV/ATF1504ASVL is designed with a power-up Reset, a feature critical for state machine initialization. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be initialized, and the state of each output will depend on the polarity of its buffer. However, due to the asynchronous nature of Reset and uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

- The V_{CC} rise must be monotonic
- After Reset occurs, all input and feedback setup times must be met before driving the clock pin high
- The clock must remain stable during Power-up Reset

The ATF1504ASV/ATF1504ASVL has two options for the hysteresis about the Reset level, V_{RST}, Small and Large. To ensure a robust operating environment in applications where the device is operated near 3.0V, it is recommended that during the fitting process users configure the device with the Power-up Reset hysteresis set to Large. Users of the POF2JED conversion utility should include the flag "-power_reset" on the command line after "filename.POF". To allow the registers to be properly reinitialized with the Large hysteresis option selected, the following condition is added:

- If V_{CC} falls below 2.0V, it must shut off completely before the device is turned on again

When the Large hysteresis option is active, I_{CC} is reduced by several hundred microamps as well.

Details on the power Reset hysteresis feature are available in the "ATF15XX Power-on Reset Hysteresis Feature" application note.

Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF1504ASV(L) fuse patterns. Once programmed, fuse verify is inhibited. However, the 16-bit User Signature remains accessible.

Programming

ATF1504ASV(L) devices are in-system programmable (ISP) devices utilizing the 4-pin JTAG protocol. This capability eliminates package handling normally required for programming and facilitates rapid design iterations and field changes.

Microchip provides ISP hardware and software to allow programming of the ATF1504ASV(L) via the PC. ISP is performed by using either a download cable, a comparable board tester or a simple microprocessor interface.

To facilitate ISP programming by the Automated Test Equipment (ATE) vendors, Serial Vector Format (SVF) files can be created by Microchip provided software utilities.

ATF1504ASV(L) devices can also be programmed using standard third-party programmers. With a third-party programmer, the JTAG ISP port can be disabled, thereby allowing four additional I/O pins to be used for logic.

Refer to Programming of PLDs application note for more details.

ISP Programming Protection

The ATF1504ASV(L) has a special feature that locks the device and prevents the inputs and I/O from driving if the programming process is interrupted for any reason. The inputs and I/O default to high Z state during such a condition. In addition, the pin-keeper option preserves the former state during device programming, if this circuit was previously programmed on the device. This prevents disturbing the operation of other circuits in the system while the ATF1504ASV(L) is being programmed via ISP.

All ATF1504ASV(L) devices are initially shipped in the erased state, thereby making them ready to use for ISP.

1.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (†)

Temperature under bias ..... -40°C to +85°C

Storage temperature ..... -65°C to +150°C

Voltage on any pin with respect to ground[1] ..... -2.0V to +7.0V

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

TABLE 1-1: DC AND AC OPERATING CONDITIONS

	Industrial
Operating Temperature (Ambient)	-40°C to +85°C
V_{CC} (V_{CCIO}/V_{CCINT}) Power Supply	3.0V to 3.6V

TABLE 1-2: DC CHARACTERISTICS

Symbol	Parameter	Minimum	Typical	Maximum	Units	Condition	
I_{IL}	Input or I/O Low Leakage Current	—	-2	-10	µA	V_{IN} = GND	
I_{IH}	Input or I/O High Leakage Current	—	2	10	µA	V_{IN} = V_{CC}	
I_{OZ}	Tri-State Output Off-State Current	-40	—	40	µA	V_O = V_{CC} or GND	
I_{CC1}	Power Supply Current, Standby	—	75	—	mA	V_{CC} = Max V_{IN} = 0, V_{CC}	Std power
		—	5	—	µA	V_{CC} = Max V_{IN} = 0, V_{CC}	"L" power
I_{CC2}	Power Supply Current, Power-Down mode	—	0.1	5	mA	V_{CC} = Max V_{IN} = 0, V_{CC}	"PD" mode
I_{CC3}[1]	Reduced Power mode Supply Current, Standby	—	55	—	mA	V_{CC} = Max V_{IN} = 0, V_{CC}	Std power
V_{IL}	Input Low Voltage	-0.3	—	0.8	V		
V_{IH}	Input High Voltage	1.7	—	V_{CCIO} + 0.3	V		
V_{OL}	Output Low Voltage (3.3V TTL)	—	—	0.45	V	V_{IN} = V_{IH} or V_{IL} V_{CCIO} = Min, I_{OL} = 8 mA	
	Output Low Voltage (3.3V CMOS)	—	—	0.2	V	V_{IN} = V_{IH} or V_{IL} V_{CCIO} = Min, I_{OL} = 0.1 mA	
V_{OH}	Output High Voltage (3.3V TTL)	2.4	—	—	V	V_{IN} = V_{IH} or V_{IL} V_{CCIO} = Min, I_{OH} = -1.5 mA	
	Output High Voltage (3.3V CMOS)	V_{CCIO} - 0.2	—	—	V	V_{IN} = V_{IH} or V_{IL} V_{CCIO} = Min, I_{OH} = -0.1 mA	

Note 1: When macrocell reduced-power feature is enabled.

TABLE 1-3: PIN CAPACITANCE

	Typical	Maximum	Units	Conditions
CIN	—	8	pF	VIN = 0V; f = 1.0 MHz
CI/O	—	8	pF	VOUT = 0V; f = 1.0 MHz

Note 1: Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

2: The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Timing Model

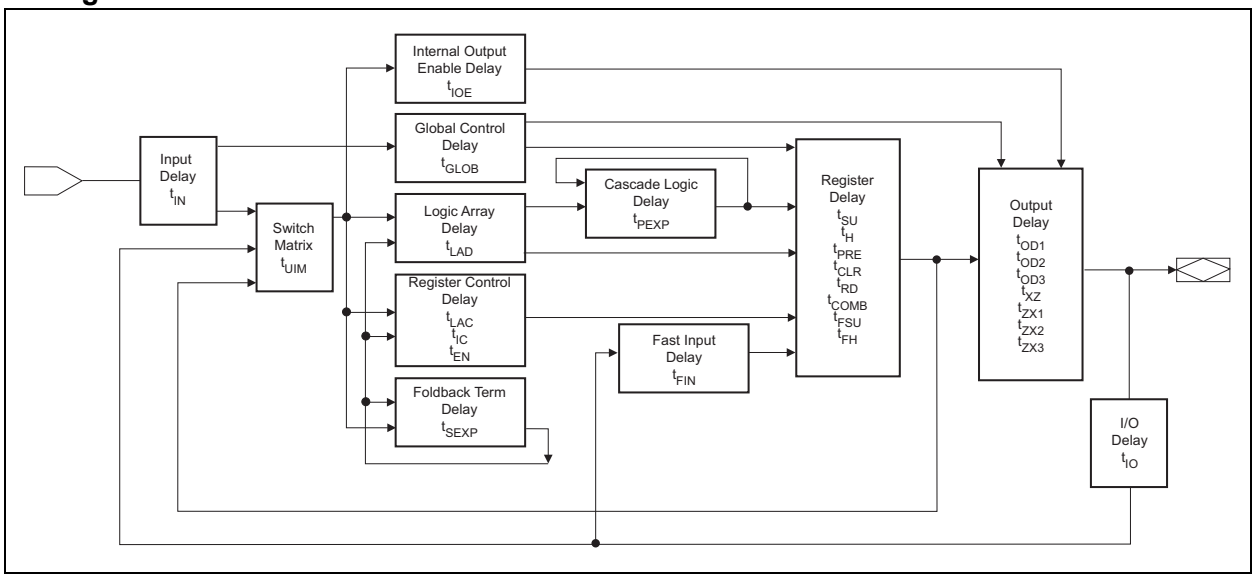


TABLE 1-4: AC CHARACTERISTICS

Symbol	Parameter	-15		-20		Units
		Min.	Max.	Min.	Max.	
tPD1	Input or Feedback to Non-Registered Output	3	15	—	20	ns
tPD2	I/O Input or Feedback to Non-Registered Feedback	3	12	—	16	ns
tSU	Global Clock Setup Time	11	—	13.5	—	ns
tH	Global Clock Hold Time	0	—	0	—	ns
tFSU	Global Clock Setup Time of Fast Input	3	—	3	—	ns
tFH	Global Clock Hold Time of Fast Input	1.0	—	2	—	ns
tCOP	Global Clock to Output Delay	—	9	—	12	ns
tCH	Global Clock High Time	5	—	6	—	ns
tCL	Global Clock Low Time	5	—	6	—	ns
tASU	Array Clock Setup Time	5	—	7	—	ns
tAH	Array Clock Hold Time	4	—	4	—	ns
tACOP	Array Clock Output Delay	—	15	—	18.5	ns
tACH	Array Clock High Time	6	—	8	—	ns

TABLE 1-4: AC CHARACTERISTICS (CONTINUED)

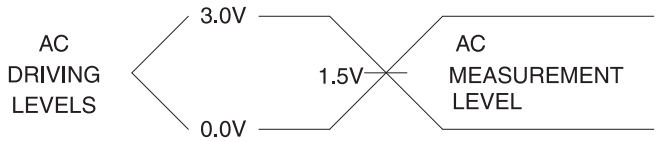
Symbol	Parameter	-15		-20		Units
		Min.	Max.	Min.	Max.	
t_{ACL}	Array Clock Low Time	6	—	8	—	ns
t_{CNT}	Minimum Clock Global Period	—	13	—	17	ns
f_{CNT}	Maximum Internal Global Clock Frequency	76.9	—	66	—	MHz
t_{ACNT}	Minimum Array Clock Period	—	13	—	17	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	76.9	—	58.8	—	MHz
f_{MAX}	Maximum Clock Frequency	100	—	83.3	—	MHz
t_{IN}	Input Pad and Buffer Delay	—	2	—	2.5	ns
t_{IO}	I/O Input Pad and Buffer Delay	—	2	—	2.5	ns
t_{FIN}	Fast Input Delay	—	2	—	2	ns
t_{SEXP}	Foldback Term Delay	—	8	—	10	ns
t_{PEXP}	Cascade Logic Delay	—	1	—	1	ns
t_{LAD}	Logic Array Delay	—	6	—	8	ns
t_{LAC}	Logic Control Delay	—	3.5	—	4.5	ns
t_{IOE}	Internal Output Enable Delay	—	3	—	3	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)	—	3	—	4	ns
t_{OD3}	Output Buffer and Pad Delay (Slow slew rate = ON; V_{CCIO} = 3.3V; C_L = 35 pF)	—	5	—	6	ns
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)	—	7	—	9	ns
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 3.3V; C_L = 35 pF)	—	10	—	11	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)	—	6	—	7	ns
t_{SU}	Register Setup Time	5	—	6	—	ns
t_H	Register Hold Time	4	—	5	—	ns
t_{FSU}	Register Setup Time of Fast Input	2	—	2	—	ns
t_{FH}	Register Hold Time of Fast Input	2	—	2	—	ns
t_{RD}	Register Delay	—	2	—	2.5	ns
t_{COMB}	Combinatorial Delay	—	2	—	3	ns
t_{IC}	Array Clock Delay	—	6	—	7	ns
t_{EN}	Register Enable Time	—	6	—	7	ns
t_{GLOB}	Global Control Delay	—	2	—	3	ns
t_{PRE}	Register Preset Time	—	4	—	5	ns
t_{CLR}	Register Clear Time	—	4	—	5	ns
t_{UIM}	Switch Matrix Delay	—	2	—	2.5	ns

TABLE 1-4: AC CHARACTERISTICS (CONTINUED)

Symbol	Parameter	-15		-20		Units
		Min.	Max.	Min.	Max.	
t_{RPA}	Reduced-Power Adder[1]	—	10	—	13	ns

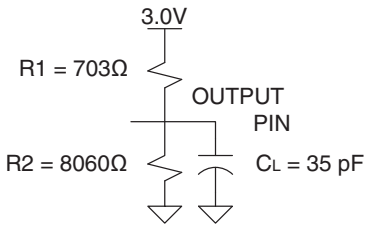
Note 1: The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL} or t_{ACH}, t_{EN} and t_{SEXP} parameters for macrocells running in the Reduced-Power mode.

FIGURE 1-1: INPUT TEST WAVEFORMS AND MEASUREMENT LEVELS



Note: t_R, t_F = 1.5 ns typical

FIGURE 1-2: OUTPUT AC TEST LOADS



Power-Down Mode

The ATF1504ASV(L) includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 5 mA. During power-down, all output data and internal logic states are latched internally and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high Z state at the onset will remain at high Z. During power-down, all input signals except the Power-Down pin are blocked.

Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The Power-Down mode feature is enabled in the logic design file or as a design software option. Designs using the Power-Down pin may not use the PD pin as a logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

TABLE 1-5: POWER-DOWN AC CHARACTERISTICS(1)(2)(3)

Symbol	Parameter	-15		-20		Units
		Min.	Max.	Min.	Max.	
t_{IVDH}	Valid I, I/O before PD High	15	—	20	—	ns
t_{GVDH}	Valid OE(2) before PD High	15	—	20	—	ns
t_{CVDH}	Valid Clock(2) before PD High	15	—	20	—	ns
t_{DHIX}	I, I/O Don't Care after PD High	—	25	—	30	ns
t_{DHGX}	OE(2) Don't Care after PD High	—	25	—	30	ns
t_{DHCX}	Clock(2) Don't Care after PD High	—	25	—	30	ns
t_{DLIV}	PD Low to Valid I, I/O	—	1	—	1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)	—	1	—	1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)	—	1	—	1	µs
t_{DLOV}	PD Low to Valid Output	—	1	—	1	µs

Note 1: For slow slew outputs, add t_{SSO}.

2: Pin or product term.

3: Includes t_{RPA} for reduced-power bit enabled.

JTAG-BST/ISP Overview

The JTAG boundary-scan testing is controlled by the Test Access Port (TAP) controller in the ATF1504ASV(L). The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan cell) adjacent to each component so that signals at component boundaries can be controlled and observed using scan testing principles. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing.

The ATF1504ASV(L) does not include a Test Reset (TRST) input pin because the TAP controller is automatically reset at power-up. The five JTAG modes supported include: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE and HIGHZ. The ATF1504ASV(L)'s ISP can be fully described using JTAG's BSDL as described in IEEE Standard 1149.1. This allows ATF1504ASV(L) programming to be described and implemented using any one of the third-party development tools supporting this standard.

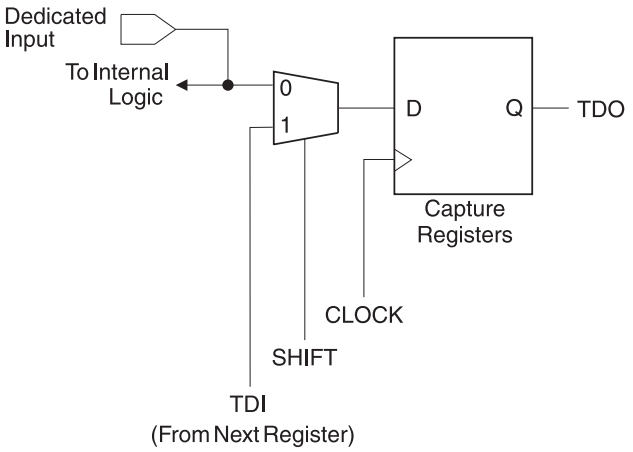
The ATF1504ASV(L) has the option of using four JTAG-standard I/O pins for boundary-scan testing (BST) and in-system programming (ISP) purposes. The ATF1504ASV(L) is programmable through the four JTAG pins using the IEEE standard JTAG programming protocol established by IEEE Standard 1149.1 using 3.3V TTL/CMOS-level programming signals from the ISP interface for in-system programming. The JTAG feature is a programmable option. If JTAG (BST or ISP) is not needed, then the four JTAG control pins are available as I/O pins.

JTAG Boundary-Scan Cell (BSC)

The ATF1504ASV(L) contains up to 64 I/O pins and four input pins, depending on the device type and package type selected. Each input pin and I/O pin has its own boundary-scan cell (BSC) in order to support boundary-scan testing as described in detail by IEEE Standard 1149.1. A typical BSC consists of three capture registers or scan registers and up to two update registers.

There are two types of BSCs, one for input or I/O pin, and one for the macrocells. The BSCs in the device are chained together through the capture registers. Input to the capture register chain is fed in from the TDI pin while the output is directed to the TDO pin. Capture registers are used to capture active device data signals, to shift data in and out of the device and to load data into the update registers. Control signals are generated internally by the JTAG TAP controller. The BSC configuration for the input and I/O pins and macrocells are shown in Figure 1-3 and Figure 1-4.

FIGURE 1-3: BSC CONFIGURATION FOR INPUT AND I/O PINS (EXCEPT JTAG TAP PINS)



Note: The ATF1504ASV(L) has pull-up option on TMS and TDI pins. This feature is selected as a design option.

FIGURE 1-4: BSC CONFIGURATION FOR MACROCELL

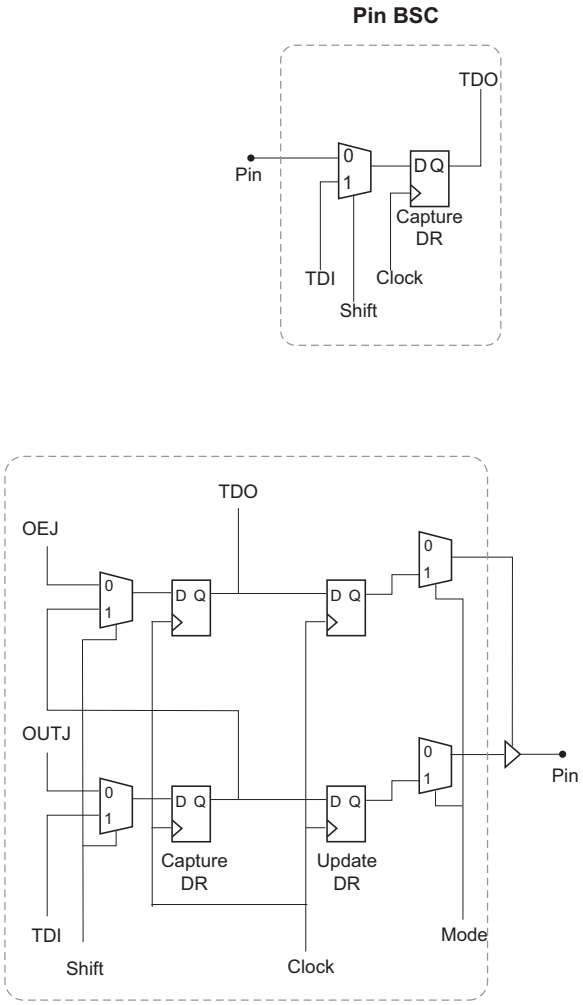


TABLE 1-6: DEDICATED PINOUTS

Dedicated Pin	44-Lead TQFP	44-Lead J-lead	100-Lead TQFP
INPUT/OE2(1)/GCLK2(2)	40	2	90
INPUT/GCLR(3)	39	1	89
INPUT/OE1(1)	38	44	88
INPUT/GCLK1(2)	37	43	87
I/O /GCLK3(2)	35	41	85
I/O / PD (1,2)(4)	5, 19	11, 25	12, 42
I/O / TDI (JTAG)(5)	1	7	4
I/O / TMS (JTAG)(5)	7	13	15
I/O / TCK (JTAG)(5)	26	32	62
I/O / TDO (JTAG)(5)	32	38	73
GND(6)	4, 16, 24, 36	10, 22, 30, 42	11, 26, 38, 43, 59, 74, 86, 95
VCC(7)	9, 17, 29, 41	3, 15, 23, 35	3, 18, 34, 39, 51, 66, 82, 91
N/C	—	—	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78
# of Signal Pins	36	36	68
# User I/O Pins	32	32	64

Note 1: OE (1, 2) = Global OE pins
2: GCLK (1, 2, 3) = Global Clock pins
3: GCLR = Global Clear pin
4: PD (1, 2) = Power-Down pins
5: TDI, TMS, TCK. TDO = JTAG pins used for boundary-scan testing or in-system programming
6: GND = Ground pins
7: VCC = VCC (VCCINT/VCCIO) pins for the device

TABLE 1-7: I/O PINOUTS

MC	PLC	44-Lead PLCC	44-Lead TQFP	100-Lead TQFP	MC	PLC	44-Lead PLCC	44-Lead TQFP	100-Lead TQFP
1	A	12	6	14	33	C	24	18	40
2	A	—	—	13	34	C	—	—	41
3	A/**PD1**	11	5	12	35	C/**PD2**	25	19	42
4	A	9	3	10	36	C	26	20	44
5	A	8	2	9	37	C	27	21	45
6	A	—	—	8	38	C	—	—	46
7	A	—	—	6	39	C	—	—	47
8/**TDI**	A	7	1	4	40	C	28	22	48
9	A	—	—	100	41	C	29	23	52
10	A	—	—	99	42	C	—	—	54
11	A	6	44	98	43	C	—	—	56
12	A	—	—	97	44	C	—	—	57
13	A	—	—	96	45	C	—	—	58
14	A	5	43	94	46	C	31	25	60
15	A	—	—	93	47	C	—	—	61
16	A	4	42	92	48/**TCK**	C	32	26	62
17	B	21	15	37	49	D	33	27	63
18	B	—	—	36	50	D	—	—	64
19	B	20	14	35	51	D	34	28	65
20	B	19	13	33	52	D	36	30	67
21	B	18	12	32	53	D	37	31	68
22	B	—	—	31	54	D	—	—	69
23	B	—	—	30	55	D	—	—	71
24	B	17	11	29	56/**TDO**	D	38	32	73
25	B	16	10	25	57	D	39	33	75
26	B	—	—	23	58	D	—	—	76
27	B	—	—	21	59	D	—	—	79
28	B	—	—	20	60	D	—	—	80
29	B	—	—	19	61	D	—	—	81
30	B	14	8	17	62	D	40	34	83
31	B	—	—	16	63	D	—	—	84
32/**TMS**	B	13	7	15	64	D/**GCLK3**	41	35	85

FIGURE 1-5: SUPPLY CURRENT VS. SUPPLY VOLTAGE – ATF1504ASV (T_A = 25°C, F = 0)

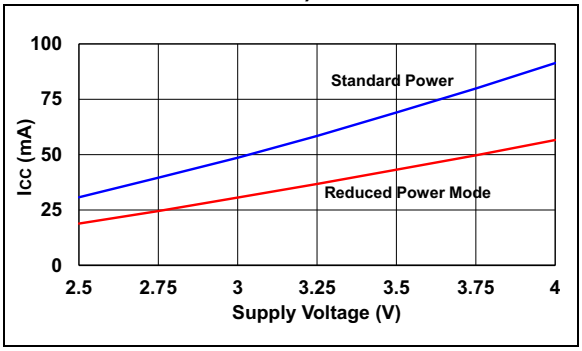


FIGURE 1-6: SUPPLY CURRENT VS. SUPPLY VOLTAGE – PIN-CONTROLLED POWER-DOWN MODE (T_A = 25°C, F = 0)

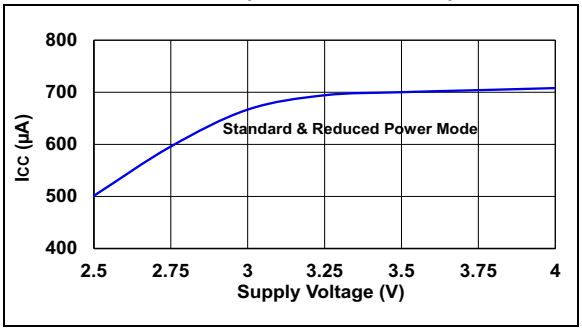


FIGURE 1-7: SUPPLY CURRENT VS. FREQUENCY – ATF1504ASV (T_A = 25°C)

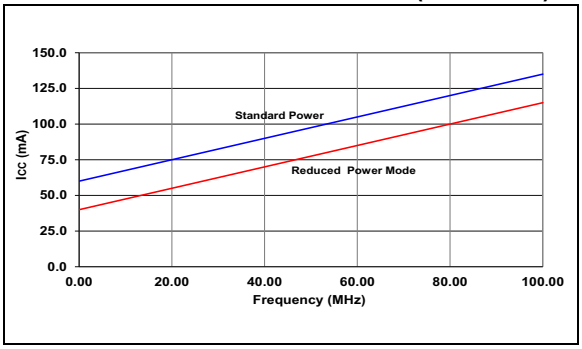


FIGURE 1-8: SUPPLY CURRENT VS. SUPPLY VOLTAGE – ATF1504ASVL (T_A = 25°C, F = 0)

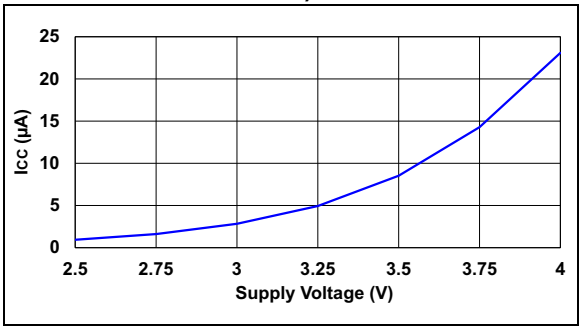


FIGURE 1-9: SUPPLY CURRENT VS. FREQUENCY – ATF1504ASVL (T_A = 25°C)

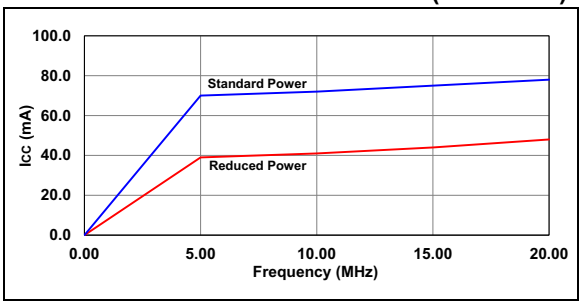


FIGURE 1-10: OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE (V_{OH} = 2.4V, T_A = 25°C)

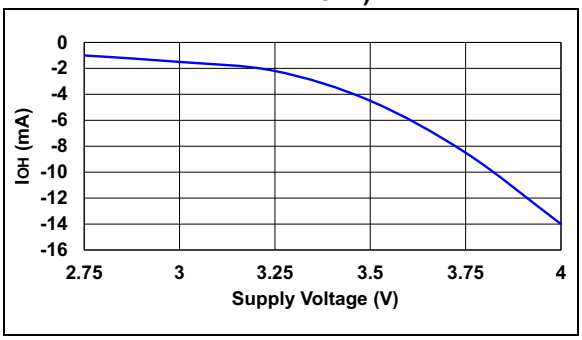


FIGURE 1-11: OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)

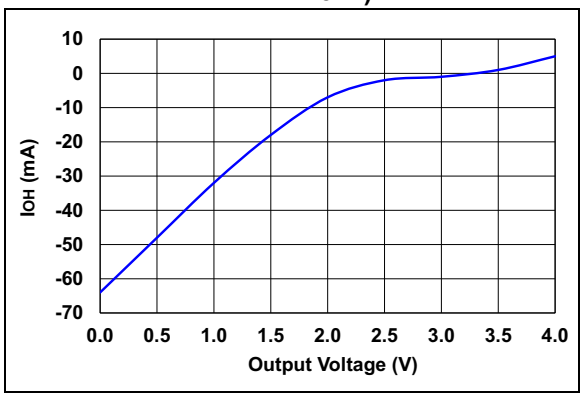


FIGURE 1-12: OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE (V_{OL} = 0.5V, T_A = 25°C)

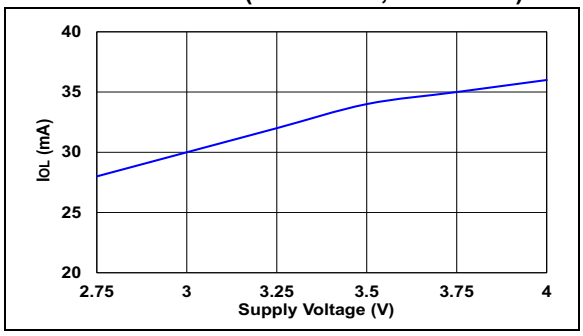


FIGURE 1-13: OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)

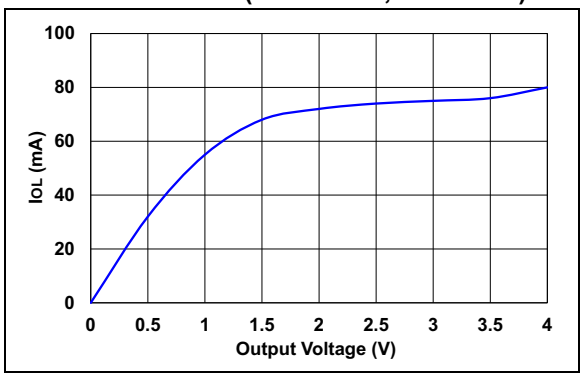


FIGURE 1-14: INPUT CLAMP CURRENT VS. INPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)

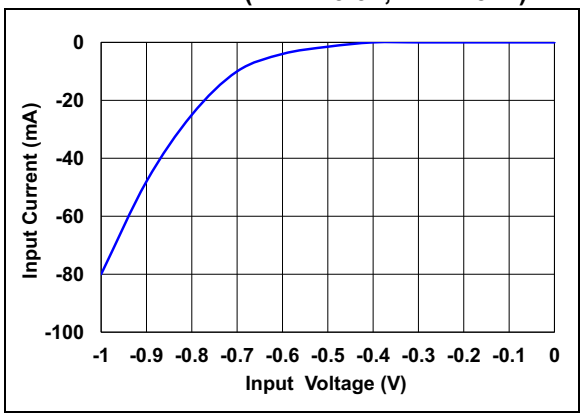
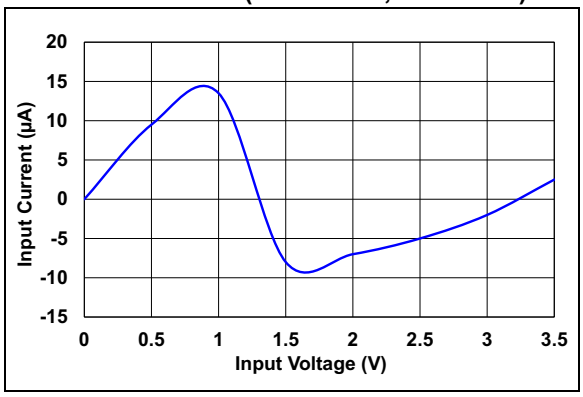


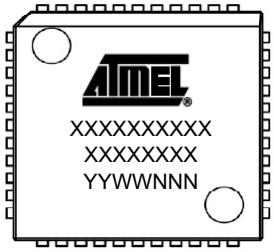
FIGURE 1-15: INPUT CURRENT VS. INPUT VOLTAGE (V_{CC} = 3.3V, T_A = 25°C)



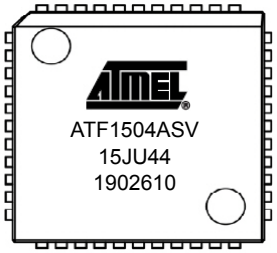
2.0 PACKAGING INFORMATION

2.1 Package Marking Information

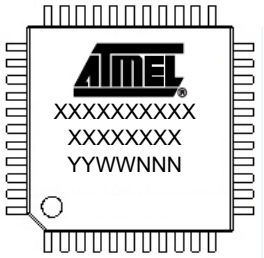
44-Lead PLCC



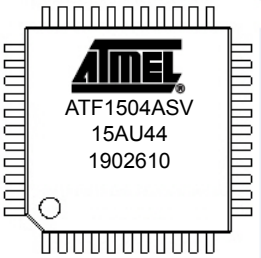
Example



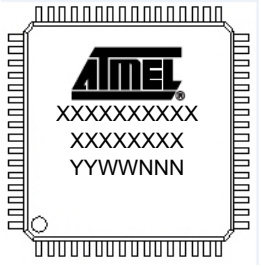
44-Lead TQFP



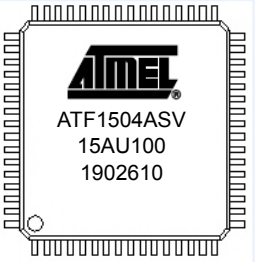
Example



100-Lead TQFP



Example

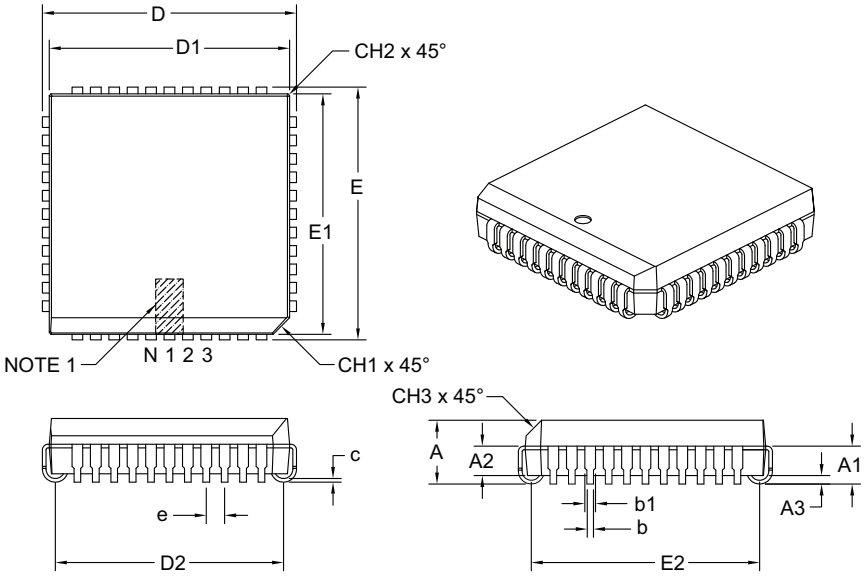


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	*	This packages are RoHs compliant. The JEDEC® designator can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

44-Lead Plastic Leaded Chip Carrier (L) – Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		.050	
Overall Height	A	.165	.172	.180
Contact Height	A1	.090	.105	.120
Molded Package to Contact	A2	.062	–	.083
Standoff §	A3	.020	–	–
Corner Chamfer	CH1	.042	–	.048
Chamfers	CH2	–	–	.020
Side Chamfer	CH3	.042	–	.056
Overall Width	E	.685	.690	.695
Overall Length	D	.685	.690	.695
Molded Package Width	E1	.650	.653	.656
Molded Package Length	D1	.650	.653	.656
Footprint Width	E2	.582	.610	.638
Footprint Length	D2	.582	.610	.638
Lead Thickness	c	.0075	–	.0125
Upper Lead Width	b1	.026	–	.032
Lower Lead Width	b	.013	–	.021

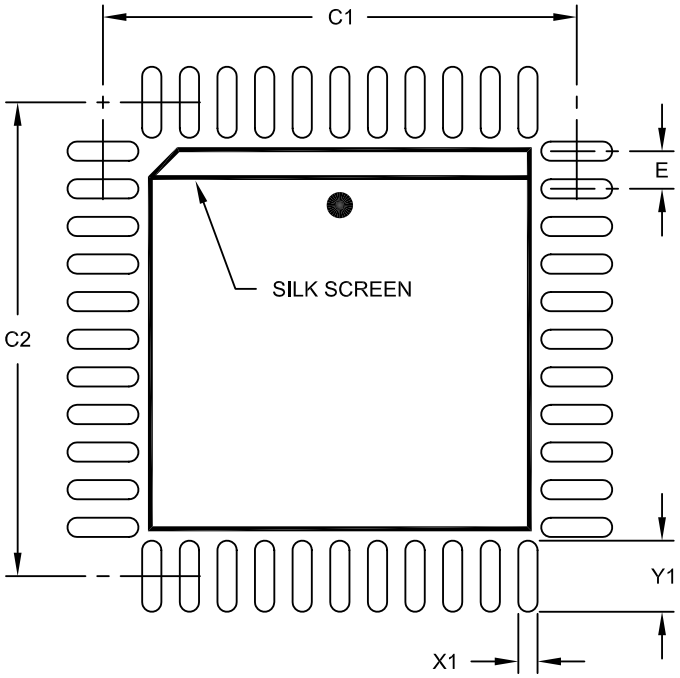
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

Microchip Technology Drawing C04-048B

44-Lead Plastic Leaded Chip Carrier (L) - Square [PLCC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		.050 BSC	
Contact Pad Spacing	C1		.630	
Contact Pad Spacing	C2		.630	
Contact Pad Width (X44)	X1			.026
Contact Pad Length (X44)	Y1			.094

Notes:

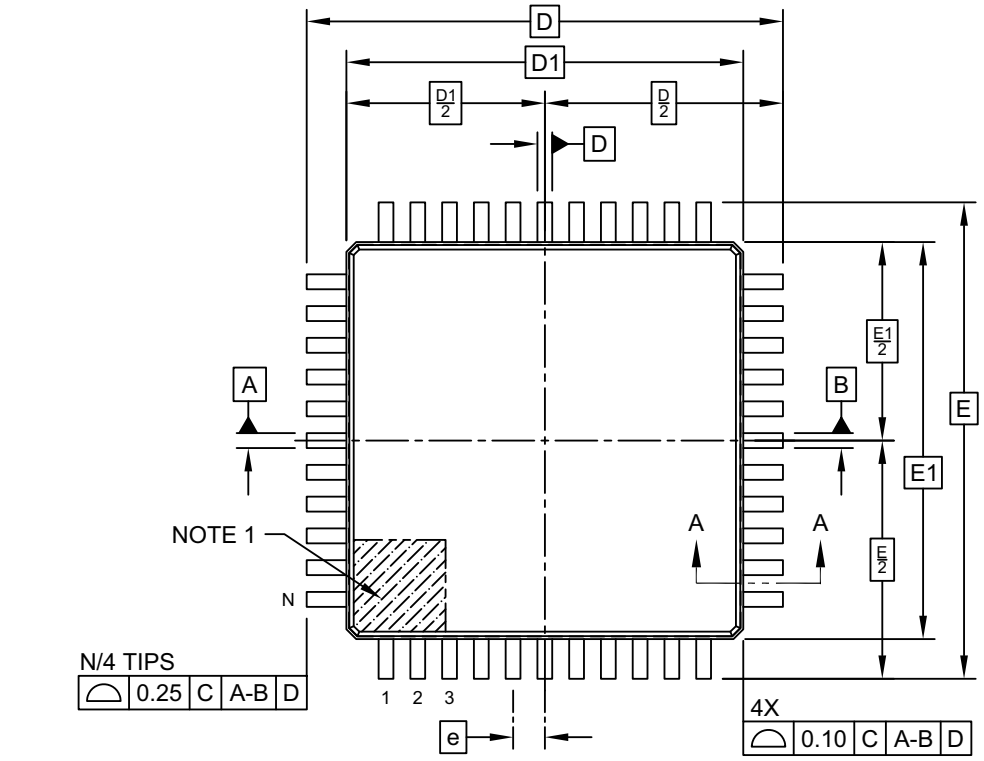
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

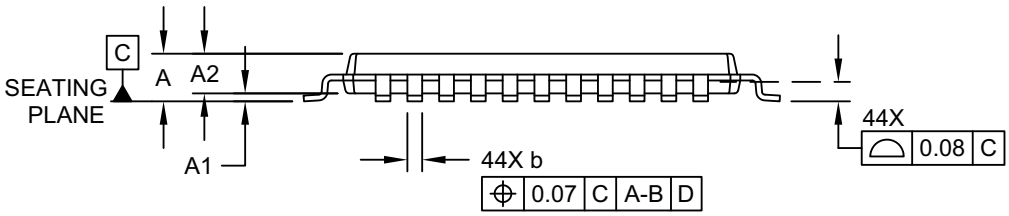
Microchip Technology Drawing No. C04-2048A

44-Lead Plastic Thin Quad Flatpack (3EB) - 10x10x1.0 mm Body [TQFP]
Atmel Legacy Global Package Code AIX

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

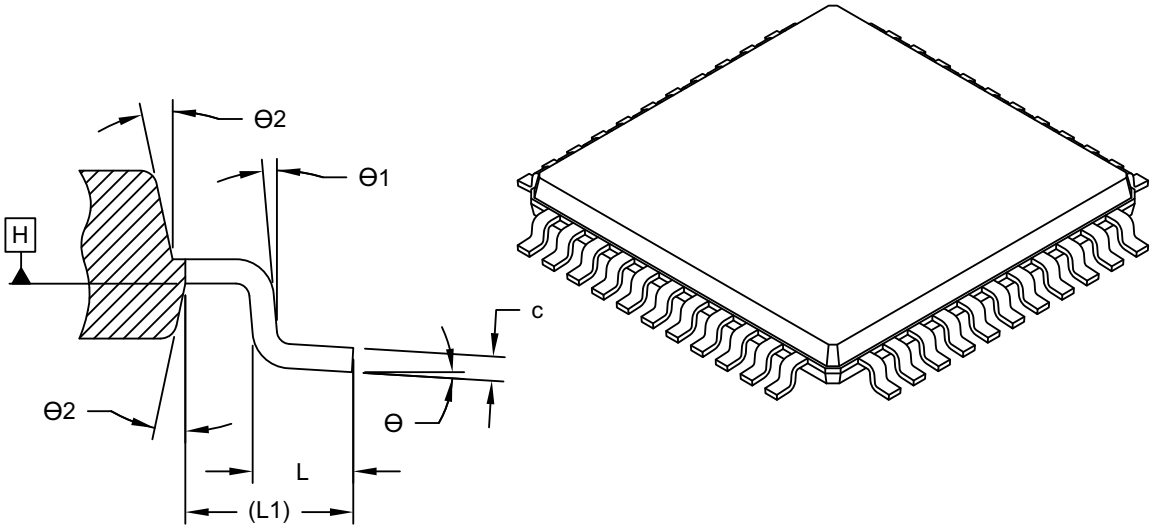


SIDE VIEW

Microchip Technology Drawing C04-21019-3EB Rev A Sheet 1 of 2

44-Lead Plastic Thin Quad Flatpack (3EB) - 10x10x1.0 mm Body [TQFP]
Atmel Legacy Global Package Code AIX

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		44	
Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		12.00 BSC	
Molded Package Length	D1		10.00 BSC	
Overall Width	E		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Terminal Width	b	0.30	-	0.45
Terminal Thickness	c	0.09	-	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	-
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Terminal-to-Exposed-Pad	Θ2	11°	12°	13°

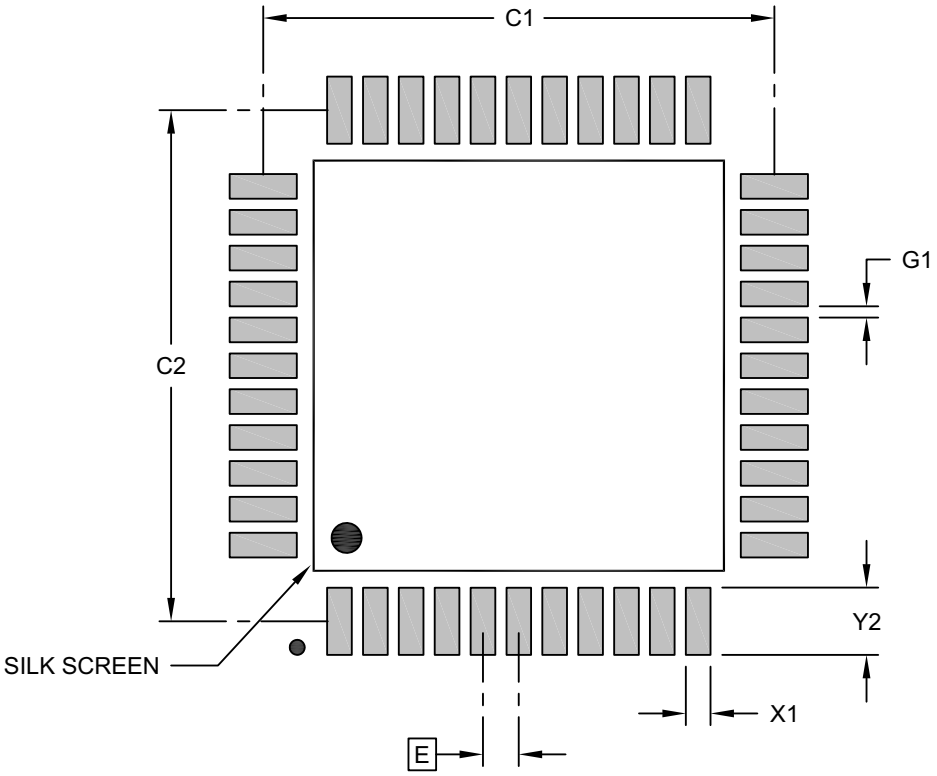
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21019-3EB Rev A Sheet 2 of 2

44-Lead Plastic Thin Quad Flatpack (3EB) - 10x10x1.0 mm Body [TQFP]
Atmel Legacy Global Package Code AIX

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X20)	X1			0.55
Contact Pad Length (X20)	Y1			1.50
Contact Pad to Center Pad (X20)	G1	0.25		

Notes:

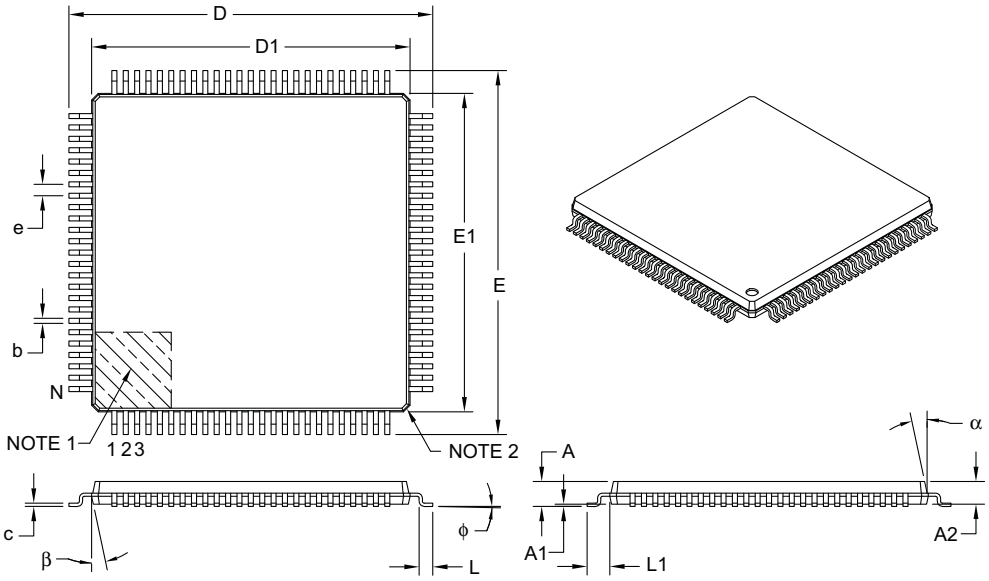
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-23019-3EB Rev A

100-Lead Plastic Thin Quad Flatpack (PF) – 14x14x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		100	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		16.00 BSC	
Overall Length	D		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Molded Package Length	D1		14.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

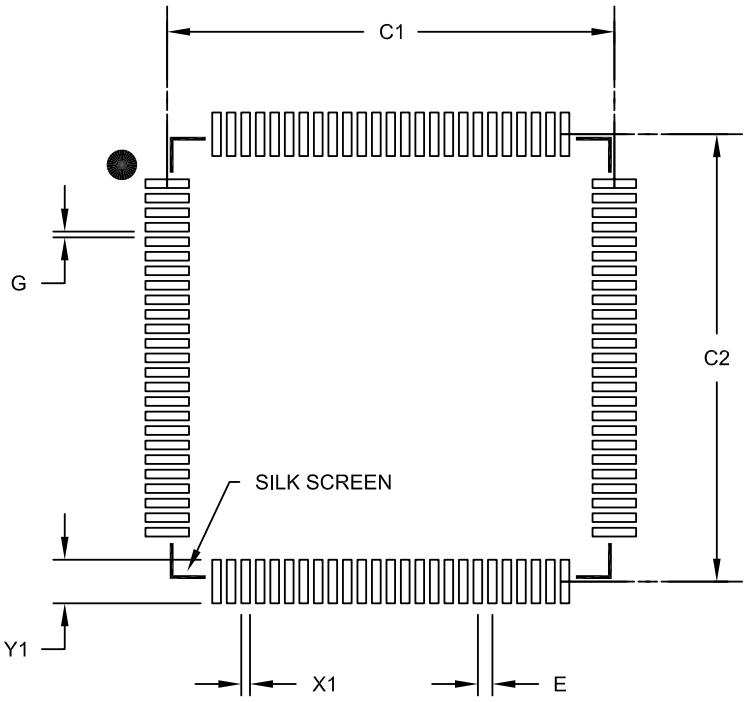
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-110B

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

APPENDIX A: REVISION HISTORY

Revision A (03/2019)

Updated to the Microchip template. Microchip DS20006185 replaces Atmel document 1409. Removed commercial temperature, 68-/84-lead PLCCs and 100-lead PQFP.

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	X	XXX	-[X](1)
Device	Speed Grade	Package Type	Temperature Range	Lead Count	Tape and Reel Option

Device:	ATF1504ASV = 3.3V Standard-Power 64 MC CPLD ATF1504ASVL = 3.3V Low-Power 64 MC CPLD	
Speed Grade:	15 = 15 ns (t_{PD}) 20 = 20 ns (t_{PD})	
Package Type:	A = TQFP (Thin Profile Plastic Quad Flat Package) J = PLCC (Plastic J-leaded Chip Carrier)	
Temperature Range:	U = -40°C to +85°C (Industrial)	
Lead Count:	44 = 44 Leads 100 = 100 Leads	
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel(1)	

Examples:

a) ATF1504ASV-15JU44-T = Industrial temp., Tape and Reel, PLCC package.

b) ATF1504ASV-15JU44 = Industrial temp., PLCC package.

c) ATF1504ASV-15AU44 = Industrial temp., TQFP package.

d) ATF1504ASV-15AU100 = Industrial temp., TQFP package.

e) ATF1504ASVL-20JU44-T = Industrial temp., Tape and Reel, TQFP package.

f) ATF1504ASVL-20JU44 = Industrial temp., TQFP package.

g) ATF1504ASVL-20AU44 = Industrial temp., TQFP package.

h) ATF1504ASV-15AU100 = Industrial temp., TQFP package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

ORDERING INFORMATION

ATF1504ASV(L) Green Package Options (Pb/Halide-Free/RoHS Compliant)

$t_{PD}1$ (ns)	t_{COP} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
15	9	100	ATF1504ASV-15AU44	44A	Industrial (-40°C to +85°C)
			ATF1504ASV-15JU44	44J	
			ATF1504ASV-15AU100	100A	
20	12	83.3	ATF1504ASVL-20AU44	44A	Industrial (-40°C to +85°C)
			ATF1504ASVL-20JU44	44J	
			ATF1504ASVL-20AU100	100A	

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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