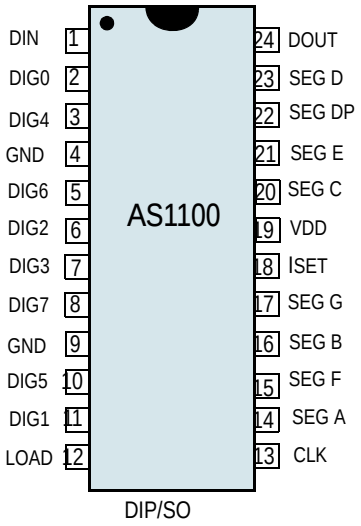
4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	DIN	**Data input.** Data is programmed into the 16Bit shift register on the rising CLK edge
2, 3, 5:8, 10, 11	DIG 0 : DIG 7	8 digit driver lines that sink the current from the common cathode of the display. In shutdown mode the AS1100 switches the outputs to VDD.
4, 9	GND	Both GND pins must be connected.
12	LOAD/CS	**Strobe input.** With the rising edge of the LOAD signal the 16 bit of serial data is latched into the register.
13	CLK	**Clock input.** The interface is capable to support clock frequencies up to 10MHz. The serial data is clocked into the internal shift register with the rising edge of the CLK signal. On the DOUT pin the data is applied with the falling edge of CLK.
14:17, 20:23	SEGA:G, DP	**Seven segment driver lines including the decimal point.** When a segment is turned off the output is connected to GND.
18	ISET	The current into ISET determines the peak current through the segments and therefore the brightness.
19	VDD	**Positive Supply Voltage** (+5V)
24	DOUT	**Serial data output for cascading drivers.** The output is valid after 16.5 clock cycles. The output is never set to high impedance.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
Electrical Parameters				
VDD to GND	-0.3	+6	V	
DIN, CLK, LOAD to GND	-0.3	+6	V	
All other Pins to GND	-0.3	VDD + 0.3	V	
VOUT	-0.3	7	V	
Current				
DIG0–DIG7 Sink Current		500	mA	
SEGA–G, DP Source Current		100	mA	
Latch up Immunity		±200	mA	Norm: JEDEC 78
Electrostatic Discharge				
Electro Static Discharge at Digital Outputs		+500	V	Norm: MIL 883 E method 3015
Electro Static Discharge at all other pins		+1000	V	
Continuous Power Dissipation (TA = +85°C)				
Narrow Plastic DIP		1066	mW	Derate 13.3mW/°C above +70ºC
Wide SO		941	mW	Derate 11.8mW/°C above +70ºC
Temperature Ranges and Storage Conditions				
Storage Temperature Range	-55	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Humidity non-condensing[1]	8	85	%	
Moisture Sensitive Level [1]		1		Represents a max. floor life time of unlimited

1. only valid for the SOIC 24-pin package

6 Electrical Characteristics

V_{DD} = 5V, R_{SET} = 9.53kΩ±1%, T_A = T_{MIN} to T_{MAX}, unlesss otherwise noted.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{AMB}	Operating Temperature Range		-40		+85	ºC
V_{DD}	Operating Supply Voltage		4.0	5.0	5.5	V
I_{DDSD}	Shutdown Supply Current	All digital inputs at V_{DD} or GND, TA = +25ºC		20	50	µA
I_{DD}	Operating Supply Current	R_{SET} = open circuit			500	µA
		All segments and decimal point on, I_{SEG} = -40mA		330		mA
f_{OSC}	Display Scan Rate	8 digits scanned	500	800	1300	Hz
I_{DIGIT}	Digit Drive Sink Current	V_{OUT} = 0.65V	320			mA
I_{SEG}	Segment Drive Source Current	T_A = +25ºC, V_{OUT} = (V_{DD} -1V)	-30	-40	-45	mA
ΔI_{SEG}	Segment Drive Current Matching			3.0		%
I_{DIGIT}	Digit Drive Source Current	Digit off, V_{DIGIT} = (V_{DD} -0.3V)	-2			mA
I_{SEG}	Segment Drive Sink Current	Segment off, V_{SEG} = 0.3V	5			mA
Logic Inputs						
I_{IH}, I_{IL}	Input Current DIN, CLK, LOAD	V_{IN} = 0V or V_{DD}	-1		1	µA
V_{IH}	Logic High Input Voltage		3.5			V
V_{IL}	Logic Low Input Voltage				0.8	V
V_{OH}	Output High Voltage	DOUT, I_{SOURCE} = -1mA	V_{DD} - 1			V
V_{OL}	Output Low Voltage	DOUT, I_{SINK} = 1.6mA			0.4	V
	Hysteresis Voltage	DIN, CLK, LOAD		1		V
Timing Characteristics						
t_{CP}	CLK Clock Period		100			ns
t_{CH}	CLK Pulse Width High		50			ns
t_{CL}	CLK Pulse Width Low		50			ns
t_{CSH}	CLK Rise to LOAD Rise Hold Time		0			ns
t_{DS}	DIN Setup Time		25			ns
t_{DH}	DIN Hold Time		0			ns
t_{DO}	Output Data Propagation Delay	C_{LOAD} = 50pF			25	ns
t_{LDCK}	LOAD Rising Edge to Next Clock Rising Edge		50			ns
t_{CSW}	Minimum LOAD Pulse High		50			ns
t_{DSPD}	Data-to-Segment Delay				2.25	ms

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

7 Typical Operating Characteristics

Figure 3. Segment Driver Capability, V_{DD} = 5V, Logic Level = High

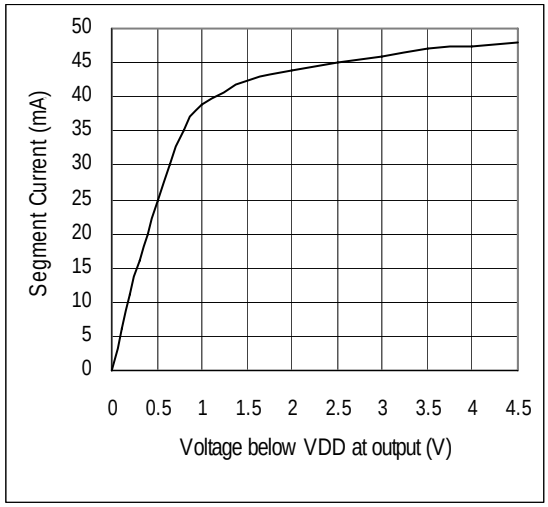
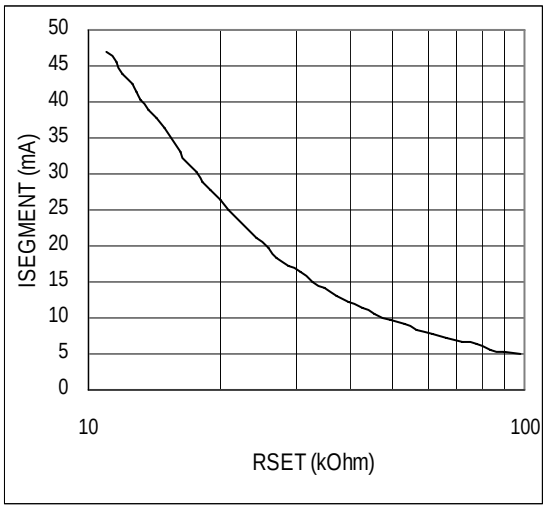


Figure 4. Segment Current vs. R_{SET}



8 Detailed Description

8.1 Serial-Addressing Modes

Programming of the AS1100 is done via 4 wire serial interface. A programming sequence consists of 16-bit packages. The data is shifted into the internal 16 Bit register with the rising edge of the CLK signal. With the rising edge of the LOAD signal the data is latched into a digital or control register depending on the address. The LOAD signal must go to high after the 16th rising clock edge. The LOAD signal can also come later but just before the next rising edge of CLK, otherwise data would be lost. The content of the internal shift register is applied 16.5 clock cycles later to the DOUT pin. The data is clocked out at the falling edge of CLK. The Bits of the 16Bit-programming package are described in Table 5. The first 4 Bits D15-D12 are don't care, D11-D8 contain the address and D7-D0 contain the data. The first bit is D15, the most significant bit (MSB). The exact timing is given in Figure 5.

Figure 5. Timing Diagram

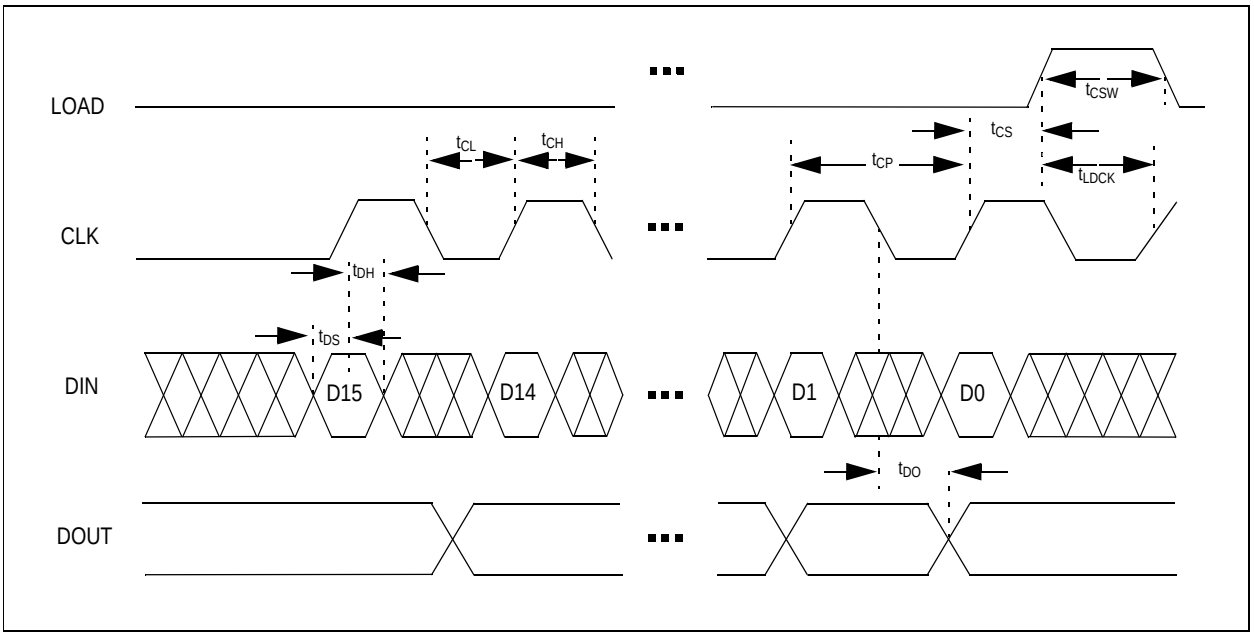


Table 4. Serial Data Format (16bits)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	Address				MSB	Data					LSB	

8.2 Digit and Control Registers

The AS1100 incorporates 15 registers, which are listed in Table 5. The digit and control registers are selected via the 4Bit address word. The 8 digit registers are realized with a 64bit memory. Each digit can be controlled directly without rewriting the whole contents. The control registers consist of decode mode, display intensity, number of scanned digits, shutdown, display test, and reset/external clock register.

8.3 Shutdown Mode

The AS1100 features a shutdown mode, where it consumes only 20µA current. The shutdown mode is entered via a write to register 0Ch. Then all segment current sources are pulled to ground and all digit drivers are connected to V_{DD}, so that nothing is displayed. All internal digit registers keep the programmed values. The shutdown mode can either be used for power saving or for generating a flashing display by repeatedly entering and leaving the shutdown mode. The AS1100 needs typically 250µs to exit the shutdown mode. During shutdown the AS1100 is fully programmable. Only the display test function overrides the shutdown mode.

8.4 Initial Power-Up

After powering up the system all register are reset, so that the display is blank. The AS1100 starts the shutdown mode. All registers should be programmed for normal operation. The default settings enable only scan of one digit, the internal decoder is disabled, data register and intensity register are set to the minimum value.

8.5 Decode-Mode Register

In the AS1100 a BCD decoder is included. Every digit can be selected via register 09h to be decoded. The BCD code consists of the numbers 0-9, E,H, L,P and -. In register 09h a logic high enables the decoder for the appropriate digit. In case that the decoder is bypassed (logic low) the data Bits D7-D0 correspond to the segment lines of the AS1100. In Table 7 some possible settings for register 09h are shown. Bit D7, which corresponds to the decimal point, is not affected by the settings of the decoder. Logic high means that the decimal point is displayed. In Table 8 the font of the Code B decoder is shown. In Table 9 the correspondence of the register to the appropriate segments of a 7 segment display is shown (see Figure 6).

8.6 Intensity Control and Interdigit Blanking

Brightness of the display can be controlled in an analog way by changing the external resistor (R_{SET}). The current, which flows between V_{DD} and ISET, defines the current that flows through the LEDs. The LED current is 100 times the ISET current. The minimum value of R_{SET} should be 9.53kΩ, which corresponds to 40mA segment current. The brightness of the display can also be controlled digitally via register 0Ah. The brightness can be programmed in 16 steps and is shown in Table 10. An internal pulse width modulator controls the intensity of the display.

8.7 Scan-Limit Register

The scan limit register 0Bh selects the number of digits displayed. When all 8 digits are displayed the update frequency is typically 800Hz. If the number of digits displayed is reduced, the update frequency is reduced as well. The frequency can be calculated using 8fOSC/N, where N is the number of digits. Since the number of displayed digits influences the brightness, the resistor R_{SET} should be adjusted accordingly. The Table 12 shows the maximum allowed current, when fewer than 4 digits are used. To avoid differences in brightness the scan limit register should not be used to blank portions of the display (leading zeros).

Table 5. Register Address Map

Register	Address					Hex Code
	D15-D12	D11	D10	D9	D8	
No-Op	X	0	0	0	0	0xX0
Digit 0	X	0	0	0	1	0xX1
Digit 1	X	0	0	1	0	0xX2
Digit 2	X	0	0	1	1	0xX3
Digit 3	X	0	1	0	0	0xX4
Digit 4	X	0	1	0	1	0xX5
Digit 5	X	0	1	1	0	0xX6
Digit 6	X	0	1	1	1	0xX7
Digit 7	X	1	0	0	0	0xX8
Decode Mode	X	1	0	0	1	0xX9
Intensity	X	1	0	1	0	0xXA
Scan Limit	X	1	0	1	1	0xXB
Shutdown	X	1	1	0	0	0xXC
Not used	X	1	1	0	1	0xXD
Reset and ext. Clock	X	1	1	1	0	0xXE
Display Test	X	1	1	1	1	0xXF

Table 6. Shutdown Register Format (address (hex) = 0xXC

Mode	Address Code (Hex)	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode	0xXC	X	X	X	X	X	X	X	0
Normal Operation	0xXC	X	X	X	X	X	X	X	1

Table 7. Decode-mode Register Examples (address (hex) = 0xX9

Decode Mode	Register Data								Hex Code
	D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digits 7–0	0	0	0	0	0	0	0	0	0x00
Code B decode for digit 0 No decode for digits 7–1	0	0	0	0	0	0	0	1	0x01
Code B decode for digits 3–0 No decode for digits 7– 4	0	0	0	0	1	1	1	1	0x0F
Code B decode for digits 7–0	1	1	1	1	1	1	1	1	0xFF

Table 8. Code B font

7-Segment Character	Register Data						On Segments = 1							
	D7*	D6-D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
--		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
blank		X	1	1	1	1		0	0	0	0	0	0	0

Note: The decimal point is set by bit D7 = 1

Table 9. No-decode Mode Data Bits and Corresponding Segment Lines

	Register Data							
	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

Figure 6. Standard 7-segment LED

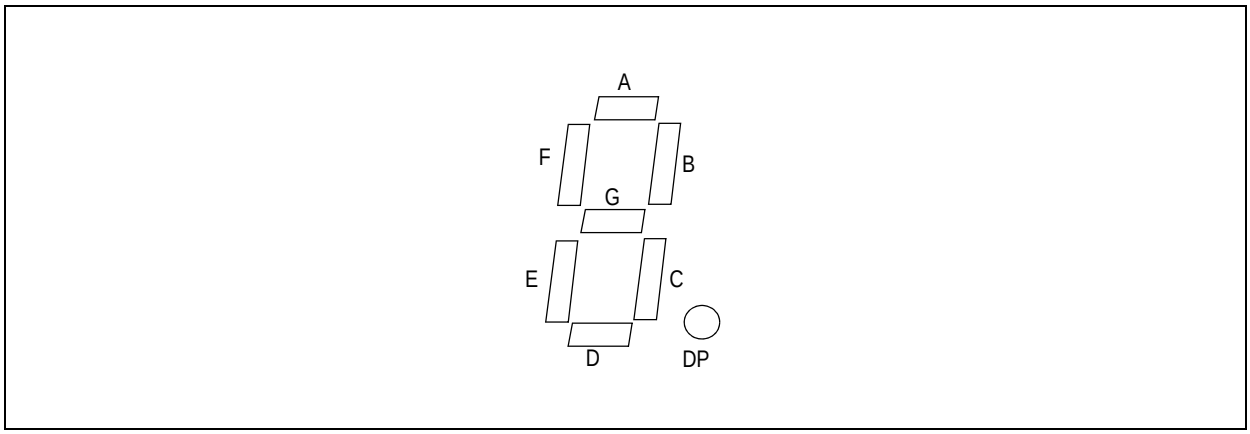


Table 10. Intensity Register Format (address (hex) = 0xXA)

Duty Cycle	D7	D6	D5	D4	D3	D2	D1	D0	Hex Code
1/32 (min on)	X	X	X	X	0	0	0	0	0xX0
3/32	X	X	X	X	0	0	0	1	0xX1
5/32	X	X	X	X	0	0	1	0	0xX2
7/32	X	X	X	X	0	0	1	1	0xX3
9/32	X	X	X	X	0	1	0	0	0xX4
11/32	X	X	X	X	0	1	0	1	0xX5
13/32	X	X	X	X	0	1	1	0	0xX6
15/32	X	X	X	X	0	1	1	1	0xX7
17/32	X	X	X	X	1	0	0	0	0xX8
19/32	X	X	X	X	1	0	0	1	0xX9
21/32	X	X	X	X	1	0	1	0	0xXA
23/32	X	X	X	X	1	0	1	1	0xXB
25/32	X	X	X	X	1	1	0	0	0xXC
27/32	X	X	X	X	1	1	0	1	0xXD
29/32	X	X	X	X	1	1	1	0	0xXE
31/32 (max on)	X	X	X	X	1	1	1	1	0xXF

Table 11. Scan-limit Register Format (address (hex) = 0xXB)

Decode Mode	Register Data								Hex Code
	D7	D6	D5	D4	D3	D2	D1	D0	
Display digit 0 only	X	X	X	X	X	0	0	0	0xX0
Display digit 0 & 1	X	X	X	X	X	0	0	1	0xX1
Display digit 0 1 2	X	X	X	X	X	0	1	0	0xX2
Display digit 0 1 2 3	X	X	X	X	X	0	1	1	0xX3
Display digit 0 1 2 3 4	X	X	X	X	X	1	0	0	0xX4
Display digit 0 1 2 3 4 5	X	X	X	X	X	1	0	1	0xX5
Display digit 0 1 2 3 4 5 6	X	X	X	X	X	1	1	0	0xX6
Display digit 0 1 2 3 4 5 6 7	X	X	X	X	X	1	1	1	0xX7

8.8 Display Test Register

With the display test register 0Fh all LED can be tested. In the test mode all LEDs are switched on at maximum brightness (duty cycle 31/32). All programming of digit and control registers are maintained. The format of the register is given in Table 13.

Table 12. Maximum Segment Current for 1-, 2-, or 3-digit Displays

Number of digits Displayed	Maximum Segment Current (mA)
1	10
2	20
3	30

Table 13. Display-test Register Format (address (hex) = 0xXF)

Mode	Register Data							
	D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	X	X	X	X	X	X	X	0
Display Test Mode	X	X	X	X	X	X	X	1

Note: The AS1100 remains in display-test mode until the display-test register is reconfigured for normal operation.

8.9 No-Op Register (Cascading of AS1100)

The no-operation register 00h is used when AS1100s are cascaded in order to support more than 8 digit displays. The cascading must be done in a way that all DOUT are connected to DINof the following AS1100. The LOAD and CLK signals are connected to all devices. For a write operation for example to the fifth device the command must be followed by four no-operation commands. When the LOAD signal finally goes to high all shift registers are latched. The first four devices have got no-operation commands and only the fifth device sees the intended command and updates its register.

8.10 Reset and External Clock Register

This register is addressed via the serial interface. It allows to switch the device to external clock mode (If D0=1 the CLK pin of the serial interface operates as system clock input.) and to apply an external reset (D1). This brings all registers (except reg. E) to default state. For standard operation the register contents should be "00h".

Table 14. Reset and External Clock Register (address (hex) = oxXE)

Mode	Address code (Hex)	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation, internal clock	0xXE	X	X	X	X	X	X	0	0
Normal Operation, external clock	0xXE	X	X	X	X	X	X	0	1
Reset state, internal clock	0xXE	X	X	X	X	X	X	1	0
Reset state, external clock	0xXE	X	X	X	X	X	X	1	1

9 Application Information

9.1 Supply Bypassing and Wiring

In order to achieve optimal performance the AS1100 shall be placed very close to the LED display to minimize effects of electromagnetic interference and wiring inductance. Furthermore, it is recommended to connect a 10µF electrolytic and a 0.1µF ceramic capacitor between VDD and GND to avoid power supply ripple. Also, both GNDs must be connected to ground.

9.2 Selecting RSET Resistor and Using External Drivers

The current through the segments is controlled via the external resistor RSET. Segment current is about 100 times the current in ISET. The right values for ISET are given in Table 15. The maximum current the AS1100 can drive is 40mA. If higher currents are needed, external drivers must be used. In that case it is no longer necessary that the AS1100 drives high currents. A recommended value for RSET is 47kΩ. In cases that the AS1100 only drives few digits, Table 12 specifies the maximum currents and RSET must be set accordingly. Refer to absolute maximum ratings to calculate acceptable limits for ambient temperature, segment current, and the LED forward-voltage drop.

Table 15. RSET vs. Segment Current and LED Forward Voltage

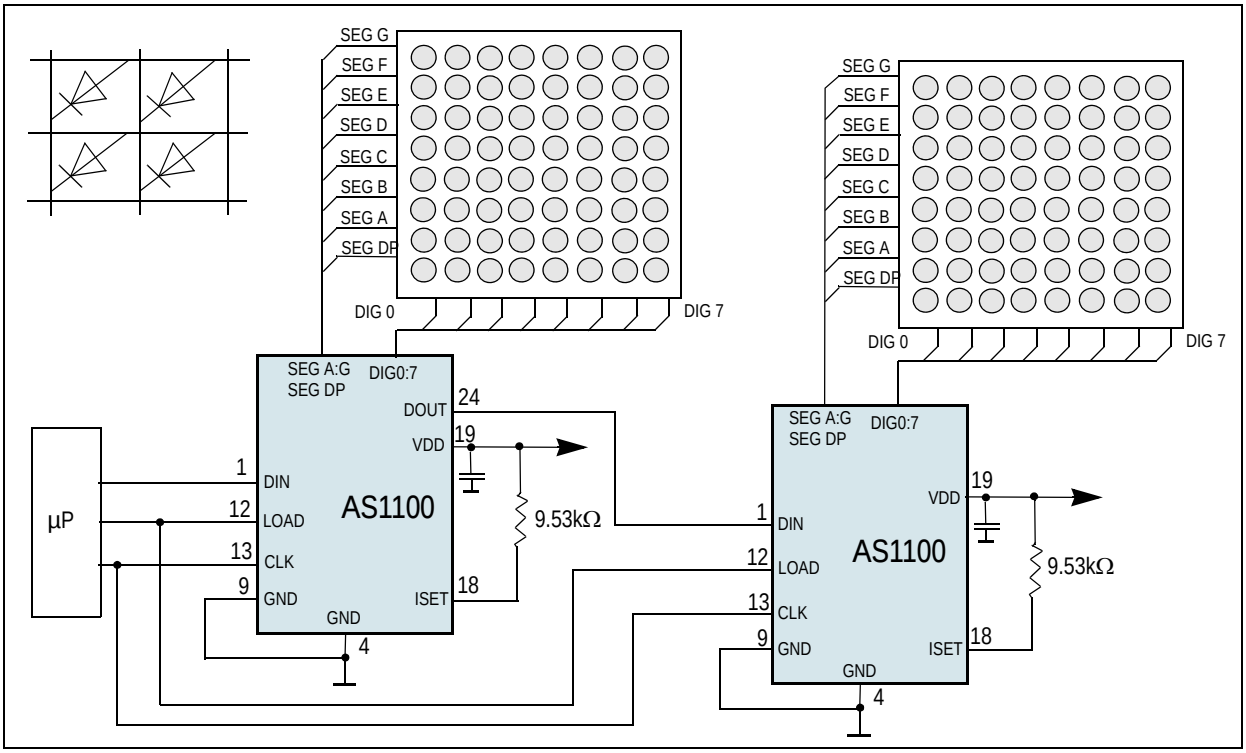
ISEG (mA)	VLED(V)				
	1.5	2.0	2.5	3.0	3.5
40	12.2kΩ	11.8kΩ	11.0kΩ	10.6kΩ	9.69kΩ
30	17.8kΩ	17.1kΩ	15.8kΩ	15.0kΩ	14.0kΩ
20	29.8kΩ	28.0kΩ	25.9kΩ	24.5kΩ	22.6kΩ
10	66.7kΩ	63.7kΩ	59.3kΩ	55.4kΩ	51.2kΩ

9.3 8x8 LED Dot Matrix Driver

The example in Figure 7 uses the AS1100 to drive an 8x8 LED dot matrix. The LED columns have common cathode and are connected to the DIG0-7 outputs. The rows are connected to the segment drivers. Each of the 64 LEDs can be addressed separately. The columns are selected via the digits as shown in Table 5. The decode mode register (0xX9) has to be programmed to '00000000' as stated in Table 4. The single LEDs in a column can be addressed as stated in Table 9, where D0 corresponds to segment G and D7 corresponds to segment DP.

Note: For a multiple-digit dot matrix, multiple AS1100 devices must be cascaded.

Figure 7. Application Example as LED Dot Matrix Driver



9.4 Calculating the Power Dissipation

The upper limit for power dissipation (PD) for the AS1100 is determined from the following equation:

$$PD = (V_{DD} \times 0.5mA) + (V_{DD} - V_{LED})(DUTY \times I_{SEG} \times N) \quad (EQ\ 1)$$

Where:

V_{DD} = supply voltage
DUTY = duty cycle set by intensity register
N = number of segments driven (worst case is 8)
V_{LED} = LED forward voltage
I_{SEG} = segment current set by R_{SET}

Dissipation Example:

I_{SEG} = 40mA, N = 8, DUTY = 31/32, VLED = 1.8V at 40mA, V_{DD} = 5.25V

PD = 5.25V(0.5mA) + (5.25V - 1.8V)(31/32 x 40mA x 8) = 1.07W

Thus, for a PDIP package θ_{JA} = +75°C/W (from Table 13), the maximum allowed ambient temperature T_A is given by:

$T_{J,MAX} = T_A + PD \times \theta_{JA} = 150°C = T_A + 1.07W \times 75°C/W$.

Where:

T_A = +69.7°C.

The T_A limit for SO Packages in the dissipation example above is +59.0°C.

Table 16. Package Thermal Resistance Data

Package	Thermal Resistance (θ_{JA})
24 Narrow DIP	+75ºC/W
24 Wide SO	+85ºC/w
Maximum Junction Temperature (T_J) = +150ºC	
Maximum Ambient Temperature (T_A) = +85ºC	

10 Package Drawings and Markings

Figure 8. AS1100 Marking

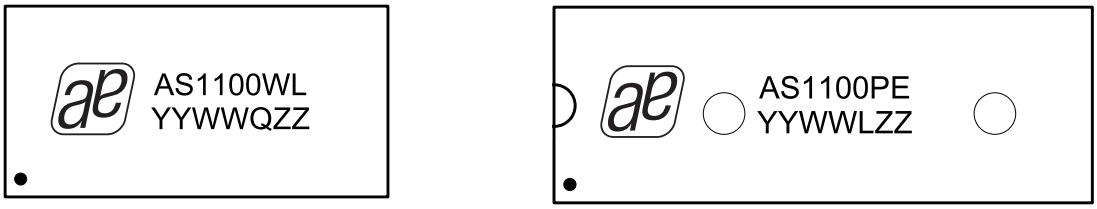
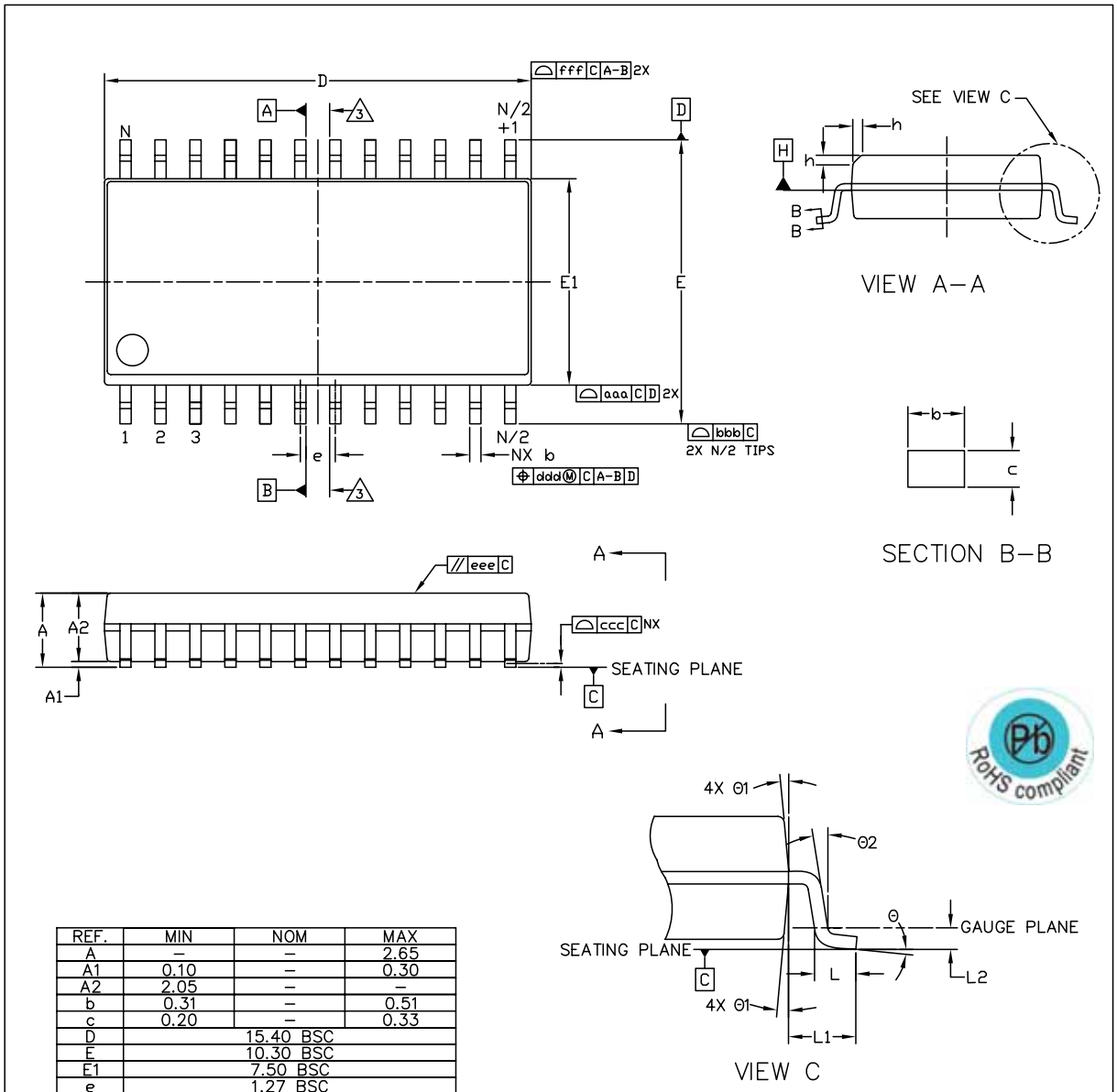


Table 17. Packaging Code YYWWQZZ

YY	WW	Q or L	ZZ
last two digits of the current year	manufacturing week	plant identifier	free choice / traceability code

Figure 9. SOIC 24-pin Package Diagram



REF.	MIN	NOM	MAX
A	–	–	2.65
A1	0.10	–	0.30
A2	2.05	–	–
b	0.31	–	0.51
c	0.20	–	0.33
D		15.40 BSC	
E		10.30 BSC	
E1		7.50 BSC	
e		1.27 BSC	
L	0.40	–	1.27
L1		1.40 REF	
L2		0.25 BSC	
h	0.25	–	0.75
θ	0°	–	8°
θ1	5°	–	15°
θ2	0°	–	–
aaa		0.10	
bbb		0.33	
ccc		0.10	
ddd		0.25	
eee		0.10	
fff		0.20	
ggg		0.15	
N		24	

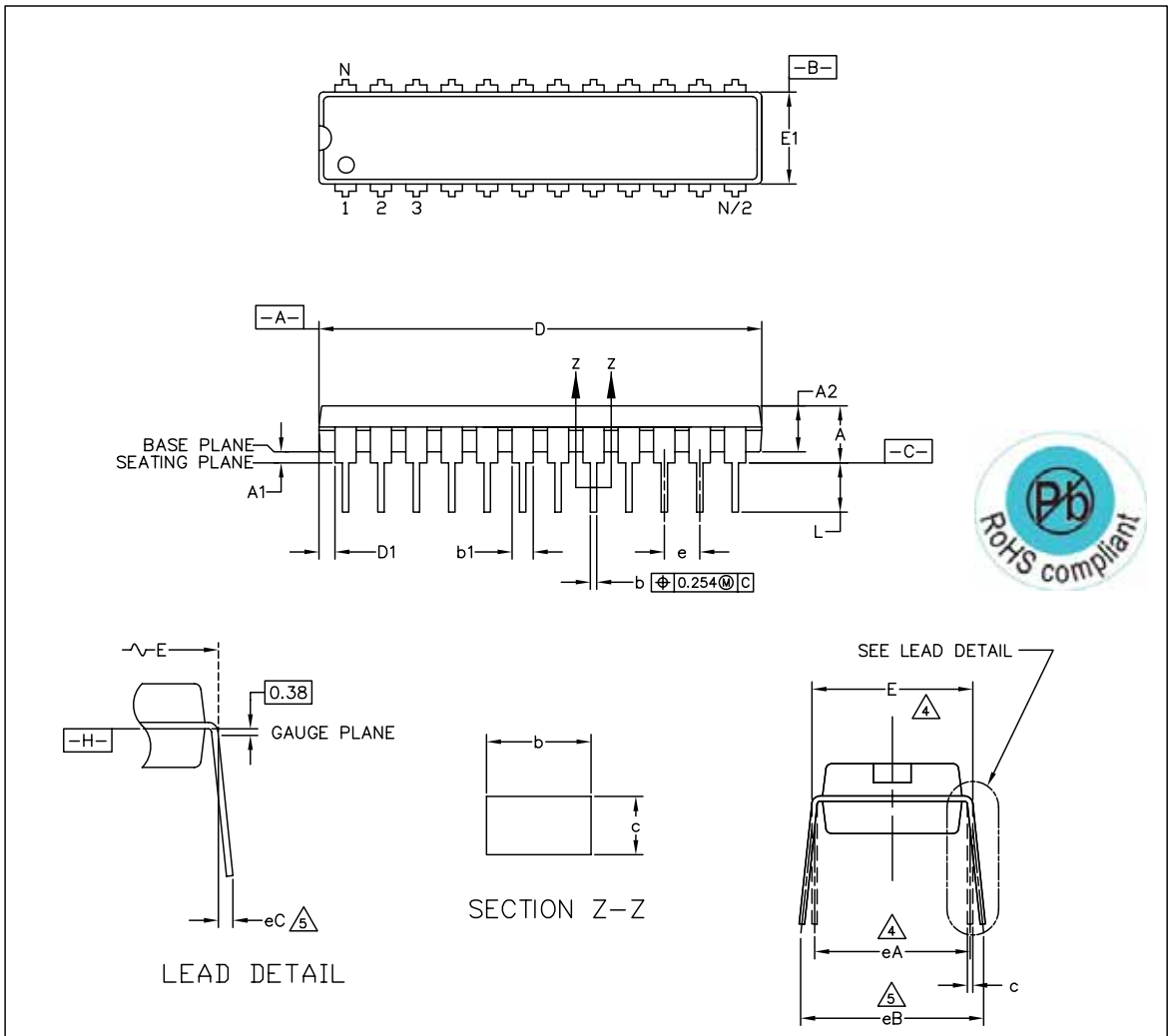
NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.

3 DATUMS A & B TO BE DETERMINED AT DATUM H.

austriamicrosystems a leap ahead in analog			ASSEMBLY ENGINEERING	
DRAWN RH8	DATE 2010.12.20	REV. N/C	TITLE SOIC 300MIL, 24 LEAD	REFERENCE DOCUMENT JEDEC MS – 013 LATEST REVISION
CHECKED GBO	DATE 2010.12.20		DRAWING NO. JKC	UNIT
APPROVED MKR	DATE 2010.12.20	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

Figure 10. PDIP 24-pin Package Diagram [1]



REF.	MIN	NOM	MAX
A	–	–	5.33
A1	0.38	–	–
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b1	1.14	1.52	1.78
b2	0.76	0.99	1.14
c	0.20	0.25	0.36
D	31.24	31.75	32.51
D1	1.27	–	–
E	7.62	7.87	8.26
E1	6.10	6.35	7.11
e		2.54 BSC	
eA		7.62 BSC	
eB	–	–	10.92
eC	0	–	1.52
L	2.92	3.30	3.81
N		24	

NOTE:

1. DIMENSIONS & TOLERANCEING CONFIRM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. N IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS.
4. E AND eA MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM -C-.
5. eB AND eC ARE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. DATUM PLANE -H- CONICIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

austriamicrosystems a leap ahead in analog			ASSEMBLY ENGINEERING	
DRAWN RH8	DATE 2010.12.23	REV. N/C	TITLE PDIP 300MIL, 24 LEAD	REFERENCE DOCUMENT JEDEC MS – 001 LATEST REVISION
CHECKED GBO	DATE 2010.12.23		DRAWING NO. WHP	UNIT
APPROVED MKR	DATE 2010.12.23	SHEET 1 OF 1	DIMENSION AND TOLERANCE	SCALE NOT IN SCALE

1. For more Information on the PDIP 24-pin package see Ordering Information on page 16.

11 Ordering Information

The device is available as the standard products shown in Table 18.

Table 18. Ordering Information

Ordering Code	Marking	Description	Temp Range	Delivery Form	Package
AS1100PL[1]	AS1100PL	Serially Interfaced, 8-Digit LED Driver	0ºC to +70ºC	Tubes	PDIP 24-pin
AS1100WL	AS1100WL	Serially Interfaced, 8-Digit LED Driver	0ºC to +70ºC	Tubes	SOIC 24-pin
AS1100PE[1]	AS1100PE	Serially Interfaced, 8-Digit LED Driver	-40ºC to +85ºC	Tubes	PDIP 24-pin
AS1100WE	AS1100WE	Serially Interfaced, 8-Digit LED Driver	-40ºC to +85ºC	Tubes	SOIC 24-pin
AS1100WL-T	AS1100WL	Serially Interfaced, 8-Digit LED Driver	0ºC to +70ºC	Tape & Reel	SOIC 24-pin
AS1100WE-T	AS1100WE	Serially Interfaced, 8-Digit LED Driver	-40ºC to +85ºC	Tape & Reel	SOIC 24-pin

1. The PDIP 24-pin Package reached end of life. There is the possibility for a last time buy order until end of July 2011.

Note: All products are RoHS compliant.
Buy our products or get free samples online at ICdirect: http://www.austriamicrosystems.com/ICdirect

Technical Support is found at http://www.austriamicrosystems.com/Technical-Support

For further information and requests, please contact us mailto:sales@austriamicrosystems.com
or find your local distributor at http://www.austriamicrosystems.com/distributor

Copyrights

Disclaimer

Devices sold by austriamicrosystems AG are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. austriamicrosystems AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. austriamicrosystems AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with austriamicrosystems AG for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by austriamicrosystems AG for each application. For shipments of less than 100 parts the manufacturing flow might show deviations from the standard production flow, such as test flow or test location.

The information furnished here by austriamicrosystems AG is believed to be correct and accurate. However, austriamicrosystems AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of austriamicrosystems AG rendering of technical or other services.

Contact Information

Headquarters

austriamicrosystems AG
Tobelbaderstrasse 30
A-8141 Unterpremstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

For Sales Offices, Distributors and Representatives, please visit:

http://www.austriamicrosystems.com/contact