

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	200			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =160V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	3	5	6	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =3.8A T _J =125°C		0.55 1.1	0.7 1.32	Ω
g _{FS}	Forward Transconductance	V _{DS} =15V, I _D =3.8A		8.7		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.8	1	V
I _S	Maximum Body-Diode Continuous Current ^G				6	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	170	215	260	pF
C _{oss}	Output Capacitance		20	32	50	pF
C _{rss}	Reverse Transfer Capacitance		3	7.2	15	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		5.5		Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =25V, I _D =3.8A		3.82		nC
Q _{g(4.5V)}	Total Gate Charge			0.92		nC
Q _{gs}	Gate Source Charge			1.42		nC
Q _{gd}	Gate Drain Charge			1.47		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =25V, R _L =6.5Ω, R _{GEN} =3Ω		6.3		ns
t _r	Turn-On Rise Time			3.3		ns
t _{D(off)}	Turn-Off DelayTime			10.5		ns
t _f	Turn-Off Fall Time			2.8		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =3.8A, dI/dt=100A/μs		59		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3.8A, dI/dt=100A/μs		142		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

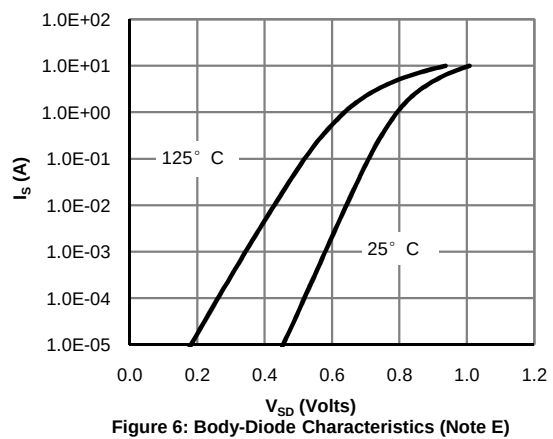
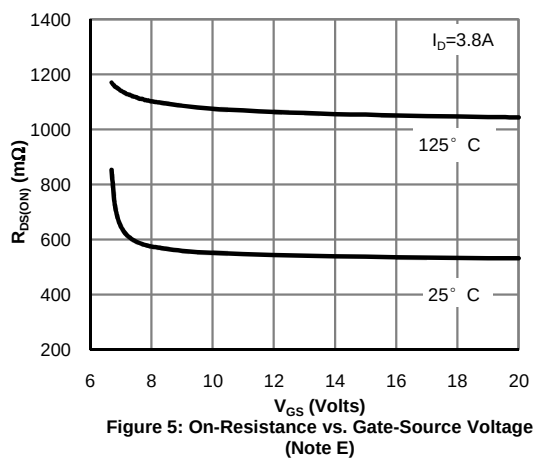
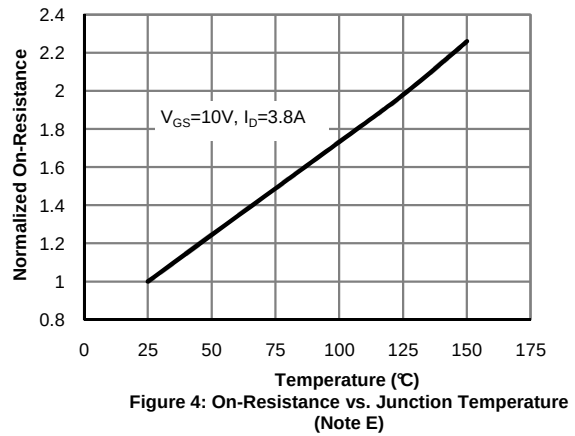
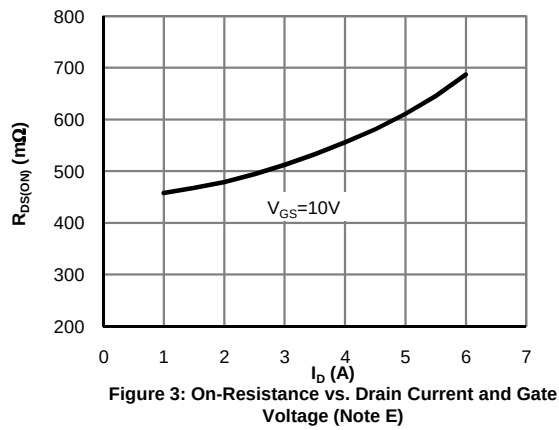
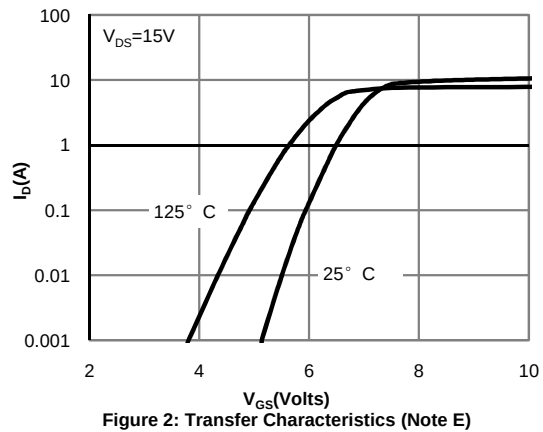
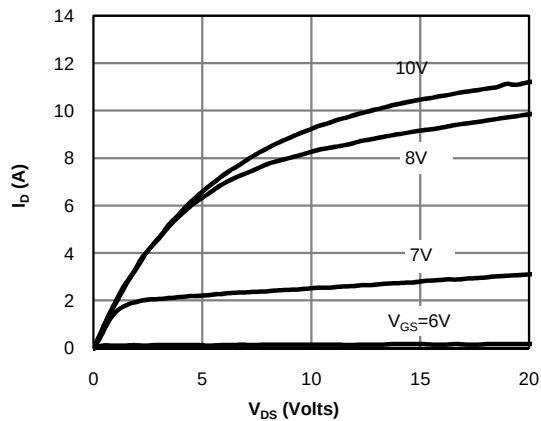
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

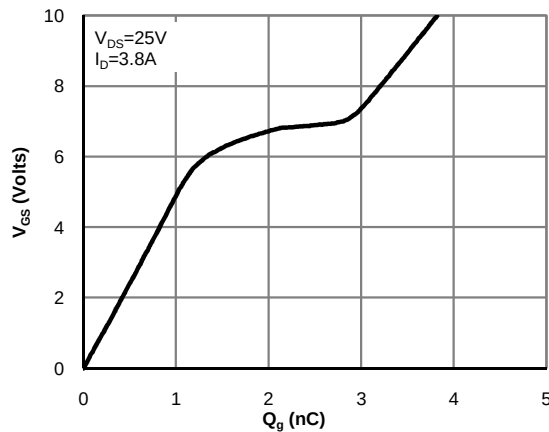


Figure 7: Gate-Charge Characteristics

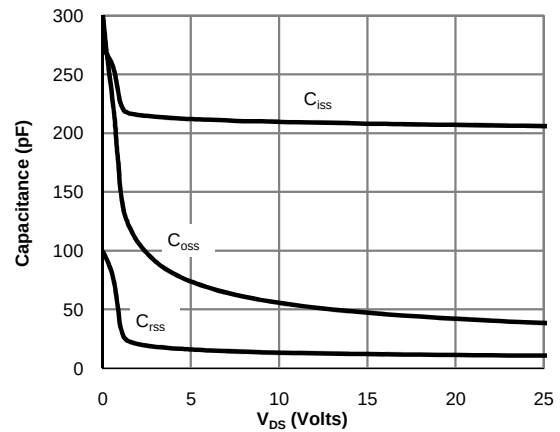


Figure 8: Capacitance Characteristics

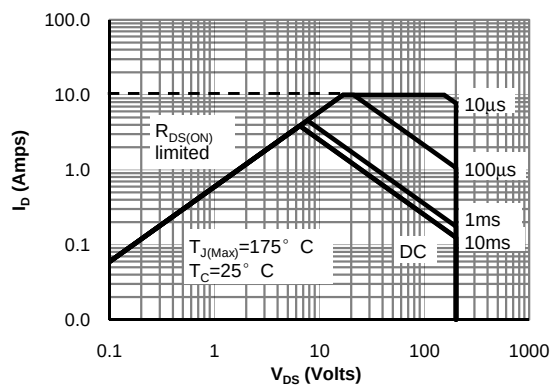


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

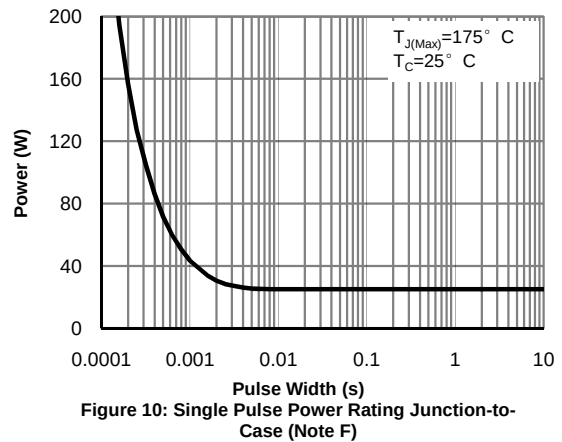


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

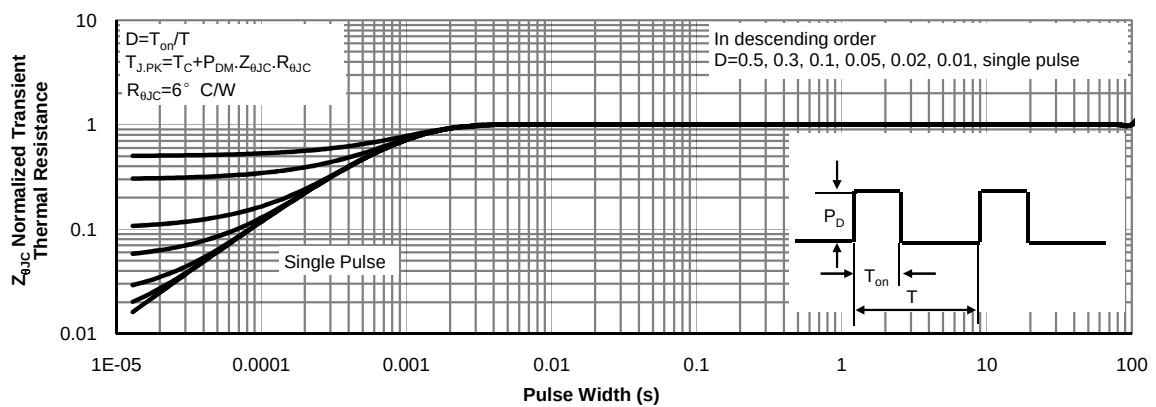
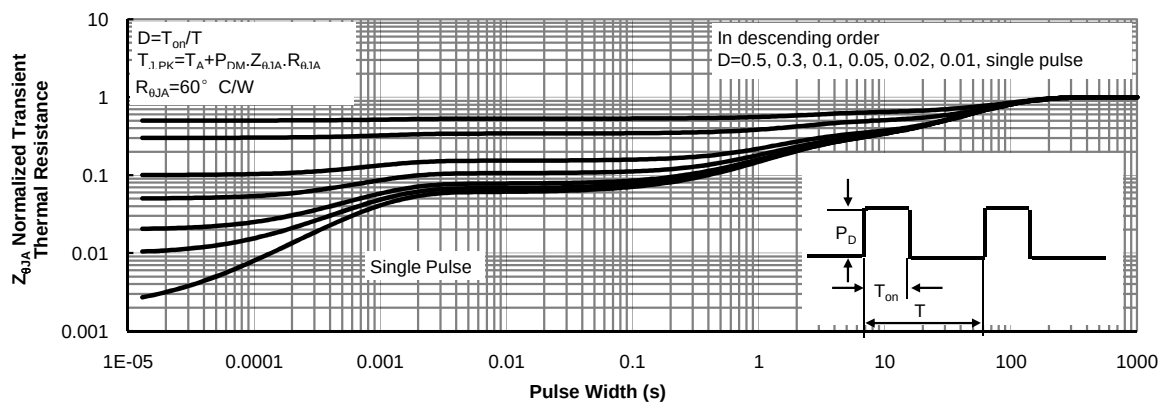
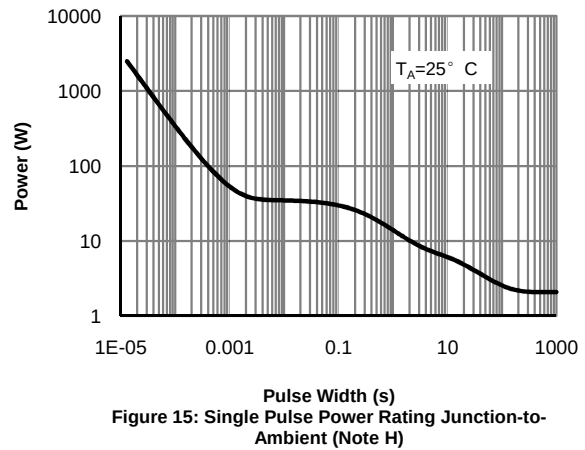
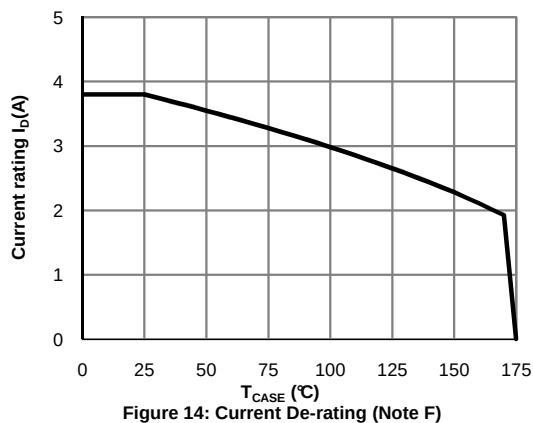
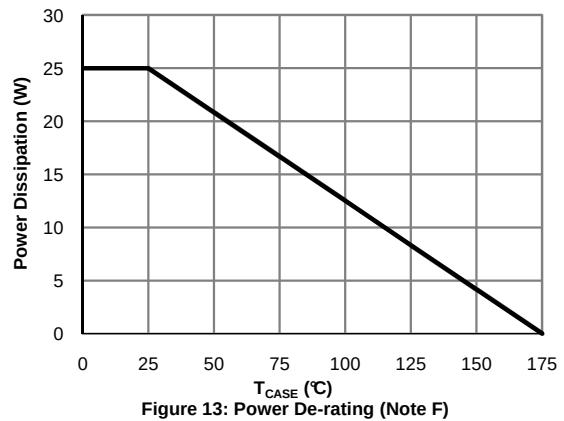
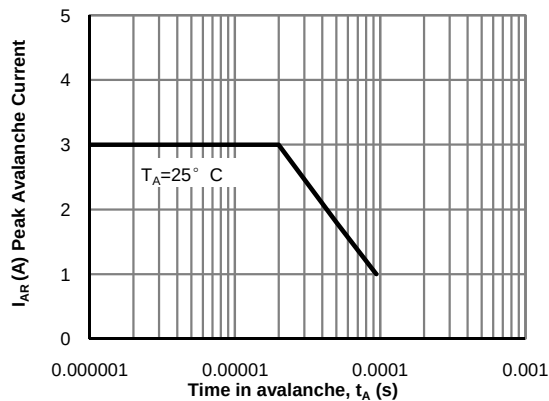
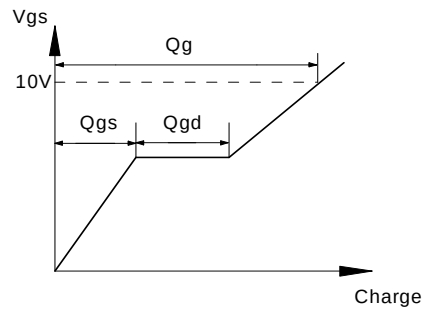
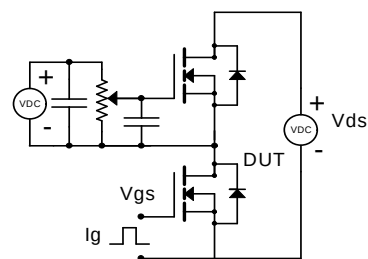


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

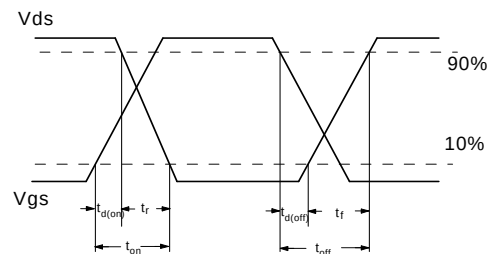
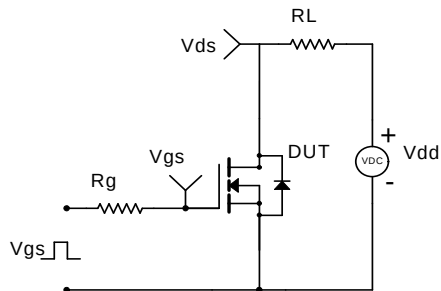
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



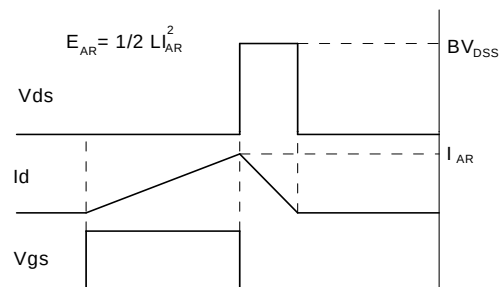
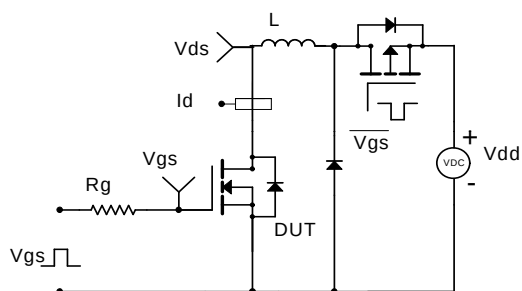
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

