ADW11000–SPECIFICATIONS

ANALOG SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V, CDS Mode, f_{ADCCLK} = 15 MHz, $f_{CDSCLK1}$ = $f_{CDSCLK2}$ = 5 MHz, PGA Gain = 1, Input range = 4 V p-p, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
MAXIMUM CONVERSION RATE				
3-Channel Mode with CDS		30		MSPS
2-Channel Mode with CDS		30		MSPS
1-Channel Mode with CDS		18		MSPS
ACCURACY (ENTIRE SIGNAL PATH)				
ADC Resolution		16		Bits
Integral Nonlinearity (INL)		±16		LSB
Differential Nonlinearity (DNL)		±0.5		LSB
No Missing Codes		Guaranteed		
ANALOG INPUTS				
Input Signal Range (Programmable)[1]		2.0/4.0		V p-p
Allowable Reset Transient[1]		1.0		V
Input Limits[2]	AVSS – 0.3		AVDD + 0.3	V
Input Capacitance		10		pF
Input Bias Current		10		nA
AMPLIFIERS				
PGA Gain	1		6	V/V
PGA Gain Resolution[2]		64		Steps
PGA Gain Monotonicity		Guaranteed		
Programmable Offset	–300		+300	mV
Programmable Offset Resolution		512		Steps
Programmable Offset Monotonicity		Guaranteed		
NOISE AND CROSSTALK				
Total Output Noise @ PGA Minimum		3.0		LSB rms
Total Output Noise @ PGA Maximum		9.0		LSB rms
Channel-to-Channel Crosstalk				
@ 15 MSPS		70		dB
@ 6 MSPS		90		dB
POWER SUPPLY REJECTION				
AVDD = 5 V ± 0.25 V		0.1		% FSR
DIFFERENTIAL VREF (at 25°C)				
CAPT–CAPB		2.0		V
TEMPERATURE RANGE				
Operating	–40		+105	°C
Storage	–65		+150	°C
POWER SUPPLIES				
AVDD	4.75	5.0	5.25	V
DRVDD	3.0	5.0	5.25	V
OPERATING CURRENT				
AVDD		75		mA
DRVDD		5		mA
Power-Down Mode		200		µA
POWER DISSIPATION				
3-Channel Mode		400		mW
1-Channel Mode		300		mW

NOTES

[1]Linear Input Signal Range is from 0 V to 4 V when the CCD's reference level is clamped to 4 V by the ADW11000's input clamp.

[2]The PGA Gain is approximately "linear in dB" and follows the equation: $Gain = \frac{6.0}{1 + 5.0\left[\frac{63 - G}{63}\right]}$ where G is the register value.

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V, CDS Mode, f_{ADCCLK} = 15 MHz, $f_{CDSCLK1}$ = $f_{CDSCLK2}$ = 5 MHz, C_L = 10 pF, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.0			V
Low Level Input Voltage	V_{IL}			0.8	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage	V_{OH}	4.5			V
Low Level Output Voltage	V_{OL}			0.1	V
High Level Output Current	I_{OH}		50		µA
Low Level Output Current	I_{OL}		50		µA
LOGIC OUTPUTS (with DRVDD = 3 V)					
High Level Output Voltage, (I_{OH} = 50 µA)	V_{OH}	2.95			V
Low Level Output Voltage (I_{OL} = 50 µA)	V_{OL}			0.05	V

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V, specs are for 16-bit performance.)

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK PARAMETERS					
3-Channel Pixel Rate	t_{PRA}	200			ns
1-Channel Pixel Rate	t_{PRB}	80			ns
ADCCLK Pulsewidth	t_{ADCLK}	30			ns
CDSCLK1 Pulsewidth	t_{C1}	8			ns
CDSCLK2 Pulsewidth	t_{C2}	8			ns
CDSCLK1 Falling to CDSCLK2 Rising	t_{C1C2}	0			ns
ADCCLK Falling to CDSCLK2 Rising	t_{ADC2}	0			ns
CDSCLK2 Rising to ADCCLK Rising	t_{C2ADR}	5			ns
CDSCLK2 Falling to ADCCLK Falling	t_{C2ADF}	30			ns
CDSCLK2 Falling to CDSCLK1 Rising	t_{C2C1}	5			ns
Aperture Delay for CDS Clocks	t_{AD}		2		ns
SERIAL INTERFACE					
Maximum SCLK Frequency	f_{SCLK}	10			MHz
SLOAD to SCLK Set-Up Time	t_{LS}	10			ns
SCLK to SLOAD Hold Time	t_{LH}	10			ns
SDATA to SCLK Rising Set-Up Time	t_{DS}	10			ns
SCLK Rising to SDATA Hold Time	t_{DH}	10			ns
SCLK Falling to SDATA Valid	t_{RDV}	10			ns
DATA OUTPUTS					
Output Delay	t_{OD}		6		ns
3-State to Data Valid	t_{DV}		10		ns
Output Enable High to 3-State	t_{HZ}		10		ns
Latency (Pipeline Delay)			3 (Fixed)		Cycles

NOTES

It is recommended that CDSCLK falling edges do not occur within the first 10 ns following an ADCCLK edge.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect To	Min	Max	Unit
VIN, CAPT, CAPB	AVSS	–0.3	AVDD + 0.3	V
Digital Inputs	AVSS	–0.3	AVDD + 0.3	V
AVDD	AVSS	–0.5	+6.5	V
DRVDD	DRVSS	–0.5	+6.5	V
AVSS	DRVSS	–0.3	+0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

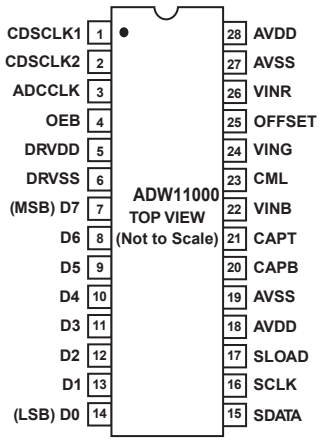
*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS
Thermal Resistance
28-Lead 5.3 mm SSOP
θ_{JA} = 109°C/W
θ_{JC} = 39°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADW11000 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1	CDSCLK1	DI	CDS Reference Level Sampling Clock
2	CDSCLK2	DI	CDS Data Level Sampling Clock
3	ADCCLK	DI	A/D Converter Sampling Clock
4	OEB	DI	Output Enable, Active Low
5	DRVDD	P	Digital Output Driver Supply
6	DRVSS	P	Digital Output Driver Ground
7	D7	DO	Data Output MSB. ADC DB15 High Byte, ADC DB7 Low Byte
8	D6	DO	Data Output. ADC DB14 High Byte, ADC DB6 Low Byte
9	D5	DO	Data Output. ADC DB13 High Byte, ADC DB5 Low Byte
10	D4	DO	Data Output. ADC DB12 High Byte, ADC DB4 Low Byte
11	D3	DO	Data Output. ADC DB11 High Byte, ADC DB3 Low Byte
12	D2	DO	Data Output. ADC DB10 High Byte, ADC DB2 Low Byte
13	D1	DO	Data Output. ADC DB9 High Byte, ADC DB1 Low Byte
14	D0	DO	Data Output LSB. ADC DB8 High Byte, ADC DB0 Low Byte
15	SDATA	DI/DO	Serial Interface Data Input/Output
16	SCLK	DI	Serial Interface Clock Input
17	SLOAD	DI	Serial Interface Load Pulse
18, 28	AVDD	P	5 V Analog Supply
19, 27	AVSS	P	Analog Ground
20	CAPB	AO	ADC Bottom Reference Voltage Decoupling
21	CAPT	AO	ADC Top Reference Voltage Decoupling
22	VINB	AI	Analog Input, Blue Channel
23	CML	AO	Internal Bias Level Decoupling
24	VING	AI	Analog Input, Green Channel
25	OFFSET	AO	Clamp Bias Level Decoupling
26	VINR	AI	Analog Input, Red Channel

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

Integral nonlinearity error refers to the deviation of each individual code from a line drawn from "zero scale" through "positive full scale." The point used as "zero scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 16-bit resolution indicates that all 65536 codes, respectively, must be present over all operating ranges.

OFFSET ERROR

The first ADC code transition should occur at a level 1/2 LSB above the nominal zero scale voltage. The offset error is the deviation of the actual first code transition level from the ideal level.

GAIN ERROR

The last code transition should occur for an analog value 1 1/2 LSB below the nominal full scale voltage. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

INPUT REFERRED NOISE

The rms output noise is measured using histogram techniques. The ADC output codes' standard deviation is calculated in LSB, and can be converted to an equivalent voltage, using the relationship 1 LSB = 4 V/65536 = 61 μV. The noise may then be referred to the input of the ADW11000 by dividing by the PGA gain.

CHANNEL-TO-CHANNEL CROSSTALK

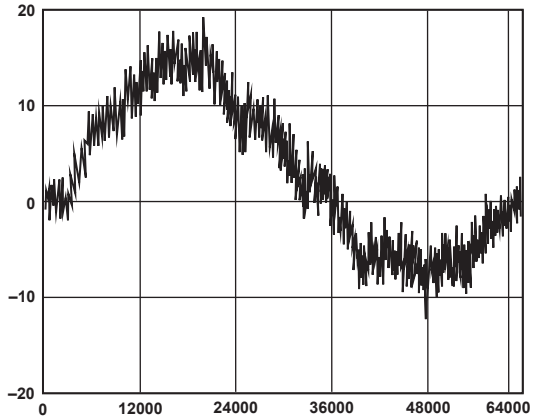
In an ideal 3-channel system, the signal in one channel will not influence the signal level of another channel. The channel-to-channel crosstalk specification is a measure of the change that occurs in one channel as the other two channels are varied. In the ADW11000, one channel is grounded and the other two channels are exercised with full scale input signals. The change in the output codes from the first channel is measured and compared with the result when all three channels are grounded. The difference is the channel-to-channel crosstalk, stated in LSB.

APERTURE DELAY

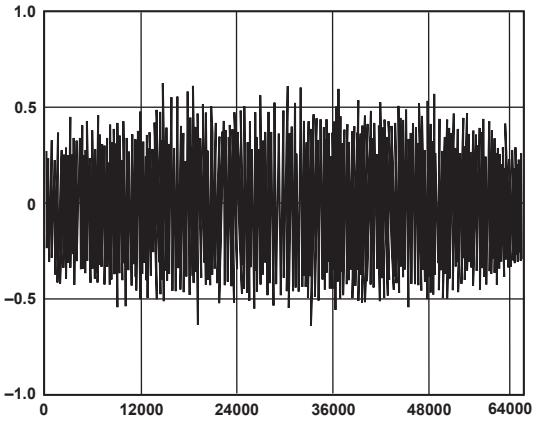
The aperture delay is the time delay that occurs from when a sampling edge is applied to the ADW11000 until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low, so the aperture delay is measured from each clock's falling edge to the instant the actual internal sample is taken.

POWER SUPPLY REJECTION

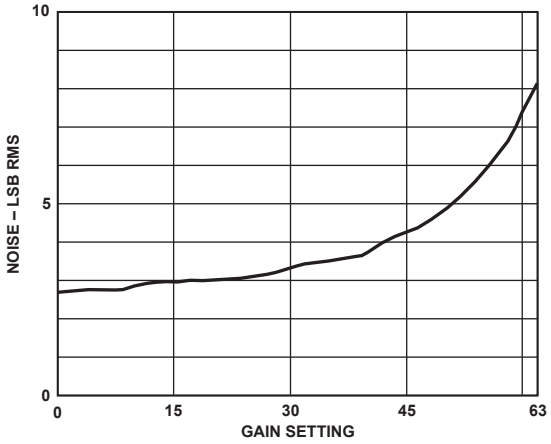
Power supply rejection specifies the maximum full-scale change that occurs from the initial value when the supplies are varied over the specified limits.



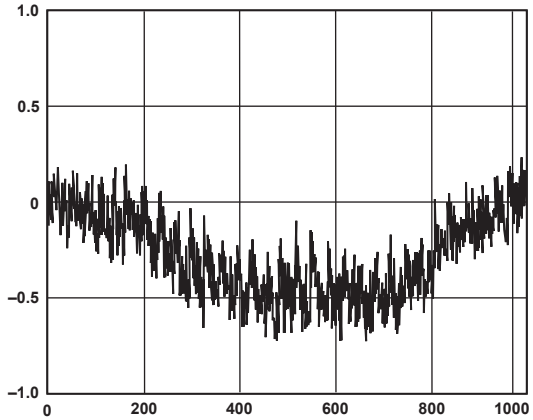
TPC 1. Typical INL Performance at 15 MSPS



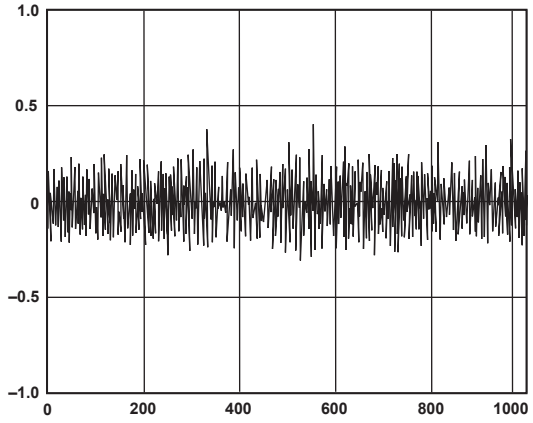
TPC 2. Typical DNL Performance at 15 MSPS



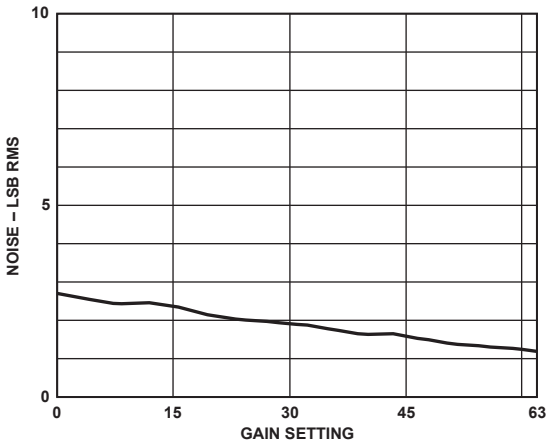
TPC 3. Output Noise vs. Gain



TPC 4. Typical INL Performance at 30 MSPS



TPC 5. Typical DNL Performance at 30 MSPS



TPC 6. Input Referred Noise vs. Gain

TIMING DIAGRAMS

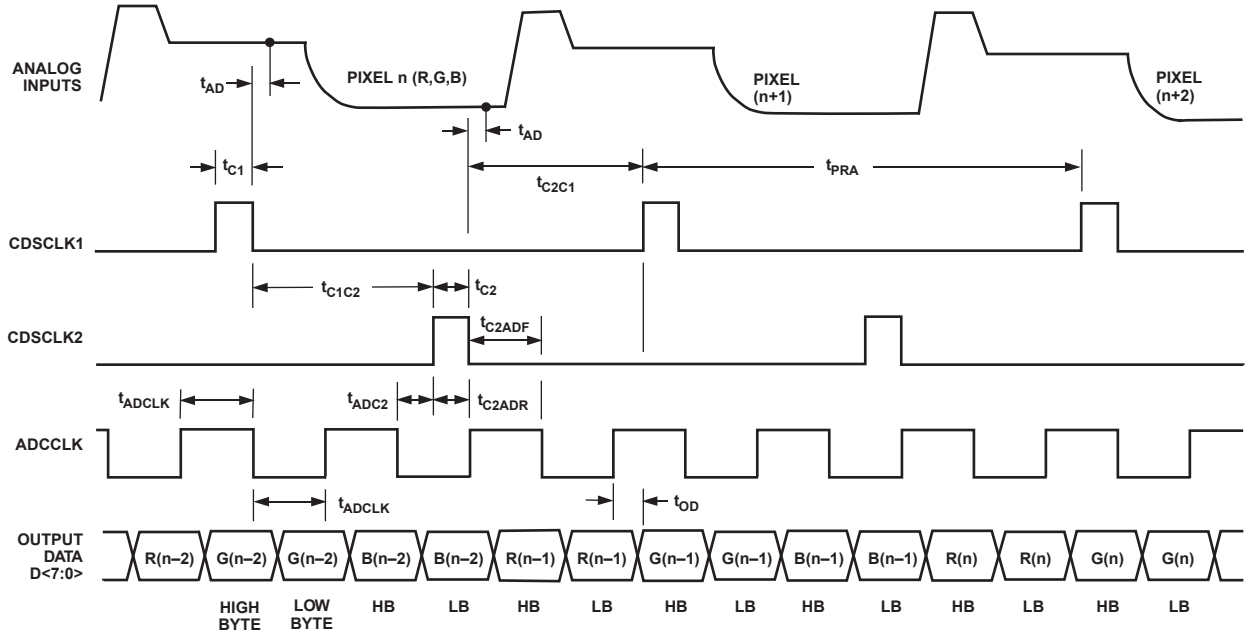


Figure 1. 3-Channel CDS Mode Timing

It is recommended that CDSCLK falling edges do not occur within the first 10 ns following an ADCCLK edge.

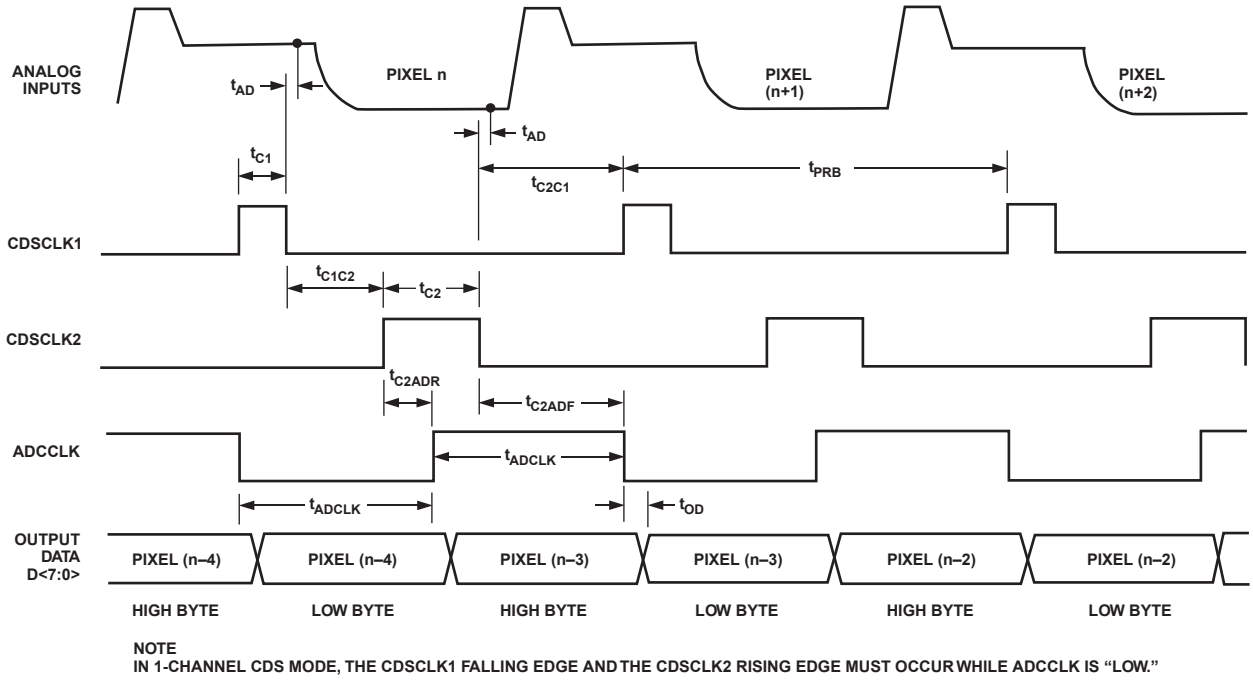


Figure 2. 1-Channel CDS Mode Timing

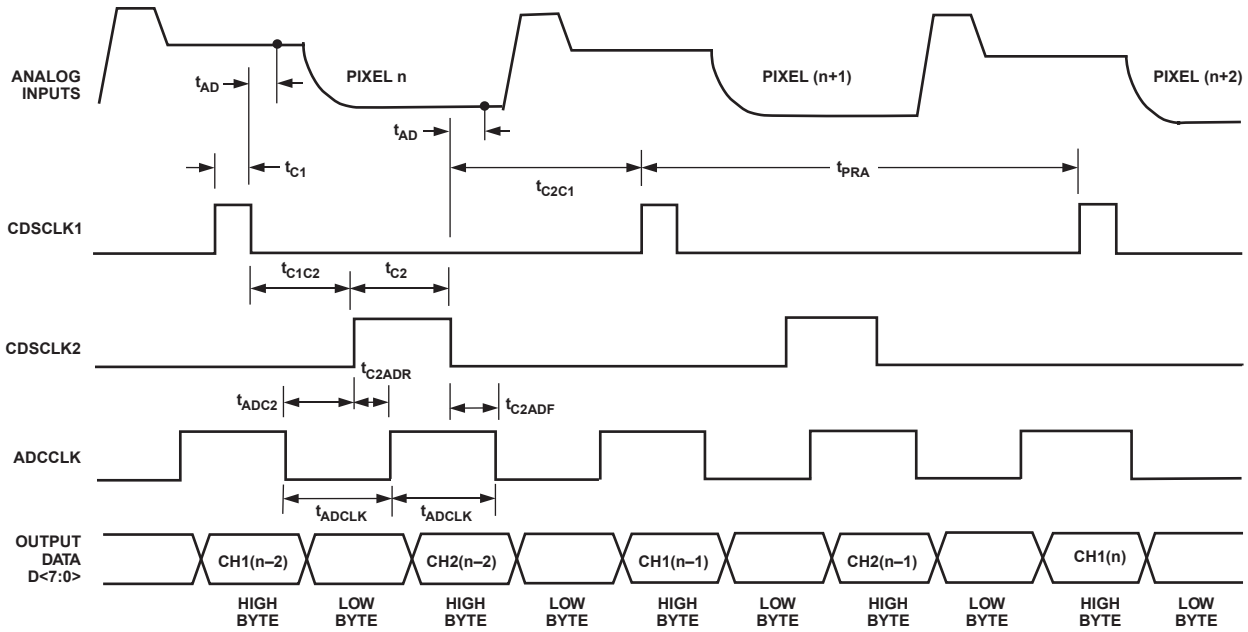


Figure 3. 2-Channel CDS Mode Timing

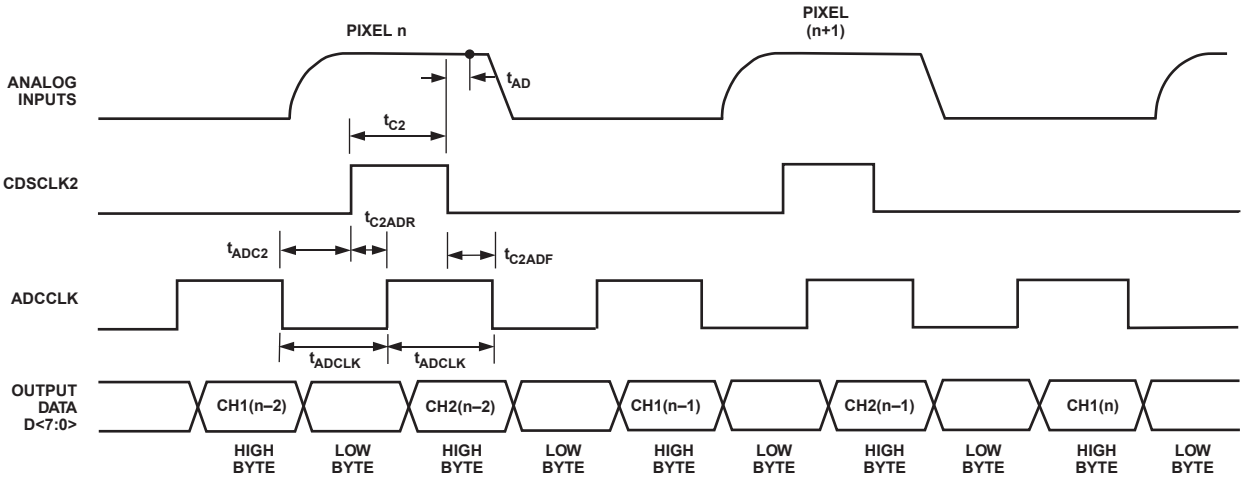


Figure 4. 2-Channel SHA Mode Timing

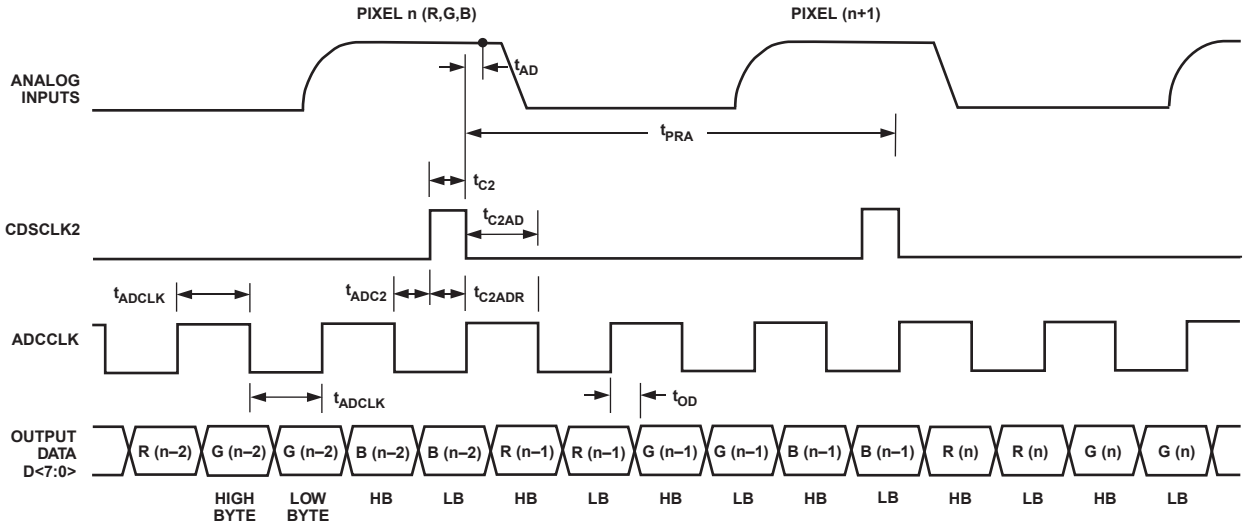


Figure 5. 3-Channel SHA Mode Timing

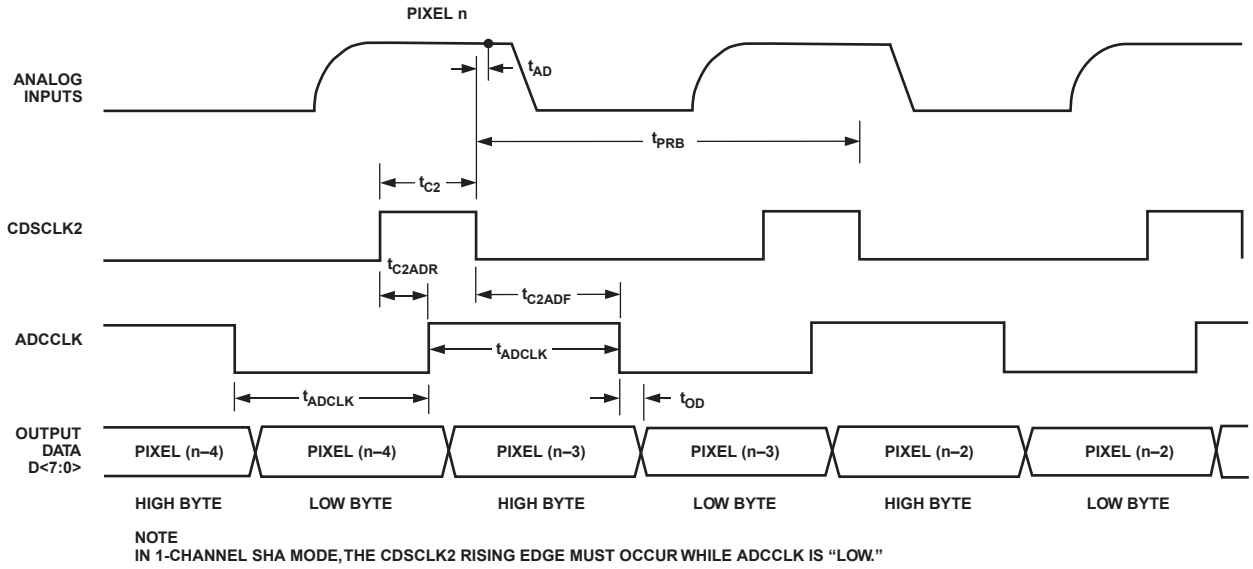


Figure 6. 1-Channel SHA Mode Timing

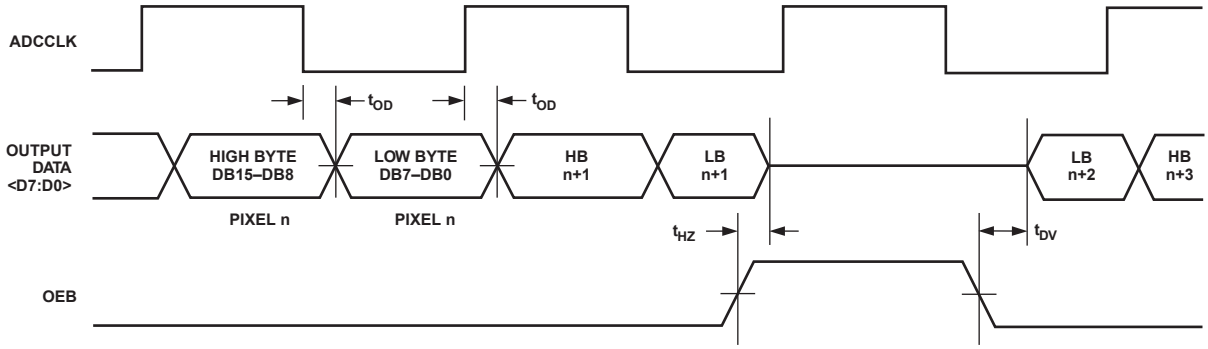


Figure 7. Digital Output Data Timing

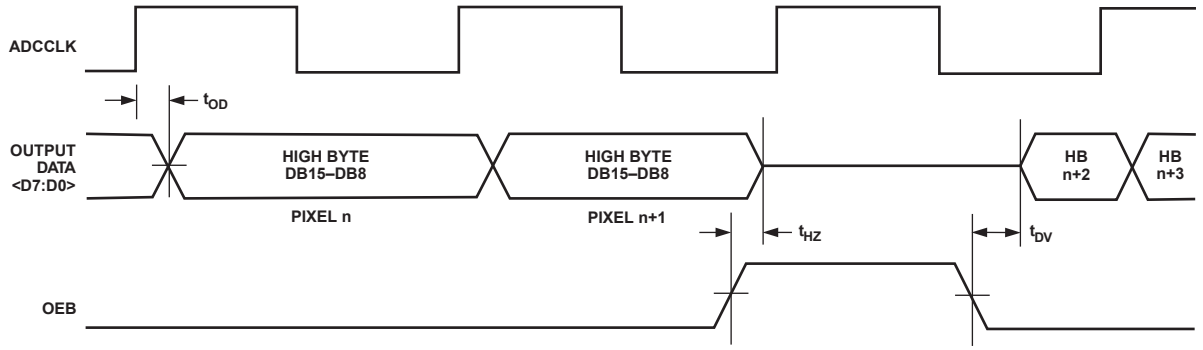


Figure 8. Single Byte Mode Digital Output Data Timing

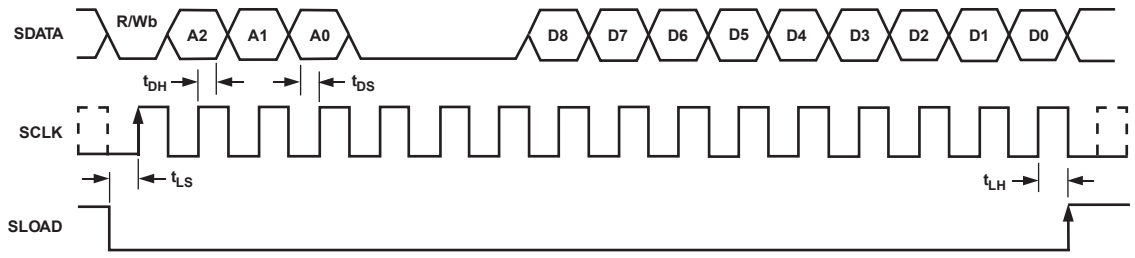


Figure 9. Serial Write Operation Timing

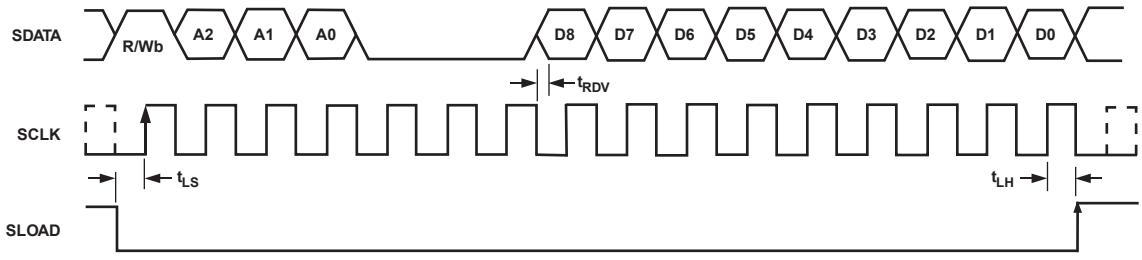
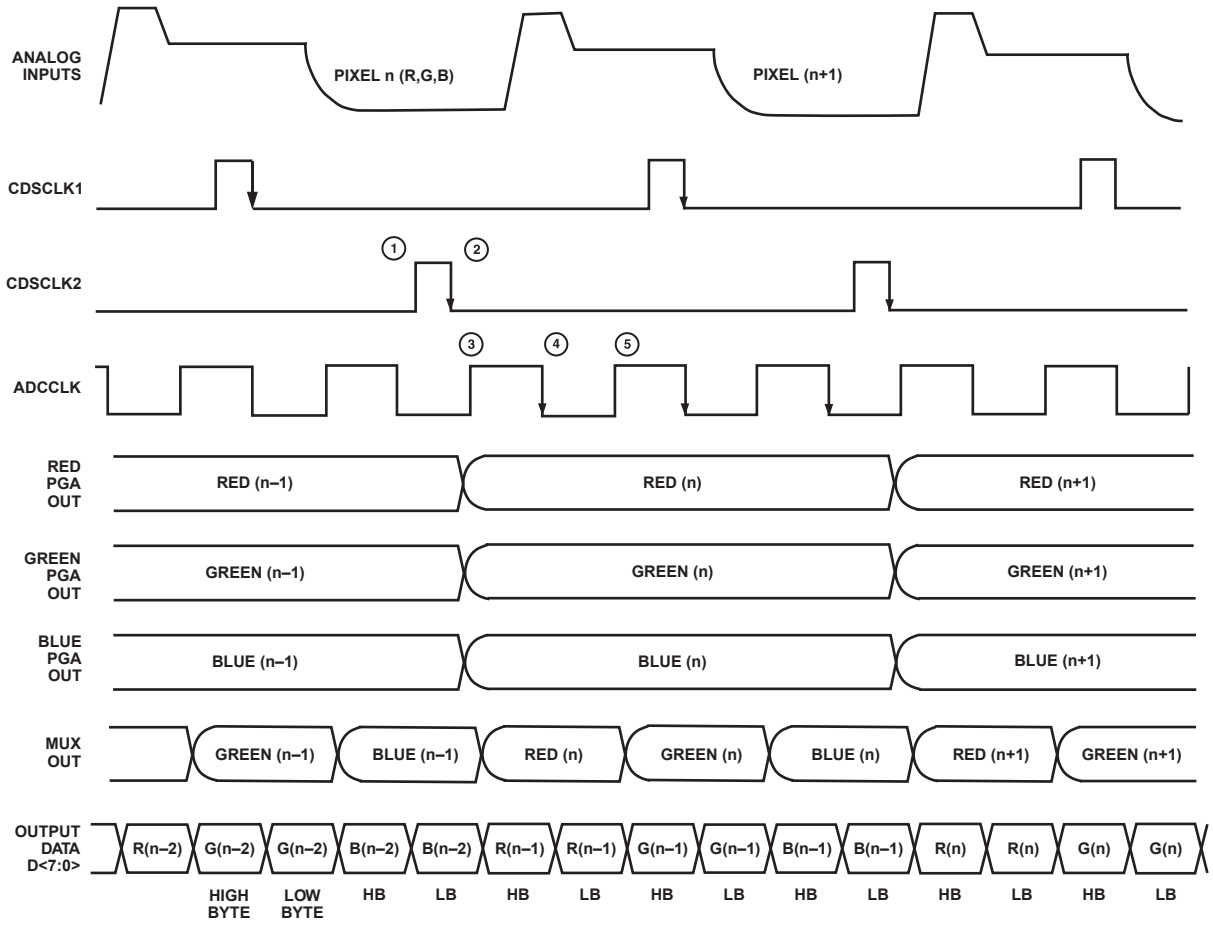


Figure 10. Serial Read Operation Timing



NOTES
1. THE MUX STATE MACHINE IS INTERNALLY RESET AT THE CDSCLK2 RISING EDGE.
2. EACH PIXEL IS SAMPLED AND AMPLIFIED BY THE PGAs AT CDSCLK2 FALLING EDGE.
3. AFTER CDSCLK2 RISING EDGE, THE NEXT ADCCLK RISING EDGE WILL ALWAYS SELECT RED PGA OUTPUT.
4. THE ADC SAMPLES THE MUX OUTPUT ON ADCCLK FALLING EDGES.
5. THE MUX SWITCHES TO THE NEXT PGA OUTPUT AT ADCCLK RISING EDGES.

Figure 11. Internal Timing Diagram for 3-Channel CDS Mode

FUNCTIONAL DESCRIPTION

The ADW11000 can be operated in six different modes: 3-Channel CDS Mode, 3-Channel SHA Mode, 2-Channel CDS Mode, 2-Channel SHA Mode, 1-Channel CDS Mode, and 1-Channel SHA Mode. Each mode is selected by programming the Configuration Registers through the serial interface. For more detail on CDS or SHA mode operation, see the Circuit Operation section.

3-Channel CDS Mode

In 3-Channel CDS Mode, the ADW11000 simultaneously samples the Red, Green, and Blue input voltages from the CCD outputs. The sampling points for each Correlated Double Sampler (CDS) are controlled by CDSCLK1 and CDSCLK2 (see Figures 11 and 13). CDSCLK1's falling edge samples the reference level of the CCD waveform. CDSCLK2's falling edge samples the data level of the CCD waveform. Each CDS amplifier outputs the difference between the CCD's reference and data levels. Next, the output voltage of each CDS amplifier is level-shifted by an Offset DAC. The voltages are then scaled by the three Programmable Gain Amplifiers before being multiplexed through the 16-Bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The offset and gain values for the Red, Green, and Blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX Configuration register.

Timing for this mode is shown in Figure 1. It is recommended that the falling edge of CDSCLK2 occur before the rising edge of ADCCLK, although this is not required to satisfy the minimum timing constraints. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is three clock cycles.

3-Channel SHA Mode

In 3-Channel SHA Mode, the ADW11000 simultaneously samples the Red, Green, and Blue input voltages. The sampling point is controlled by CDSCLK2. CDSCLK2's falling edge samples the input waveforms on each channel. The output voltages from the three SHAs are modified by the offset DACs and then scaled by the three PGAs. The outputs of the PGAs are then multiplexed through the 16-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The input signal is sampled with respect to the voltage applied to the OFFSET pin (see Figure 14). With the OFFSET pin grounded, a zero volt input corresponds to the ADC's zero scale output. The OFFSET pin may also be used as a coarse offset adjust pin. A voltage applied to this pin will be subtracted from the voltages applied to the Red, Green, and Blue inputs in the first amplifier stage of the ADW11000. The input clamp is disabled in this mode. For more information, see the Circuit Operation section.

Timing for this mode is shown in Figure 5. CDSCLK1 should be grounded in this mode. Although it is not required, it is recommended that the falling edge of CDSCLK2 occur before the rising edge of ADCCLK. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is three ADCCLK cycles.

The offset and gain values for the Red, Green, and Blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX Configuration register.

2-Channel CDS Mode

The 2-Channel Mode is selected by writing a "1" into two of the channel select bits of the MUX register (D4–D6). Bit D5 of the configuration register also needs to be set low to take the part out of 3-Channel Mode. The channels that will be used is determined by the contents of Bits D4–D6 of the MUX Configuration Register (see Table III). The combination of inputs that can be selected are; RG, RB, or GB by writing a "1" into the appropriate bit. The sample order is selected by Bit D7. If D7 is high, the MUX will sample in the following order: RG or RB or GB depending on which channels are turned on. If Bit D7 is set low the mux will sample in the following order: GR or BR or BG depending on which channels are turned on.

The ADW11000 simultaneously samples the selected channels' input voltages from the CCD outputs. The sampling points for each Correlated Double Sampler (CDS) are controlled by CDSCLK1 and CDSCLK2 (see Figure 11). CDSCLK1's falling edge samples the reference level of the CCD waveform. CDSCLK2's falling edge samples the data level of the CCD waveform. Each CDS amplifier outputs the difference between the CCD's reference and data levels. Next, the output voltage of each CDS amplifier is level-shifted by an Offset DAC. The voltages are then scaled by the two Programmable Gain Amplifiers before being multiplexed through the 16-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The offset and gain values for the Red, Green, and Blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX Configuration Register.

Timing for this mode is shown in Figure 3. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is three clock cycles.

2-Channel SHA Mode

The 2-Channel Mode is selected by writing a "1" into two of the channel select bits of the MUX Register (D4–D6). Bit D5 of the configuration register also needs to be set low to take the part out of 3-Channel Mode. The channels that will be used is determined by the contents of Bits D4–D6 of the MUX Configuration Register (see Table III). The combination of inputs that can be selected are; RG, RB, or GB by writing a "1" into the appropriate bit. The sample order is selected by Bit D7. If D7 is high, the mux will sample in the following order: RG or RB or GB, depending on which channels are turned on. If Bit D7 is set low, the mux will sample in the following order: GR or BR or BG, depending on which channels are turned on.

In 2-Channel SHA Mode, the ADW11000 simultaneously samples the selected channels' input voltages. The sampling point is controlled by CDSCLK2. CDSCLK2's falling edge samples the input waveforms on each channel. The output voltages from the two SHAs are modified by the offset DACs and then scaled by the two PGAs. The outputs of the PGAs are then multiplexed through the 16-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The input signal is sampled with respect to the voltage applied to the OFFSET pin (see Figure 14). With the OFFSET pin grounded, a zero volt input corresponds to the ADC's zero scale output. The OFFSET pin may also be used as a coarse offset

adjust pin. A voltage applied to this pin will be subtracted from the voltages applied to the Red, Green, and Blue inputs in the first amplifier stage of the ADW11000. The input clamp is disabled in this mode. For more information, see the Circuit Operation section.

Timing for this mode is shown in Figure 4. CDSCLK1 should be grounded in this mode. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is three ADCCLK cycles. The offset and gain values for the Red, Green, and Blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX Configuration Register.

1-Channel CDS Mode

This mode operates the same way as the 3-Channel CDS mode. The difference is that the multiplexer remains fixed in this mode, so only the channel specified in the MUX Configuration Register is processed.

Timing for this mode is shown in Figure 2.

1-Channel SHA Mode

This mode operates the same way as 3-Channel SHA mode, except that the multiplexer remains stationary. Only the channel specified in the MUX Configuration Register is processed.

Timing for this mode is shown in Figure 6. CDSCLK1 should be grounded in this mode of operation.

Configuration Register

The Configuration Register controls the ADW11000's operating mode and bias levels. Bits D8 and D1 should always be set low. Bit D7 controls the input range of the ADW11000. Setting D7 high sets the input range to 4 V while setting Bit D7 low sets the input range to 2 V. Bit D6 controls the internal voltage reference. If the ADW11000's internal voltage reference is used, then this bit is set high. Setting Bit D6 low will disable the internal voltage reference, allowing an external voltage reference to be used. Setting Bit D5 high will configure the ADW11000 for 3-channel operation. If D5 is set low, the part will be in either 2CH or 1CH mode based on the settings in the MUX Configuration Register (See Table III and the MUX Configuration Register description). Setting Bit D4 high will enable the CDS mode of operation, and setting this bit low will enable the SHA mode of operation. Bit D3 sets the dc bias level of the ADW11000's input clamp.

This bit should always be set high for the 4 V clamp bias, unless a CCD with a reset feedthrough transient exceeding 2 V is used. If the 3 V clamp bias level is used, then the peak-to-peak input signal range to the ADW11000 is reduced to 3 V maximum. Bit D2 controls the power-down mode. Setting Bit D2 high will place the ADW11000 into a very low-power "sleep" mode. All register contents are retained while the ADW11000 is in the powered-down state. Bit D0 controls the output mode of the ADW11000. Setting Bit D0 high will enable a single byte output mode where only the 8 MSBs of the 16 b ADC will be output on each rising edge of ADCCLK (see Figure 8). If Bit D0 is set low, then the 16 b ADC output is multiplexed into two bytes. The MSByte is output on ADCCLK rising edge and the LSByte is output on ADCCLK falling edge.

Table I. Internal Register Map

Register Name	Address			Data Bits								
	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	0	Input Rng	VREF	3CH Mode	CDS On	Clamp	Pwr Dn	0	1 Byte Out
MUX Config	0	0	1	0	RGB/BGR	Red	Green	Blue	0	0	0	0
Red PGA	0	1	0	0	0	0	MSB					LSB
Green PGA	0	1	1	0	0	0	MSB					LSB
Blue PGA	1	0	0	0	0	0	MSB					LSB
Red Offset	1	0	1	MSB								LSB
Green Offset	1	1	0	MSB								LSB
Blue Offset	1	1	1	MSB								LSB

Table II. Configuration Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Input Range	Internal VREF	3CH Mode	CDS Operation	Input Clamp Bias	Power-Down	Set to 0	Output Mode
	1 = 4 V* 0 = 2 V	1 = Enabled* 0 = Disabled	1 = On* 0 = Off	1 = CDS Mode* 0 = SHA Mode	1 = 4 V* 0 = 3 V	1 = On 0 = Off (Normal)*		0 = 2 Byte* 1 = 1 Byte

*Power-on default value.

MUX Configuration Register

The MUX Configuration Register controls the sampling channel order and the 2-Channel Mode configuration in the ADW11000. Bits D8 and D3–D0 should always be set low. Bit D7 is used when operating in 3-Channel or 2-Channel Mode. Setting Bit D7 high will sequence the MUX to sample the Red channel first, then the Green channel, and then the Blue channel. When in 3-channel mode, the CDSCLK2 pulse always resets the MUX to sample the Red channel first (see Figure 11). When Bit D7 is set low, the channel order is reversed to Blue first, Green second, and Red third. The CDSCLK2 pulse will always reset the MUX to sample the Blue channel first. Bits D6, D5, and D4 are used when operating in 1 or 2-Channel Mode. Bit D6 is set high to sample the Red channel. Bit D5 is set high to sample the Green channel. Bit D4 is set high to sample the Blue channel. The MUX will remain stationary during 1-channel mode. Two-Channel Mode is selected by setting two of the channel select Bits (D4–D6) high. The MUX samples the channels in the order selected by Bit D7.

PGA Gain Registers

There are three PGA registers for individually programming the gain in the Red, Green, and Blue channels. Bits D8, D7, and D6 in each register must be set low, and Bits D5 through D0 control the gain range from 1× to 6× in 64 increments. See Figure 17 for a graph of the PGA gain versus PGA register code. The coding for the PGA registers is straight binary, with an all "zeros" word corresponding to the minimum gain setting (1×) and an all "ones" word corresponding to the maximum gain setting (6×).

Offset Registers

There are three Offset Registers for individually programming the offset in the Red, Green, and Blue channels. Bits D8 through D0 control the offset range from –300 mV to +300 mV in 512 increments. The coding for the Offset Registers is Sign Magnitude, with D8 as the sign bit. Table V shows the offset range as a function of the Bits D8 through D0.

Table III. MUX Configuration Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	MUX Order 1 = R-G-B* 0 = B-G-R	Channel Select 1 = RED* 0 = Off	Channel Select 1 = GREEN 0 = Off*	Channel Select 1 = BLUE 0 = Off*	Set to 0	Set to 0	Set to 0	Set to 0

*Power-on default value.

Table IV. PGA Gain Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0	Gain (V/V)	Gain (dB)
Set to 0	Set to 0	Set to 0	MSB					LSB		
0	0	0	0	0	0	0	0	0*	1.0	0.0
0	0	0	0	0	0	0	0	1	1.013	0.12
				•					•	•
				•					•	•
				•					•	•
0	0	0	1	1	1	1	1	1	5.56	14.9
0	0	0	1	1	1	1	1	1	6.0	15.56

*Power-on default value.

Table V. Offset Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0	Offset (mV)
MSB								LSB	
0	0	0	0	0	0	0	0	0*	0
0	0	0	0	0	0	0	0	1	+1.2
				•					•
				•					•
				•					•
0	1	1	1	1	1	1	1	1	+300
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	–1.2
				•					•
				•					•
				•					•
1	1	1	1	1	1	1	1	1	–300

*Power-on default value.

CIRCUIT OPERATION

Analog Inputs—CDS Mode Operation

Figure 12 shows the analog input configuration for the CDS mode of operation. Figure 13 shows the internal timing for the sampling switches. The CCD reference level is sampled when CDSCLK1 transitions from high to low, opening S1. The CCD data level is sampled when CDSCLK2 transitions from high to low, opening S2. S3 is then closed, generating a differential output voltage representing the difference between the two sampled levels.

The input clamp is controlled by CDSCLK1. When CDSCLK1 is high, S4 closes and the internal bias voltage is connected to the analog input. The bias voltage charges the external 0.1 µF input capacitor, level-shifting the CCD signal into the ADW11000's input common-mode range. The time constant of the input clamp is determined by the internal 5 kΩ resistance and the external 0.1 µF input capacitance.

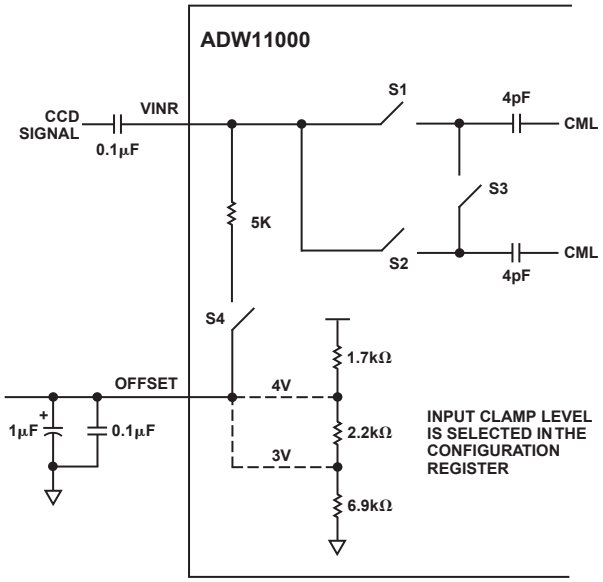


Figure 12. CDS-Mode Input Configuration (All Three Channels Are Identical)

External Input Coupling Capacitors

The recommended value for the input coupling capacitors is 0.1 µF. While it is possible to use a smaller capacitor, this larger value is chosen for several reasons:

Crosstalk

The input coupling capacitor creates a capacitive divider with any parasitic capacitance between PCB traces and on chip traces. C_{IN} should be large relative to these parasitic capacitances in order to minimize this effect. For example, with a 100 pF input capacitance and just a few hundred fF of parasitic capacitance on the PCB and/or the IC the imaging system could expect to have hundreds of LSBs of crosstalk at the 16 b level. Using a large capacitor value = 0.1 µF will minimize any errors due to crosstalk.

Signal Attenuation

The input coupling capacitor creates a capacitive divider with a CMOS integrated circuit's input capacitance, attenuating the CCD signal level. C_{IN} should be large relative to the IC's 10 pF input capacitance in order to minimize this effect.

Linearity

Some of the input capacitance of a CMOS IC is junction capacitance, which varies nonlinearly with applied voltage. If the input coupling capacitor is too small, then the attenuation of the CCD signal will vary nonlinearly with signal level. This will degrade the system linearity performance.

Sampling Errors

The internal 4 pF sample capacitors have a "memory" of the previously sampled pixel. There is a charge redistribution error between C_{IN} and the internal sample capacitors for larger pixel-to-pixel voltage swings. As the value of C_{IN} is reduced, the resulting error in the sampled voltage will increase. With a C_{IN} value of 0.1 µF, the charge redistribution error will be less than 1 LSB for a full-scale pixel-to-pixel voltage swing.

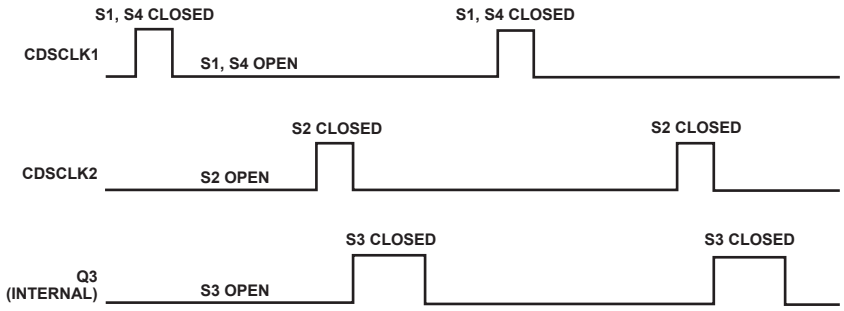


Figure 13. CDS-Mode Internal Switch Timing

Analog Inputs—SHA Mode Operation

Figure 14 shows the analog input configuration for the SHA mode of operation. Figure 15 shows the internal timing for the sampling switches. The input signal is sampled when CDSCLK2 transitions from high to low, opening S1. The voltage on the OFFSET pin is also sampled on the falling edge of CDSCLK2, when S2 opens. S3 is then closed, generating a differential output voltage representing the difference between the sampled input voltage and the OFFSET voltage. The input clamp is disabled during SHA mode operation.

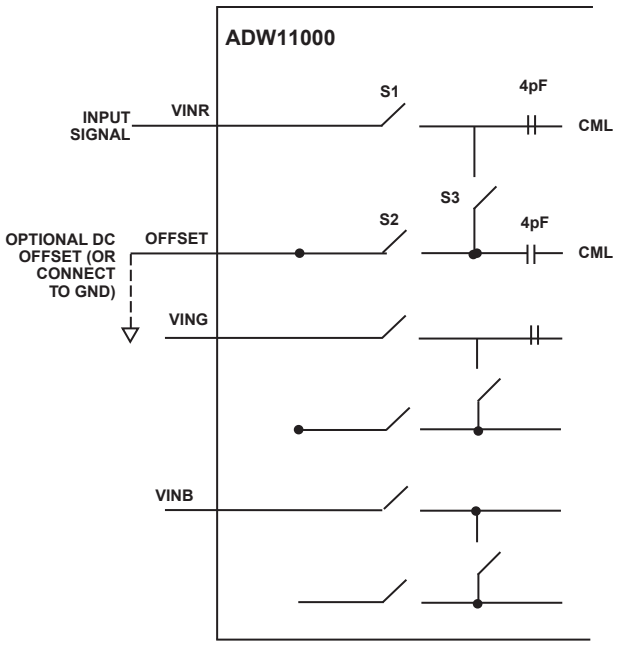


Figure 14. SHA-Mode Input Configuration (All Three Channels Are Identical)

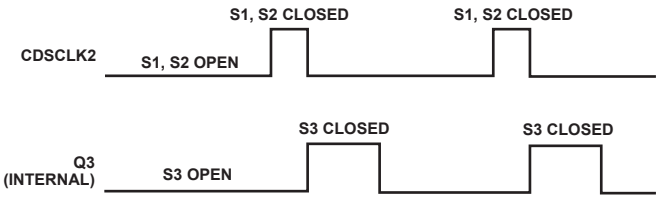


Figure 15. SHA-Mode Internal Switch Timing

Figure 16 shows how the OFFSET pin may be used in a CIS application for coarse offset adjustment. Many CIS signals have dc offsets ranging from several hundred millivolts to more than 1 V. By connecting the appropriate dc voltage to the OFFSET pin, the CIS signal will be restored to "zero." After the large dc offset is removed, the signal can be scaled using the PGA to maximize the ADC's dynamic range.

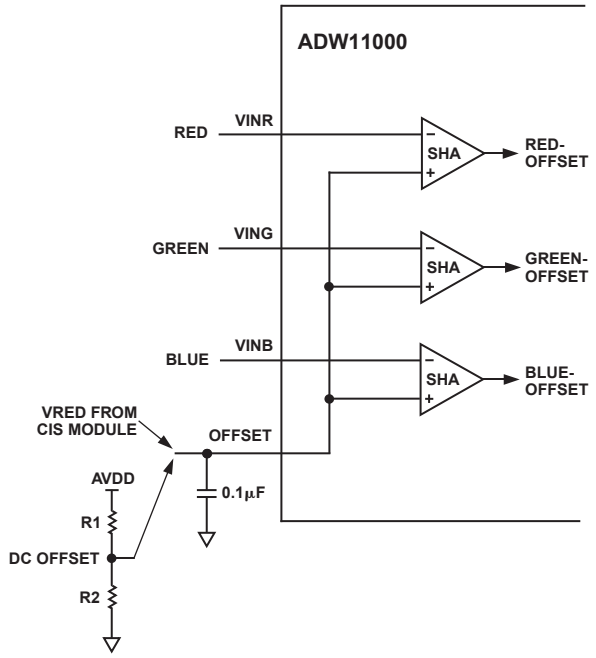


Figure 16. SHA-Mode Used with External DC Offset

Programmable Gain Amplifiers

The ADW11000 uses one Programmable Gain Amplifier (PGA) for each channel. Each PGA has a gain range from 1× (0 dB) to 6.0× (15.56 dB), adjustable in 64 steps. Figure 17 shows the PGA gain as a function of the PGA register code. Although the gain curve is approximately "linear in dB," the gain in V/V varies nonlinearly with register code, following the equation:

$$Gain = \frac{6.0}{1 + 5.0\left[\frac{63 - G}{63}\right]}$$

where G is the decimal value of the gain register contents, and varies from 0 to 63.

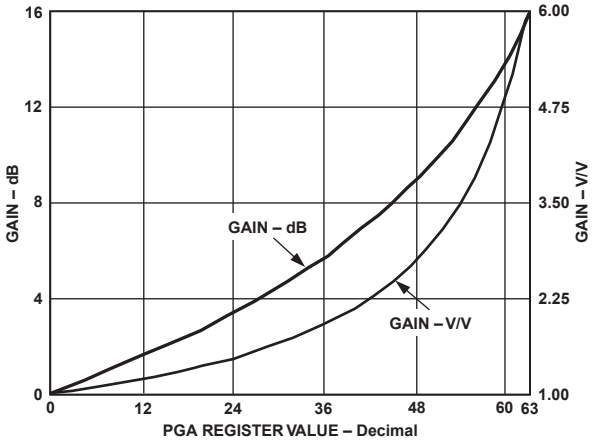


Figure 17. PGA Gain Transfer Function

APPLICATIONS INFORMATION

Circuit and Layout Recommendations

The recommended circuit configuration for 3-Channel CDS Mode operation is shown in Figure 18. The recommended input coupling capacitor value is 0.1 µF (see Circuit Operation section for more details). A single ground plane is recommended for the ADW11000. A separate power supply may be used for DRVDD, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as the rest of the ADW11000. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC, or by using external digital buffers. To minimize the effect of digital transients during major output code transitions, the falling edge of CDSCLK2 should occur coincident with or before the rising edge of ADCCLK (see Figures 1 through 6 for timing). All 0.1 µF decoupling capacitors should be located as close as possible to the ADW11000 pins. When operating in 1CH or 2CH Mode, the unused analog inputs should be grounded.

For 3-Channel SHA Mode, all of the above considerations also apply, except that the analog input signals are directly connected to the ADW11000 without the use of coupling capacitors. The analog input signals must already be dc-biased between 0 V and 4 V. Also, the OFFSET pin should be grounded if the inputs to the ADW11000 are to be referenced to ground, or a dc offset voltage should be applied to the OFFSET pin in the case where a coarse offset needs to be removed from the inputs. (See Figure 16 and the Circuit Operation section for more details.)

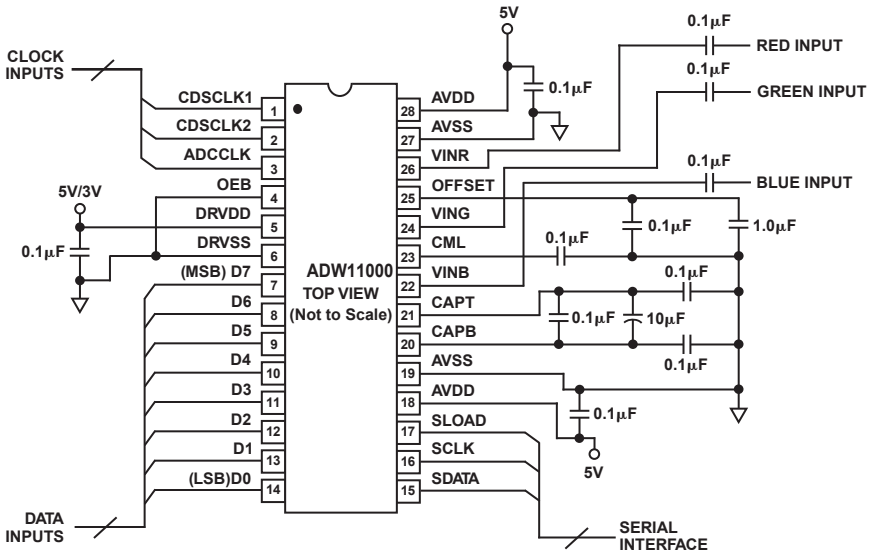


Figure 18. Recommended Circuit Configuration, 3-Channel CDS Mode

OUTLINE DIMENSIONS

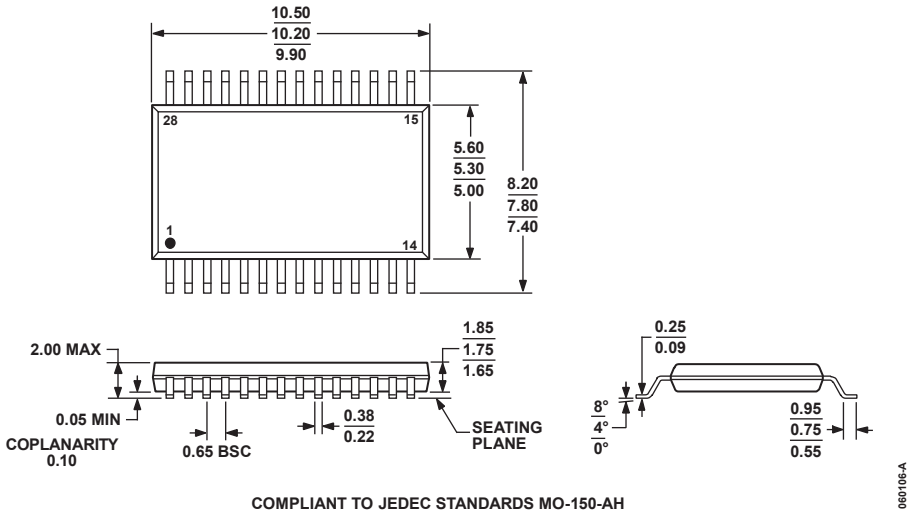


Figure 19. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

Revision History

Location	Page
Data Sheet changed from REV. 0 to REV. A.	
Edits to ORDERING GUIDE	4
Edits to Figure 2	8
Edits to Figure 6	10
6/12—Rev. A to Rev. B	
Changes to Ordering Guide	20
11/12—Rev. B to Qn.	
Added Automotive Grade Product Information (Throughout)	1
Changes to Ordering Guide	20

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD9826KRSZ	–40°C to +85°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD9826KRSZRL	–40°C to +85°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADW11000YRSZ	–40°C to +105°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
ADW11000YRSZRL	–40°C to +105°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADW11000 models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

D02367-0-11/12(Sp0)