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6/07—Revision 0: Initial Version

SPECIFICATIONS

Typical is given for $V_S = V_{S_LVPECL} = 3.3 \text{ V} \pm 5\%$; $V_S \leq V_{CP} \leq 5.25 \text{ V}$; $T_A = 25^\circ\text{C}$; $R_{SET} = 4.12 \text{ k}\Omega$; $CP_{RSET} = 5.1 \text{ k}\Omega$, unless otherwise noted. Minimum and maximum values are given over full V_S and T_A (-40°C to $+85^\circ\text{C}$) variation.

POWER SUPPLY REQUIREMENTS

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|----------------------|-------|------|-------|------------|--|
| V_S | 3.135 | 3.3 | 3.465 | V | $3.3 \text{ V} \pm 5\%$ |
| V_{S_LVPECL} | 2.375 | | V_S | V | Nominally 2.5 V to $3.3 \text{ V} \pm 5\%$ |
| V_{CP} | V_S | | 5.25 | V | Nominally 3.3 V to $5.0 \text{ V} \pm 5\%$ |
| RSET Pin Resistor | | 4.12 | | k Ω | Sets internal biasing currents; connect to ground |
| CPRSET Pin Resistor | 2.7 | 5.1 | 10 | k Ω | Sets internal CP current range, nominally 4.8 mA ($CP_Isb = 600 \mu\text{A}$); actual current can be calculated by: $CP_Isb = 3.06/CPRSET$; connect to ground |
| BYPASS Pin Capacitor | | 220 | | nF | Bypass for internal LDO regulator; necessary for LDO stability; connect to ground |

PLL CHARACTERISTICS

Table 2.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|------|----------------|---------------|--|
| VCO (ON-CHIP) | | | | | |
| Frequency Range | 2050 | | 2335 | MHz | See Figure 15 |
| VCO Gain (K_{VCO}) | | 50 | | MHz/V | See Figure 10 |
| Tuning Voltage (V_T) | 0.5 | | $V_{CP} - 0.5$ | V | $V_{CP} \leq V_S$ when using internal VCO; outside of this range, the CP spurs may increase due to CP up/down mismatch |
| Frequency Pushing (Open-Loop) | | 1 | | MHz/V | |
| Phase Noise at 100 kHz Offset | | -107 | | dBc/Hz | $f = 2175 \text{ MHz}$ |
| Phase Noise at 1 MHz Offset | | -124 | | dBc/Hz | $f = 2175 \text{ MHz}$ |
| REFERENCE INPUTS | | | | | |
| Differential Mode ($\overline{\text{REFIN}}$, $\overline{\text{REFIN}}$) | | | | | Differential mode (can accommodate single-ended input by ac grounding undriven input) |
| Input Frequency | 0 | | 250 | MHz | Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage) |
| Input Sensitivity | | 250 | | mV p-p | PLL figure of merit (FOM) increases with increasing slew rate; see Figure 14 |
| Self-Bias Voltage, $\overline{\text{REFIN}}$ | 1.35 | 1.60 | 1.75 | V | Self-bias voltage of $\overline{\text{REFIN}}$ ¹ |
| Self-Bias Voltage, $\overline{\text{REFIN}}$ | 1.30 | 1.50 | 1.60 | V | Self-bias voltage of $\overline{\text{REFIN}}$ ¹ |
| Input Resistance, $\overline{\text{REFIN}}$ | 4.0 | 4.8 | 5.9 | k Ω | Self-biased ¹ |
| Input Resistance, $\overline{\text{REFIN}}$ | 4.4 | 5.3 | 6.4 | k Ω | Self-biased ¹ |
| Dual Single-Ended Mode ($\overline{\text{REF1}}$, $\overline{\text{REF2}}$) | | | | | Two single-ended CMOS-compatible inputs |
| Input Frequency (AC-Coupled) | 20 | | 250 | MHz | Slew rate $> 50 \text{ V}/\mu\text{s}$ |
| Input Frequency (DC-Coupled) | 0 | | 250 | MHz | Slew rate $> 50 \text{ V}/\mu\text{s}$; CMOS levels |
| Input Sensitivity (AC-Coupled) | | 0.8 | | V p-p | Should not exceed V_S p-p |
| Input Logic High | 2.0 | | | V | |
| Input Logic Low | | | 0.8 | V | |
| Input Current | -100 | | +100 | μA | |
| Input Capacitance | | 2 | | pF | Each pin, $\overline{\text{REFIN}}/\overline{\text{REFIN}}$ ($\overline{\text{REF1}}/\overline{\text{REF2}}$) |
| PHASE/FREQUENCY DETECTOR (PFD) | | | | | |
| PFD Input Frequency | | | 100 | MHz | Antibacklash pulse width = 1.3 ns, 2.9 ns |
| | | | 45 | MHz | Antibacklash pulse width = 6.0 ns |
| Antibacklash Pulse Width | | 1.3 | | ns | Register 0x017[1:0] = 01b |
| | | 2.9 | | ns | Register 0x017[1:0] = 00b; Register 0x017[1:0] = 11b |
| | | 6.0 | | ns | Register 0x017[1:0] = 10b |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|--------|------|--------|---|
| CHARGE PUMP (CP) | | | | | |
| I _{CP} Sink/Source | | | | | Programmable |
| High Value | | 4.8 | | mA | With CP _{RSET} = 5.1 kΩ |
| Low Value | | 0.60 | | mA | |
| Absolute Accuracy | | 2.5 | | % | CP _V = V _{CP} /2 |
| CP _{RSET} Range | | 2.7/10 | | kΩ | |
| I _{CP} High Impedance Mode Leakage | | 1 | | nA | |
| Sink-and-Source Current Matching | | 2 | | % | 0.5 < CP _V < V _{CP} – 0.5 V |
| I _{CP} vs. CP _V | | 1.5 | | % | 0.5 < CP _V < V _{CP} – 0.5 V |
| I _{CP} vs. Temperature | | 2 | | % | CP _V = V _{CP} /2 |
| PRESCALER (PART OF N DIVIDER) | | | | | See the VCXO/VCO Feedback Divider N—P, A, B, R section |
| Prescaler Input Frequency | | | | | |
| P = 1 FD | | | 300 | MHz | |
| P = 2 FD | | | 600 | MHz | |
| P = 3 FD | | | 900 | MHz | |
| P = 2 DM (2/3) | | | 200 | MHz | |
| P = 4 DM (4/5) | | | 1000 | MHz | |
| P = 8 DM (8/9) | | | 2400 | MHz | |
| P = 16 DM (16/17) | | | 3000 | MHz | |
| P = 32 DM (32/33) | | | 3000 | MHz | |
| Prescaler Output Frequency | | | 300 | MHz | A, B counter input frequency (prescaler input frequency divided by P) |
| PLL DIVIDER DELAYS | | | | | Register 0x019: R, Bits[5:3]; N, Bits[2:0]; see Table 54 |
| 000 | | Off | | ps | |
| 001 | | 330 | | ps | |
| 010 | | 440 | | ps | |
| 011 | | 550 | | ps | |
| 100 | | 660 | | ps | |
| 101 | | 770 | | ps | |
| 110 | | 880 | | ps | |
| 111 | | 990 | | ps | |
| NOISE CHARACTERISTICS | | | | | |
| In-Band Phase Noise of the Charge Pump/Phase Frequency Detector (In-Band Is Within the LBW of the PLL) | | | | | The PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20log(N) (where N is the value of the N divider) |
| At 500 kHz PFD Frequency | | –165 | | dBc/Hz | |
| At 1 MHz PFD Frequency | | –162 | | dBc/Hz | |
| At 10 MHz PFD Frequency | | –151 | | dBc/Hz | |
| At 50 MHz PFD Frequency | | –143 | | dBc/Hz | |
| PLL Figure of Merit (FOM) | | –220 | | dBc/Hz | Reference slew rate > 0.25 V/ns; FOM + 10log (f _{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed loop, the phase noise, as observed at the VCO output, is increased by 20log(N) |
| PLL DIGITAL LOCK DETECT WINDOW ² | | | | | Signal available at LD, STATUS, and REFMON pins when selected by appropriate register settings |
| Required to Lock (Coincidence of Edges) | | | | | Selected by Register 0x017[1:0] and Register 0x018[4] |
| Low Range (ABP 1.3 ns, 2.9 ns) | | 3.5 | | ns | Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b |
| High Range (ABP 1.3 ns, 2.9 ns) | | 7.5 | | ns | Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b |
| High Range (ABP 6.0 ns) | | 3.5 | | ns | Register 0x017[1:0] = 10b; Register 0x018[4] = 0b |
| To Unlock After Lock (Hysteresis) ² | | | | | |
| Low Range (ABP 1.3 ns, 2.9 ns) | | 7 | | ns | Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 1b |
| High Range (ABP 1.3 ns, 2.9 ns) | | 15 | | ns | Register 0x017[1:0] = 00b, 01b, 11b; Register 0x018[4] = 0b |
| High Range (ABP 6.0 ns) | | 11 | | ns | Register 0x017[1:0] = 10b; Register 0x018[4] = 0b |

¹ REFIN and $\overline{\text{REFIN}}$ self-bias points are offset slightly to avoid chatter on an open input condition.

² For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK INPUTS

Table 3.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|----------------|------|-----|---------------|--|
| CLOCK INPUTS (CLK, $\overline{\text{CLK}}$) | | | | | Differential input |
| Input Frequency | 0 ¹ | | 2.4 | GHz | High frequency distribution (VCO divider) |
| Input Sensitivity, Differential | 0 ¹ | 150 | 1.6 | GHz mV p-p | Distribution only (VCO divider bypassed) Measured at 2.4 GHz; jitter performance is improved with slew rates > 1 V/ns |
| Input Level, Differential | | | 2 | V p-p | Larger voltage swings may turn on the protection diodes and may degrade jitter performance |
| Input Common-Mode Voltage, V_{CM} | 1.3 | 1.57 | 1.8 | V | Self-biased; enables ac coupling |
| Input Common-Mode Range, V_{CMR} | 1.3 | | 1.8 | V | With 200 mV p-p signal applied; dc-coupled |
| Input Sensitivity, Single-Ended | | 150 | | mV p-p | CLK ac-coupled; $\overline{\text{CLK}}$ ac-bypassed to RF ground |
| Input Resistance | 3.9 | 4.7 | 5.7 | k Ω | Self-biased |
| Input Capacitance | | 2 | | pF | |

¹ Below about 1 MHz, the input should be dc-coupled. Care should be taken to match V_{CM} .

CLOCK OUTPUTS

Table 4.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----------------------|-----------------------|-----------------------|------|---|
| LVPECL CLOCK OUTPUTS | | | | | Termination = 50 Ω to $V_{\text{S}} - 2 \text{ V}$ |
| OUT0, OUT1, OUT2, OUT3, OUT4, OUT5 | | | | | Differential (OUT, $\overline{\text{OUT}}$) |
| Output Frequency, Maximum | 2950 | | | MHz | Using direct to output; see Figure 25 for peak-to-peak differential amplitude |
| Output High Voltage (V_{OH}) | $V_{\text{S}} - 1.12$ | $V_{\text{S}} - 0.98$ | $V_{\text{S}} - 0.84$ | V | |
| Output Low Voltage (V_{OL}) | $V_{\text{S}} - 2.03$ | $V_{\text{S}} - 1.77$ | $V_{\text{S}} - 1.49$ | V | |
| Output Differential Voltage (V_{OD}) | 550 | 790 | 980 | mV | $V_{\text{OH}} - V_{\text{OL}}$ for each leg of a differential pair for default amplitude setting with driver not toggling; see Figure 25 for variation over frequency |
| LVDS CLOCK OUTPUTS | | | | | Differential termination 100 Ω at 3.5 mA |
| OUT6, OUT7, OUT8, OUT9 | | | | | Differential (OUT, $\overline{\text{OUT}}$) |
| Output Frequency | | | 800 | MHz | The AD9516 outputs toggle at higher frequencies, but the output amplitude may not meet the V_{OD} specification; see Figure 26 |
| Differential Output Voltage (V_{OD}) | 247 | 360 | 454 | mV | $V_{\text{OH}} - V_{\text{OL}}$ measurement across a differential pair at the default amplitude setting with output driver not toggling; see Figure 26 for variation over frequency |
| Delta V_{OD} | | | 25 | mV | This is the absolute value of the difference between V_{OD} when the normal output is high vs. when the complementary output is high |
| Output Offset Voltage (V_{OS}) | 1.125 | 1.24 | 1.375 | V | $(V_{\text{OH}} + V_{\text{OL}})/2$ across a differential pair |
| Delta V_{OS} | | | 25 | mV | This is the absolute value of the difference between V_{OS} when the normal output is high vs. when the complementary output is high |
| Short-Circuit Current (I_{SA} , I_{SB}) | | 14 | 24 | mA | Output shorted to GND |
| CMOS CLOCK OUTPUTS | | | | | Single-ended; termination = 10 pF |
| OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, OUT9B | | | | | |
| Output Frequency | | | 250 | MHz | See Figure 27 |
| Output Voltage High (V_{OH}) | $V_{\text{S}} - 0.1$ | | | V | At 1 mA load |
| Output Voltage Low (V_{OL}) | | | 0.1 | V | At 1 mA load |

TIMING CHARACTERISTICS

Table 5.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|-------|------|------------------|--|
| LVPECL | | | | | Termination = 50 Ω to $V_S - 2$ V; level = 810 mV |
| Output Rise Time, t_{RP} | | 70 | 180 | ps | 20% to 80%, measured differentially |
| Output Fall Time, t_{FP} | | 70 | 180 | ps | 80% to 20%, measured differentially |
| PROPAGATION DELAY, t_{PECL} , CLK-TO-LVPECL OUTPUT | | | | | |
| High Frequency Clock Distribution Configuration | 835 | 995 | 1180 | ps | See Figure 43 |
| Clock Distribution Configuration | 773 | 933 | 1090 | ps | See Figure 45 |
| Variation with Temperature | | 0.8 | | ps/ $^{\circ}$ C | |
| OUTPUT SKEW, LVPECL OUTPUTS ¹ | | | | | |
| LVPECL Outputs That Share the Same Divider | | 5 | 15 | ps | |
| LVPECL Outputs on Different Dividers | | 13 | 40 | ps | |
| All LVPECL Outputs Across Multiple Parts | | | 220 | ps | |
| LVDS | | | | | Termination = 100 Ω differential; 3.5 mA |
| Output Rise Time, t_{RL} | | 170 | 350 | ps | 20% to 80%, measured differentially ² |
| Output Fall Time, t_{FL} | | 160 | 350 | ps | 20% to 80%, measured differentially ² |
| PROPAGATION DELAY, t_{LVDS} , CLK-TO-LVDS OUTPUT | | | | | Delay off on all outputs |
| OUT6, OUT7, OUT8, OUT9 | | | | | |
| For All Divide Values | 1.4 | 1.8 | 2.1 | ns | |
| Variation with Temperature | | 1.25 | | ps/ $^{\circ}$ C | |
| OUTPUT SKEW, LVDS OUTPUTS ¹ | | | | | Delay off on all outputs |
| LVDS Outputs That Share the Same Divider | | 6 | 62 | ps | |
| LVDS Outputs on Different Dividers | | 25 | 150 | ps | |
| All LVDS Outputs Across Multiple Parts | | | 430 | ps | |
| CMOS | | | | | Termination = open |
| Output Rise Time, t_{RC} | | 495 | 1000 | ps | 20% to 80%; $C_{LOAD} = 10$ pF |
| Output Fall Time, t_{FC} | | 475 | 985 | ps | 80% to 20%; $C_{LOAD} = 10$ pF |
| PROPAGATION DELAY, t_{CMOS} , CLK-TO-CMOS OUTPUT | | | | | Fine delay off |
| For All Divide Values | 1.6 | 2.1 | 2.6 | ns | |
| Variation with Temperature | | 2.6 | | ps/ $^{\circ}$ C | |
| OUTPUT SKEW, CMOS OUTPUTS ¹ | | | | | Fine delay off |
| CMOS Outputs That Share the Same Divider | | 4 | 66 | ps | |
| All CMOS Outputs on Different Dividers | | 28 | 180 | ps | |
| All CMOS Outputs Across Multiple Parts | | | 675 | ps | |
| DELAY ADJUST ³ | | | | | LVDS and CMOS |
| Shortest Delay Range ⁴ | | | | | Register 0xA1 (0xA4, 0xA7, 0xAA), Bits[5:0] = 101111b |
| Zero Scale | 50 | 315 | 680 | ps | Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 000000b |
| Full Scale | 540 | 880 | 1180 | ps | Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 101111b |
| Longest Delay Range ⁴ | | | | | Register 0xA1 (0xA4, 0xA7, 0xAA), Bits[5:0] = 000000b |
| Zero Scale | 200 | 570 | 950 | ps | Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 000000b |
| Quarter Scale | 1.72 | 2.31 | 2.89 | ns | Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 001100b |
| Full Scale | 5.7 | 8.0 | 10.1 | ns | Register 0xA2 (0xA5, 0xA8, 0xAB), Bits[5:0] = 101111b |
| Delay Variation with Temperature | | | | | |
| Short Delay Range ⁵ | | | | | |
| Zero Scale | | 0.23 | | ps/ $^{\circ}$ C | |
| Full Scale | | -0.02 | | ps/ $^{\circ}$ C | |
| Long Delay Range ⁵ | | | | | |
| Zero Scale | | 0.3 | | ps/ $^{\circ}$ C | |
| Full Scale | | 0.24 | | ps/ $^{\circ}$ C | |

¹ This is the difference between any two similar delay paths while operating at the same voltage and temperature.² Corresponding CMOS drivers set to A for noninverting and B for inverting.³ The maximum delay that can be used is a little less than one-half the period of the clock. A longer delay disables the output.⁴ Incremental delay; does not include propagation delay.⁵ All delays between zero scale and full scale can be estimated by linear interpolation.

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; VCO DIVIDER NOT USED)

Table 6.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|------|-----|--------|---|
| CLK-TO-LVPECL ADDITIVE PHASE NOISE CLK = 1 GHz, Output = 1 GHz Divider = 1 | | | | | Distribution section only; does not include PLL and VCO Input slew rate > 1 V/ns |
| At 10 Hz Offset | | -109 | | dBc/Hz | |
| At 100 Hz Offset | | -118 | | dBc/Hz | |
| At 1 kHz Offset | | -130 | | dBc/Hz | |
| At 10 kHz Offset | | -139 | | dBc/Hz | |
| At 100 kHz Offset | | -144 | | dBc/Hz | |
| At 1 MHz Offset | | -146 | | dBc/Hz | |
| At 10 MHz Offset | | -147 | | dBc/Hz | |
| At 100 MHz Offset | | -149 | | dBc/Hz | |
| CLK = 1 GHz, Output = 200 MHz Divider = 5 | | | | | Input slew rate > 1 V/ns |
| At 10 Hz Offset | | -120 | | dBc/Hz | |
| At 100 Hz Offset | | -126 | | dBc/Hz | |
| At 1 kHz Offset | | -139 | | dBc/Hz | |
| At 10 kHz Offset | | -150 | | dBc/Hz | |
| At 100 kHz Offset | | -155 | | dBc/Hz | |
| At 1 MHz Offset | | -157 | | dBc/Hz | |
| >10 MHz Offset | | -157 | | dBc/Hz | |
| CLK-TO-LVDS ADDITIVE PHASE NOISE CLK = 1.6 GHz, Output = 800 MHz Divider = 2 | | | | | Distribution section only; does not include PLL and VCO Input slew rate > 1 V/ns |
| At 10 Hz Offset | | -103 | | dBc/Hz | |
| At 100 Hz Offset | | -110 | | dBc/Hz | |
| At 1 kHz Offset | | -120 | | dBc/Hz | |
| At 10 kHz Offset | | -127 | | dBc/Hz | |
| At 100 kHz Offset | | -133 | | dBc/Hz | |
| At 1 MHz Offset | | -138 | | dBc/Hz | |
| At 10 MHz Offset | | -147 | | dBc/Hz | |
| At 100 MHz Offset | | -149 | | dBc/Hz | |
| CLK = 1.6 GHz, Output = 400 MHz Divider = 4 | | | | | Input slew rate > 1 V/ns |
| At 10 Hz Offset | | -114 | | dBc/Hz | |
| At 100 Hz Offset | | -122 | | dBc/Hz | |
| At 1 kHz Offset | | -132 | | dBc/Hz | |
| At 10 kHz Offset | | -140 | | dBc/Hz | |
| At 100 kHz Offset | | -146 | | dBc/Hz | |
| At 1 MHz Offset | | -150 | | dBc/Hz | |
| >10 MHz Offset | | -155 | | dBc/Hz | |
| CLK-TO-CMOS ADDITIVE PHASE NOISE CLK = 1 GHz, Output = 250 MHz Divider = 4 | | | | | Distribution section only; does not include PLL and VCO Input slew rate > 1 V/ns |
| At 10 Hz Offset | | -110 | | dBc/Hz | |
| At 100 Hz Offset | | -120 | | dBc/Hz | |
| At 1 kHz Offset | | -127 | | dBc/Hz | |
| At 10 kHz Offset | | -136 | | dBc/Hz | |
| At 100 kHz Offset | | -144 | | dBc/Hz | |
| At 1 MHz Offset | | -147 | | dBc/Hz | |
| >10 MHz Offset | | -154 | | dBc/Hz | |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|------|-----|--------|--------------------------|
| CLK = 1 GHz, Output = 50 MHz Divider = 20 | | | | | Input slew rate > 1 V/ns |
| At 10 Hz Offset | | -124 | | dBc/Hz | |
| At 100 Hz Offset | | -134 | | dBc/Hz | |
| At 1 kHz Offset | | -142 | | dBc/Hz | |
| At 10 kHz Offset | | -151 | | dBc/Hz | |
| At 100 kHz Offset | | -157 | | dBc/Hz | |
| At 1 MHz Offset | | -160 | | dBc/Hz | |
| >10 MHz Offset | | -163 | | dBc/Hz | |

CLOCK OUTPUT ABSOLUTE PHASE NOISE (INTERNAL VCO USED)

Table 7.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|-------------------------------------|-----|------|-----|--------|---------------------------------------|
| LVPECL ABSOLUTE PHASE NOISE | | | | | Internal VCO; direct to LVPECL output |
| VCO = 2.335 GHz; Output = 2.335 GHz | | | | | |
| At 1 kHz Offset | | -46 | | dBc/Hz | |
| At 10 kHz Offset | | -78 | | dBc/Hz | |
| At 100 kHz Offset | | -105 | | dBc/Hz | |
| At 1 MHz Offset | | -124 | | dBc/Hz | |
| At 10 MHz Offset | | -141 | | dBc/Hz | |
| At 40 MHz Offset | | -146 | | dBc/Hz | |
| VCO = 2.175 GHz; Output = 2.175 GHz | | | | | |
| At 1 kHz Offset | | -51 | | dBc/Hz | |
| At 10 kHz Offset | | -80 | | dBc/Hz | |
| At 100 kHz Offset | | -107 | | dBc/Hz | |
| At 1 MHz Offset | | -124 | | dBc/Hz | |
| At 10 MHz Offset | | -142 | | dBc/Hz | |
| At 40 MHz Offset | | -146 | | dBc/Hz | |
| VCO = 2.05 GHz; Output = 2.05 GHz | | | | | |
| At 1 kHz Offset | | -53 | | dBc/Hz | |
| At 10 kHz Offset | | -82 | | dBc/Hz | |
| At 100 kHz Offset | | -108 | | dBc/Hz | |
| At 1 MHz Offset | | -127 | | dBc/Hz | |
| At 10 MHz Offset | | -142 | | dBc/Hz | |
| At 40 MHz Offset | | -147 | | dBc/Hz | |

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING INTERNAL VCO)

Table 8.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|-----|-----|--------|---|
| LVPECL OUTPUT ABSOLUTE TIME JITTER | | | | | Application example based on a typical setup where the reference source is clean, so a wider PLL loop bandwidth is used; reference = 15.36 MHz; R = 1 |
| VCO = 2.21 GHz; LVPECL = 245.76 MHz; PLL LBW = 138 kHz | | 146 | | fs rms | Integration BW = 200 kHz to 10 MHz |
| | | 329 | | fs rms | Integration BW = 12 kHz to 20 MHz |
| VCO = 2.21 GHz; LVPECL = 122.88 MHz; PLL LBW = 138 kHz | | 151 | | fs rms | Integration BW = 200 kHz to 10 MHz |
| | | 329 | | fs rms | Integration BW = 12 kHz to 20 MHz |
| VCO = 2.21 GHz; LVPECL = 61.44 MHz; PLL LBW = 138 kHz | | 203 | | fs rms | Integration BW = 200 kHz to 10 MHz |
| | | 376 | | fs rms | Integration BW = 12 kHz to 20 MHz |

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK CLEANUP USING INTERNAL VCO)

Table 9.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|--------|--|
| LVPECL OUTPUT ABSOLUTE TIME JITTER | | | | | Application example based on a typical setup where the reference source is jittery, so a narrower PLL loop bandwidth is used; reference = 10.0 MHz; R = 20 |
| VCO = 2.18 GHz; LVPECL = 155.52 MHz; PLL LBW = 125 Hz | | 515 | | fs rms | Integration BW = 12 kHz to 20 MHz |
| VCO = 2.21 GHz; LVPECL = 122.88 MHz; PLL LBW = 125 Hz | | 570 | | fs rms | Integration BW = 12 kHz to 20 MHz |

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL VCXO)

Table 10.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---------------------------------------|-----|-----|-----|--------|---|
| LVPECL OUTPUT ABSOLUTE TIME JITTER | | | | | Application example based on a typical setup using an external 245.76 MHz VCXO (Toyocom TCO-2112); reference = 15.36 MHz; R = 1 |
| LVPECL = 245.76 MHz; PLL LBW = 125 Hz | | 54 | | fs rms | Integration BW = 200 kHz to 5 MHz |
| | | 77 | | fs rms | Integration BW = 200 kHz to 10 MHz |
| | | 109 | | fs rms | Integration BW = 12 kHz to 20 MHz |
| LVPECL = 122.88 MHz; PLL LBW = 125 Hz | | 79 | | fs rms | Integration BW = 200 kHz to 5 MHz |
| | | 114 | | fs rms | Integration BW = 200 kHz to 10 MHz |
| | | 163 | | fs rms | Integration BW = 12 kHz to 20 MHz |
| LVPECL = 61.44 MHz; PLL LBW = 125 Hz | | 124 | | fs rms | Integration BW = 200 kHz to 5 MHz |
| | | 176 | | fs rms | Integration BW = 200 kHz to 10 MHz |
| | | 259 | | fs rms | Integration BW = 12 kHz to 20 MHz |

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER NOT USED)

Table 11.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|-----|-----|--------|---|
| LVPECL OUTPUT ADDITIVE TIME JITTER | | | | | Distribution section only; does not include PLL and VCO; uses rising edge of clock signal |
| CLK = 622.08 MHz; LVPECL = 622.08 MHz; Divider = 1 | | 40 | | fs rms | BW = 12 kHz to 20 MHz |
| CLK = 622.08 MHz; LVPECL = 155.52 MHz; Divider = 4 | | 80 | | fs rms | BW = 12 kHz to 20 MHz |
| CLK = 1.6 GHz; LVPECL = 100 MHz; Divider = 16 | | 215 | | fs rms | Calculated from SNR of ADC method; DCC not used for even divides |
| CLK = 500 MHz; LVPECL = 100 MHz; Divider = 5 | | 245 | | fs rms | Calculated from SNR of ADC method; DCC on |
| LVDS OUTPUT ADDITIVE TIME JITTER | | | | | Distribution section only; does not include PLL and VCO; uses rising edge of clock signal |
| CLK = 1.6 GHz; LVDS = 800 MHz; Divider = 2; VCO Divider Not Used | | 85 | | fs rms | BW = 12 kHz to 20 MHz |
| CLK = 1 GHz; LVDS = 200 MHz; Divider = 5 | | 113 | | fs rms | BW = 12 kHz to 20 MHz |
| CLK = 1.6 GHz; LVDS = 100 MHz; Divider = 16 | | 280 | | fs rms | Calculated from SNR of ADC method; DCC not used for even divides |
| CMOS OUTPUT ADDITIVE TIME JITTER | | | | | Distribution section only; does not include PLL and VCO; uses rising edge of clock signal |
| CLK = 1.6 GHz; CMOS = 100 MHz; Divider = 16 | | 365 | | fs rms | Calculated from SNR of ADC method; DCC not used for even divides |

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER USED)

Table 12.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|--------|---|
| LVPECL OUTPUT ADDITIVE TIME JITTER | | | | | Distribution section only; does not include PLL and VCO; uses rising edge of clock signal |
| CLK = 2.4 GHz; VCO DIV = 2; LVPECL = 100 MHz; Divider = 12; Duty-Cycle Correction = Off | | 210 | | fs rms | Calculated from SNR of ADC method |
| LVDS OUTPUT ADDITIVE TIME JITTER | | | | | Distribution section only; does not include PLL and VCO; uses rising edge of clock signal |
| CLK = 2.4 GHz; VCO DIV = 2; LVDS = 100 MHz; Divider = 12; Duty-Cycle Correction = Off | | 285 | | fs rms | Calculated from SNR of ADC method |
| CMOS OUTPUT ADDITIVE TIME JITTER | | | | | Distribution section only; does not include PLL and VCO; uses rising edge of clock signal |
| CLK = 2.4 GHz; VCO DIV = 2; CMOS = 100 MHz; Divider = 12; Duty-Cycle Correction = Off | | 350 | | fs rms | Calculated from SNR of ADC method |

DELAY BLOCK ADDITIVE TIME JITTER

Table 13.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|------|-----|--------|-----------------------------|
| DELAY BLOCK ADDITIVE TIME JITTER ¹ | | | | | Incremental additive jitter |
| 100 MHz Output | | | | | |
| Delay (1600 μ A, 0x1C) Fine Adj. 000000 | | 0.54 | | ps rms | |
| Delay (1600 μ A, 0x1C) Fine Adj. 101111 | | 0.60 | | ps rms | |
| Delay (800 μ A, 0x1C) Fine Adj. 000000 | | 0.65 | | ps rms | |
| Delay (800 μ A, 0x1C) Fine Adj. 101111 | | 0.85 | | ps rms | |
| Delay (800 μ A, 0x4C) Fine Adj. 000000 | | 0.79 | | ps rms | |
| Delay (800 μ A, 0x4C) Fine Adj. 101111 | | 1.2 | | ps rms | |
| Delay (400 μ A, 0x4C) Fine Adj. 000000 | | 1.2 | | ps rms | |
| Delay (400 μ A, 0x4C) Fine Adj. 101111 | | 2.0 | | ps rms | |
| Delay (200 μ A, 0x1C) Fine Adj. 000000 | | 1.3 | | ps rms | |
| Delay (200 μ A, 0x1C) Fine Adj. 101111 | | 2.5 | | ps rms | |
| Delay (200 μ A, 0x4C) Fine Adj. 000000 | | 1.9 | | ps rms | |
| Delay (200 μ A, 0x4C) Fine Adj. 101111 | | 3.8 | | ps rms | |

¹ This value is incremental. That is, it is in addition to the jitter of the LVDS or CMOS output without the delay. To estimate the total jitter, the LVDS or CMOS output jitter should be added to this value using the root sum of the squares (RSS) method.

SERIAL CONTROL PORT

Table 14.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|---------|---|
| $\overline{\text{CS}}$ (INPUT) | | | | | $\overline{\text{CS}}$ has an internal 30 k Ω pull-up resistor |
| Input Logic 1 Voltage | 2.0 | | | V | |
| Input Logic 0 Voltage | | | 0.8 | V | |
| Input Logic 1 Current | | | 3 | μ A | |
| Input Logic 0 Current | | 110 | | μ A | |
| Input Capacitance | | 2 | | pF | |
| SCLK (INPUT) | | | | | SCLK has an internal 30 k Ω pull-down resistor |
| Input Logic 1 Voltage | 2.0 | | | V | |
| Input Logic 0 Voltage | | | 0.8 | V | |
| Input Logic 1 Current | | 110 | | μ A | |
| Input Logic 0 Current | | | 1 | μ A | |
| Input Capacitance | | 2 | | pF | |
| SDIO (WHEN INPUT) | | | | | |
| Input Logic 1 Voltage | 2.0 | | | V | |
| Input Logic 0 Voltage | | | 0.8 | V | |
| Input Logic 1 Current | | 10 | | nA | |
| Input Logic 0 Current | | 20 | | nA | |
| Input Capacitance | | 2 | | pF | |
| SDIO, SDO (OUTPUTS) | | | | | |
| Output Logic 1 Voltage | 2.7 | | | V | |
| Output Logic 0 Voltage | | | 0.4 | V | |
| TIMING | | | | | |
| Clock Rate (SCLK, $1/t_{\text{SCLK}}$) | | | 25 | MHz | |
| Pulse Width High, t_{HIGH} | 16 | | | ns | |
| Pulse Width Low, t_{LOW} | 16 | | | ns | |
| SDIO to SCLK Setup, t_{DS} | 2 | | | ns | |
| SCLK to SDIO Hold, t_{DH} | 1.1 | | | ns | |
| SCLK to Valid SDIO and SDO, t_{DV} | | | 8 | ns | |
| $\overline{\text{CS}}$ to SCLK Setup and Hold, $t_{\text{S}}, t_{\text{H}}$ | 2 | | | ns | |
| $\overline{\text{CS}}$ Minimum Pulse Width High, t_{PWH} | 3 | | | ns | |

PD, RESET, AND SYNC PINS

Table 15.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|-----------------------|-----|-----|-----|-------------------------|--|
| INPUT CHARACTERISTICS | | | | | These pins each have a 30 k Ω internal pull-up resistor |
| Logic 1 Voltage | 2.0 | | | V | |
| Logic 0 Voltage | | | 0.8 | V | |
| Logic 1 Current | | 110 | | μ A | |
| Logic 0 Current | | | 1 | μ A | |
| Capacitance | | 2 | | pF | |
| RESET TIMING | | | | | |
| Pulse Width Low | 50 | | | ns | |
| SYNC TIMING | | | | | |
| Pulse Width Low | 1.5 | | | High speed clock cycles | High speed clock is CLK input signal |

LD, STATUS, AND REFMON PINS

Table 16.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|-----|-----|------|--|
| OUTPUT CHARACTERISTICS | | | | | When selected as a digital output (CMOS); there are other modes in which these pins are not CMOS digital outputs; see Table 54, Register 0x017, Register 0x01A, and Register 0x01B |
| Output Voltage High (V_{OH}) | 2.7 | | | V | |
| Output Voltage Low (V_{OL}) | | | 0.4 | V | |
| MAXIMUM TOGGLE RATE | | 100 | | MHz | Applies when mux is set to any divider or counter output, or PFD up/down pulse; also applies in analog lock detect mode; usually debug mode only; beware that spurs may couple to output when any of these pins are toggling |
| ANALOG LOCK DETECT Capacitance | | 3 | | pF | On-chip capacitance; used to calculate RC time constant for analog lock detect readback; use a pull-up resistor |
| REF1, REF2, AND VCO FREQUENCY STATUS MONITOR Normal Range | 1.02 | | | MHz | Frequency above which the monitor always indicates the presence of the reference |
| Extended Range (REF1 and REF2 Only) | 8 | | | kHz | Frequency above which the monitor always indicates the presence of the reference |
| LD PIN COMPARATOR Trip Point | | 1.6 | | V | |
| Hysteresis | | 260 | | mV | |

POWER DISSIPATION

Table 17.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|-----|-----|------|---|
| POWER DISSIPATION, CHIP | | | | | |
| Power-On Default | | 1.0 | 1.2 | W | No clock; no programming; default register values; does not include power dissipated in external resistors |
| Full Operation; CMOS Outputs at 195 MHz | | 1.6 | 2.2 | W | PLL on; internal VCO = 2335 MHz; VCO divider = 2; all channel dividers on; six LVPECL outputs at 584 MHz; eight CMOS outputs (10 pF load) at 195 MHz; all fine delay on, maximum current; does not include power dissipated in external resistors |
| Full Operation; LVDS Outputs at 195 MHz | | 1.6 | 2.3 | W | PLL on; internal VCO = 2335 MHz; VCO divider = 2; all channel dividers on; six LVPECL outputs at 584 MHz; four LVDS outputs at 195 MHz; all fine delay on, maximum current; does not include power dissipated in external resistors |
| $\overline{\text{PD}}$ Power-Down | | 75 | 185 | mW | $\overline{\text{PD}}$ pin pulled low; does not include power dissipated in terminations |
| $\overline{\text{PD}}$ Power-Down, Maximum Sleep | | 31 | | mW | $\overline{\text{PD}}$ pin pulled low; PLL power-down, Register 0x010[1:0] = 01b; SYNC power-down, Register 0x230[2] = 1b; REF for distribution power-down, Register 0x230[1] = 1b |
| V_{CP} Supply | | 4 | 4.8 | mW | PLL operating; typical closed loop configuration |
| POWER DELTAS, INDIVIDUAL FUNCTIONS | | | | | Power delta when a function is enabled/disabled |
| VCO Divider | | 30 | | mW | VCO divider bypassed |
| REFIN (Differential) | | 20 | | mW | All references off to differential reference enabled |
| REF1, REF2 (Single-Ended) | | 4 | | mW | All references off to REF1 or REF2 enabled; differential reference not enabled |
| VCO | | 70 | | mW | CLK input selected to VCO selected |
| PLL | | 75 | | mW | PLL off to PLL on, normal operation; no reference enabled |
| Channel Divider | | 30 | | mW | Divider bypassed to divide-by-2 to divide-by-32 |
| LVPECL Channel (Divider Plus Output Driver) | | 160 | | mW | No LVPECL output on to one LVPECL output on, independent of frequency |
| LVPECL Driver | | 90 | | mW | Second LVPECL output turned on, same channel |
| LVDS Channel (Divider Plus Output Driver) | | 120 | | mW | No LVDS output on to one LVDS output on; see Figure 8 for dependence on output frequency |
| LVDS Driver | | 50 | | mW | Second LVDS output turned on, same channel |
| CMOS Channel (Divider Plus Output Driver) | | 100 | | mW | Static; no CMOS output on to one CMOS output on; see Figure 9 for variation over output frequency |
| CMOS Driver (Second in Pair) | | 0 | | mW | Static; second CMOS output, same pair, turned on |
| CMOS Driver (First in Second Pair) | | 30 | | mW | Static; first output, second pair, turned on |
| Fine Delay Block | | 50 | | mW | Delay block off to delay block enabled; maximum current setting |

TIMING DIAGRAMS

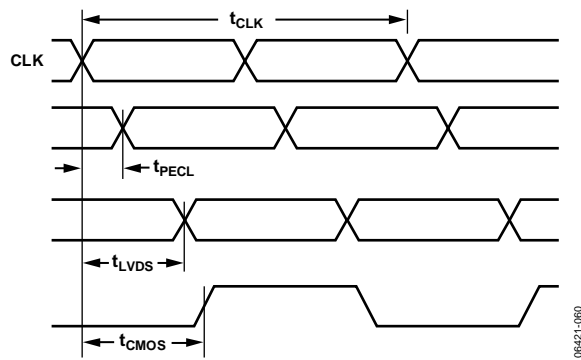
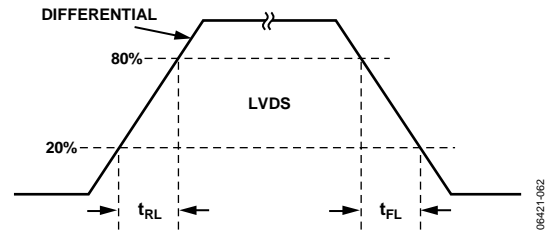
Figure 2. CLK/ $\overline{\text{CLK}}$ to Clock Output Timing, DIV = 1

Figure 4. LVDS Timing, Differential

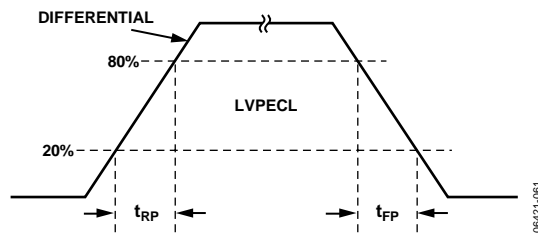


Figure 3. LVPECL Timing, Differential

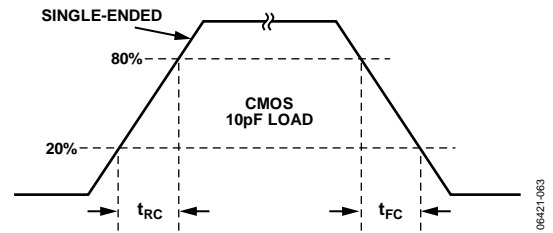


Figure 5. CMOS Timing, Single-Ended, 10 pF Load

ABSOLUTE MAXIMUM RATINGS

Table 18.

| Parameter | Rating |
|---|-------------------------|
| VS, VS_LVPECL to GND | −0.3 V to +3.6 V |
| VCP to GND | −0.3 V to +5.8 V |
| REFIN, $\overline{\text{REFIN}}$ to GND | −0.3 V to $V_S + 0.3$ V |
| REFIN to $\overline{\text{REFIN}}$ | −3.3 V to +3.3 V |
| RSET to GND | −0.3 V to $V_S + 0.3$ V |
| CPRSET to GND | −0.3 V to $V_S + 0.3$ V |
| CLK, $\overline{\text{CLK}}$ to GND | −0.3 V to $V_S + 0.3$ V |
| CLK to $\overline{\text{CLK}}$ | −1.2 V to +1.2 V |
| SCLK, SDIO, SDO, $\overline{\text{CS}}$ to GND | −0.3 V to $V_S + 0.3$ V |
| OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$ to GND | −0.3 V to $V_S + 0.3$ V |
| SYNC to GND | −0.3 V to $V_S + 0.3$ V |
| REFMON, STATUS, LD to GND | −0.3 V to $V_S + 0.3$ V |
| Junction Temperature ¹ | 150°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (10 sec) | 300°C |

¹ See Table 19 for θ_{JA} .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 19.

| Package Type ¹ | θ_{JA} | Unit |
|---------------------------|---------------|------|
| 64-Lead LFCSP | 24 | °C/W |

¹ Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-2

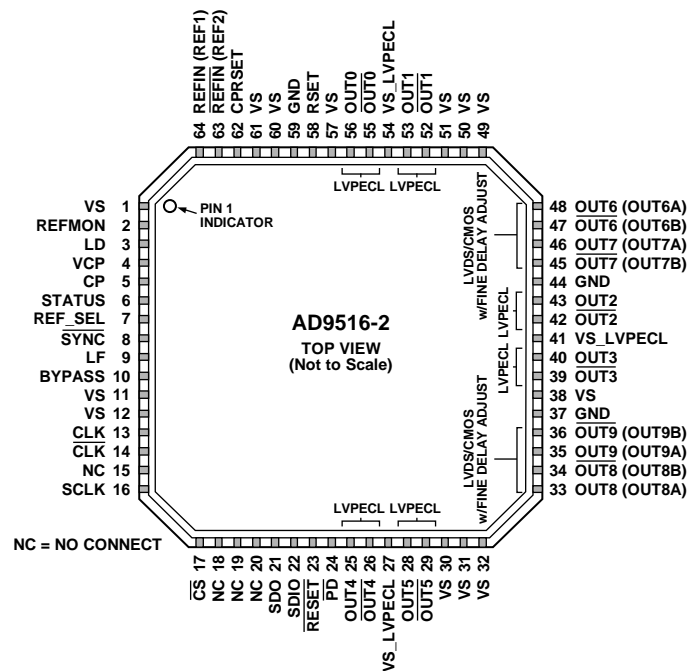
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. THE EXTERNAL PADDLE ON THE BOTTOM OF THE PACKAGE MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.
2. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

06421-003

Figure 6. Pin Configuration

Table 20. Pin Function Descriptions

| Pin No. | Input/Output | Pin Type | Mnemonic | Description |
|---|--------------|--------------------------|--------------------------|--|
| 1, 11, 12, 30, 31, 32, 38, 49, 50, 51, 57, 60, 61 | I | Power | VS | 3.3 V Power Pins. |
| 2 | I | 3.3 V CMOS | REFMON | Reference Monitor (Output). This pin has multiple selectable outputs; see Table 54, Register 0x01B. |
| 3 | O | 3.3 V CMOS | LD | Lock Detect (Output). This pin has multiple selectable outputs; see Table 54, Register 0x1A. |
| 4 | I | Power | VCP | Power Supply for Charge Pump (CP); $V_S \leq V_{CP} \leq 5.0$ V. |
| 5 | O | 3.3 V CMOS | CP | Charge Pump (Output). Connects to external loop filter. |
| 6 | O | 3.3 V CMOS | STATUS | Status (Output). This pin has multiple selectable outputs; see Table 54, Register 0x017. |
| 7 | I | 3.3 V CMOS | REF_SEL | Reference Select. Selects REF1 (low) or REF2 (high). This pin has an internal 30 k Ω pull-down resistor. |
| 8 | I | 3.3 V CMOS | $\overline{\text{SYNC}}$ | Manual Synchronizations and Manual Holdover. This pin initiates a manual synchronization and is also used for manual holdover. Active low. This pin has an internal 30 k Ω pull-up resistor. |
| 9 | I | Loop filter | LF | Loop Filter (Input). Connects to VCO control voltage node internally. This pin has 31 pF of internal capacitance to ground, which may influence the loop filter design for large (>500 kHz) loop bandwidths. |
| 10 | O | Loop filter | BYPASS | This pin is for bypassing the LDO to ground with a capacitor. |
| 13 | I | Differential clock input | CLK | Along with $\overline{\text{CLK}}$, this is the differential input for the clock distribution section. |
| 14 | I | Differential clock input | $\overline{\text{CLK}}$ | Along with CLK, this is the differential input for the clock distribution section. |

| Pin No. | Input/ Output | Pin Type | Mnemonic | Description |
|------------------|------------------|----------------------|---------------------------|---|
| 15, 18, 19, 20 | N/A | NC | NC | No Connect. Do not connect to this pin. |
| 16 | I | 3.3 V CMOS | SCLK | Serial Control Port Data Clock Signal. |
| 17 | I | 3.3 V CMOS | \overline{CS} | Serial Control Port Chip Select, Active Low. This pin has an internal 30 k Ω pull-up resistor. |
| 21 | O | 3.3 V CMOS | SDO | Serial Control Port Unidirectional Serial Data Out. |
| 22 | I/O | 3.3 V CMOS | SDIO | Serial Control Port Bidirectional Serial Data In/Out. |
| 23 | I | 3.3 V CMOS | \overline{RESET} | Chip Reset, Active Low. This pin has an internal 30 k Ω pull-up resistor. |
| 24 | I | 3.3 V CMOS | \overline{PD} | Chip Power-Down, Active Low. This pin has an internal 30 k Ω pull-up resistor. |
| 27, 41, 54 | I | Power | VS_LVPECL | Extended Voltage 2.5 V to 3.3 V LVPECL Power Pins. |
| 37, 44, 59, EPAD | N/A | GND | GND | Ground Pins, Including External Paddle (EPAD). The external paddle on the bottom of the package must be connected to ground for proper operation. |
| 56 | O | LVPECL | $\overline{OUT0}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 55 | O | LVPECL | $\overline{OUT0}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 53 | O | LVPECL | $\overline{OUT1}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 52 | O | LVPECL | $\overline{OUT1}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 43 | O | LVPECL | $\overline{OUT2}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 42 | O | LVPECL | $\overline{OUT2}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 40 | O | LVPECL | $\overline{OUT3}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 39 | O | LVPECL | $\overline{OUT3}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 25 | O | LVPECL | $\overline{OUT4}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 26 | O | LVPECL | $\overline{OUT4}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 28 | O | LVPECL | $\overline{OUT5}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 29 | O | LVPECL | $\overline{OUT5}$ | LVPECL Output; One Side of a Differential LVPECL Output. |
| 48 | O | LVDS or CMOS | $\overline{OUT6}$ (OUT6A) | LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output. |
| 47 | O | LVDS or CMOS | $\overline{OUT6}$ (OUT6B) | LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output. |
| 46 | O | LVDS or CMOS | $\overline{OUT7}$ (OUT7A) | LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output. |
| 45 | O | LVDS or CMOS | $\overline{OUT7}$ (OUT7B) | LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output. |
| 33 | O | LVDS or CMOS | $\overline{OUT8}$ (OUT8A) | LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output. |
| 34 | O | LVDS or CMOS | $\overline{OUT8}$ (OUT8B) | LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output. |
| 35 | O | LVDS or CMOS | $\overline{OUT9}$ (OUT9A) | LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output. |
| 36 | O | LVDS or CMOS | $\overline{OUT9}$ (OUT9B) | LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output. |
| 58 | O | Current set resistor | RSET | A resistor connected to this pin sets internal bias currents. Nominal value = 4.12 k Ω . |
| 62 | O | Current set resistor | CPRSET | A resistor connected to this pin sets the CP current range. Nominal value = 5.1 k Ω . |
| 63 | I | Reference input | \overline{REFIN} (REF2) | Along with \overline{REFIN} , this pin is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF2. |
| 64 | I | Reference input | REFIN (REF1) | Along with \overline{REFIN} , this pin is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF1. |

TYPICAL PERFORMANCE CHARACTERISTICS

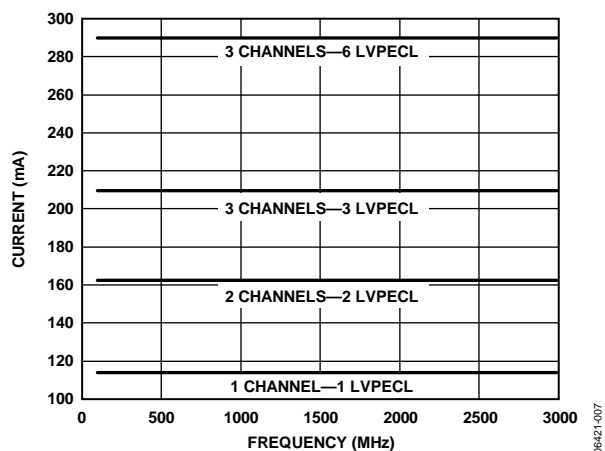


Figure 7. Current vs. Frequency, Direct to Output, LVPECL Outputs

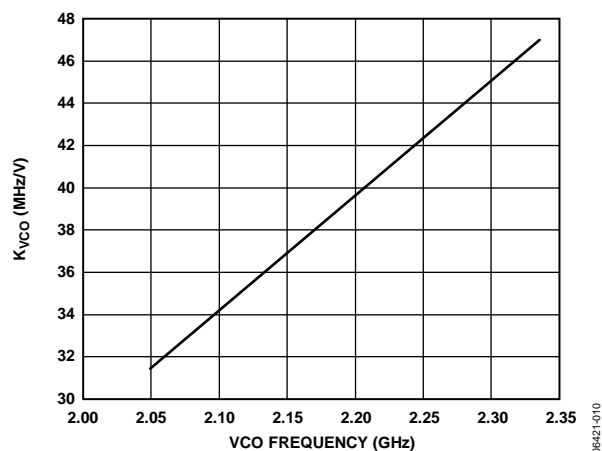
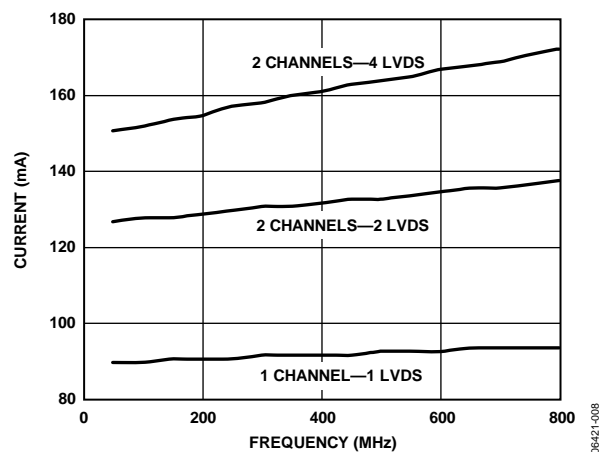
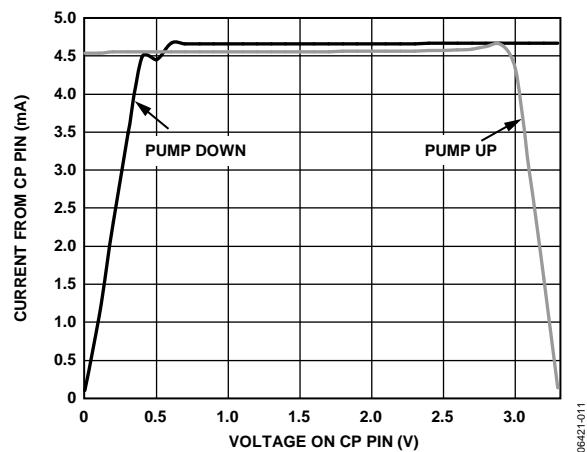
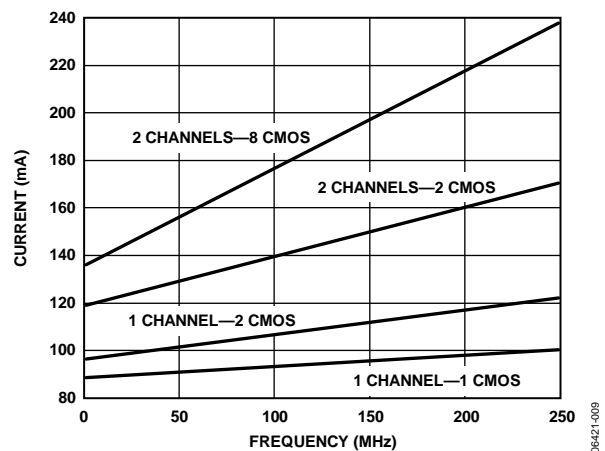
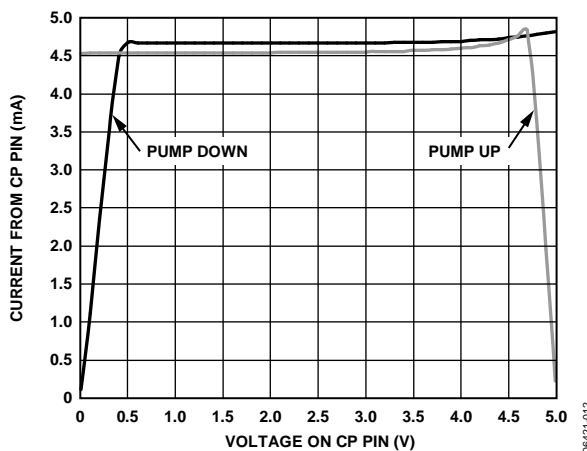
Figure 10. VCO K_{VCO} vs. FrequencyFigure 8. Current vs. Frequency—LVDS Outputs
(Includes Clock Distribution Current Draw)Figure 11. Charge Pump Characteristics at $V_{CP} = 3.3\text{ V}$ 

Figure 9. Current vs. Frequency—CMOS Outputs

Figure 12. Charge Pump Characteristics at $V_{CP} = 5.0\text{ V}$

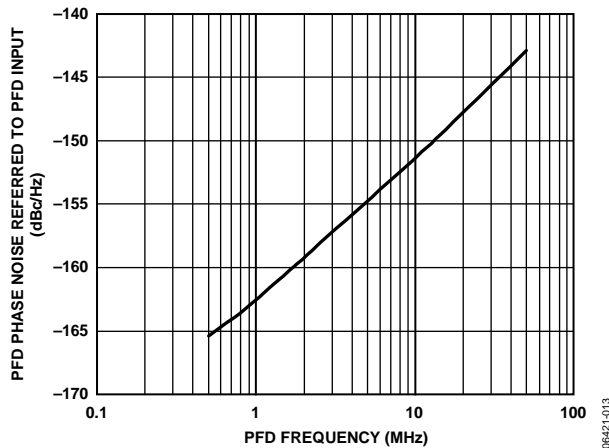


Figure 13. PFD Phase Noise Referred to PFD Input vs. PFD Frequency

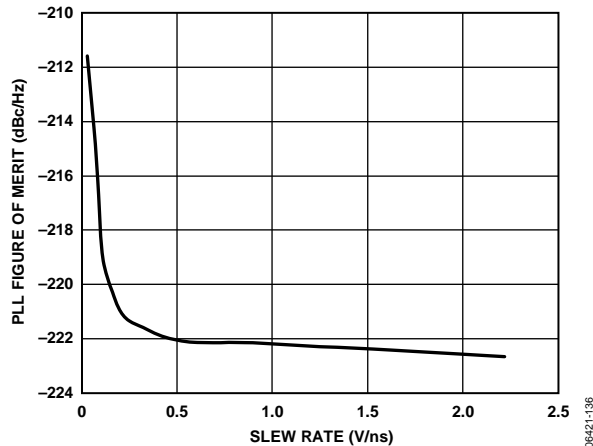


Figure 14. PLL Figure of Merit (FOM) vs. Slew Rate at $\overline{\text{REFIN}}/\overline{\text{REFIN}}$

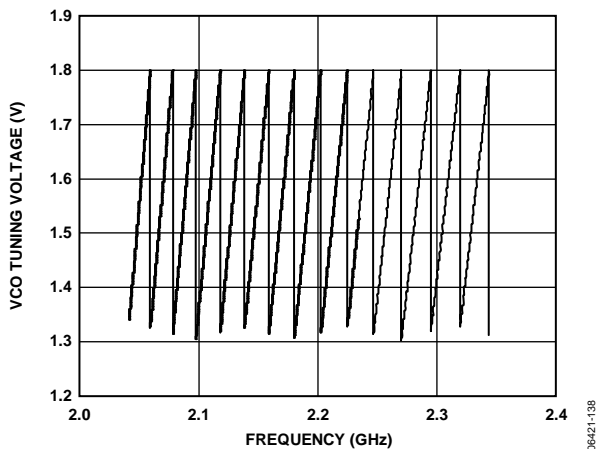


Figure 15. VCO Tuning Voltage vs. Frequency
(Note that VCO calibration centers the dc tuning voltage for the PLL setup that is active during calibration.)

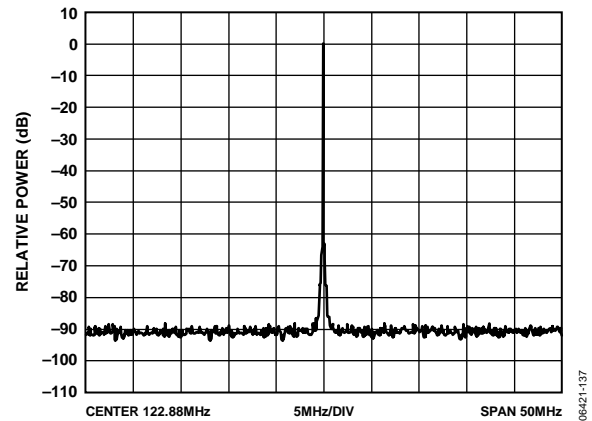


Figure 16. PFD/CP Spurs; 122.88 MHz; PFD = 15.36 MHz;
LBW = 138 kHz; I_{CP} = 3.0 mA; F_{VCO} = 2.21 GHz

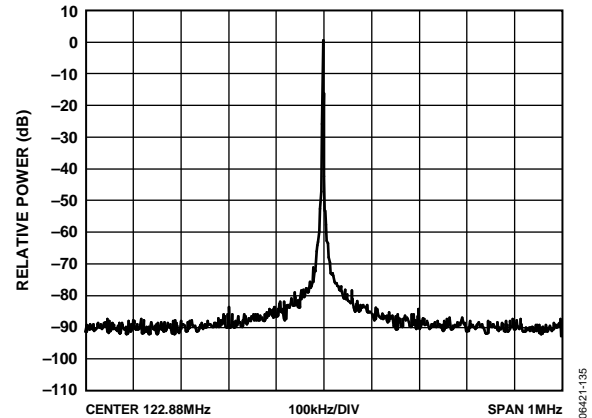


Figure 17. Output Spectrum, LVPECL; 122.88 MHz; PFD = 15.36 MHz;
LBW = 138 kHz; I_{CP} = 3.0 mA; F_{VCO} = 2.21 GHz

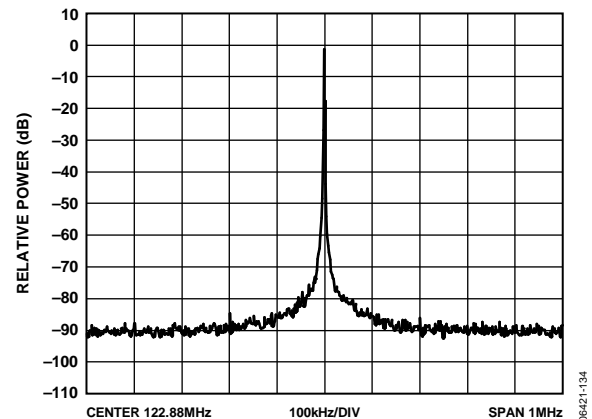


Figure 18. Output Spectrum, LVDS; 122.88 MHz; PFD = 15.36 MHz;
LBW = 138 kHz; I_{CP} = 3.0 mA; F_{VCO} = 2.21 GHz

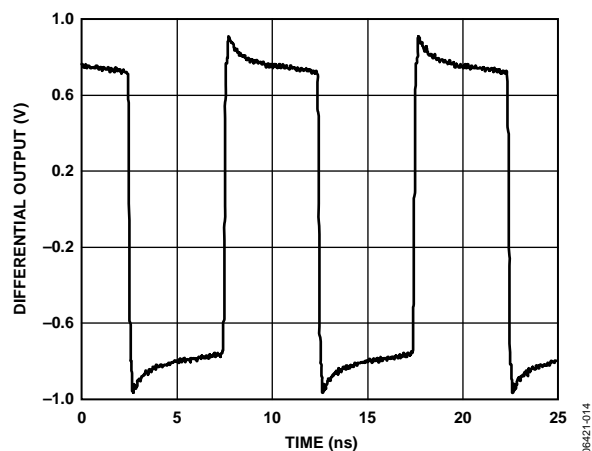


Figure 19. LVPECL Output (Differential) at 100 MHz

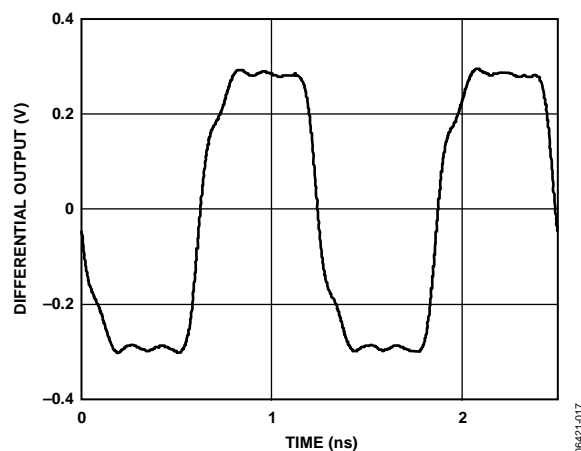


Figure 22. LVDS Output (Differential) at 800 MHz

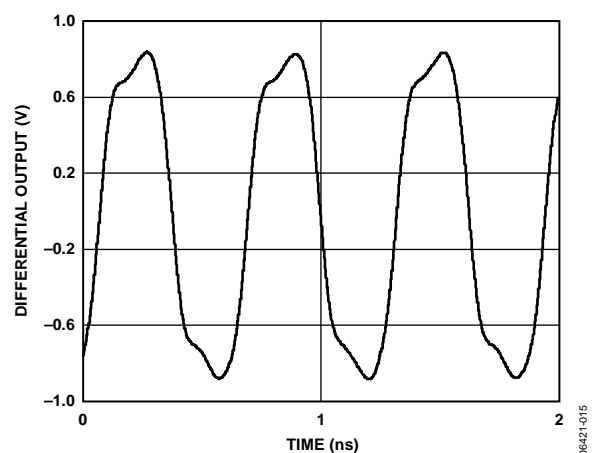


Figure 20. LVPECL Output (Differential) at 1600 MHz

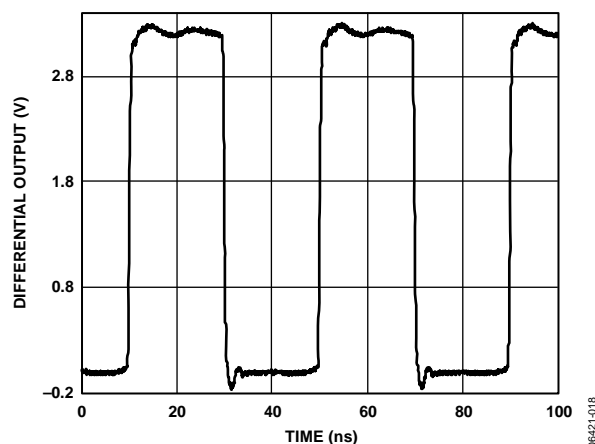


Figure 23. CMOS Output at 25 MHz

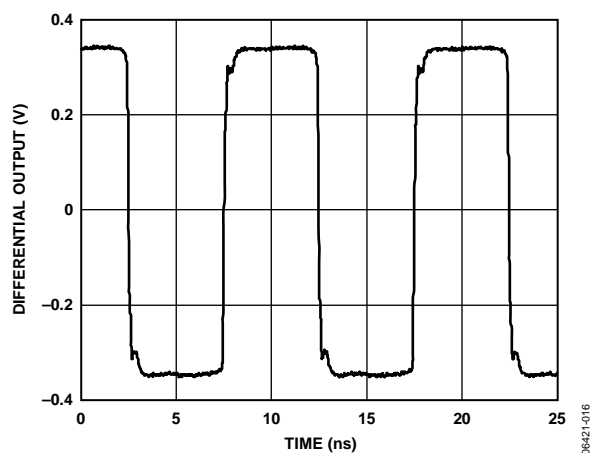


Figure 21. LVDS Output (Differential) at 100 MHz

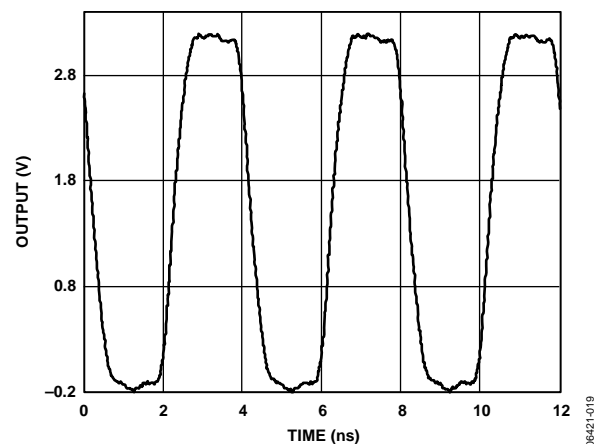


Figure 24. CMOS Output at 250 MHz

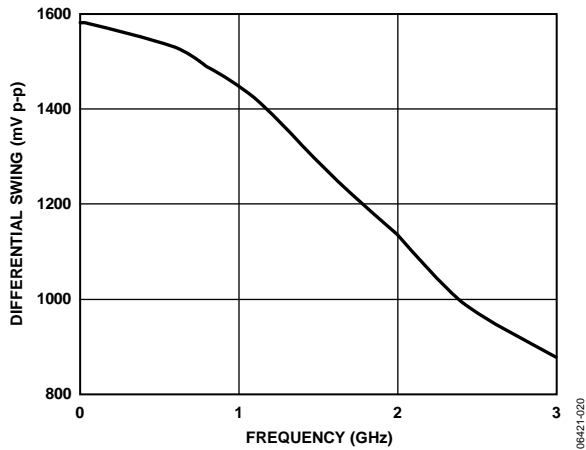


Figure 25. LVPECL Differential Swing vs. Frequency Using a Differential Probe Across the Output Pair

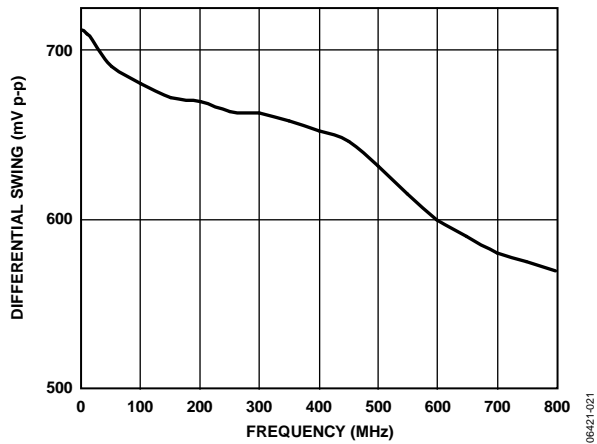


Figure 26. LVDS Differential Swing vs. Frequency Using a Differential Probe Across the Output Pair

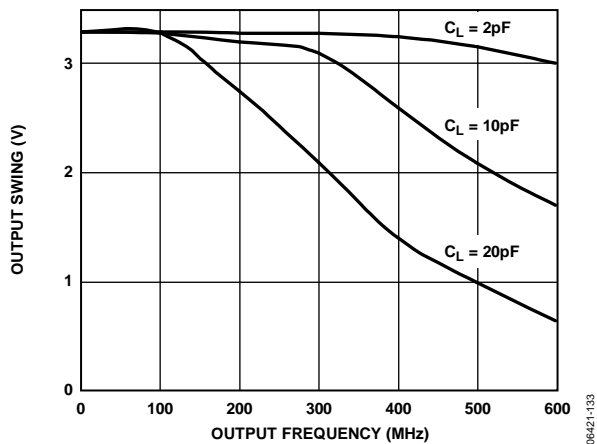


Figure 27. CMOS Output Swing vs. Frequency and Capacitive Load

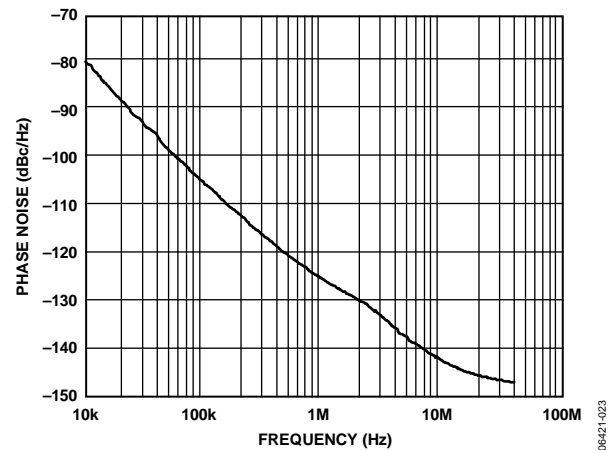


Figure 28. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2335 MHz

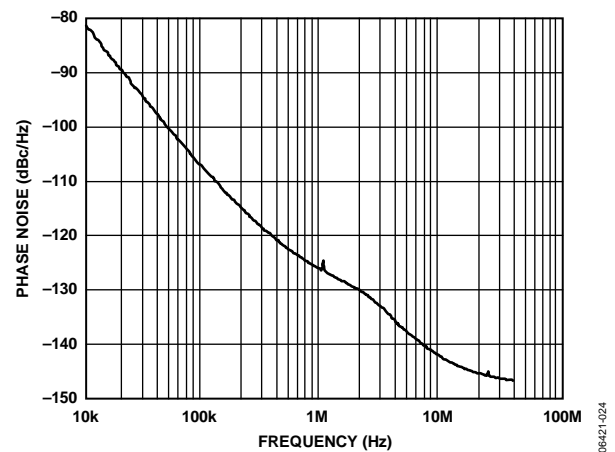


Figure 29. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2175 MHz

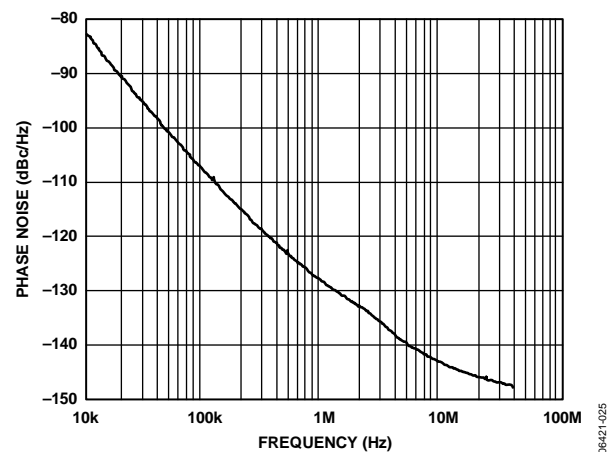


Figure 30. Internal VCO Phase Noise (Absolute) Direct to LVPECL at 2050 MHz

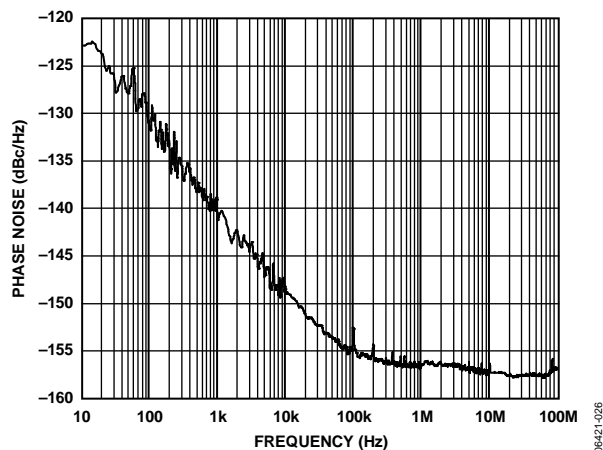


Figure 31. Phase Noise (Additive) LVPECL at 245.76 MHz, Divide-by-1

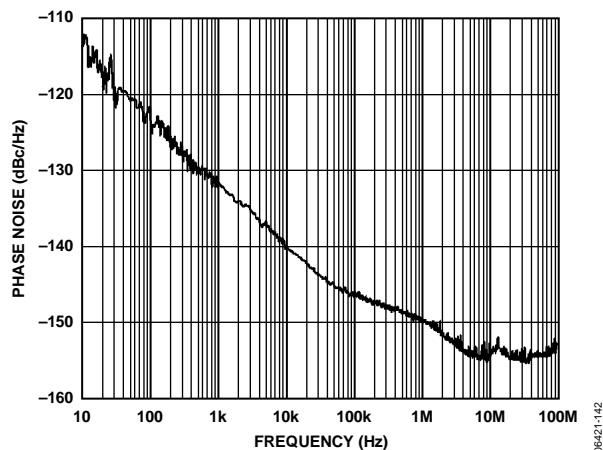


Figure 34. Phase Noise (Additive) LVDS at 200 MHz, Divide-by-1

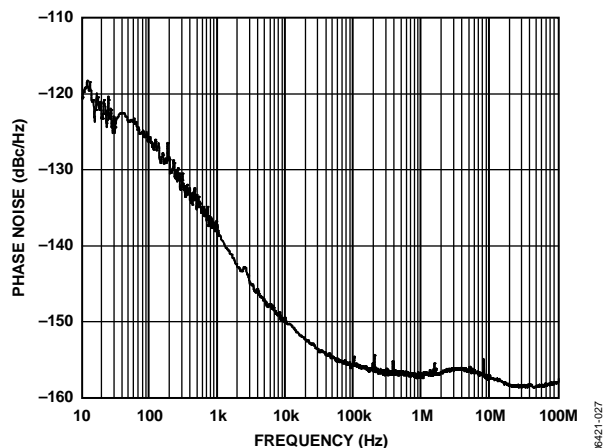


Figure 32. Phase Noise (Additive) LVPECL at 200 MHz, Divide-by-5

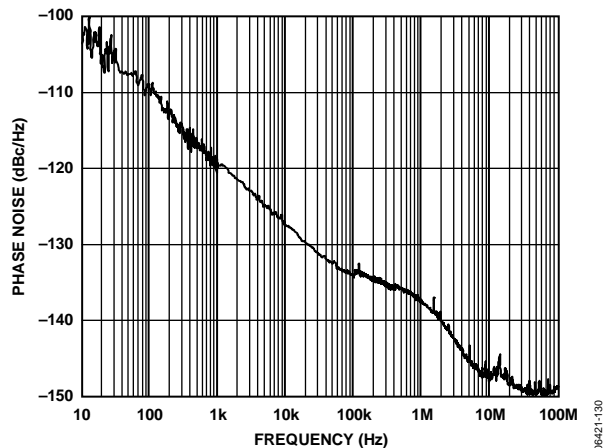


Figure 35. Phase Noise (Additive) LVDS at 800 MHz, Divide-by-2

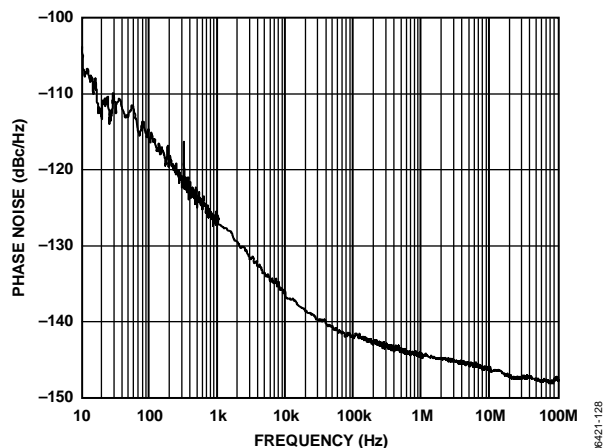


Figure 33. Phase Noise (Additive) LVPECL at 1600 MHz, Divide-by-1

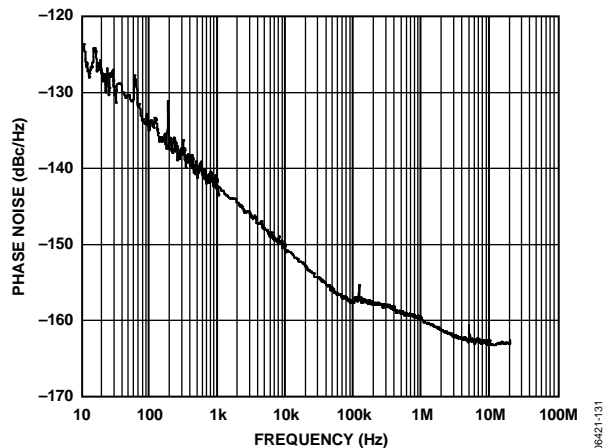


Figure 36. Phase Noise (Additive) CMOS at 50 MHz, Divide-by-20

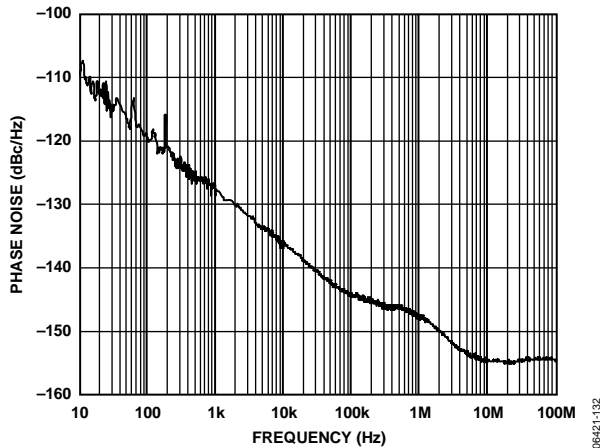


Figure 37. Phase Noise (Additive) CMOS at 250 MHz, Divide-by-4

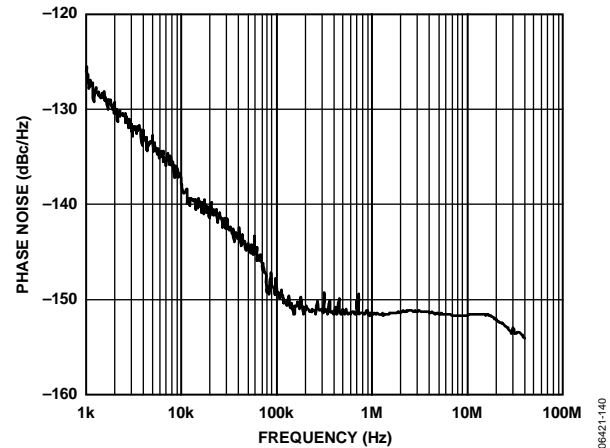


Figure 40. Phase Noise (Absolute), External VCXO (Toyocom TCO-2112) at 245.76 MHz; PFD = 15.36 MHz; LBW = 250 Hz; LVPECL Output = 245.76 MHz

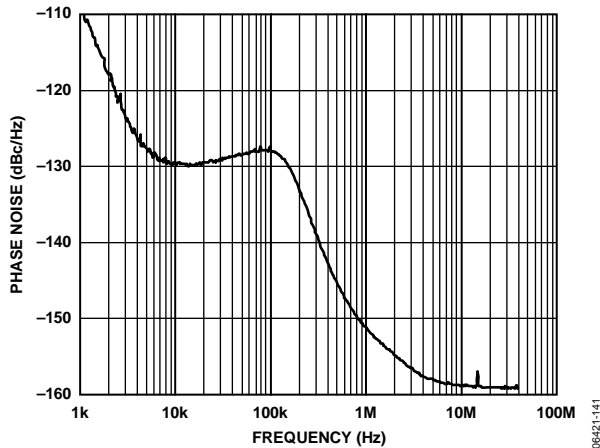


Figure 38. Phase Noise (Absolute) Clock Generation; Internal VCO at 2.21 GHz; PFD = 15.36 MHz; LBW = 138 kHz; LVPECL Output = 122.88 MHz

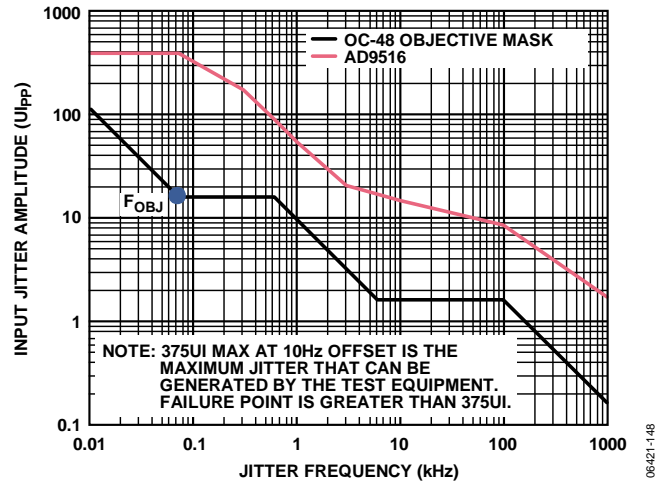


Figure 41. GR-253 Jitter Tolerance Plot

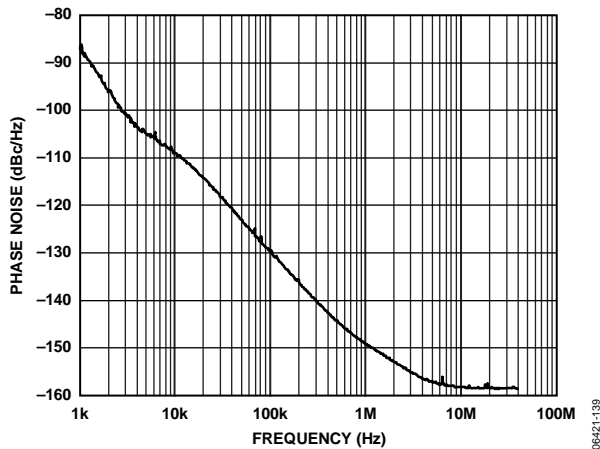


Figure 39. Phase Noise (Absolute) Clock Cleanup; Internal VCO at 2.18 GHz; PFD = 19.44 MHz; LBW = 12.8 kHz; LVPECL Output = 155.52 MHz

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in dB) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in units of seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

DETAILED BLOCK DIAGRAM

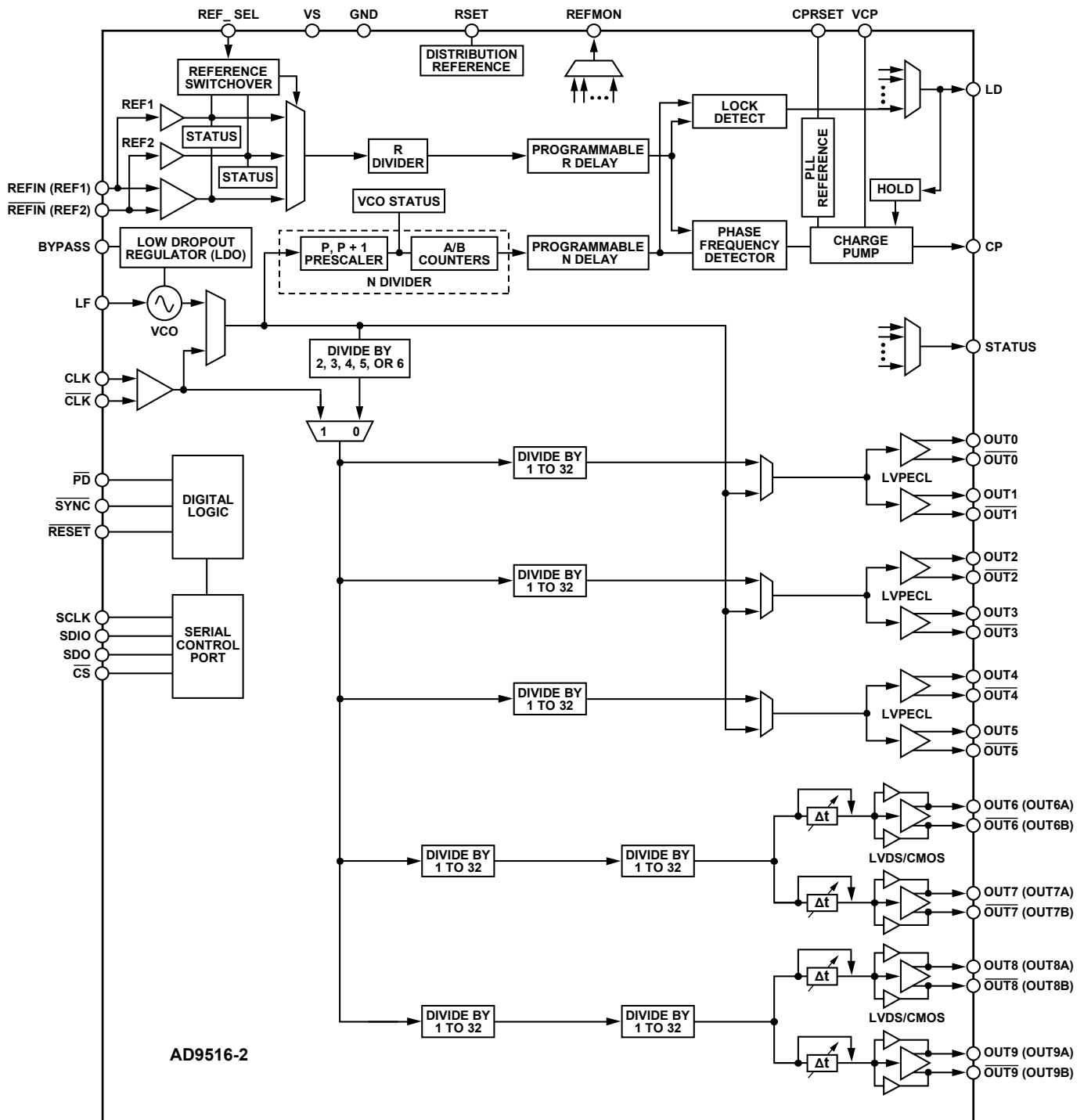


Figure 42. Detailed Block Diagram

THEORY OF OPERATION

OPERATIONAL CONFIGURATIONS

The AD9516 can be configured in several ways. These configurations must be set up by loading the control registers (see Table 52 and Table 53 through Table 62). Each section or function must be individually programmed by setting the appropriate bits in the corresponding control register or registers.

High Frequency Clock Distribution—CLK or External VCO > 1600 MHz

The AD9516 power-up default configuration has the PLL powered off and the routing of the input set so that the CLK/CLK input is connected to the distribution section through the VCO divider (divide-by-2/divide-by-3/divide-by-4/divide-by-5/divide-by-6). This is a distribution only mode that allows for an external input up to 2400 MHz (see Table 3). The maximum frequency that can be applied to the channel dividers is 1600 MHz; therefore, higher input frequencies must be divided down before reaching the channel dividers. This input routing can also be used for lower input frequencies, but the minimum divide is 2 before the channel dividers.

When the PLL is enabled, this routing also allows the use of the PLL with an external VCO or VCXO with a frequency of less than 2400 MHz. In this configuration, the internal VCO is not used and is powered off. The external VCO/VCXO feeds directly into the prescaler.

The register settings shown in Table 21 are the default values of these registers at power-up or after a reset operation. If the contents of the registers are altered by prior programming after power-up or reset, these registers can also be set intentionally to these values.

After the appropriate register values are programmed, Register 0x232 must be set to 0x01 for the values to take effect.

Table 21. Default Settings of Some PLL Registers

| Register | Function |
|-------------------|--|
| 0x010[1:0] = 01b | PLL asynchronous power-down (PLL off). |
| 0x1E0[2:0] = 010b | Set VCO divider = 4. |
| 0x1E1[0] = 0b | Use the VCO divider. |
| 0x1E1[1] = 0b | CLK selected as the source. |

When using the internal PLL with an external VCO, the PLL must be turned on.

Table 22. Settings When Using an External VCO

| Register | Function |
|------------------|---|
| 0x010[1:0] = 00b | PLL normal operation (PLL on). |
| 0x010 to 0x01D | PLL settings. Select and enable a reference input; set R, N (P, A, B), PFD polarity, and I_{CP} , according to the intended loop configuration. |
| 0x1E1[1] = 0b | CLK selected as the source. |

An external VCO requires an external loop filter that must be connected between CP and the tuning pin of the VCO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO being used.

Table 23. Setting the PFD Polarity

| Register | Function |
|---------------|---|
| 0x010[7] = 0b | PFD polarity positive (higher control voltage produces higher frequency). |
| 0x010[7] = 1b | PFD polarity negative (higher control voltage produces lower frequency). |

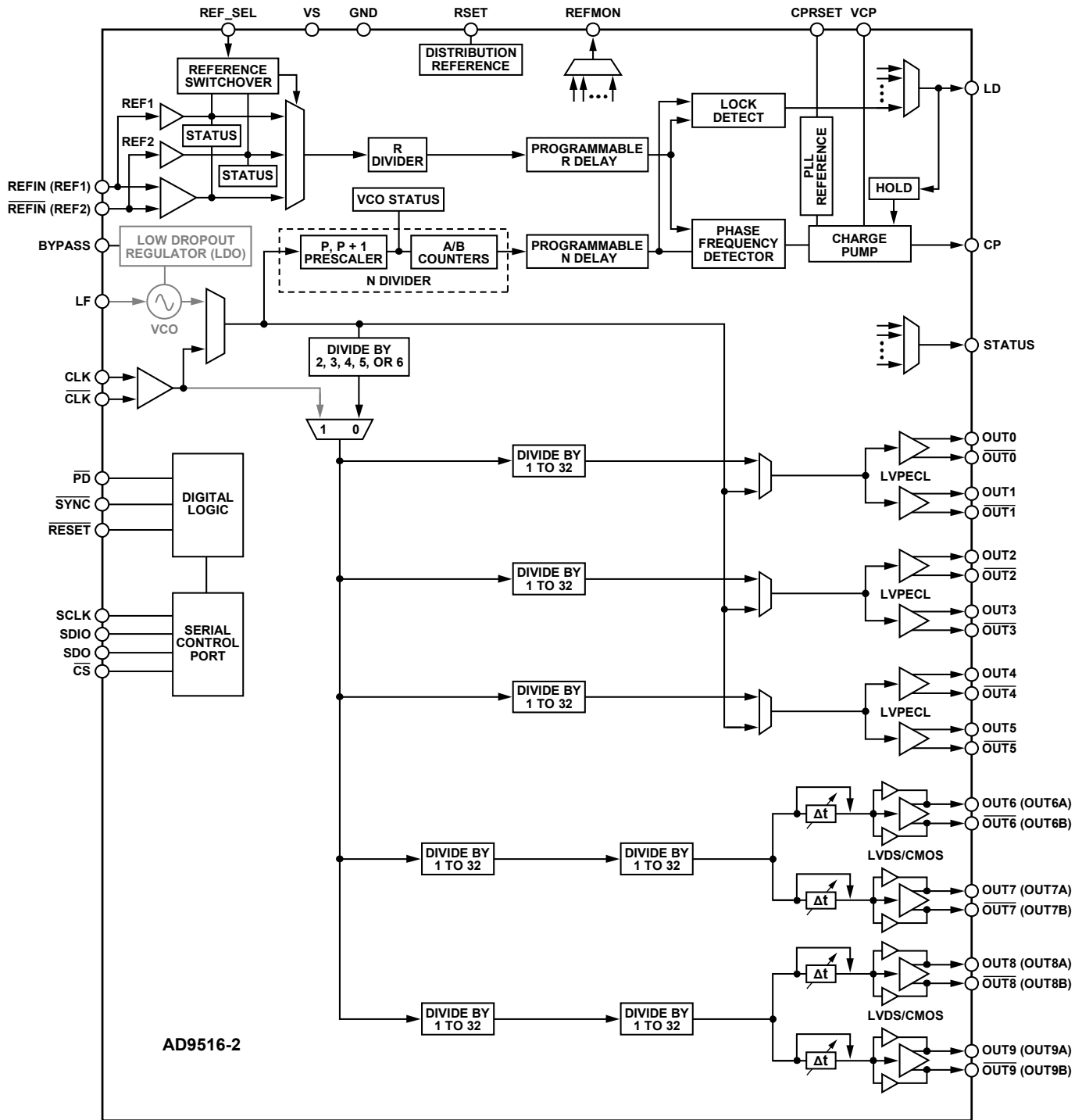


Figure 43. High Frequency Clock Distribution or External VCO > 1600 MHz

06421-028

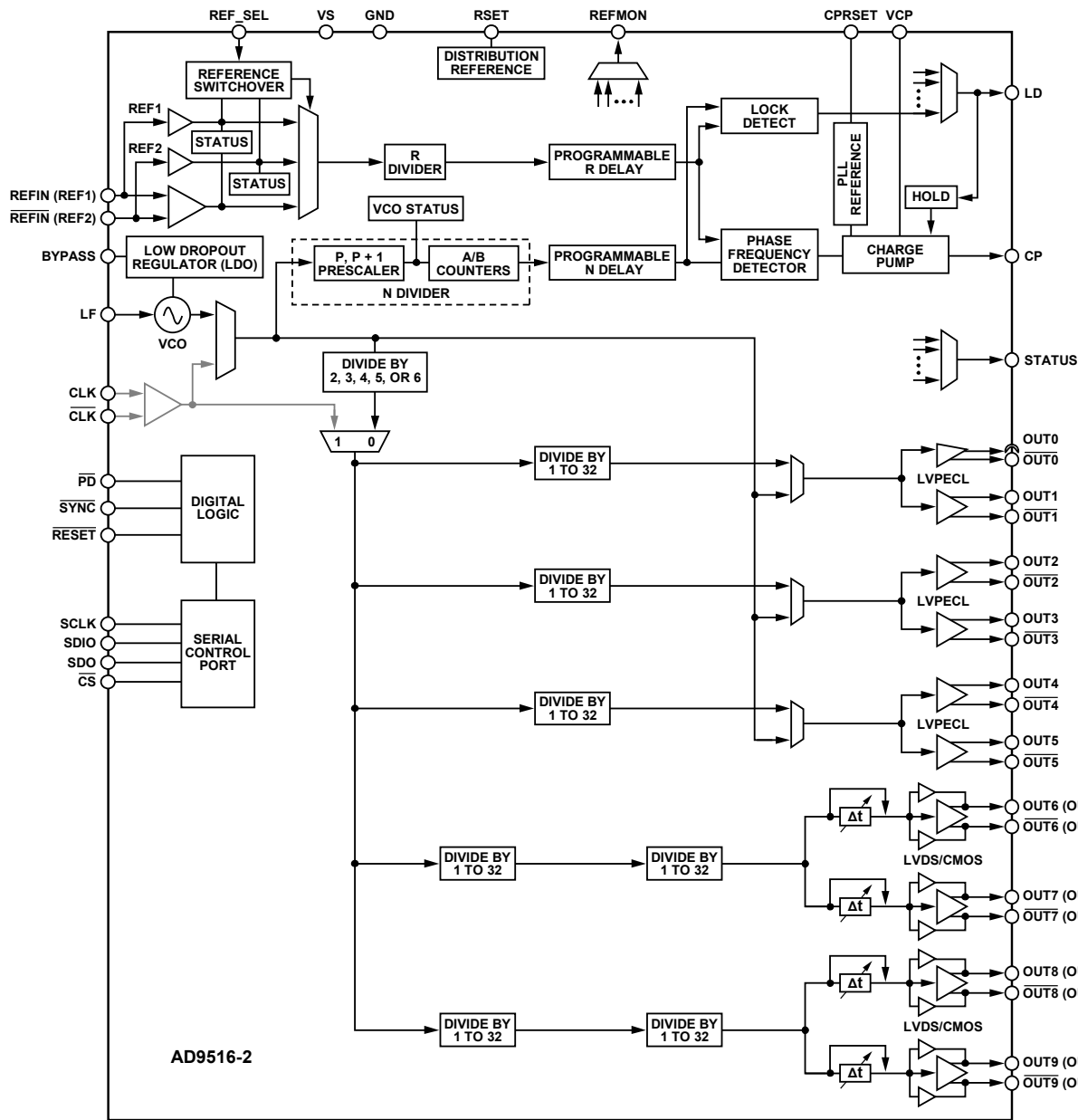


Figure 44. Internal VCO and Clock Distribution

Internal VCO and Clock Distribution

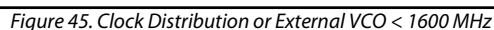
When using the internal VCO and PLL, the VCO divider must be employed to ensure that the frequency presented to the channel dividers does not exceed their specified maximum frequency of 1600 MHz (see Table 3). The internal PLL uses an external loop filter to set the loop bandwidth. The external loop filter is also crucial to the loop stability.

When using the internal VCO, it is necessary to calibrate the VCO (Register 0x018[0]) to ensure optimal performance.

For internal VCO and clock distribution applications, use the register settings that are shown in Table 24.

Table 24. Settings When Using Internal VCO

| Register | Function |
|------------------------------|---|
| 0x010[1:0] = 00b | PLL normal operation (PLL on). |
| 0x010 to 0x01E | PLL settings. Select and enable a reference input; set R, N (P, A, B), PFD polarity, and I_{CP} , according to the intended loop configuration. |
| 0x018[0] = 0b, 0x232[0] = 1b | Reset VCO calibration. This is not required the first time after power-up, but it must be performed subsequently. |
| 0x1E0[2:0] | Set VCO divider to divide-by-2, divide-by-3, divide-by-4, divide-by-5, and divide-by-6. |
| 0x1E1[0] = 0b | Use the VCO divider as source for the distribution section. |
| 0x1E1[1] = 1b | Select VCO as the source. |
| 0x018[0] = 1b, 0x232[0] = 1b | Initiate VCO calibration. |



Clock Distribution or External VCO < 1600 MHz

When the external clock source to be distributed or the external VCO/VCXO is less than 1600 MHz, a configuration that bypasses the VCO divider can be used. This configuration differs from the High Frequency Clock Distribution—CLK or External VCO > 1600 MHz section only in that the VCO divider (divide-by-2, divide-by-3, divide-by-4, divide-by-5, and divide-by-6) is bypassed. This limits the frequency of the clock source to <1600 MHz (due to the maximum input frequency allowed at the channel dividers).

Configuration and Register Settings

For clock distribution applications where the external clock is <1600 MHz, use the register settings that are shown in Table 25.

Table 25. Settings for Clock Distribution < 1600 MHz

| Register | Function |
|------------------|---|
| 0x010[1:0] = 01b | PLL asynchronous power-down (PLL off) |
| 0x1E1[0] = 1b | Bypass the VCO divider as source for distribution section |
| 0x1E1[1] = 0b | CLK selected as the source |

When using the internal PLL with an external VCO of <1600 MHz, the PLL must be turned on.

Table 26. Settings for Using Internal PLL with External VCO < 1600 MHz

| Register | Function |
|------------------|--|
| 0x1E1[0] = 1b | Bypass the VCO divider as source for distribution section |
| 0x010[1:0] = 00b | PLL normal operation (PLL on), along with other appropriate PLL settings in Register 0x010 to Register 0x01E |

An external VCO/VCXO requires an external loop filter that must be connected between CP and the tuning pin of the VCO/VCXO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO/VCXO being used.

Table 27. Setting the PFD Polarity

| Register | Function |
|---------------|--|
| 0x010[7] = 0b | PFD polarity positive (higher control voltage produces higher frequency) |
| 0x010[7] = 1b | PFD polarity negative (higher control voltage produces lower frequency) |

After the appropriate register values are programmed, Register 0x232 must be set to 0x01 for the values to take effect.

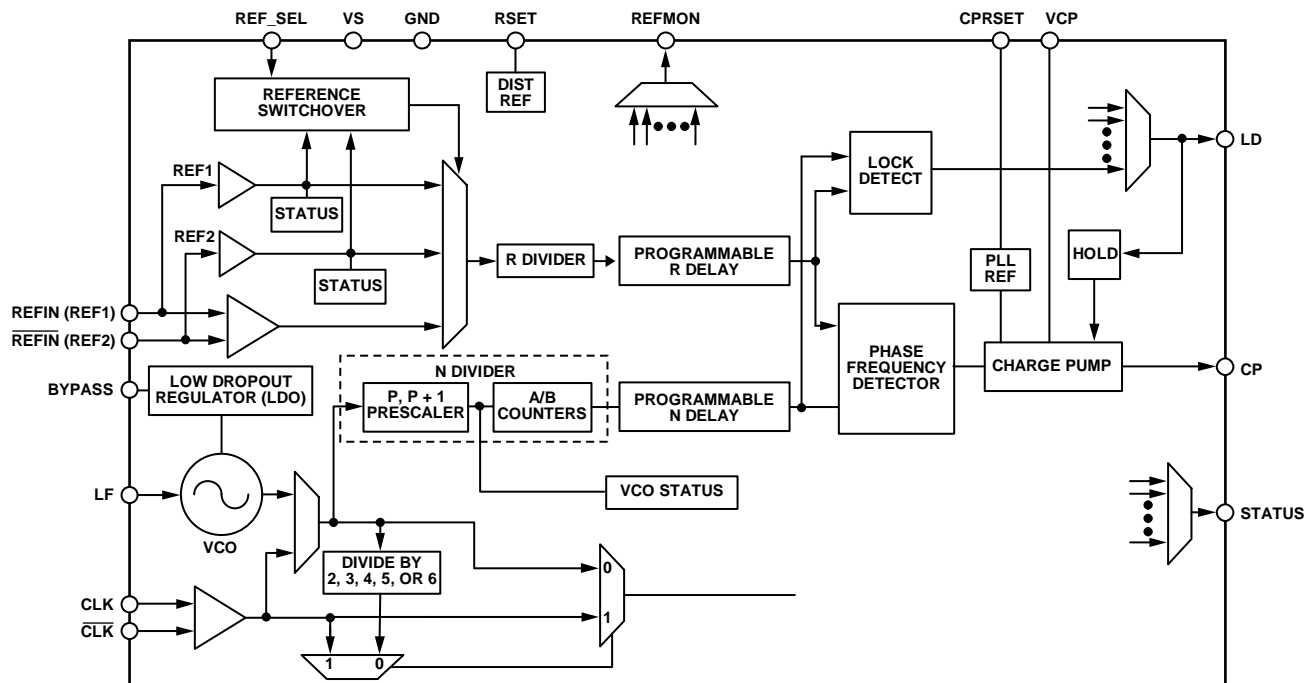
Phase-Locked Loop (PLL)

Figure 46. PLL Functional Blocks

The AD9516 includes an on-chip PLL with an on-chip VCO. The PLL blocks can be used either with the on-chip VCO to create a complete phase-locked loop, or with an external VCO or VCXO. The PLL requires an external loop filter, which usually consists of a small number of capacitors and resistors. The configuration and components of the loop filter help to establish the loop bandwidth and stability of the operating PLL.

The AD9516 PLL is useful for generating clock frequencies from a supplied reference frequency. This includes conversion of reference frequencies to much higher frequencies for subsequent division and distribution. In addition, the PLL can be exploited to clean up jitter and phase noise on a noisy reference. The exact choices of PLL parameters and loop dynamics are very application specific. The flexibility and depth of the AD9516 PLL allow the part to be tailored to function in many different applications and signal environments.

Configuration of the PLL

The AD9516 allows flexible configuration of the PLL, accommodating various reference frequencies, PFD comparison frequencies, VCO frequencies, internal or external VCO/VCXO, and loop dynamics. This is accomplished by the various settings that include the R divider, the N divider, the PFD polarity (only applicable to external VCO/VCXO), the antibacklash pulse width, the charge pump current, the selection of internal VCO or external VCO/VCXO, and the loop bandwidth.

These are managed through programmable register settings (see Table 52 and Table 54) and by the design of the external loop filter. Successful PLL operation and satisfactory PLL loop performance are highly dependent upon proper configuration of the PLL settings. The design of the external loop filter is crucial to the proper operation of the PLL. A thorough knowledge of PLL theory and design is helpful.

ADIsimCLK™ (V1.2 or later) is a free program that can help with the design and exploration of the capabilities and features of the AD9516, including the design of the PLL loop filter. It is available at www.analog.com/clocks.

Phase Frequency Detector (PFD)

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. The antibacklash pulse width is set by Register 0x017[1:0].

An important limit to keep in mind is the maximum frequency allowed into the PFD, which in turn determines the correct antibacklash pulse setting. The antibacklash pulse setting is specified in the phase/frequency detector parameter of Table 2.

Charge Pump (CP)

The charge pump is controlled by the PFD. The PFD monitors the phase and frequency relationship between its two inputs, and tells the CP to pump up or pump down to charge or discharge the integrating node (part of the loop filter). The integrated and filtered CP current is transformed into a voltage that drives the tuning node of the internal VCO through the LF pin (or the tuning pin of an external VCO) to move the VCO frequency up or down. The CP can be set (Register 0x010[6:4]) for high impedance (allows holdover operation), for normal operation (attempts to lock the PLL loop), for pump up, or for pump down (test modes). The CP current is programmable in eight steps from (nominally) 600 μA to 4.8 mA. The exact value of the CP current LSB is set by the CPRSET resistor, which is nominally 5.1 k Ω . If the value of the resistor connected to the CP_RSET pin is doubled, the resulting charge pump current range becomes 300 μA to 2.4 mA.

On-Chip VCO

The AD9516 includes an on-chip VCO covering the frequency range shown in Table 2. The calibration procedure ensures that the VCO operating voltage is centered for the desired VCO frequency. The VCO must be calibrated when the VCO loop is first set up, as well as any time the nominal VCO frequency changes. However, once the VCO is calibrated, the VCO has sufficient operating range to stay locked over temperature and voltage extremes without needing additional calibration. See the VCO Calibration section for more information.

The on-chip VCO is powered by an on-chip, low dropout (LDO), linear voltage regulator. The LDO provides some isolation of the VCO from variations in the power supply voltage level. The BYPASS pin should be connected to ground by a 220 nF capacitor to ensure stability. This LDO employs the same technology used in the anyCAP® line of regulators from Analog Devices, Inc., making it insensitive to the type of capacitor used. Driving an external load from the BYPASS pin is not supported.

Note that the reference input signal must be present and the VCO divider must not be static during VCO calibration.

PLL External Loop Filter

When using the internal VCO, the external loop filter should be referenced to the BYPASS pin for optimal noise and spurious performance. An example of an external loop filter for a PLL that uses the internal VCO is shown in Figure 47. The third-order design shown in Figure 47 usually offers best performance. A loop filter must be calculated for each desired PLL configuration. The values of the components depend upon the VCO frequency, the K_{VCO} , the PFD frequency, the CP current, the desired loop bandwidth, and the desired phase margin. The loop filter affects the phase noise, the loop settling time, and loop stability. A basic knowledge of PLL theory is helpful for understanding loop filter design. ADIsimCLK can help with calculation of a loop filter according to the application requirements.

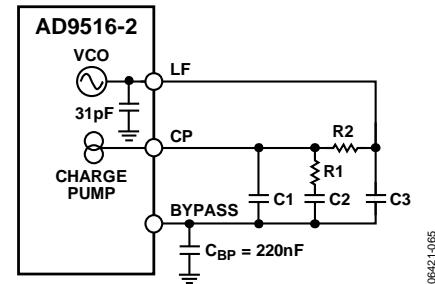


Figure 47. Example of External Loop Filter for a PLL Using the Internal VCO

When using an external VCO, the external loop filter should be referenced to ground. See Figure 48 for an example of an external loop filter for a PLL using an external VCO.

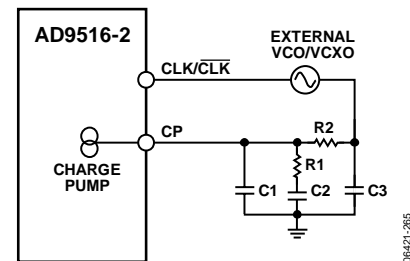


Figure 48. Example of External Loop Filter for a PLL Using an External VCO

PLL Reference Inputs

The AD9516 features a flexible PLL reference input circuit that allows either a fully differential input or two separate single-ended inputs. The input frequency range for the reference inputs is specified in Table 2. Both the differential and the single-ended inputs are self-biased, allowing for easy ac coupling of input signals.

The differential input and the single-ended inputs share the two pins, REFIN/REFIN (REF1 and REF2, respectively). The desired reference input type is selected and controlled by Register 0x01C (see Table 52 and Table 54).

When the differential reference input is selected, the self-bias level of the two sides is offset slightly (~100 mV, see Table 2) to prevent chattering of the input buffer when the reference is slow or missing. This increases the voltage swing that is required of the driver and overcomes the offset. The differential reference input can be driven by either ac-coupled LVDS or ac-coupled LVPECL signals.

The single-ended inputs can be driven by either a dc-coupled CMOS level signal or an ac-coupled sine wave or square wave. Each single-ended input can be independently powered down when not needed to increase isolation and reduce power. Either a differential or a single-ended reference must be specifically enabled. All PLL reference inputs are off by default.

The differential reference input is powered down whenever the PLL is powered down, or when the differential reference input is not selected. The single-ended buffers power down when the PLL is powered down, and when their individual power down registers are set. When the differential mode is selected, the single-ended inputs are powered down.

In differential mode, the reference input pins are internally self-biased so that they can be ac-coupled via capacitors. It is possible to dc couple to these inputs. If the differential REFIN is driven by a single-ended signal, the unused side ($\overline{\text{REFIN}}$) should be decoupled via a suitable capacitor to a quiet ground. Figure 49 shows the equivalent circuit of REFIN.

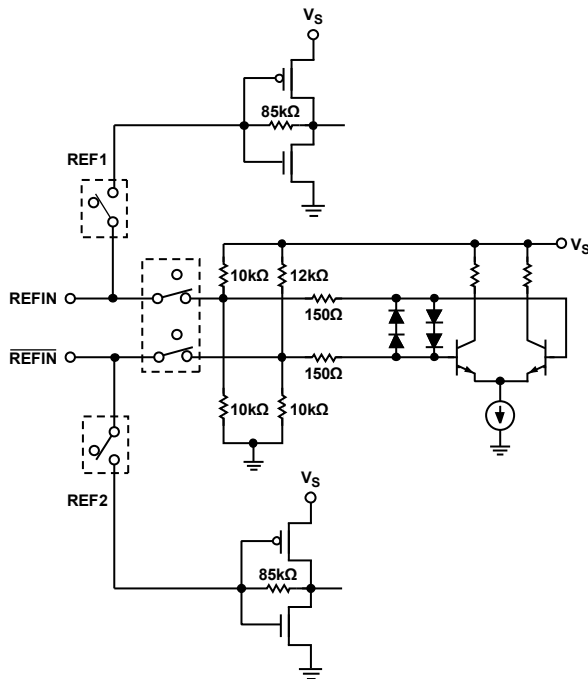


Figure 49. REFIN Equivalent Circuit

Reference Switchover

The AD9516 supports dual single-ended CMOS inputs, as well as a single differential reference input. In the dual single-ended reference mode, the AD9516 supports automatic and manual PLL reference clock switching between REF1 (on Pin REFIN) and REF2 (on Pin REFIN). This feature supports networking and other applications that require smooth switching of redundant references. When used in conjunction with the automatic holdover function, the AD9516 can achieve a worst-case reference input switchover with an output frequency disturbance as low as 10 ppm.

When using reference switchover, the single-ended reference inputs should be dc-coupled CMOS levels and never be allowed to go to high impedance. If these inputs are allowed to go to high impedance, noise may cause the buffer to chatter, causing a false detection of the presence of a reference.

Reference switchover can be performed manually or automatically. Manual switchover is performed either through Register 0x01C or by using the REF_SEL pin. Manual switchover requires the presence of a clock on the reference input that is being switched to, or that the deglitching feature be disabled (Register 0x01C[7]). The reference switching logic fails if this condition isn't met, and the PLL does not reacquire.

Automatic revertive switchover relies on the REFMON pin to indicate when REF1 disappears. By programming Register 0x01B = 0xF7 and Register 0x01C = 0x26, the REFMON pin is programmed to be high when REF1 is invalid, which commands the switch to REF2. When REF1 is valid again, the REFMON pin goes low, and the part again locks to REF1. It is also possible to use the STATUS pin for this function, and REF2 can be used as the preferred reference.

A switchover deglitch feature ensures that the PLL does not receive rising edges that are far out of alignment with the newly selected reference.

Automatic nonrevertive switching is not supported.

Reference Divider R

The reference inputs are routed to the reference divider, R. R (a 14-bit counter) can be set to any value from 0 to 16383 by writing to Register 0x011 and Register 0x012. (Both R = 0 and R = 1 give divide-by-1.) The output of the R divider goes to one of the PFD inputs to be compared to the VCO frequency divided by the N divider. The frequency applied to the PFD must not exceed the maximum allowable frequency, which depends on the antibacklash pulse setting (see Table 2).

The R counter has its own reset. R counter can be reset using the shared reset bit of the R, A, and B counters. It can also be reset by a SYNC operation.

VCO/VCO Feedback Divider N—P, A, B, R

The N divider is a combination of a prescaler (P) and two counters, A and B. The total divider value is

$$N = (P \times B) + A$$

where the value of P can be 2, 4, 8, 16, or 32.

Prescaler

The prescaler of the AD9516 allows for two modes of operation: a fixed divide (FD) mode of 1, 2, or 3, and dual modulus (DM) mode where the prescaler divides by P and (P + 1) {2 and 3, 4 and 5, 8 and 9, 16 and 17, or 32 and 33}. The prescaler modes of operation are given in Table 54, Register 0x016[2:0]. Not all modes are available at all frequencies (see Table 2).

When operating the AD9516 in dual modulus mode (P/(P + 1)), the equation used to relate input reference frequency to VCO output frequency is

$$f_{VCO} = (f_{REF}/R) \times (P \times B + A) = f_{REF} \times N/R$$

However, when operating the prescaler in FD mode, 1, 2, or 3, the A counter is not used (A = 0) and the equation simplifies to

$$f_{VCO} = (f_{REF}/R) \times (P \times B) = f_{REF} \times N/R$$

When A = 0, the divide is a fixed divide of P = 2, 4, 8, 16, or 32, in which case the previous equation also applies.

By using combinations of DM and FD modes, the AD9516 can achieve values of N all the way down to $N = 1$ and up to $N = 26,2175$. Table 28 shows how a 10 MHz reference input can be locked to any integer multiple of N.

Note that the same value of N can be derived in different ways, as illustrated by the case of $N = 12$. The user can choose a fixed divide mode of $P = 2$ with $B = 6$; use the dual modulus mode of $2/3$ with $A = 0$, $B = 6$; or use the dual modulus mode of $4/5$ with $A = 0$, $B = 3$.

The maximum frequency into the prescaler in $2/3$ dual-modulus mode is limited to 200 MHz. There are only two cases where this frequency limitation limits the flexibility of that N divider: $N = 7$ and $N = 11$. In these two cases, the maximum frequency into the prescaler is 300 MHz and is achieved by using the $P = 1$ FD mode. In all other cases, the user can achieve the desired N divider value by using the other prescaler modes.

A and B Counters

The B counter must be ≥ 3 or bypassed, and, unlike the R counter, $A = 0$ is actually zero.

When the prescaler is in dual modulus mode, the A counter must be less than the B counter.

The maximum input frequency to the A/B counter is reflected in the maximum prescaler output frequency (~300 MHz) that is specified in Table 2. This is the prescaler input frequency (VCO or

CLK) divided by P. For example, a dual modulus mode of $P = 8/9$ is not allowed if the VCO frequency is greater than 2400 MHz because the frequency going to the A/B counter is too high.

When the AD9516 B counter is bypassed ($B = 1$), the A counter should be set to 0, and the overall resulting divide is equal to the prescaler setting, P. The possible divide ratios in this mode are 1, 2, 3, 4, 8, 16, and 32. This mode is useful only when an external VCO/VCXO is used because the frequency range of the internal VCO requires an overall feedback divider greater than 32.

Although manual reset is not normally required, the A/B counters have their own reset bit. Alternatively, the A and B counters can be reset using the shared reset bit of the R, A, and B counters. Note that these reset bits are not self-clearing.

R, A, and B Counters—SYNC Pin Reset

The R, A and B counters can also be reset simultaneously through the SYNC pin. This function is controlled by Register 0x019[7:6] (see Table 54). The SYNC pin reset is disabled by default.

R and N Divider Delays

Both the R and N dividers feature a programmable delay cell. These delays can be enabled to allow adjustment of the phase relationship between the PLL reference clock and the VCO or CLK. Each delay is controlled by three bits. The total delay range is about 1 ns. See Register 0x019 in Table 54.

Table 28. Using a 10 MHz Reference Input to Generate Different VCO Frequencies

| f_{REF} (MHz) | R | P | A | B | N | f_{VCO} (MHz) | Mode | Comments/Conditions |
|--------------------|---|---|---|---|----|--------------------|------|--|
| 10 | 1 | 1 | X | 1 | 1 | 10 | FD | $P = 1$, $B = 1$ (A and B counters are bypassed). |
| 10 | 1 | 2 | X | 1 | 2 | 20 | FD | $P = 2$, $B = 1$ (A and B counters are bypassed). |
| 10 | 1 | 1 | X | 3 | 3 | 30 | FD | A counter is bypassed. |
| 10 | 1 | 1 | X | 4 | 4 | 40 | FD | A counter is bypassed. |
| 10 | 1 | 1 | X | 5 | 5 | 50 | FD | A counter is bypassed. |
| 10 | 1 | 2 | X | 3 | 6 | 60 | FD | A counter is bypassed. |
| 10 | 1 | 2 | 0 | 3 | 6 | 60 | DM | |
| 10 | 1 | 2 | 1 | 3 | 7 | 70 | DM | Maximum frequency into prescaler in $P = 2/3$ mode is 200 MHz. If $N = 7$ or $N = 11$ is desired for prescaler input frequency of 200 MHz to 300 MHz, use $P = 1$, and $N = 7$ or 11, respectively. |
| 10 | 1 | 2 | 2 | 3 | 8 | 80 | DM | |
| 10 | 1 | 2 | 1 | 4 | 9 | 90 | DM | |
| 10 | 1 | 2 | X | 5 | 10 | 100 | FD | |
| 10 | 1 | 2 | 0 | 5 | 10 | 100 | DM | |
| 10 | 1 | 2 | 1 | 5 | 11 | 110 | DM | |
| 10 | 1 | 2 | X | 6 | 12 | 120 | FD | |
| 10 | 1 | 2 | 0 | 6 | 12 | 120 | DM | |
| 10 | 1 | 4 | 0 | 3 | 12 | 120 | DM | $P = 8$ is not allowed ($2700 \div 8 > 300$ MHz). $P = 32$ is not allowed ($A > B$ not allowed). |
| 10 | 1 | 4 | 1 | 3 | 13 | 130 | DM | $P = 32$, $A = 22$, $B = 84$. $P = 16$ is also permitted. |

DIGITAL LOCK DETECT (DLD)

By selecting the proper output through the mux on each pin, the DLD function can be made available at the LD, STATUS, and REFMON pins. The DLD circuit indicates a lock when the time difference of the rising edges at the PFD inputs is less than a specified value (the lock threshold). The loss of a lock is indicated when the time difference exceeds a specified value (the unlock threshold). Note that the unlock threshold is wider than the lock threshold, which allows some phase error in excess of the lock window to occur without chattering on the lock indicator.

The lock detect window timing depends on three settings: the digital lock detect window bit (Register 0x018[4]), the anti-backlash pulse width setting (Register 0x017[1:0], see Table 2), and the lock detect counter (Register 0x018[6:5]). A lock is not indicated until there is a programmable number of consecutive PFD cycles with a time difference that is less than the lock detect threshold. The lock detect circuit continues to indicate a lock until a time difference greater than the unlock threshold occurs on a single subsequent cycle. For the lock detect to work properly, the period of the PFD frequency must be greater than the unlock threshold. The number of consecutive PFD cycles required for lock is programmable (Register 0x018[6:5]).

Analog Lock Detect (ALD)

The AD9516 provides an ALD function that can be selected for use at the LD pin. There are two versions of ALD, as follows:

- N-channel open-drain lock detect. This signal requires a pull-up resistor to positive supply, VS. The output is normally high with short, low going pulses. Lock is indicated by the minimum duty cycle of the low-going pulses.
- P-channel open-drain lock detect. This signal requires a pull-down resistor to GND. The output is normally low with short, high going pulses. Lock is indicated by the minimum duty cycle of the high-going pulses.

The analog lock detect function requires an R-C filter to provide a logic level indicating lock/unlock.

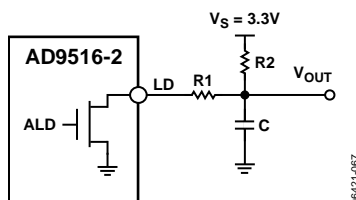


Figure 50. Example of Analog Lock Detect Filter, Using N-Channel Open-Drain Driver

Current Source Digital Lock Detect (DLD)

During the PLL locking sequence, it is normal for the DLD signal to toggle a number of times before remaining steady when the PLL is completely locked and stable. There may be applications where it is desirable to have DLD asserted only after the PLL is solidly locked. This is made possible by using the current source lock detect function. This function is set

when it is selected as the output from the LD pin control (Register 0x01A[5:0]).

The current source lock detect provides a current of 110 μ A when DLD is true, and it shorts to ground when DLD is false. If a capacitor is connected to the LD pin, it charges at a rate that is determined by the current source during the DLD true time but is discharged nearly instantly when DLD is false. By monitoring the voltage at the LD pin (top of the capacitor), it is possible to get a logic high level only after the DLD has been true for a sufficiently long time. Any momentary DLD false resets the charging. By selecting a properly sized capacitor, it is possible to delay a lock detect indication until the PLL is stably locked, and the lock detect does not chatter.

The voltage on the capacitor can be sensed by an external comparator connected to the LD pin. However, there is an internal LD pin comparator that can be read at the REFMON pin control (Register 0x01B[4:0]) or the STATUS pin control (Register 0x017[7:2]) as an active high signal. It is also available as an active low signal (REFMON, Register 0x01B[4:0] and STATUS, Register 0x017[7:2]). The internal LD pin comparator trip point and hysteresis are listed in Table 16.

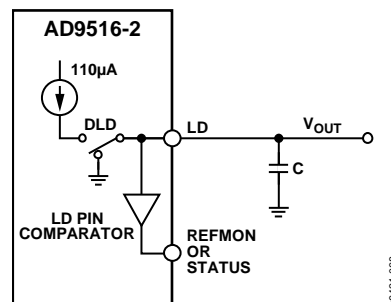


Figure 51. Current Source Lock Detect

External VCXO/VCO Clock Input (CLK/CLK)

CLK is a differential input that can be used as an input to drive the AD9516 clock distribution section. This input can receive up to 2.4 GHz. The pins are internally self-biased and the input signal should be ac-coupled via capacitors.

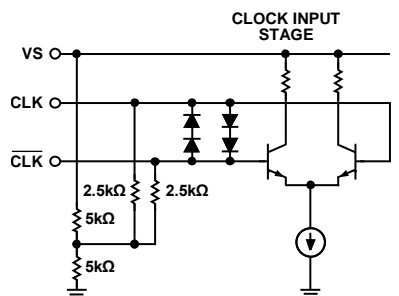


Figure 52. CLK Equivalent Input Circuit

The CLK/CLK input can be used either as a distribution only input (with the PLL off), or as a feedback input for an external VCO/VCXO using the internal PLL, when the internal VCO is not used. The CLK/CLK input can be used for frequencies up to 2.4 GHz.

Holdover

The AD9516 PLL has a holdover function. Holdover is implemented by putting the charge pump into a state of high impedance. This is useful when the PLL reference clock is lost. Holdover mode allows the VCO to maintain a relatively constant frequency even though there is no reference clock. Without this function, the charge pump is placed into a constant pump-up or pump-down state resulting in a massive VCO frequency shift. Because the charge pump is placed in a high impedance state, any leakage that occurs at the charge pump output or the VCO tuning node causes a drift of the VCO frequency. This can be mitigated by using a loop filter that contains a large capacitive component because this drift is limited by the current leakage induced slew rate (I_{LEAK}/C) of the VCO control voltage. For most applications, the frequency accuracy is sufficient for 3 sec to 5 sec.

Both a manual holdover, using the $\overline{\text{SYNC}}$ pin, and an automatic holdover mode are provided. To use either function, the holdover function must be enabled (Register 0x01D[0] and Register 0x01D[2]).

Note that the VCO cannot be calibrated with the holdover enabled because the holdover resets the N divider during calibration, which prevents proper calibration. Disable holdover before issuing a VCO calibration.

Manual Holdover Mode

A manual holdover mode can be enabled that allows the user to place the charge pump into a high impedance state when the $\overline{\text{SYNC}}$ pin is asserted low. This operation is edge sensitive, not level sensitive. The charge pump enters a high impedance state immediately. To take the charge pump out of a high impedance state take the $\overline{\text{SYNC}}$ pin high. The charge pump then leaves high impedance state synchronously with the next PFD rising edge from the reference clock. This prevents extraneous charge pump events from occurring during the time between $\overline{\text{SYNC}}$ going high and the next PFD event. This also means that the charge pump stays in a high impedance state as long as there is no reference clock present.

The B-counter (in the N divider) is reset synchronously with the charge pump leaving the high impedance state on the reference path PFD event. This helps align the edges out of the R and N dividers for faster settling of the PLL. Because the prescaler is not reset, this feature works best when the B and R numbers are close because this results in a smaller phase difference for the loop to settle out.

When using this mode, set the channel dividers to ignore the $\overline{\text{SYNC}}$ pin (at least after an initial $\overline{\text{SYNC}}$ event). If the dividers are not set to ignore the $\overline{\text{SYNC}}$ pin, the distribution outputs turn off each time $\overline{\text{SYNC}}$ is taken low to put the part into holdover.

Automatic/Internal Holdover Mode

When enabled, this function automatically puts the charge pump into a high impedance state when the loop loses lock. The assumption is that the only reason the loop loses lock is due to the PLL losing the reference clock; therefore, the holdover function puts the charge pump into a high impedance state to maintain the VCO frequency as close as possible to the original frequency before the reference clock disappears.

See Figure 53 for a flowchart of the internal/automatic holdover function operation.

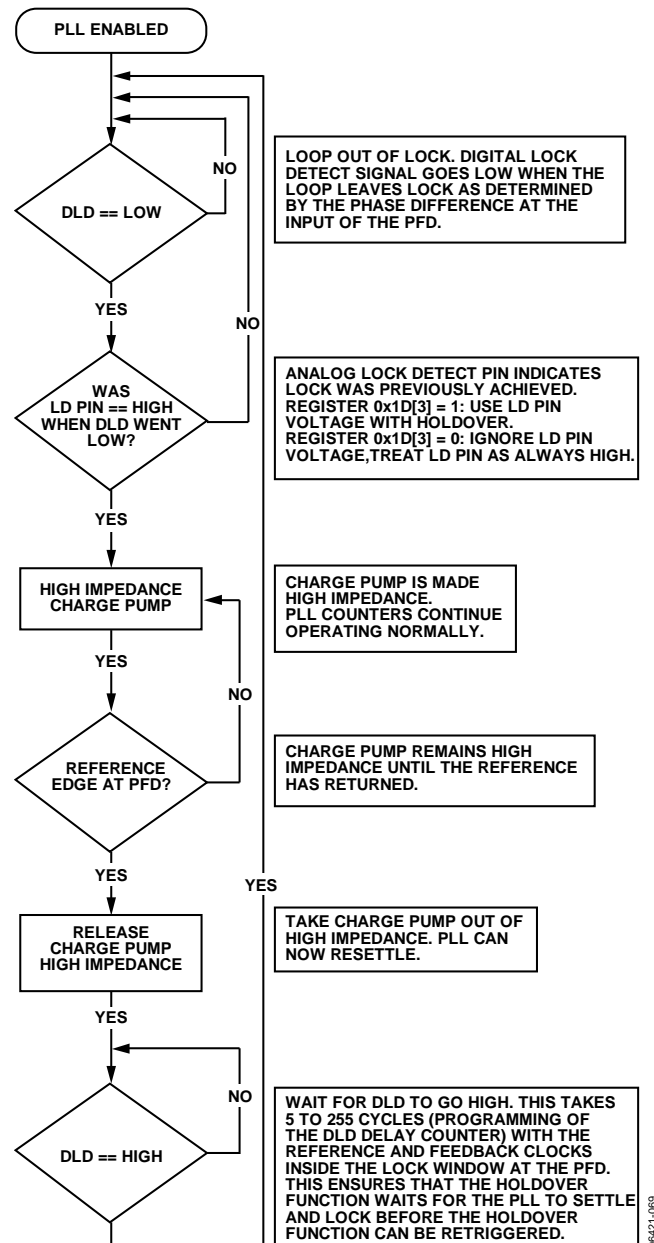


Figure 53. Flowchart of Automatic/Internal Holdover Mode

The holdover function senses the logic level of the LD pin as a condition to enter holdover. The signal at LD can be from the DLD, ALD, or current source LD mode. It is possible to disable the LD comparator (Register 0x01D[3]), which causes the holdover function to always sense LD as high. If DLD is used, it is possible for the DLD signal to chatter some while the PLL is reacquiring lock. The holdover function may retrigger, thereby preventing the holdover mode from ever terminating. Use of the current source lock detect mode is recommended to avoid this situation (see the Current Source Digital Lock Detect section).

Once in holdover mode, the charge pump stays in a high impedance state as long as there is no reference clock present.

As in the external holdover mode, the B counter (in the N divider) is reset synchronously with the charge pump leaving the high impedance state on the reference path PFD event. This helps align the edges out of the R and N dividers for faster settling of the PLL and to reduce frequency errors during settling. Because the prescaler is not reset, this feature works best when the B and R numbers are close because this results in a smaller phase difference for the loop to settle out.

After leaving holdover, the loop then reacquires lock and the LD pin must charge (if Register 0x01D[3] = 1) before it can re-enter holdover (CP high impedance).

The holdover function always responds to the state of the currently selected reference (Register 0x01C). If the loop loses lock during a reference switchover (see the Reference Switchover section), holdover is triggered briefly until the next reference clock edge at the PFD.

The following registers affect the internal/automatic holdover function:

- Register 0x018[6:5], lock detect counter. These bits change the number of consecutive PFD cycles with edges inside the lock detect window that are required for the DLD indicator to indicate lock. This impacts the time required before the LD pin can begin to charge as well as the delay from the end of a holdover event until the holdover function can be reengaged.
- Register 0x018[3], disable digital lock detect. This bit must be set to a 0 to enable the DLD circuit. Internal/automatic holdover does not operate correctly without the DLD function enabled.
- Register 0x01A[5:0], lock detect pin output select. Set these bits to 000100b for the current source lock detect mode if using the LD pin comparator. Load the LD pin with a capacitor of an appropriate value.
- Register 0x01D[3], enable LD pin comparator. 1 = enable, 0 = disable. When disabled, the holdover function always senses the LD pin as high.
- Register 0x01D[1], enable external holdover control.
- Register 0x01D[0] and Register 0x01D[2], holdover function enable. If holdover is disabled, both external and internal/automatic holdover are disabled.

For example, to use automatic holdover with the following:

- Automatic reference switchover, prefer REF1
- Digital lock detect: five PFD cycles, high range window
- Automatic holdover using the LD pin comparator

Set the following registers (in addition to the normal PLL registers):

- Register 0x018[6:5] = 00b; lock detect counter = five cycles.
- Register 0x018[4] = 0b; lock detect window = high range.
- Register 0x018[3] = 0b; DLD normal operation.
- Register 0x01A[5:0] = 000100b; current source lock detect mode.
- Register 0x01B[7:0] = 0xF7; set REFMON pin to status of REF1 (active low).
- Register 0x01C[2:1] = 11b; enable REF1 and REF2 input buffers.
- Register 0x01D[3] = 1b; enable LD pin comparator.
- Register 0x01D[2] = 1b; enable the holdover function.
- Register 0x01D[1] = 0b; use internal/automatic holdover mode.
- Register 0x01D[0] = 1b; enable the holdover function. (VCO calibration must be complete before this bit is enabled.)
- Connect REFMON pin to REFSEL pin.

Frequency Status Monitors

The AD9516 contains three frequency status monitors that are used to indicate if the PLL reference (or references in the case of single-ended mode) and the VCO have fallen below a threshold frequency. A diagram showing their location in the PLL is shown in Figure 54.

The PLL reference frequency monitors have two threshold frequencies: normal and extended (see Table 16). The reference frequency monitor thresholds are selected in Register 0x01B[7:5]. Frequency monitor status can be found in Register 0x01F[3:1].

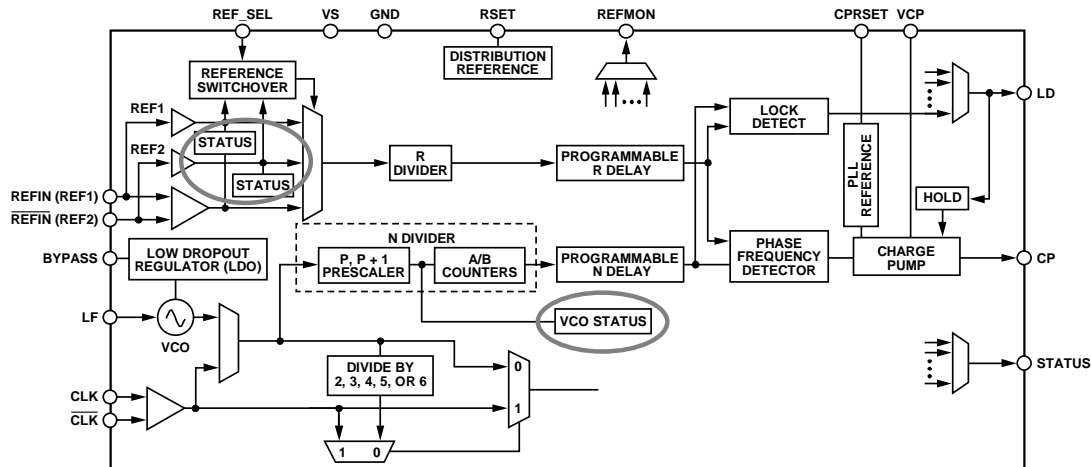


Figure 54. Reference and VCO Status Monitors

VCO Calibration

The AD9516 on-chip VCO must be calibrated to ensure proper operation over process and temperature. The VCO calibration is controlled by a calibration controller running off of a divided REFIN clock. The calibration requires that the PLL be set up properly to lock the PLL loop and that the REFIN clock be present. During the first initialization after a power-up or a reset of the AD9516, a VCO calibration sequence is initiated by setting Register 0x018[0] = 1b. This can be done as part of the initial setup, before executing update registers (Register 0x232[0] = 1b). Subsequent to the initial setup, a VCO calibration sequence is initiated by resetting Register 0x018[0] = 0b, executing an update registers operation, setting Register 0x018[0] = 1b, and executing another update registers operation. A readback bit, Bit 6 in Register 0x01F, indicates when a VCO calibration is finished by returning a logic true (that is, 1b).

The sequence of operations for the VCO calibration is as follows:

- Program the PLL registers to the proper values for the PLL loop. Note that that automatic holdover mode must be disabled, and the VCO divider must not be set to “Static.”
- Ensure that the input reference signal is present.
- For the initial setting of the registers after a power-up or reset, initiate VCO calibration by setting Register 0x018[0] = 1b. Subsequently, whenever a calibration is desired, set Register 0x018[0] = 0b, update registers; and then set Register 0x018[0] = 1b, update registers.
- A SYNC operation is initiated internally, causing the outputs to go to a static state determined by normal SYNC function operation.
- VCO calibrates to the desired setting for the requested VCO frequency.
- Internally, the SYNC signal is released, allowing outputs to continue clocking.
- PLL loop is closed.
- PLL locks.

A sync is executed during the VCO calibration; therefore, the outputs of the AD9516 are held static during the calibration, which prevents unwanted frequencies from being produced. However, at the end of a VCO calibration, the outputs may resume clocking before the PLL loop is completely settled.

The VCO calibration clock divider is set as shown in Table 54 (Register 0x018[2:1]).

The calibration divider divides the PFD frequency (reference frequency divided by R) down to the calibration clock. The calibration occurs at the PFD frequency divided by the calibration divider setting. Lower VCO calibration clock frequencies result in longer times for a calibration to be completed.

The VCO calibration clock frequency is given by

$$f_{\text{CAL_CLOCK}} = f_{\text{REFIN}} / (R \times \text{cal_div})$$

where:

f_{REFIN} is the frequency of the REFIN signal.

R is the value of the R divider.

cal_div is the division set for the VCO calibration divider (Register 0x018[2:1]).

The VCO calibration takes 4400 calibration clock cycles. Therefore, the VCO calibration time in PLL reference clock cycles is given by

$$\text{Time to Calibrate VCO} =$$

$$4400 \times R \times \text{cal_div PLL Reference Clock Cycles}$$

Table 29. Example Time to Complete a VCO Calibration with Different f_{REFIN} Frequencies

| f_{REFIN} (MHz) | R Divider | PFD | Time to Calibrate VCO |
|--------------------------|-----------|---------|-----------------------|
| 100 | 1 | 100 MHz | 88 μ s |
| 10 | 10 | 1 MHz | 8.8 ms |
| 10 | 100 | 100 kHz | 88 ms |

VCO calibration must be manually initiated. This allows for flexibility in deciding what order to program registers and when to initiate a calibration, instead of having it happen every time certain PLL registers have their values change. For example, this allows for the VCO frequency to be changed by small amounts without having an automatic calibration occur each time; this should be done with caution and only when the user knows that the VCO control voltage is not going to exceed the nominal best performance limits. For example, a few 100 kHz steps are fine, but a few MHz might not be). In addition, because the calibration procedure results in rapid changes in the VCO frequency, the distribution section is automatically placed in SYNC until the calibration is finished. Therefore, this temporary loss of outputs must be expected.

A VCO calibration should be initiated under the following conditions:

- After changing any of the PLL R, P, B, and A divider settings, or after a change in the PLL reference clock frequency. This, in effect, means any time a PLL register or reference clock is changed such that a different VCO frequency results.
- Whenever system calibration is desired. The VCO is designed to operate properly over extremes of temperatures even when first calibrated at the opposite extreme. However, a VCO calibration can be initiated at any time, if desired.

CLOCK DISTRIBUTION

A clock channel consists of a pair (or double pair, in the case of CMOS) of outputs that share a common divider. A clock output consists of the drivers that connect to the output pins. The clock outputs have either LVPECL or LVDS/CMOS signal levels at the pins.

The AD9516 has five clock channels: three channels are LVPECL (six outputs); two channels are LVDS/CMOS (up to four LVDS outputs, or up to eight CMOS outputs).

Each channel has its own programmable divider that divides the clock frequency that is applied to its input. The LVPECL channel dividers can divide by any integer from 2 to 32, or the divider can be bypassed to achieve a divide by one. Each LVDS/CMOS channel divider contains two of these divider blocks in a cascaded configuration. The total division of the channel is the product of the divide value of the cascaded dividers. This allows divide values of $(1 \text{ to } 32) \times (1 \text{ to } 32)$, or up to 1024 (note that this is not all values from 1 to 1024 but only the set of numbers that are the product of the two dividers).

Because the internal VCO frequency is above the maximum channel divider input frequency (1600 MHz), the VCO divider must be used after the on-chip VCO. The VCO divider can be set to divide by 2, 3, 4, 5, or 6. External clock signals connected to the CLK input also require the VCO divider if the frequency of the signal is greater than 1600 MHz.

The channel dividers allow for a selection of various duty cycles, depending on the currently set division. That is, for any specific division, D , the output of the divider can be set to high for $N + 1$ input clock cycles and low for $M + 1$ input clock cycles (where $D = N + M + 2$). For example, a divide-by-5 can be high for one divider input cycle and low for four cycles, or a divide-by-5 can be high for three divider input cycles and low for two cycles. Other combinations are also possible.

The channel dividers include a duty-cycle correction function, that can be disabled. In contrast to the selectable duty cycle just described, this function can correct a non-50% duty cycle caused by an odd division. However, this requires that the division be set by $M = N + 1$.

In addition, the channel dividers allow a coarse phase offset or delay to be set. Depending on the division selected, the output can be delayed by up to 31 input clock cycles. The divider outputs can also be set to start high or start low.

Internal VCO or External CLK as Clock Source

The clock distribution of the AD9516 has two clock input sources: an internal VCO or an external clock connected to the CLK/CLK pins. Either the internal VCO or CLK must be chosen as the source of the clock signal to distribute. When the internal VCO is selected as the source, the VCO divider must be used. When CLK is selected as the source, it is not necessary to use the VCO divider if the CLK frequency is less than the maximum channel divider input frequency (1600 MHz); otherwise, the VCO divider must be used to reduce the frequency to one acceptable by the channel dividers. Table 30 shows how the VCO, CLK, and VCO divider are selected. Register 0x1E1[1:0] selects the channel divider source and determines whether the VCO divider is used. It is not possible to select the VCO without using the VCO divider.

Table 30. Selecting VCO or CLK as Source for Channel Divider, and Whether VCO Divider Is Used

| Register 0x1E1 | | Channel Divider Source | VCO Divider |
|----------------|-------|------------------------|-------------|
| Bit 1 | Bit 0 | | |
| 0 | 0 | CLK | Used |
| 0 | 1 | CLK | Not used |
| 1 | 0 | VCO | Used |
| 1 | 1 | Not allowed | Not allowed |

CLK or VCO Direct to LVPECL Outputs

It is possible to connect either the internal VCO or the CLK (whichever is selected as the input to the VCO divider) directly to the LVPECL outputs, OUT0 to OUT5. This configuration can pass frequencies up to the maximum frequency of the VCO directly to the LVPECL outputs. The LVPECL outputs may not be able to provide full voltage swing at the highest frequencies.

To connect the LVPECL outputs directly to the internal VCO or CLK, the VCO divider must be selected as the source to the distribution section, even if no channel uses it.

Either the internal VCO or the CLK can be selected as the source for the direct to output routing.

Table 31. Settings for Routing VCO Divider Input Directly to LVPECL Outputs

| Register Setting | Selection |
|------------------|---|
| 0x1E1[1:0] = 00b | CLK is the source; VCO divider selected |
| 0x1E1[1:0] = 10b | VCO is the source; VCO divider selected |
| 0x192[1] = 1b | Direct to output OUT0, OUT1 |
| 0x195[1] = 1b | Direct to output OUT2, OUT3 |
| 0x198[1] = 1b | Direct to output OUT4, OUT5 |

Clock Frequency Division

The total frequency division is a combination of the VCO divider (when used) and the channel divider. When the VCO divider is used, the total division from the VCO or CLK to the output is the product of the VCO divider (2, 3, 4, 5, 6) and the division of the channel divider. Table 32 and Table 33 indicate how the frequency division for a channel is set. For the LVPECL outputs, there is only one divider per channel. For the LVDS/CMOS outputs, there are two dividers (X.1, X.2) cascaded per channel.

Table 32. Frequency Division for Divider 0 to Divider 2

| CLK or VCO Selected | VCO Divider | Channel Divider | Direct to Output | Frequency Division |
|---------------------|-------------|-----------------|------------------|----------------------|
| CLK/VCO | 2 to 6 | 1 (bypassed) | Yes | 1 |
| CLK/VCO | 2 to 6 | 1 (bypassed) | No | (2 to 6) × (1) |
| CLK/VCO | 2 to 6 | 2 to 32 | No | (2 to 6) × (2 to 32) |
| CLK | Not used | 1 (bypassed) | No | 1 |
| CLK | Not used | 2 to 32 | No | 2 to 32 |

Table 33. Frequency Division for Divider 3 and Divider 4

| CLK or VCO Selected | VCO Divider | Channel Divider | | Frequency Division |
|---------------------|-------------|-----------------|--------------|----------------------------------|
| | | X.1 | X.2 | |
| CLK/VCO | 2 to 6 | 1 (bypassed) | 1 (bypassed) | (2 to 6) × (1) × (1) |
| CLK/VCO | 2 to 6 | 2 to 32 | 1 (bypassed) | (2 to 6) × (2 to 32) × (1) |
| CLK/VCO | 2 to 6 | 2 to 32 | 2 to 32 | (2 to 6) × (2 to 32) × (2 to 32) |
| CLK | Not used | 1 | 1 | 1 |
| CLK | Not used | 2 to 32 | 1 | (2 to 32) × (1) |
| CLK | Not used | 2 to 32 | 2 to 32 | 2 to 32 × (2 to 32) |

The channel dividers feeding the LVPECL output drivers contain one 2-to-32 frequency divider. This divider provides for division by 2 to 32. Division by 1 is accomplished by bypassing the divider. The dividers also provide for a programmable duty cycle, with optional duty-cycle correction when the divide ratio is odd. A phase offset or delay in increments of the input clock cycle is selectable. The channel dividers operate with a signal at their inputs up to 1600 MHz. The features and settings of the dividers are selected by programming the appropriate setup and control registers (see Table 52 through Table 62).

VCO Divider

The VCO divider provides frequency division between the internal VCO or the external CLK input and the clock distribution channel dividers. The VCO divider can be set to divide by 2, 3, 4, 5, or 6 (see Table 60, Register 0x1E0[2:0]).

Channel Dividers—LVPECL Outputs

Each pair of LVPECL outputs is driven by a channel divider. There are three channel dividers (0, 1, and 2) driving a total of six LVPECL outputs (OUT0 to OUT5). Table 34 lists the register locations used for setting the division and other functions of these dividers. The division is set by the values of M and N. The divider can be bypassed (equivalent to divide-by-1, divider circuit is powered down) by setting the bypass bit. The duty-cycle correction can be enabled or disabled according to the setting of the DCCOFF bits.

Table 34. Setting D_x for Divider 0, Divider 1, and Divider 2¹

| Divider | Low Cycles M | High Cycles N | Bypass | DCCOFF |
|---------|--------------|---------------|----------|----------|
| 0 | 0x190[7:4] | 0x190[3:0] | 0x191[7] | 0x192[0] |
| 1 | 0x193[7:4] | 0x193[3:0] | 0x194[7] | 0x195[0] |
| 2 | 0x196[7:4] | 0x196[3:0] | 0x197[7] | 0x198[0] |

¹ Note that the value stored in the register = # of cycles minus 1.

Channel Frequency Division (0, 1, and 2)

For each channel (where the channel number is x: 0, 1, or 2), the frequency division, D_x, is set by the values of M and N (four bits each, representing Decimal 0 to Decimal 15), where

$$\text{Number of Low Cycles} = M + 1$$

$$\text{Number of High Cycles} = N + 1$$

The cycles are cycles of the clock signal currently routed to the input of the channel dividers (VCO divider out or CLK).

When a divider is bypassed, D_x = 1.

Otherwise, D_x = (N + 1) + (M + 1) = N + M + 2. This allows each channel divider to divide by any integer from 2 to 32.

Duty Cycle and Duty-Cycle Correction (0, 1, and 2)

The duty cycle of the clock signal at the output of a channel is a result of some or all of the following conditions:

- What are the M and N values for the channel?
- Is the DCC enabled?
- Is the VCO divider used?
- What is the CLK input duty cycle? (The internal VCO has a 50% duty cycle.)

The DCC function is enabled by default for each channel divider. However, the DCC function can be disabled individually for each channel divider by setting the DCCOFF bit for that channel.

Certain M and N values for a channel divider result in a non-50% duty cycle. A non-50% duty cycle can also result with an even division, if $M \neq N$. The duty-cycle correction function automatically corrects non-50% duty cycles at the channel divider output to 50% duty cycle. Duty-cycle correction requires the following channel divider conditions:

- An even division must be set as $M = N$
- An odd division must be set as $M = N + 1$

When not bypassed or corrected by the DCC function, the duty cycle of each channel divider output is the numerical value of $(N + 1)/(N + M + 2)$, expressed as a percentage (%).

The duty cycle at the output of the channel divider for various configurations is shown in Table 35 to Table 37.

Table 35. Duty Cycle with VCO Divider, Input Duty Cycle Is 50%

| VCO Divider | D _x N + M + 2 | Output Duty Cycle | |
|-------------|-----------------------------|-----------------------|---------------------------|
| | | DCCOFF = 1 | DCCOFF = 0 |
| Even | 1 (divider bypassed) | 50% | 50% |
| Odd = 3 | 1 (divider bypassed) | 33.3% | 50% |
| Odd = 5 | 1 (divider bypassed) | 40% | 50% |
| Even, Odd | Even | $(N + 1)/(N + M + 2)$ | 50%; requires $M = N$ |
| Even, Odd | Odd | $(N + 1)/(N + M + 2)$ | 50%; requires $M = N + 1$ |

Table 36. Duty Cycle with VCO Divider, Input Duty Cycle Is X%

| VCO Divider | D _x N + M + 2 | Output Duty Cycle | |
|-------------|-----------------------------|-----------------------|--|
| | | DCCOFF = 1 | DCCOFF = 0 |
| Even | 1 (divider bypassed) | 50% | 50% |
| Odd = 3 | 1 (divider bypassed) | 33.3% | $(1 + X\%)/3$ |
| Odd = 5 | 1 (divider bypassed) | 40% | $(2 + X\%)/5$ |
| Even | Even | $(N + 1)/(N + M + 2)$ | 50%, requires $M = N$ |
| | Odd | $(N + 1)/(N + M + 2)$ | 50%, requires $M = N + 1$ |
| Odd = 3 | Even | $(N + 1)/(N + M + 2)$ | 50%, requires $M = N$ |
| Odd = 3 | Odd | $(N + 1)/(N + M + 2)$ | $(3N + 4 + X\%)/(6N + 9)$, requires $M = N + 1$ |
| Odd = 5 | Even | $(N + 1)/(N + M + 2)$ | 50%, requires $M = N$ |
| Odd = 5 | Odd | $(N + 1)/(N + M + 2)$ | $(5N + 7 + X\%)/(10N + 15)$, requires $M = N + 1$ |

Table 37. Channel Divider Output Duty Cycle When the VCO Divider Is Not Used

| Input Clock Duty Cycle | D _x N + M + 2 | Output Duty Cycle | |
|------------------------|-----------------------------|-----------------------|---|
| | | DCCOFF = 1 | DCCOFF = 0 |
| Any | 1 | 1 (divider bypassed) | Same as input duty cycle |
| Any | Even | $(N + 1)/(M + N + 2)$ | 50%, requires $M = N$ |
| 50% | Odd | $(N + 1)/(M + N + 2)$ | 50%, requires $M = N + 1$ |
| X% | Odd | $(N + 1)/(M + N + 2)$ | $(N + 1 + X\%)/(2 \times N + 3)$, requires $M = N + 1$ |

The internal VCO has a duty cycle of 50%. Therefore, when the VCO is connected directly to the output, the duty cycle is 50%. If the CLK input is routed directly to the output, the duty cycle of the output is the same as the CLK input.

Phase Offset or Coarse Time Delay (0, 1, and 2)

Each channel divider allows for a phase offset, or a coarse time delay, to be programmed by setting register bits (see Table 38). These settings determine the number of cycles (successive rising edges) of the channel divider input frequency by which to offset or delay the rising edge of the output of the divider. This delay is with respect to a nondelayed output (that is, with a phase offset of zero). The amount of the delay is set by five bits loaded into the phase offset (PO) register, plus the start high (SH) bit for each channel divider. When the start high bit is set, the delay is also affected by the number of low cycles (M) that are programmed for the divider.

The SYNC function must be used to make phase offsets effective (see the Synchronizing the Outputs—SYNC Function section).

Table 38. Setting Phase Offset and Division for Divider 0, Divider 1, and Divider 2

| Divider | Start High (SH) | Phase Offset (PO) | Low Cycles (M) | High Cycles (N) |
|---------|-----------------|-------------------|----------------|-----------------|
| 0 | 0x191[4] | 0x191[3:0] | 0x190[7:4] | 0x190[3:0] |
| 1 | 0x194[4] | 0x194[3:0] | 0x193[7:4] | 0x193[3:0] |
| 2 | 0x197[4] | 0x197[3:0] | 0x196[7:4] | 0x196[3:0] |

Let

Δt = delay (in seconds).

Δc = delay (in cycles of clock signal at input to D_X).

T_X = period of the clock signal at the input of the divider, D_X (in seconds).

$\Phi = 16 \times SH[4] + 8 \times PO[3] + 4 \times PO[2] + 2 \times PO[1] + 1 \times PO[0]$

The channel divide-by is set as N = high cycles, and M = low cycles.

Case 1

For $\Phi \leq 15$:

$\Delta t = \Phi \times T_X$

$\Delta c = \Delta t / T_X = \Phi$

Case 2

For $\Phi \geq 16$:

$\Delta t = (\Phi - 16 + M + 1) \times T_X$

$\Delta c = \Delta t / T_X$

By giving each divider a different phase offset, output-to-output delays can be set in increments of the channel divider input clock cycle. Figure 55 shows the results of setting such a coarse offset between outputs.

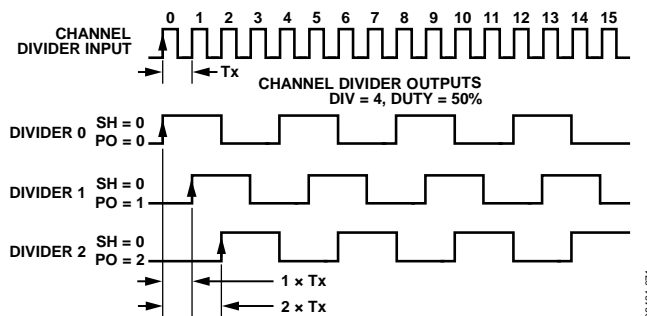


Figure 55. Effect of Coarse Phase Offset (or Delay)

Channel Dividers—LVDS/CMOS Outputs

Channel Divider 3 and Channel Divider 4 each drive a pair of LVDS outputs, giving a total of four LVDS outputs (OUT6 to OUT9). Alternatively, each of these LVDS differential outputs can be configured individually as a pair (A and B) of CMOS single-ended outputs, providing for up to eight CMOS outputs. By default, the B output of each pair is off but can be turned on as desired.

Channel Divider 3 and Channel Divider 4 each consist of two cascaded, 2 to 32, frequency dividers. The channel frequency division is $D_{X,1} \times D_{X,2}$ or up to 1024. Divide-by-1 is achieved by bypassing one or both of these dividers. Both of the dividers also have DCC enabled by default, but this function can be disabled, if desired, by setting the DCCOFF bit of the channel. A coarse phase offset or delay is also programmable (see the Phase Offset or Coarse Time Delay (Divider 3 and Divider 4) section). The channel dividers operate up to 1600 MHz. The features and settings of the dividers are selected by programming the appropriate setup and control registers (see Table 52 and Table 53 through Table 62).

Table 39. Setting Division (D_X) for Divider 3, Divider 4¹

| Divider | | M | N | Bypass | DCCOFF |
|---------|-----|------------|------------|----------|----------|
| 3 | 3.1 | 0x199[7:4] | 0x199[3:0] | 0x19C[4] | 0x19D[0] |
| | 3.2 | 0x19B[7:4] | 0x19B[3:0] | 0x19C[5] | 0x19D[0] |
| 4 | 4.1 | 0x19E[7:4] | 0x19E[3:0] | 0x1A1[4] | 0x1A2[0] |
| | 4.2 | 0x1A0[7:4] | 0x1A0[3:0] | 0x1A1[5] | 0x1A2[0] |

¹ Note that the value stored in the register = # of cycles minus 1.

Channel Frequency Division (Divider 3 and Divider 4)

The division for each channel divider is set by the bits in the registers for the individual dividers ($X.Y = 3.1, 3.2, 4.1, \text{ and } 4.2$)

$$\text{Number of Low Cycles} = M_{X,Y} + 1$$

$$\text{Number of High Cycles} = N_{X,Y} + 1$$

When both $X.1$ and $X.2$ are bypassed, $D_X = 1 \times 1 = 1$.

When only $X.2$ is bypassed, $D_X = (N_{X,1} + M_{X,1} + 2) \times 1$.

When both $X.1$ and $X.2$ are not bypassed, $D_X = (N_{X,1} + M_{X,1} + 2) \times (N_{X,2} + M_{X,2} + 2)$.

By cascading the dividers, channel division up to 1024 can be obtained. However, not all integer value divisions from 1 to 1024 are obtainable; only the values that are the product of the separate divisions of the two dividers ($D_{X,1} \times D_{X,2}$) can be realized.

If only one divider is needed when using Divider 3 and Divider 4, use the first one ($X.1$) and bypass the second one ($X.2$). Do not bypass $X.1$ and use $X.2$.

Duty Cycle and Duty-Cycle Correction (Divider 3 and Divider 4)

The same duty cycle and DCC considerations apply to Divider 3 and Divider 4 as to Divider 0, Divider 1, and Divider 2 (see the Duty Cycle and Duty-Cycle Correction (0, 1, and 2) section; however, with these channel dividers, the number of possible configurations is even more complex.

Duty-cycle correction on Divider 3 and Divider 4 requires the following channel divider conditions:

- An even D_{XY} must be set as $M_{XY} = N_{XY}$ (low cycles = high cycles).
- An odd D_{XY} must be set as $M_{XY} = N_{XY} + 1$ (the number of low cycles must be one greater than the number of high cycles).
- If only one divider is bypassed, it must be the second divider, X_2 .
- If only one divider has an even divide by, it must be the second divider, X_2 .

The possibilities for the duty cycle of the output clock from Divider 3 and Divider 4 are shown in Table 40 through Table 44.

Table 40. Divider 3, Divider 4 Duty Cycle; VCO Divider Used; Duty Cycle Correction Off (DCCOFF = 1)

| VCO Divider | $D_{X,1}$ | $D_{X,2}$ | Output Duty Cycle |
|-------------|-------------------------|-------------------------|---|
| | $N_{X,1} + M_{X,1} + 2$ | $N_{X,2} + M_{X,2} + 2$ | |
| Even | 1 | 1 | 50% |
| Odd = 3 | 1 | 1 | 33.3% |
| Odd = 5 | 1 | 1 | 40% |
| Even | Even, odd | 1 | $(N_{X,1} + 1) / (N_{X,1} + M_{X,1} + 2)$ |
| Odd | Even, odd | 1 | $(N_{X,1} + 1) / (N_{X,1} + M_{X,1} + 2)$ |
| Even | Even, odd | Even, odd | $(N_{X,2} + 1) / (N_{X,2} + M_{X,2} + 2)$ |
| Odd | Even, odd | Even, odd | $(N_{X,2} + 1) / (N_{X,2} + M_{X,2} + 2)$ |

Table 41. Divider 3, Divider 4 Duty Cycle; VCO Divider Not Used; Duty Cycle Correction Off (DCCOFF = 1)

| Input Clock Duty Cycle | $D_{X,1}$ | $D_{X,2}$ | Output Duty Cycle |
|------------------------|-------------------------|-------------------------|---|
| | $N_{X,1} + M_{X,1} + 2$ | $N_{X,2} + M_{X,2} + 2$ | |
| 50% | 1 | 1 | 50% |
| X% | 1 | 1 | X% |
| 50% | Even, odd | 1 | $(N_{X,1} + 1) / (N_{X,1} + M_{X,1} + 2)$ |
| X% | Even, odd | 1 | $(N_{X,1} + 1) / (N_{X,1} + M_{X,1} + 2)$ |
| 50% | Even, odd | Even, odd | $(N_{X,2} + 1) / (N_{X,2} + M_{X,2} + 2)$ |
| X% | Even, odd | Even, odd | $(N_{X,2} + 1) / (N_{X,2} + M_{X,2} + 2)$ |

Table 42. Divider 3, Divider 4 Duty Cycle; VCO Divider Used; Duty Cycle Correction Is On (DCCOFF = 0); VCO Divider Input Duty Cycle = 50%

| VCO Divider | $D_{X,1}$ | $D_{X,2}$ | Output Duty Cycle |
|-------------|---------------------------------|---------------------------------|-------------------|
| | $N_{X,1} + M_{X,1} + 2$ | $N_{X,2} + M_{X,2} + 2$ | |
| Even | 1 | 1 | 50% |
| Odd | 1 | 1 | 50% |
| Even | Even ($N_{X,1} = M_{X,1}$) | 1 | 50% |
| Odd | Even ($N_{X,1} = M_{X,1}$) | 1 | 50% |
| Even | Odd ($M_{X,1} = N_{X,1} + 1$) | 1 | 50% |
| Odd | Odd ($M_{X,1} = N_{X,1} + 1$) | 1 | 50% |
| Even | Even ($N_{X,1} = M_{X,1}$) | Even ($N_{X,2} = M_{X,2}$) | 50% |
| Odd | Even ($N_{X,1} = M_{X,1}$) | Even ($N_{X,2} = M_{X,2}$) | 50% |
| Even | Odd ($M_{X,1} = N_{X,1} + 1$) | Even ($N_{X,2} = M_{X,2}$) | 50% |
| Odd | Odd ($M_{X,1} = N_{X,1} + 1$) | Even ($N_{X,2} = M_{X,2}$) | 50% |
| Even | Odd ($M_{X,1} = N_{X,1} + 1$) | Odd ($M_{X,2} = N_{X,2} + 1$) | 50% |
| Odd | Odd ($M_{X,1} = N_{X,1} + 1$) | Odd ($M_{X,2} = N_{X,2} + 1$) | 50% |

Table 43. Divider 3, Divider 4 Duty Cycle; VCO Divider Used; Duty Cycle Correction On (DCCOFF = 0); VCO Divider Input Duty Cycle = X%

| VCO Divider | $D_{X,1}$ | $D_{X,2}$ | Output Duty Cycle |
|-------------|---------------------------------|---------------------------------|---|
| | $N_{X,1} + M_{X,1} + 2$ | $N_{X,2} + M_{X,2} + 2$ | |
| Even | 1 | 1 | 50% |
| Odd = 3 | 1 | 1 | $(1 + X\%) / 3$ |
| Odd = 5 | 1 | 1 | $(2 + X\%) / 5$ |
| Even | Even ($N_{X,1} = M_{X,1}$) | 1 | 50% |
| Odd | Even ($N_{X,1} = M_{X,1}$) | 1 | 50% |
| Even | Odd ($M_{X,1} = N_{X,1} + 1$) | 1 | 50% |
| Odd = 3 | Odd ($M_{X,1} = N_{X,1} + 1$) | 1 | $(3N_{X,1} + 4 + X\%) / (6N_{X,1} + 9)$ |
| Odd = 5 | Odd ($M_{X,1} = N_{X,1} + 1$) | 1 | $(5N_{X,1} + 7 + X\%) / (10N_{X,1} + 15)$ |
| Even | Even ($N_{X,1} = M_{X,1}$) | Even ($N_{X,2} = M_{X,2}$) | 50% |
| Odd | Even ($N_{X,1} = M_{X,1}$) | Even ($N_{X,2} = M_{X,2}$) | 50% |
| Even | Odd ($M_{X,1} = N_{X,1} + 1$) | Even ($N_{X,2} = M_{X,2}$) | 50% |
| Odd | Odd ($M_{X,1} = N_{X,1} + 1$) | Even ($N_{X,2} = M_{X,2}$) | 50% |
| Even | Odd ($M_{X,1} = N_{X,1} + 1$) | Odd ($M_{X,2} = N_{X,2} + 1$) | 50% |
| Odd = 3 | Odd ($M_{X,1} = N_{X,1} + 1$) | Odd ($M_{X,2} = N_{X,2} + 1$) | $(6N_{X,1}N_{X,2} + 9N_{X,1} + 9N_{X,2} + 13 + X\%) / (3(2N_{X,1} + 3)(2N_{X,2} + 3))$ |
| Odd = 5 | Odd ($M_{X,1} = N_{X,1} + 1$) | Odd ($M_{X,2} = N_{X,2} + 1$) | $(10N_{X,1}N_{X,2} + 15N_{X,1} + 15N_{X,2} + 22 + X\%) / (5(2N_{X,1} + 3)(2N_{X,2} + 3))$ |

Table 44. Divider 3, Divider 4 Duty Cycle; VCO Divider Not Used; Duty Cycle Correction On (DCCOFF = 0)

| Input Clock Duty Cycle | D _{X,1} | D _{X,2} | Output Duty Cycle |
|------------------------|--|--|---|
| | N _{X,1} + M _{X,1} + 2 | N _{X,2} + M _{X,2} + 2 | |
| 50% | 1 | 1 | 50% |
| 50% | Even (N _{X,1} = M _{X,1}) | 1 | 50% |
| X% | 1 | 1 | X% (High) |
| X% | Even (N _{X,1} = M _{X,1}) | 1 | 50% |
| 50% | Odd (M _{X,1} = N _{X,1} + 1) | 1 | 50% |
| X% | Odd (M _{X,1} = N _{X,1} + 1) | 1 | (N _{X,1} + 1 + X%)/ (2N _{X,1} + 3) |
| | Odd (M _{X,1} = N _{X,1} + 1) | 1 | (N _{X,1} + 1 + X%)/ (2N _{X,1} + 3) |
| | Even (N _{X,1} = M _{X,1}) | Even (N _{X,2} = M _{X,2}) | 50% |
| X% | Even (N _{X,1} = M _{X,1}) | Even (N _{X,2} = M _{X,2}) | 50% |
| 50% | Odd (M _{X,1} = N _{X,1} + 1) | Even (N _{X,2} = M _{X,2}) | 50% |
| X% | Odd (M _{X,1} = N _{X,1} + 1) | Even (N _{X,2} = M _{X,2}) | 50% |
| 50% | Odd (M _{X,1} = N _{X,1} + 1) | Odd (M _{X,2} = N _{X,2} + 1) | 50% |
| X% | Odd (M _{X,1} = N _{X,1} + 1) | Odd (M _{X,2} = N _{X,2} + 1) | (2N _{X,1} N _{X,2} + 3N _{X,1} + 3N _{X,2} + 4 + X%)/ ((2N _{X,1} + 3)(2N _{X,2} + 3)) |

Phase Offset or Coarse Time Delay (Divider 3 and Divider 4)

Divider 3 and Divider 4 can be set to have a phase offset or delay. The phase offset is set by a combination of the bits in the phase offset and start high registers (see Table 45).

Table 45. Setting Phase Offset and Division for Divider 3 and Divider 4

| Divider | | Start High (SH) | Phase Offset (PO) | Low Cycles M | High Cycles N |
|---------|-----|-----------------|-------------------|--------------|---------------|
| 3 | 3.1 | 0x19C[0] | 0x19A[3:0] | 0x199[7:4] | 0x199[3:0] |
| | 3.2 | 0x19C[1] | 0x19A[7:4] | 0x19B[7:4] | 0x19B[3:0] |
| 4 | 4.1 | 0x1A1[0] | 0x19F[3:0] | 0x19E[7:4] | 0x19E[3:0] |
| | 4.2 | 0x1A1[1] | 0x19F[7:4] | 0x1A0[7:4] | 0x1A0[3:0] |

Let Δt = delay (in seconds).

$$\Phi_{xy} = 16 \times SH[0] + 8 \times PO[3] + 4 \times PO[2] + 2 \times PO[1] + 1 \times PO[0].$$

T_{X,1} = period of the clock signal at the input to D_{X,1} (in seconds).

T_{X,2} = period of the clock signal at the input to D_{X,2} (in seconds).

Case 1

When $\Phi_{X,1} \leq 15$ and $\Phi_{X,2} \leq 15$:

$$\Delta t = \Phi_{X,1} \times T_{X,1} + \Phi_{X,2} \times T_{X,2}$$

Case 2

When $\Phi_{X,1} \leq 15$ and $\Phi_{X,2} \geq 16$:

$$\Delta t = \Phi_{X,1} \times T_{X,1} + (\Phi_{X,2} - 16 + M_{X,2} + 1) \times T_{X,2}$$

Case 3

When $\Phi_{X,1} \geq 16$ and $\Phi_{X,2} \leq 15$:

$$\Delta t = (\Phi_{X,1} - 16 + M_{X,1} + 1) \times T_{X,1} + \Phi_{X,2} \times T_{X,2}$$

Case 4

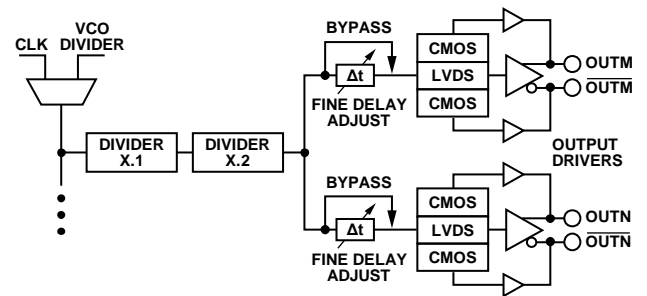
When $\Phi_{X,1} \geq 16$ and $\Phi_{X,2} \geq 16$:

$$\Delta t =$$

$$(\Phi_{X,1} - 16 + M_{X,1} + 1) \times T_{X,1} + (\Phi_{X,2} - 16 + M_{X,2} + 1) \times T_{X,2}$$

Fine Delay Adjust (Divider 3 and Divider 4)

Each AD9516 LVDS/CMOS output (OUT6 to OUT9) includes an analog delay element that can be programmed to give variable time delays (Δt) in the clock signal at that output.

**Figure 56. Fine Delay (OUT6 to OUT9)**

The amount of delay applied to the clock signal is determined by programming four registers per output (see Table 46).

Table 46. Setting Analog Fine Delays

| OUTPUT (LVDS/CMOS) | Ramp Capacitors | Ramp Current | Delay Fraction | Delay Bypass |
|--------------------|-----------------|--------------|----------------|--------------|
| OUT6 | 0x0A1[5:3] | 0x0A1[2:0] | 0x0A2[5:0] | 0x0A0[0] |
| OUT7 | 0x0A4[5:3] | 0x0A4[2:0] | 0x0A5[5:0] | 0x0A3[0] |
| OUT8 | 0x0A7[5:3] | 0x0A7[2:0] | 0x0A8[5:0] | 0x0A6[0] |
| OUT9 | 0x0AA[5:3] | 0x0AA[2:0] | 0x0AB[5:0] | 0x0A9[0] |

Calculating the Fine Delay

The following values and equations are used to calculate the delay of the delay block.

$$I_{RAMP} (\mu A) = 200 \times (Ramp\ Current + 1)$$

$$Number\ of\ Capacitors = Number\ of\ Bits = 0\ in\ Ramp\ Capacitors + 1$$

Example: 101 = 1 + 1 = 2; 110 = 1 + 1 = 2; 100 = 2 + 1 = 3; 001 = 2 + 1 = 3; 111 = 0 + 1 = 1.

$$Delay\ Range\ (ns) = 200 \times ((No.\ of\ Caps + 3) / (I_{RAMP})) \times 1.3286$$

$$Offset\ (ns) = 0.34 + (1600 - I_{RAMP}) \times 10^{-4} + \left(\frac{No.\ of\ Caps - 1}{I_{RAMP}} \right) \times 6$$

$$Delay\ Full\ Scale\ (ns) = Delay\ Range + Offset$$

$$Fine\ Delay\ (ns) =$$

$$Delay\ Range \times Delay\ Fraction \times (1/63) + Offset$$

Note that only delay fraction values up to 47 decimal (101111b; 0x2F) are supported.

In no case can the fine delay exceed one-half of the output clock period. If a delay longer than half of the clock period is attempted, the output stops clocking.

The delay function adds some jitter that is greater than that specified for the nondelayed output. This means that the delay function should be used primarily for clocking digital chips, such as FPGA, ASIC, DUC, and DDC. An output with this delay enabled may not be suitable for clocking data converters. The jitter is higher for long full scales because the delay block uses a ramp and trip points to create the variable delay. A slower ramp time produces more time jitter.

Synchronizing the Outputs—SYNC Function

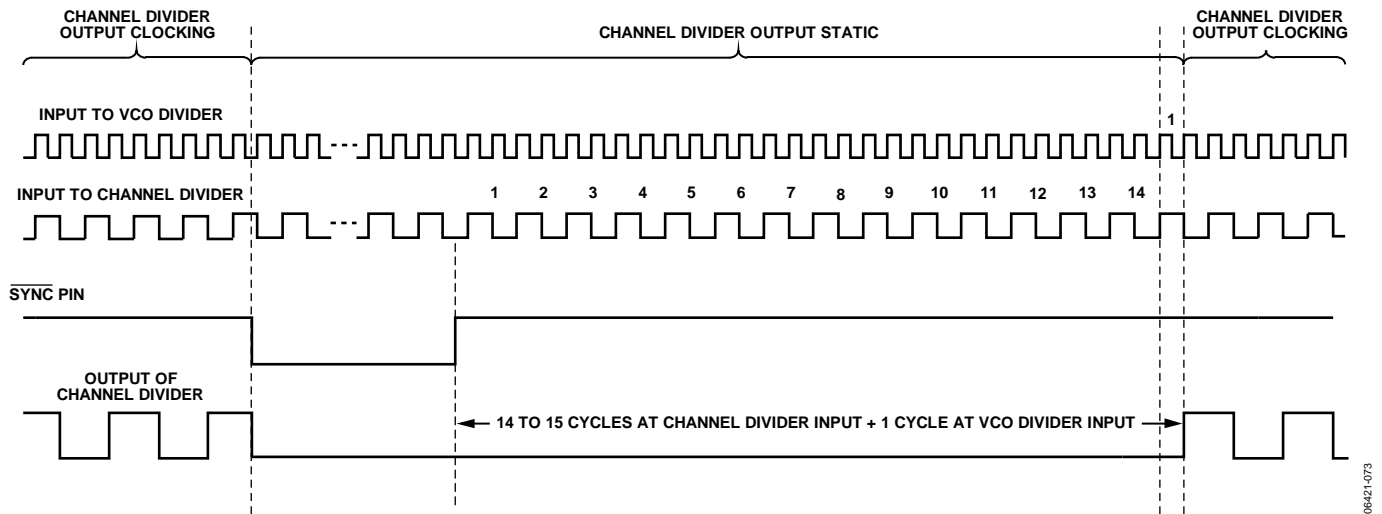
The AD9516 clock outputs can be synchronized to each other. Outputs can be individually excluded from synchronization. Synchronization consists of setting the nonexcluded outputs to a preset set of static conditions and, subsequently, releasing these outputs to continue clocking at the same instant with the preset conditions applied. This allows for the alignment of the edges of two or more outputs, or for the spacing of edges, according to the coarse phase offset settings for two or more outputs.

Synchronization of the outputs is executed in several ways, as follows:

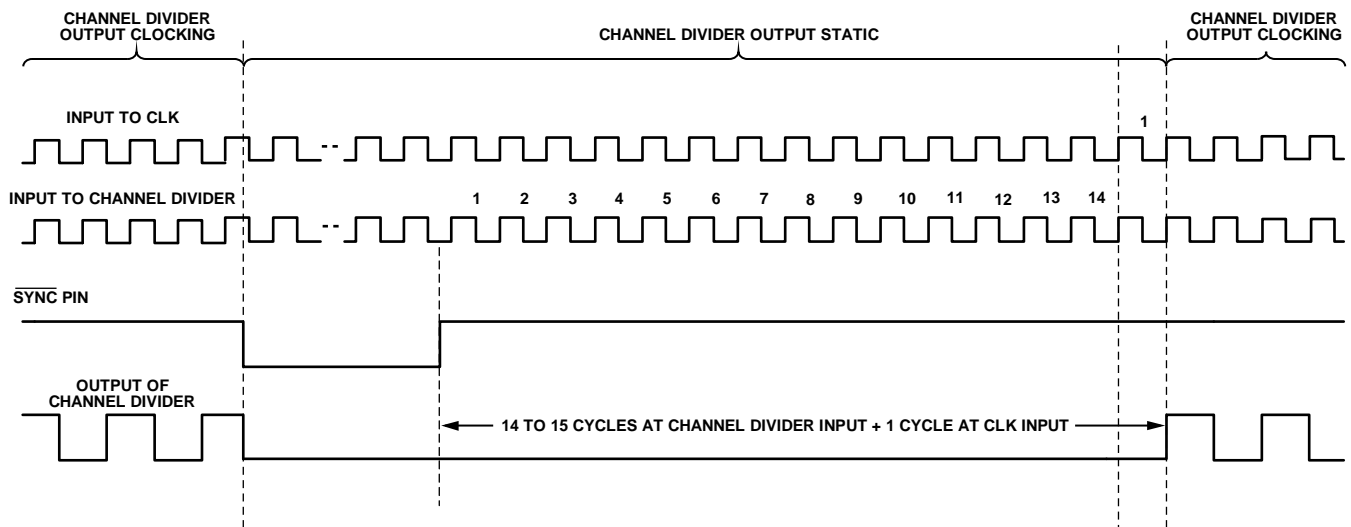
- By forcing the \overline{SYNC} pin low and then releasing it (manual sync).
- By setting and then resetting any one of the following three bits: the soft sync bit (Register 0x230[0]), the soft reset bit (Register 0x000[2] [mirrored]), and the power-down distribution reference bit (Register 0x230[1]).
- By executing synchronization of the outputs as part of the chip power-up sequence.
- By forcing the RESET pin low and then releasing it (chip reset).
- By forcing the \overline{PD} pin low and then releasing it (chip power-down).
- Following completion of a VCO calibration. An internal SYNC signal is automatically asserted at the beginning and released upon the completion of a VCO calibration.

The most common way to execute the SYNC function is to use the \overline{SYNC} pin to do a manual synchronization of the outputs. This requires a low-going signal on the \overline{SYNC} pin, which is held low and then released when synchronization is desired. The timing of the SYNC operation is shown in Figure 57 (using VCO divider) and Figure 58 (VCO divider not used). There is an uncertainty of up to one cycle of the clock at the input to the channel divider due to the asynchronous nature of the SYNC signal with respect to the clock edges inside the AD9516. The delay from the \overline{SYNC} rising edge to the beginning of synchronized output clocking is between 14 and 15 cycles of clock at the channel divider input, plus either one cycle of the VCO divider input (see Figure 57) or one cycle of the channel divider input (see Figure 58), depending on whether the VCO divider is used. Cycles are counted from the rising edge of the signal.

Another common way to execute the SYNC function is by setting and resetting the soft sync bit at Register 0x230[0] (see Table 53 through Table 62 for details). Both setting and resetting of the soft sync bit require an update all registers operation (Register 0x232[0] = 1) to take effect.



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A sync operation brings all outputs that have not been excluded (by the nosync bit) to a preset condition before allowing the outputs to begin clocking in synchronicity. The preset condition takes into account the settings in each of the channel's start high bit and its phase offset. These settings govern both the static state of each output when the SYNC operation is happening and the state and relative phase of the outputs when they begin clocking again upon completion of the SYNC operation. Between outputs and after synchronization, this allows for the setting of phase offsets.

The AD9516 outputs are in pairs, sharing a channel divider per pair (two pairs of pairs, four outputs, in the case of CMOS). The synchronization conditions apply to both outputs of a pair.

Each channel (a divider and its outputs) can be excluded from any sync operation by setting the nosync bit of the channel. Channels that are set to ignore SYNC (excluded channels) do not set their outputs static during a sync operation, and their outputs are not synchronized with those of the nonexcluded channels.

Clock Outputs

The AD9516 offers three different output level choices: LVPECL, LVDS, and CMOS. OUT0 to OUT5 are LVPECL differential outputs; and OUT6 to OUT9 are LVDS/CMOS outputs. These outputs can be configured as either LVDS differential or as pairs of single-ended CMOS outputs.

LVPECL Outputs—OUT0 to OUT5

The LVPECL differential voltage (V_{OD}) is selectable from ~400 mV to ~960 mV (see Register 0x0F0[3:2] to Register 0x0F5[3:2]). The LVPECL outputs have dedicated pins for power supply (V_{S_LVPECL}), allowing a separate power supply to be used. V_{S_LVPECL} can be from 2.5 V to 3.3 V.

The LVPECL output polarity can be set as noninverting or inverting, which allows for the adjustment of the relative polarity of outputs within an application without requiring a board layout change. Each LVPECL output can be powered down or powered up, as needed. Because of the architecture of the LVPECL output stages, there is the possibility of electrical overstress and breakdown under certain power-down conditions. For this reason, the LVPECL outputs have several power-down modes. This includes a safe power-down mode that continues to protect the output devices while powered down, although it consumes somewhat more power than a total power-down. If the LVPECL output pins are terminated, it is best to select the safe power-down mode. If the pins are not connected (unused), it is acceptable to use the total power-down mode.

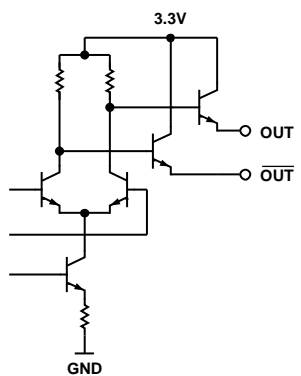


Figure 59. LVPECL Output Simplified Equivalent Circuit

LVDS/CMOS Outputs—OUT6 to OUT9

OUT6 to OUT9 can be configured as either an LVDS differential output or as a pair of CMOS single-ended outputs. The LVDS outputs allow for selectable output current from ~1.75 mA to ~7 mA.

The LVDS output polarity can be set as noninverting or inverting, which allows for the adjustment of the relative polarity of outputs within an application without requiring a board layout change. Each LVDS output can be powered down if not needed to save power.

OUT6 to OUT9 can also be CMOS outputs. Each LVDS output can be configured to be two CMOS outputs. This provides for up to eight CMOS outputs: OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, and OUT9B. When an output is configured as CMOS, CMOS Output A is automatically turned on. CMOS Output B can be turned on or off independently. The relative polarity of the CMOS outputs can also be selected for any combination of inverting and noninverting (see Table 57 for Register 0x140[7:5], Register 0x141[7:5], Register 0x142[7:5], and Register 0x143[7:5]).

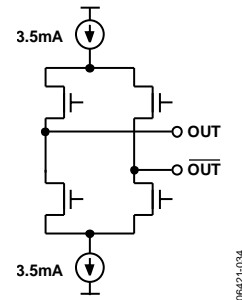


Figure 60. LVDS Output Simplified Equivalent Circuit with 3.5 mA Typical Current Source

Each LVDS/CMOS output can be powered down as needed to save power. The CMOS output power-down is controlled by the same bit that controls the LVDS power-down for that output. This power-down control affects both CMOS Output A and CMOS Output B. However, when CMOS Output A is powered up, CMOS Output B can be powered on or off separately.

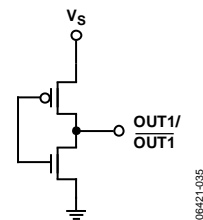


Figure 61. CMOS Equivalent Output Circuit

RESET MODES

The AD9516 has several ways to force the chip into a reset condition that restores all registers to their default values and makes these settings active.

Power-On Reset—Start-Up Conditions When V_S Is Applied

A power-on reset (POR) is issued when the V_S power supply is turned on. This initializes the chip to the power-on conditions that are determined by the default register settings. These are indicated in the Default Value (Hex) column of Table 52. At power-on, the AD9516 also executes a SYNC operation, which brings the outputs into phase alignment according to the default settings.

Asynchronous Reset via the $\overline{\text{RESET}}$ Pin

An asynchronous hard reset is executed by momentarily pulling $\overline{\text{RESET}}$ low. A reset restores the chip registers to the default settings.

Soft Reset via Register 0x000[2]

A soft reset is executed by writing Register 0x000[2] and Register 0x000[5] = 1b. This bit is not self-clearing; it must be cleared by writing Register 0x000[2] and Register 0x000[5] = 0b to reset it and complete the soft reset operation. A soft reset restores the default values to the internal registers. The soft reset bit does not require an update registers command (Register 0x232) to be issued.

POWER-DOWN MODES

Chip Power-Down via \overline{PD}

The AD9516 can be put into a power-down condition by pulling the \overline{PD} pin low. Power-down turns off most of the functions and currents inside the AD9516. The chip remains in this power-down state until \overline{PD} is brought back to logic high. When the AD9516 wakes up, it returns to the settings programmed into its registers prior to the power-down, unless the registers are changed by new programming while the \overline{PD} pin is held low.

The \overline{PD} power-down shuts down the currents on the chip, except the bias current that is necessary to maintain the LVPECL outputs in a safe shutdown mode. This is needed to protect the LVPECL output circuitry from damage that could be caused by certain termination and load configurations when tristated. Because this is not a complete power-down, it can be called sleep mode.

When the AD9516 is in a \overline{PD} power-down, the chip is in the following state:

- The PLL is off (asynchronous power-down).
- The VCO is off.
- The CLK input buffer is off.
- All dividers are off.
- All LVDS/CMOS outputs are off.
- All LVPECL outputs are in safe off mode.
- The serial control port is active, and the chip responds to commands.

If the AD9516 clock outputs must be synchronized to each other, a SYNC is required upon exiting power-down (see the Synchronizing the Outputs—SYNC Function section). A VCO calibration is not required when exiting power-down.

PLL Power-Down

The PLL section of the AD9516 can be selectively powered down. There are three PLL operating modes that are set by Register 0x010[1:0], as shown in Table 54.

In asynchronous power-down mode, the device powers down as soon as the registers are updated.

In synchronous power-down mode, the PLL power-down is gated by the charge pump to prevent unwanted frequency jumps. The device goes into power-down on the occurrence of the next charge pump event after the registers are updated.

Distribution Power-Down

The distribution section can be powered down by writing Register 0x230[1] = 1b. This turns off the bias to the distribution section. If the LVPECL power-down mode is normal operation (00b), it is possible for a low impedance load on that LVPECL output to draw significant current during this power-down. If the LVPECL power-down mode is set to 11b, the LVPECL output is not protected from reverse bias and may be damaged under certain termination conditions.

Individual Clock Output Power-Down

Any of the clock distribution outputs can be powered down individually by writing to the appropriate registers. The register map details the individual power-down settings for each output (see Table 52). The LVDS/CMOS outputs can be powered down, regardless of their output load configuration.

The LVPECL outputs have multiple power-down modes (see Table 56), which give some flexibility in dealing with the various output termination conditions. When the mode is set to 10b, the LVPECL output is protected from reverse bias to $2 V_{BE} + 1 V$. If the mode is set to 11b, the LVPECL output is not protected from reverse bias and can be damaged under certain termination conditions. This setting also affects the operation when the distribution block is powered down with Register 0x230[1] = 1b (see the Distribution Power-Down section).

Individual Circuit Block Power-Down

Other AD9516 circuit blocks (such as CLK, REF1, and REF2) can be powered down individually. This gives flexibility in configuring the part for power savings whenever certain chip functions are not needed.

SERIAL CONTROL PORT

The AD9516 serial control port is a flexible, synchronous, serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. The AD9516 serial control port is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR® protocols. The serial control port allows read/write access to all registers that configure the AD9516. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9516 serial control port can be configured for a single bidirectional I/O pin (SDIO only) or for two unidirectional I/O pins (SDIO/SDO). By default, the AD9516 is in bidirectional mode, long instruction (long instruction is only instruction mode supported).

SERIAL CONTROL PORT PIN DESCRIPTIONS

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin that acts as either an input only (unidirectional mode) or as both an input/output (bidirectional mode). The AD9516 defaults to the bidirectional I/O mode (Register 0x000[0] = 0b).

SDO (serial data out) is used only in the unidirectional I/O mode (Register 0x000[0] = 1b) as a separate output pin for reading back data.

$\overline{\text{CS}}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{\text{CS}}$ is high, SDO and SDIO are in a high impedance state. This pin is internally pulled up by a 30 kΩ resistor to VS.

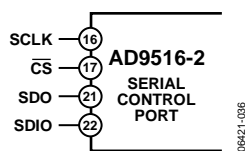


Figure 62. Serial Control Port

GENERAL OPERATION OF SERIAL CONTROL PORT

A write or a read operation to the AD9516 is initiated by pulling $\overline{\text{CS}}$ low.

$\overline{\text{CS}}$ stall high is supported in modes where three or fewer bytes of data (plus instruction data) are transferred (see Table 47). In these modes, $\overline{\text{CS}}$ can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. $\overline{\text{CS}}$ can go high on byte boundaries only and can go high during either part (instruction or data) of the transfer.

During this period, the serial control port state machine enters a wait state until all data is sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset, either by completing the remaining transfers or by returning the $\overline{\text{CS}}$ low for at least one complete SCLK cycle (but less than eight SCLK cycles). Raising the $\overline{\text{CS}}$ on a nonbyte boundary terminates the serial transfer and flushes the buffer.

In the streaming mode (see Table 47), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). $\overline{\text{CS}}$ must be raised at the end of the last byte to be transferred, thereby ending the stream mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9516. The first part writes a 16-bit instruction word into the AD9516, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9516 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation, the second part is the transfer of data into the serial control port buffer of the AD9516. Data bits are registered on the rising edge of SCLK.

The length of the transfer (1, 2, 3 bytes or streaming mode) is indicated by two bits ([W1:W0]) in the instruction byte. When the transfer is 1, 2, or 3 bytes, but not streaming, $\overline{\text{CS}}$ can be raised after each sequence of eight bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{\text{CS}}$ is lowered. Raising $\overline{\text{CS}}$ on a nonbyte boundary resets the serial control port. During a write, streaming mode does not skip over reserved or blank registers; therefore, the user must know the bit pattern to write to the reserved registers to preserve proper operation of the part. Refer to the register map (see Table 52) to determine if the default value for reserved registers is nonzero. It does not matter what data is written to blank registers.

Because data is written into a serial control port buffer area, and not directly into the actual control registers of the AD9516, an additional operation is needed to transfer the serial control port buffer contents to the actual control registers of the AD9516, thereby causing them to become active. The update registers operation consists of setting Register 0x232[0] = 1b (this bit is self-clearing). Any number of bytes of data can be changed before executing an update registers. The update registers operation simultaneously actuates all register changes that have been written to the buffer since any previous update.

Read

If the instruction word is for a read operation, the next $N \times 8$ SCLK cycles clock out the data from the address specified in the instruction word, where N is 1 to 3 as determined by $[W1:W0]$. If $N = 4$, the read operation is in streaming mode, continuing until \overline{CS} is raised. Streaming mode does not skip over reserved or blank registers. The readback data is valid on the falling edge of SCLK.

The default mode of the AD9516 serial control port is the bidirectional mode. In bidirectional mode, both the sent data and the readback data appear on the SDIO pin. It is also possible to set the AD9516 to unidirectional mode via the SDO active bit (Register 0x000[0] = 1b). In unidirectional mode, the readback data appears on the SDO pin.

A readback request reads the data that is in the serial control port buffer area, or the data that is in the active registers (see Figure 63). Readback of the buffer or active registers is controlled by Register 0x004[0].

The AD9516 supports only the long instruction mode, therefore Register 0x000[4:3] must be set to 11b. (This register uses mirrored bits). Long instruction mode is the default at power-up or reset.

The AD9516 uses Register Address 0x000 to Register Address 0x232.

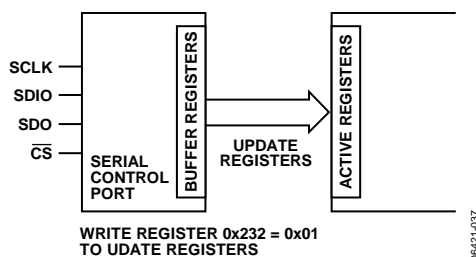


Figure 63. Relationship Between Serial Control Port Buffer Registers and Active Registers of the AD9516

THE INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/\overline{W} , which indicates whether the instruction is a read or a write. The next two bits, $[W1:W0]$, indicate the length of the transfer in bytes. The final 13 bits are the address ($[A12:A0]$) at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits $[W1:W0]$ (see Table 47).

Table 47. Byte Transfer Count

| W1 | W0 | Bytes to Transfer |
|----|----|-------------------|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | Streaming mode |

The 13 bits found in $[A12:A0]$ select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. Only Bits $[A9:A0]$ are needed to cover the range of the 0x232 registers used by the AD9516. Bits $[A12:A10]$ must always be 0b. For multibyte transfers, this address is the starting byte address. In MSB first mode, subsequent bytes decrement the address.

MSB/LSB FIRST TRANSFERS

The AD9516 instruction word and byte data can be MSB first or LSB first. Any data written to Register 0x000 must be mirrored; the upper four bits (Bits $[7:4]$) with the lower four bits (Bits $[3:0]$). This makes it irrelevant whether LSB first or MSB first is in effect. As an example of this mirroring, see the default setting for this register: 0x18, which mirrors Bit 4 and Bit 3. This sets the long instruction mode (which is the default and the only mode that is supported).

The default for the AD9516 is MSB first.

When LSB first is set by Register 0x000[1] and Register 0x000[6], it takes effect immediately because it affects only the operation of the serial control port and does not require that an update be executed.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow, in order, from the high address to the low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first is active, the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The internal byte address generator of the serial control port increments for each byte of the multibyte transfer cycle.

The AD9516 serial control port register address decrements from the register address just written toward 0x000 for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the register address of the serial control port increments from the address just written toward Address 0x232 for multibyte I/O operations.

Streaming mode always terminates when it hits Address 0x232. Note that unused addresses are not skipped during multibyte I/O operations.

Table 48. Streaming Mode (No Addresses Are Skipped)

| Write Mode | Address Direction | Stop Sequence |
|------------|-------------------|---------------------------|
| LSB first | Increment | 0x230, 0x231, 0x232, stop |
| MSB first | Decrement | 0x001, 0x000, 0x232, stop |

Table 49. Serial Control Port, 16-Bit Instruction Word, MSB First

| MSB | | | | | | | | | | | | | | LSB | |
|-----|-----|-----|---------|---------|---------|----|----|----|----|----|----|----|----|-----|----|
| I15 | I14 | I13 | I12 | I11 | I10 | I9 | I8 | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |
| R/W | W1 | W0 | A12 = 0 | A11 = 0 | A10 = 0 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

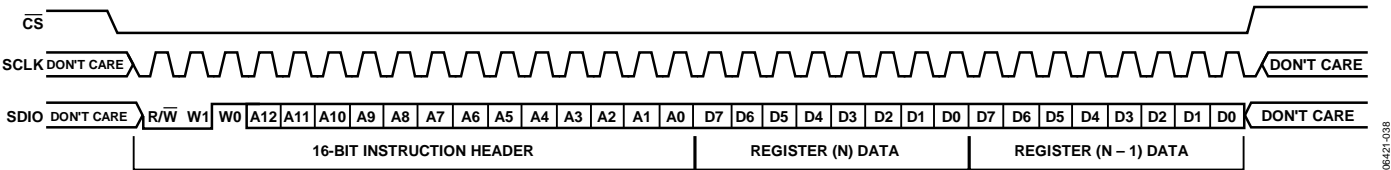


Figure 64. Serial Control Port Write—MSB First, 16-Bit Instruction, Two Bytes Data

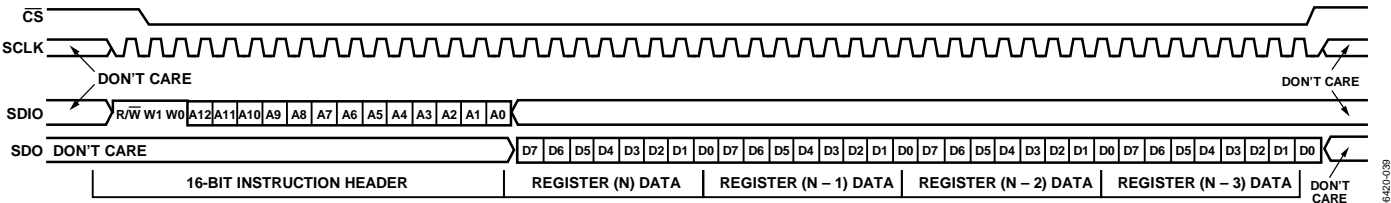


Figure 65. Serial Control Port Read—MSB First, 16-Bit Instruction, Four Bytes Data

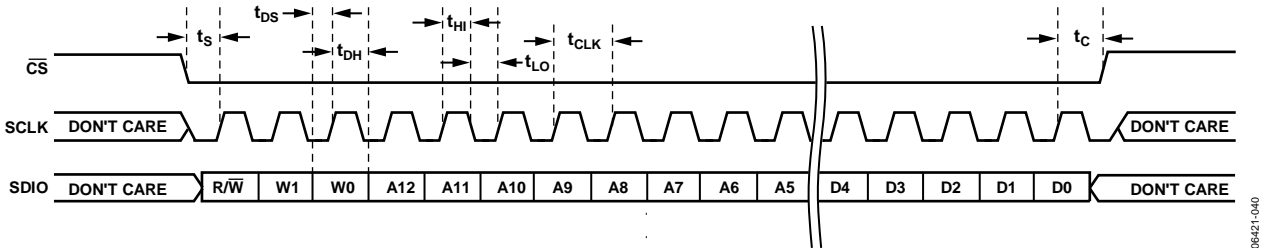


Figure 66. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

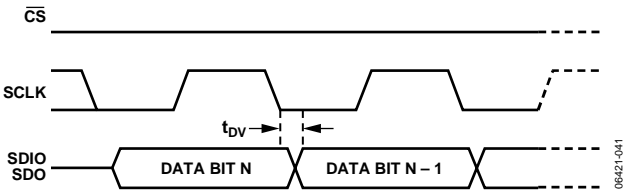


Figure 67. Timing Diagram for Serial Control Port Register Read

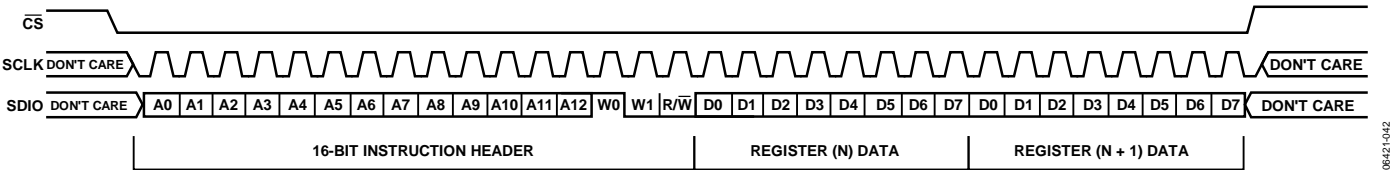


Figure 68. Serial Control Port Write—LSB First, 16-Bit Instruction, Two Bytes Data

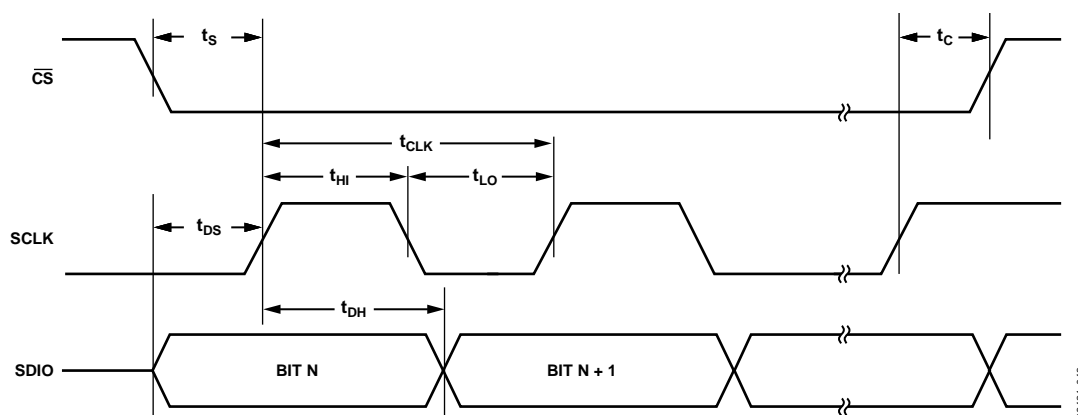


Figure 69. Serial Control Port Timing—Write

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Table 50. Serial Control Port Timing

| Parameter | Description |
|------------|---|
| t_{DS} | Setup time between data and rising edge of SCLK |
| t_{DH} | Hold time between data and rising edge of SCLK |
| t_{CLK} | Period of the clock |
| t_s | Setup time between \overline{CS} falling edge and SCLK rising edge (start of communication cycle) |
| t_c | Setup time between SCLK rising edge and \overline{CS} rising edge (end of communication cycle) |
| t_{HIGH} | Minimum period that SCLK should be in a logic high state |
| t_{LOW} | Minimum period that SCLK should be in a logic low state |
| t_{DV} | SCLK to valid SDIO and SDO (see Figure 67) |

THERMAL PERFORMANCE

Table 51. Thermal Parameters for the 64-Lead LFCSP

| Symbol | Thermal Characteristic Using a JEDEC JESD51-7 Plus JEDEC JESD51-5 2S2P Test Board | Value (°C/W) |
|----------------|--|--------------|
| θ_{JA} | Junction-to-ambient thermal resistance, natural convection per JEDEC JESD51-2 (still air) | 22.0 |
| θ_{JMA} | Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air) | 19.2 |
| θ_{JMA} | Junction-to-ambient thermal resistance, 2.0 m/sec airflow per JEDEC JESD51-6 (moving air) | 17.2 |
| Ψ_{JB} | Junction-to-board characterization parameter, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air) and JEDEC JESD51-8 | 11.6 |
| θ_{JC} | Junction-to-case thermal resistance (die-to-heat sink) per MIL-STD-883, Method 1012.1 | 1.3 |
| Ψ_{JT} | Junction-to-top-of-package characterization parameter, natural convection per JEDEC JESD51-2 (still air) | 0.1 |

The AD9516 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an airflow source can be used.

Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:

T_J is the junction temperature (°C).

T_{CASE} is the case temperature (°C) measured by the user at the top center of the package.

Ψ_{JT} is the value from Table 51.

PD is the power dissipation of the device (see Table 17).

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the following equation:

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of Ψ_{JB} are provided for package comparison and PCB design considerations.

REGISTER MAP OVERVIEW

Table 52. Register Map Overview

| Reg. Addr. (Hex) | Parameter | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | |
|---------------------------|---------------------------|-----------------------------------|---------------------------------------|--------------------------------|------------------------------------|-----------------------------|----------------------------|----------------------------|----------------------------|---------------------|------|
| Serial Port Configuration | | | | | | | | | | | |
| 0x000 | Serial port configuration | SDO active | LSB first | Soft reset | Long instruction | Long instruction | Soft reset | LSB first | SDO active | 0x18 | |
| 0x001 | Blank | | | | | | | | | | |
| 0x002 | Reserved | | | | | | | | | | |
| 0x003 | Part ID | Part ID (read only) | | | | | | | | 0x01 | |
| 0x004 | Readback control | Blank | | | | | | | Read back active registers | 0x00 | |
| PLL | | | | | | | | | | | |
| 0x010 | PFD and charge pump | PFD polarity | Charge pump current | | | Charge pump mode | | PLL power-down | | 0x7D | |
| 0x011 | R counter | 14-bit R divider, Bits[7:0] (LSB) | | | | | | | | | 0x01 |
| 0x012 | | Blank | 14-bit R divider, Bits[13:8] (MSB) | | | | | | | 0x00 | |
| 0x013 | A counter | Blank | 6-bit A counter | | | | | | | 0x00 | |
| 0x014 | B counter | 13-bit B counter, Bits[7:0] (LSB) | | | | | | | | | 0x03 |
| 0x015 | | Blank | | | 13-bit B counter, Bits[12:8] (MSB) | | | | | | 0x00 |
| 0x016 | PLL Control 1 | Set CP pin to $V_{CP}/2$ | Reset R counter | Reset A and B counters | Reset all counters | B counter bypass | Prescaler P | | | 0x06 | |
| 0x017 | PLL Control 2 | STATUS pin control | | | | | | | Antibacklash pulse width | 0x00 | |
| 0x018 | PLL Control 3 | Reserved | Lock detect counter | | Digital lock detect window | Disable digital lock detect | VCO calibration divider | | VCO cal now | 0x06 | |
| 0x019 | PLL Control 4 | R, A, B counters SYNC pin reset | | R path delay | | | N path delay | | | 0x00 | |
| 0x01A | PLL Control 5 | Reserved | Reference frequency monitor threshold | LD pin control | | | | | | | 0x00 |
| 0x01B | PLL Control 6 | VCO frequency monitor | REF2 (REFIN) frequency monitor | REF1 (REFIN) frequency monitor | REFMON pin control | | | | | | 0x00 |
| 0x01C | PLL Control 7 | Disable switchover deglitch | Select REF2 | Use REF_SEL pin | Reserved | Reserved | REF2 power-on | REF1 power-on | Differential reference | 0x00 | |
| 0x01D | PLL Control 8 | Reserved | | | PLL status register disable | LD pin comparator enable | Holdover enable | External holdover control | Holdover enable | 0x00 | |
| 0x01E | PLL Control 9 | Reserved | | | | | | | | | 0x00 |
| 0x01F | PLL readback | Reserved | VCO cal finished | Holdover active | REF2 selected | VCO frequency > threshold | REF2 frequency > threshold | REF1 frequency > threshold | Digital lock detect | N/A | |
| 0x020 to 0x04F | Blank | | | | | | | | | | |

| Reg. Addr. (Hex) | Parameter | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|--------------------------------|-----------------------|---------------------------|-------|--------------------------------|-------------|----------------------------------|--------------------------|-----------------|-------------------|---------------------|
| Fine Delay Adjust—OUT6 to OUT9 | | | | | | | | | | |
| 0x0A0 | OUT6 delay bypass | Blank | | | | | | | OUT6 delay bypass | 0x01 |
| 0x0A1 | OUT6 delay full-scale | Blank | | OUT6 ramp capacitors | | | OUT6 ramp current | | | 0x00 |
| 0x0A2 | OUT6 delay fraction | Blank | | OUT6 delay fraction | | | | | | 0x00 |
| 0x0A3 | OUT7 delay bypass | Blank | | | | | | | OUT7 delay bypass | 0x01 |
| 0x0A4 | OUT7 delay full-scale | Blank | | OUT7 ramp capacitors | | | OUT7 ramp current | | | 0x00 |
| 0x0A5 | OUT7 delay fraction | Blank | | OUT7 delay fraction | | | | | | 0x00 |
| 0x0A6 | OUT8 delay bypass | Blank | | | | | | | OUT8 delay bypass | 0x01 |
| 0x0A7 | OUT8 delay full-scale | Blank | | OUT8 ramp capacitors | | | OUT8 ramp current | | | 0x00 |
| 0x0A8 | OUT8 delay fraction | Blank | | OUT8 delay fraction | | | | | | 0x00 |
| 0x0A9 | OUT9 delay bypass | Blank | | | | | | | OUT9 delay bypass | 0x01 |
| 0x0AA | OUT9 delay full-scale | Blank | | OUT9 ramp capacitors | | | OUT9 ramp current | | | 0x00 |
| 0x0AB | OUT9 delay fraction | Blank | | OUT9 delay fraction | | | | | | 0x00 |
| 0x0AC to 0x0EF | Blank | | | | | | | | | |
| LVPECL Outputs | | | | | | | | | | |
| 0x0F0 | OUT0 | Blank | | | OUT0 invert | OUT0 LVPECL differential voltage | | OUT0 power-down | | 0x08 |
| 0x0F1 | OUT1 | Blank | | | OUT1 invert | OUT1 LVPECL differential voltage | | OUT1 power-down | | 0x0A |
| 0x0F2 | OUT2 | Blank | | | OUT2 invert | OUT2 LVPECL differential voltage | | OUT2 power-down | | 0x08 |
| 0x0F3 | OUT3 | Blank | | | OUT3 invert | OUT3 LVPECL differential voltage | | OUT3 power-down | | 0x0A |
| 0x0F4 | OUT4 | Blank | | | OUT4 invert | OUT4 LVPECL differential voltage | | OUT4 power-down | | 0x08 |
| 0x0F5 | OUT5 | Blank | | | OUT5 invert | OUT5 LVPECL differential voltage | | OUT5 power-down | | 0x0A |
| 0x0F6 to 0x13F | Blank | | | | | | | | | |
| LVDS/CMOS Outputs | | | | | | | | | | |
| 0x140 | OUT6 | OUT6 CMOS output polarity | | OUT6 LVDS/CMOS output polarity | OUT6 CMOS B | OUT6 select LVDS/CMOS | OUT6 LVDS output current | | OUT6 power-down | 0x42 |
| 0x141 | OUT7 | OUT7 CMOS output polarity | | OUT7 LVDS/CMOS output polarity | OUT7 CMOS B | OUT7 select LVDS/CMOS | OUT7 LVDS output current | | OUT7 power-down | 0x43 |
| 0x142 | OUT8 | OUT8 CMOS output polarity | | OUT8 LVDS/CMOS output polarity | OUT8 CMOS B | OUT8 select LVDS/CMOS | OUT8 LVDS output current | | OUT8 power-down | 0x42 |
| 0x143 | OUT9 | OUT9 CMOS output polarity | | OUT9 LVDS/CMOS output polarity | OUT9 CMOS B | OUT9 select LVDS/CMOS | OUT9 LVDS output current | | OUT9 power-down | 0x43 |

| Reg. Addr. (Hex) | Parameter | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|----------------------------|-----------------------|--------------------------|-------------------|----------------------|--------------------------------|--------------------------------|------------------------|----------------------------|------------------------|---------------------|
| 0x144 to 0x18F | Blank | | | | | | | | | |
| LVPECL Channel Dividers | | | | | | | | | | |
| 0x190 | Divider 0 (PECL) | Divider 0 low cycles | | | | Divider 0 high cycles | | | | 0x00 |
| 0x191 | | Divider 0 bypass | Divider 0 no sync | Divider 0 force high | Divider 0 start high | Divider 0 phase offset | | | | 0x80 |
| 0x192 | | Blank | | Reserved | | | | Divider 0 direct to output | Divider 0 DCCOFF | 0x00 |
| 0x193 | Divider 1 (PECL) | Divider 1 low cycles | | | | Divider 1 high cycles | | | | 0xBB |
| 0x194 | | Divider 1 bypass | Divider 1 no sync | Divider 1 force high | Divider 1 start high | Divider 1 phase offset | | | | 0x00 |
| 0x195 | | Blank | | Reserved | | | | Divider 1 direct to output | Divider 1 DCCOFF | 0x00 |
| 0x196 | Divider 2 (PECL) | Divider 2 low cycles | | | | Divider 2 high cycles | | | | 0x00 |
| 0x197 | | Divider 2 bypass | Divider 2 no sync | Divider 2 force high | Divider 2 start high | Divider 2 phase offset | | | | 0x00 |
| 0x198 | | Blank | | Reserved | | | | Divider 2 direct to output | Divider 2 DCCOFF | 0x00 |
| LVDS/CMOS Channel Dividers | | | | | | | | | | |
| 0x199 | Divider 3 (LVDS/CMOS) | Low Cycles Divider 3.1 | | | | High Cycles Divider 3.1 | | | | 0x22 |
| 0x19A | | Phase Offset Divider 3.2 | | | | Phase Offset Divider 3.1 | | | | 0x00 |
| 0x19B | | Low Cycles Divider 3.2 | | | | High Cycles Divider 3.2 | | | | 0x11 |
| 0x19C | | Reserved | | Bypass Divider 3.2 | Bypass Divider 3.1 | Divider 3 no sync | Divider 3 force high | Start High Divider 3.2 | Start High Divider 3.1 | 0x00 |
| 0x19D | | Blank | | Reserved | | | | | Divider 3 DCCOFF | 0x00 |
| 0x19E | Divider 4 (LVDS/CMOS) | Low Cycles Divider 4.1 | | | | High Cycles Divider 4.1 | | | | 0x22 |
| 0x19F | | Phase Offset Divider 4.2 | | | | Phase Offset Divider 4.1 | | | | 0x00 |
| 0x1A0 | | Low Cycles Divider 4.2 | | | | High Cycles Divider 4.2 | | | | 0x11 |
| 0x1A1 | | Reserved | | Bypass Divider 4.2 | Bypass Divider 4.1 | Divider 4 no sync | Divider 4 force high | Start High Divider 4.2 | Start High Divider 4.1 | 0x00 |
| 0x1A2 | | Blank | | Reserved | | | | | Divider 4 DCCOFF | 0x00 |
| 0x1A3 | Reserved | | | | | | | | | |
| 0x1A4 to 0x1DF | Blank | | | | | | | | | |
| VCO Divider and CLK Input | | | | | | | | | | |
| 0x1E0 | VCO divider | Blank | | | | Reserved | | VCO Divider | | 0x02 |
| 0x1E1 | Input CLKs | Reserved | | | Power-down clock input section | Power-down VCO clock interface | Power-down VCO and CLK | Select VCO or CLK | Bypass VCO divider | 0x00 |
| 0x1E2 to 0x22A | Blank | | | | | | | | | |

| Reg. Addr. (Hex) | Parameter | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|----------------------|----------------------|-------------|-------|-------|-------|----------|-----------------|-----------------------------------|--|---------------------|
| System | | | | | | | | | | |
| 0x230 | Power-down and sync | Reserved | | | | | Power-down sync | Power-down distribution reference | Soft sync | 0x00 |
| 0x231 | | Blank | | | | Reserved | | | | 0x00 |
| Update All Registers | | | | | | | | | | |
| 0x232 | Update all registers | Blank | | | | | | | Update all registers (self-clearing bit) | 0x00 |

REGISTER MAP DESCRIPTIONS

Table 53 through Table 62 provide a detailed description of each of the control register functions. The registers are listed by hexadecimal address. A range of bits (for example, from Bit 5 through Bit 2) is indicated using a colon and brackets, as follows: [5:2].

Table 53. Serial Port Configuration

| Reg. Addr (Hex) | Bits | Name | Description |
|-----------------|-------|----------------------------|--|
| 0x000 | [7:4] | Mirrored, Bits[3:0] | Bits[7:4] should always mirror Bits[3:0] so that it does not matter whether the part is in MSB or LSB first mode (see Bit 1, Register 0x000). The user should set the bits as follows: Bit 7 = Bit 0. Bit 6 = Bit 1. Bit 5 = Bit 2. Bit 4 = Bit 3. |
| | 3 | Long instruction | Short/long instruction mode. This part uses long instruction mode only, so this bit should always be set to 1. 0: 8-bit instruction (short). 1: 16-bit instruction (long) (default). |
| | 2 | Soft reset | Soft reset. 1: soft reset; restores default values to internal registers. Not self-clearing. Must be cleared to 0 to complete reset operation. |
| | 1 | LSB first | MSB or LSB data orientation. 0: data-oriented MSB first; addressing decrements (default). 1: data-oriented LSB first; addressing increments. |
| | 0 | SDO active | Selects unidirectional or bidirectional data transfer mode. 0: SDIO pin used for write and read; SDO set to high impedance; bidirectional mode (default). 1: SDO used for read, SDIO used for write; unidirectional mode. |
| 0x003 | [7:0] | Part ID (read only) | Uniquely identifies the dash version (-0 through -4) of the AD9516. AD9516-0: 0x01. AD9516-1: 0x41. AD9516-2: 0x81. AD9516-3: 0x43. AD9516-4: 0xC3. |
| 0x004 | 0 | Read back active registers | Selects register bank used for a readback. 0: reads back buffer registers (default). 1: reads back active registers. |

Table 54. PLL

| Reg. Addr. (Hex) | Bits | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|------------------------------------|--|--|-----------------------|------------------|----------------------|----------------------|-----------------------|---|---|------------------------------------|---|---|---------------------------------|-----|---|-----------------------------|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|---------------|
| 0x010 | 7 | PFD polarity | Sets the PFD polarity. Negative polarity is for use (if needed) with external VCO/VCXO only. The on-chip VCO requires positive polarity; Bit 7 = 0. 0: positive; higher control voltage produces higher frequency (default). 1: negative; higher control voltage produces lower frequency. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | [6:4] | CP current | Charge pump current (with CPRSET = 5.1 kΩ). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table><tr><th>6</th><th>5</th><th>4</th><th>I_{CP} (mA)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0.6</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1.2</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1.8</td></tr><tr><td>0</td><td>1</td><td>1</td><td>2.4</td></tr><tr><td>1</td><td>0</td><td>0</td><td>3.0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>3.6</td></tr><tr><td>1</td><td>1</td><td>0</td><td>4.2</td></tr><tr><td>1</td><td>1</td><td>1</td><td>4.8 (default)</td></tr></table> | 6 | 5 | 4 | I _{CP} (mA) | 0 | 0 | 0 | 0.6 | 0 | 0 | 1 | 1.2 | 0 | 1 | 0 | 1.8 | 0 | 1 | 1 | 2.4 | 1 | 0 | 0 | 3.0 | 1 | 0 | 1 | 3.6 | 1 | 1 | 0 | 4.2 | 1 | 1 | 1 | 4.8 (default) |
| | | | 6 | 5 | 4 | I _{CP} (mA) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 0 | 0 | 0.6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 0 | 1 | 1.2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 1 | 0 | 1.8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0 | 1 | 1 | 2.4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | 0 | 3.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | 1 | 3.6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 1 | 0 | 4.2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 1 | 1 | 1 | 4.8 (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | [3:2] | CP mode | Charge pump operating mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <table><tr><th>3</th><th>2</th><th>Charge Pump Mode</th></tr><tr><td>0</td><td>0</td><td>High impedance state.</td></tr><tr><td>0</td><td>1</td><td>Force source current (pump up).</td></tr><tr><td>1</td><td>0</td><td>Force sink current (pump down).</td></tr><tr><td>1</td><td>1</td><td>Normal operation (default).</td></tr></table> | | | 3 | 2 | Charge Pump Mode | 0 | 0 | High impedance state. | 0 | 1 | Force source current (pump up). | 1 | 0 | Force sink current (pump down). | 1 | 1 | Normal operation (default). | | | | | | | | | | | | | | | | | | | | | | |
| 3 | | | 2 | Charge Pump Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | | | 0 | High impedance state. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Force source current (pump up). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Force sink current (pump down). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Normal operation (default). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [1:0] | PLL power-down | PLL operating mode. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table><tr><th>1</th><th>0</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>Normal operation.</td></tr><tr><td>0</td><td>1</td><td>Asynchronous power-down (default).</td></tr><tr><td>1</td><td>0</td><td>Normal operation.</td></tr><tr><td>1</td><td>1</td><td>Synchronous power-down.</td></tr></table> | 1 | 0 | Mode | 0 | 0 | Normal operation. | 0 | 1 | Asynchronous power-down (default). | 1 | 0 | Normal operation. | 1 | 1 | Synchronous power-down. | | | | | | | | | | | | | | | | | | | | | | |
| | | 1 | 0 | Mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0 | 0 | Normal operation. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | Asynchronous power-down (default). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | Normal operation. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | Synchronous power-down. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [7:0] | 14-bit R divider, Bits[7:0] (LSB) | R divider LSBs—lower eight bits (default = 0x01). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [5:0] | 14-bit R divider, Bits[13:8] (MSB) | R divider MSBs—upper six bits (default = 0x00). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [5:0] | 6-bit A counter | A counter (part of N divider) (default = 0x00). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [7:0] | 13-bit B counter, Bits[7:0] (LSB) | B counter (part of N divider)—lower eight bits (default = 0x03). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| [4:0] | 13-bit B counter, Bits[12:8] (MSB) | B counter (part of N divider)—upper five bits (default = 0x00). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x016 | 7 | Set CP pin to V _{CP} /2 | Sets the CP pin to one-half of the V _{CP} supply voltage. 0: CP normal operation (default). 1: CP pin set to V _{CP} /2. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 6 | Reset R counter | Resets R counter (R divider). 0: normal (default). 1: holds the R counter in reset. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 5 | Reset A, B counters | Resets A and B counters (part of N divider). 0: normal (default). 1: holds the A and B counters in reset. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | Reset all counters | Resets R, A, and B counters. 0: normal (default). 1: holds the R, A, and B counters in reset. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | B counter bypass | B counter bypass. This is valid only when operating the prescaler in FD mode. 0: normal (default). 1: B counter is set to divide-by-1. This allows the prescaler setting to determine the divide for the N divider. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | | | | | |
|------------------|-------|--------------------|---|---|---|------|--------------------------------------|---|-------------------------|--|
| 0x016 | [2:0] | Prescaler P | Prescaler: DM = dual modulus, and FD = fixed divide. | | | | | | | |
| | | | 2 | 1 | 0 | Mode | Prescaler | | | |
| | | | 0 | 0 | 0 | FD | Divide-by-1. | | | |
| | | | 0 | 0 | 1 | FD | Divide-by-2. | | | |
| | | | 0 | 1 | 0 | DM | Divide-by-2 (2/3 mode). | | | |
| | | | 0 | 1 | 1 | DM | Divide-by-4 (4/5 mode). | | | |
| | | | 1 | 0 | 0 | DM | Divide-by-8 (8/9 mode). | | | |
| | | | 1 | 0 | 1 | DM | Divide-by-16 (16/17 mode). | | | |
| | | | 1 | 1 | 0 | DM | Divide-by-32 (32/33 mode) (default). | | | |
| | | | 1 | 1 | 1 | FD | Divide-by-3. | | | |
| 0x017 | [7:2] | STATUS pin control | Selects the signal that is connected to the STATUS pin. | | | | | | | |
| | | | 7 | 6 | 5 | 4 | 3 | 2 | Level or Dynamic Signal | Signal at STATUS Pin |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | LVL | Ground (dc) (default). |
| | | | 0 | 0 | 0 | 0 | 0 | 1 | DYN | N divider output (after the delay). |
| | | | 0 | 0 | 0 | 0 | 1 | 0 | DYN | R divider output (after the delay). |
| | | | 0 | 0 | 0 | 0 | 1 | 1 | DYN | A divider output. |
| | | | 0 | 0 | 0 | 1 | 0 | 0 | DYN | Prescaler output. |
| | | | 0 | 0 | 0 | 1 | 0 | 1 | DYN | PFD up pulse. |
| | | | 0 | 0 | 0 | 1 | 1 | 0 | DYN | PFD down pulse. |
| | | | 0 | X | X | X | X | X | LVL | Ground (dc); for all other cases of 0XXXXX not specified above. The selections that follow are the same as REFMON. |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | LVL | Ground (dc). |
| | | | 1 | 0 | 0 | 0 | 0 | 1 | DYN | REF1 clock (differential reference when in differential mode). |
| | | | 1 | 0 | 0 | 0 | 1 | 0 | DYN | REF2 clock (not available in differential mode). |
| | | | 1 | 0 | 0 | 0 | 1 | 1 | DYN | Selected reference to PLL (differential reference when in differential mode). |
| | | | 1 | 0 | 0 | 1 | 0 | 0 | DYN | Unselected reference to PLL (not available in differential mode). |
| | | | 1 | 0 | 0 | 1 | 0 | 1 | LVL | Status of selected reference (status of differential reference); active high. |
| | | | 1 | 0 | 0 | 1 | 1 | 0 | LVL | Status of unselected reference (not available in differential mode); active high. |
| | | | 1 | 0 | 0 | 1 | 1 | 1 | LVL | Status REF1 frequency (active high). |
| | | | 1 | 0 | 1 | 0 | 0 | 0 | LVL | Status REF2 frequency (active high). |
| | | | 1 | 0 | 1 | 0 | 0 | 1 | LVL | (Status REF1 frequency) AND (status REF2 frequency). |
| | | | 1 | 0 | 1 | 0 | 1 | 0 | LVL | (DLD) AND (status of selected reference) AND (status of VCO). |
| | | | 1 | 0 | 1 | 0 | 1 | 1 | LVL | Status of VCO frequency (active high). |
| | | | 1 | 0 | 1 | 1 | 0 | 0 | LVL | Selected reference (low = REF1, high = REF2). |
| | | | 1 | 0 | 1 | 1 | 0 | 1 | LVL | Digital lock detect (DLD); active high. |
| | | | 1 | 0 | 1 | 1 | 1 | 0 | LVL | Holdover active (active high). |
| | | | 1 | 0 | 1 | 1 | 1 | 1 | LVL | LD pin comparator output (active high). |
| | | | 1 | 1 | 0 | 0 | 0 | 0 | LVL | VS (PLL supply). |
| | | | 1 | 1 | 0 | 0 | 0 | 1 | DYN | REF1 clock (differential reference when in differential mode). |
| | | | 1 | 1 | 0 | 0 | 1 | 0 | DYN | REF2 clock (not available in differential mode). |
| | | | 1 | 1 | 0 | 0 | 1 | 1 | DYN | Selected reference to PLL (differential reference when in differential mode). |
| | | | 1 | 1 | 0 | 1 | 0 | 0 | DYN | Unselected reference to PLL (not available when in differential mode). |
| | | | 1 | 1 | 0 | 1 | 0 | 1 | LVL | Status of selected reference (status of differential reference); active low. |
| | | | 1 | 1 | 0 | 1 | 1 | 0 | LVL | Status of unselected reference (not available in differential mode); active low. |
| | | | 1 | 1 | 0 | 1 | 1 | 1 | LVL | Status of REF1 frequency (active low). |
| | | | 1 | 1 | 1 | 0 | 0 | 0 | LVL | Status of REF2 frequency (active low). |
| | | | 1 | 1 | 1 | 0 | 0 | 1 | LVL | (Status of REF1 frequency) AND (status of REF2 frequency). |
| | | | 1 | 1 | 1 | 0 | 1 | 0 | LVL | (DLD) AND (status of selected reference) AND (status of VCO). |
| | | | 1 | 1 | 1 | 0 | 1 | 1 | LVL | Status of VCO frequency (active low). |
| | | | 1 | 1 | 1 | 1 | 0 | 0 | LVL | Selected reference (low = REF2, high = REF1). |
| | | | 1 | 1 | 1 | 1 | 0 | 1 | LVL | Digital lock detect (DLD) (active low). |
| | | | 1 | 1 | 1 | 1 | 1 | 0 | LVL | Holdover active (active low). |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | LVL | LD pin comparator output (active low). |

| Reg. Addr. (Hex) | Bits | Name | Description | | |
|------------------|-------|---------------------------------------|---|----------|--------------------------------------|
| 0x017 | [1:0] | Antibacklash pulse width | 1 | 0 | Antibacklash Pulse Width (ns) |
| | | | 0 | 0 | 2.9 (default). |
| | | | 0 | 1 | 1.3. |
| | | | 1 | 0 | 6.0. |
| | | | 1 | 1 | 2.9. |
| 0x018 | [6:5] | Lock detect counter | Required consecutive number of PFD cycles with edges inside lock detect window before the DLD indicates a locked condition. | | |
| | | | 6 | 5 | PFD Cycles to Determine Lock |
| | | | 0 | 0 | 5 (default). |
| | | | 0 | 1 | 16. |
| | | | 1 | 0 | 64. |
| | | | 1 | 1 | 255. |
| | 4 | Digital lock detect window | If the time difference of the rising edges at the inputs to the PFD is less than the lock detect window time, the digital lock detect flag is set. The flag remains set until the time difference is greater than the loss-of-lock threshold. 0: high range (default). 1: low range. | | |
| | 3 | Disable digital lock detect | Digital lock detect operation. 0: normal lock detect operation (default). 1: disables lock detect. | | |
| | [2:1] | VCO cal divider | VCO calibration divider. Divider used to generate the VCO calibration clock from the PLL reference clock. | | |
| | | | 2 | 1 | VCO Calibration Clock Divider |
| | | | 0 | 0 | 2. |
| | | | 0 | 1 | 4. |
| | | | 1 | 0 | 8. |
| | | | 1 | 1 | 16 (default). |
| | [0] | VCO cal now | Bit used to initiate the VCO calibration. This bit must be toggled from 0 to 1 in the active registers. To initiate calibration, use the following three steps: first, ensure that the input reference signal is present; second, set to 0 (if not zero already), followed by an update bit (Register 0x232, Bit 0); and third, program to 1, followed by another update bit (Register 0x232, Bit 0). | | |
| 0x019 | [7:6] | R, A, B counters SYNC pin reset | 7 | 6 | Action |
| | | | 0 | 0 | Does nothing on SYNC (default). |
| | | | 0 | 1 | Asynchronous reset. |
| | | | 1 | 0 | Synchronous reset. |
| | | | 1 | 1 | Does nothing on SYNC. |
| 0x019 | [5:3] | R path delay | R path delay (default = 0x00) (see Table 2). | | |
| | [2:0] | N path delay | N path delay (default = 0x00) (see Table 2). | | |
| | [6] | Reference frequency monitor threshold | Sets the reference (REF1/REF2) frequency monitor's detection threshold frequency. This does not affect the VCO frequency monitor's detection threshold (see Table 16: REF1, REF2, and VCO Frequency Status Monitor parameter). 0: frequency valid if frequency is above the higher frequency threshold (default). 1: frequency valid if frequency is above the lower frequency threshold. | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | | | | |
|------------------|-------|--------------------------------|--|---|---|---|---|---|-------------------------|
| 0x01A | [5:0] | LD pin control | Selects the signal that is connected to the LD pin. | | | | | | |
| | | | 5 | 4 | 3 | 2 | 1 | 0 | Level or Dynamic Signal |
| | | | 0 | 0 | 0 | 0 | 0 | 0 | LVL |
| | | | 0 | 0 | 0 | 0 | 0 | 1 | DYN |
| | | | 0 | 0 | 0 | 0 | 1 | 0 | DYN |
| | | | 0 | 0 | 0 | 0 | 1 | 1 | HIZ |
| | | | 0 | 0 | 0 | 1 | 0 | 0 | CUR |
| | | | 0 | X | X | X | X | X | LVL |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | LVL |
| | | | 1 | 0 | 0 | 0 | 0 | 1 | DYN |
| | | | 1 | 0 | 0 | 0 | 1 | 0 | DYN |
| | | | 1 | 0 | 0 | 0 | 1 | 1 | DYN |
| | | | 1 | 0 | 0 | 1 | 0 | 0 | DYN |
| | | | 1 | 0 | 0 | 1 | 0 | 1 | LVL |
| | | | 1 | 0 | 0 | 1 | 1 | 0 | LVL |
| | | | 1 | 0 | 0 | 1 | 1 | 1 | LVL |
| | | | 1 | 0 | 1 | 0 | 0 | 0 | LVL |
| | | | 1 | 0 | 1 | 0 | 0 | 1 | LVL |
| | | | 1 | 0 | 1 | 0 | 1 | 0 | LVL |
| | | | 1 | 0 | 1 | 0 | 1 | 1 | LVL |
| | | | 1 | 0 | 1 | 1 | 0 | 0 | LVL |
| | | | 1 | 0 | 1 | 1 | 0 | 1 | LVL |
| | | | 1 | 0 | 1 | 1 | 1 | 0 | LVL |
| | | | 1 | 0 | 1 | 1 | 1 | 1 | LVL |
| | | | 1 | 1 | 0 | 0 | 0 | 0 | LVL |
| | | | 1 | 1 | 0 | 0 | 0 | 1 | DYN |
| | | | 1 | 1 | 0 | 0 | 1 | 0 | DYN |
| | | | 1 | 1 | 0 | 0 | 1 | 1 | DYN |
| | | | 1 | 1 | 0 | 1 | 0 | 0 | DYN |
| | | | 1 | 1 | 0 | 1 | 0 | 1 | LVL |
| | | | 1 | 1 | 0 | 1 | 1 | 0 | LVL |
| | | | 1 | 1 | 0 | 1 | 1 | 1 | LVL |
| | | | 1 | 1 | 1 | 0 | 0 | 0 | LVL |
| | | | 1 | 1 | 1 | 0 | 0 | 1 | LVL |
| | | | 1 | 1 | 1 | 0 | 1 | 0 | LVL |
| | | | 1 | 1 | 1 | 0 | 1 | 1 | LVL |
| | | | 1 | 1 | 1 | 1 | 0 | 0 | LVL |
| | | | 1 | 1 | 1 | 1 | 0 | 1 | LVL |
| | | | 1 | 1 | 1 | 1 | 1 | 0 | LVL |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | LVL |
| | | | Signal at LD Pin | | | | | | |
| | | | Digital lock detect (high = lock, low = unlock) (default). | | | | | | |
| | | | P-channel, open-drain lock detect (analog lock detect). | | | | | | |
| | | | N-channel, open-drain lock detect (analog lock detect). | | | | | | |
| | | | High-Z LD pin. | | | | | | |
| | | | Current source lock detect (110 μ A when DLD is true). | | | | | | |
| | | | Ground (dc); for all other cases of 0XXXXX not specified above. | | | | | | |
| | | | The selections that follow are the same as REFMON. | | | | | | |
| | | | Ground (dc). | | | | | | |
| | | | REF1 clock (differential reference when in differential mode). | | | | | | |
| | | | REF2 clock (not available in differential mode). | | | | | | |
| | | | Selected reference to PLL (differential reference when in differential mode). | | | | | | |
| | | | Unselected reference to PLL (not available in differential mode). | | | | | | |
| | | | Status of selected reference (status of differential reference); active high. | | | | | | |
| | | | Status of unselected reference (not available in differential mode); active high. | | | | | | |
| | | | Status REF1 frequency (active high). | | | | | | |
| | | | Status REF2 frequency (active high). | | | | | | |
| | | | (Status REF1 frequency) AND (status REF2 frequency). | | | | | | |
| | | | (DLD) AND (status of selected reference) AND (status of VCO). | | | | | | |
| | | | Status of VCO frequency (active high). | | | | | | |
| | | | Selected reference (low = REF1, high = REF2). | | | | | | |
| | | | Digital lock detect (DLD); active high. | | | | | | |
| | | | Holdover active (active high). | | | | | | |
| | | | Not available. Do not use. | | | | | | |
| | | | VS (PLL supply). | | | | | | |
| | | | REF1 clock (differential reference when in differential mode). | | | | | | |
| | | | REF2 clock (not available in differential mode). | | | | | | |
| | | | Selected reference to PLL (differential reference when in differential mode). | | | | | | |
| | | | Unselected reference to PLL (not available when in differential mode). | | | | | | |
| | | | Status of selected reference (status of differential reference); active low. | | | | | | |
| | | | Status of unselected reference (not available in differential mode); active low. | | | | | | |
| | | | Status of REF1 frequency (active low). | | | | | | |
| | | | Status of REF2 frequency (active low). | | | | | | |
| | | | (Status of REF1 frequency) AND (status of REF2 frequency). | | | | | | |
| | | | (DLD) AND (status of selected reference) AND (status of VCO). | | | | | | |
| | | | Status of VCO frequency (active low). | | | | | | |
| | | | Selected reference (low = REF2, high = REF1). | | | | | | |
| | | | Digital lock detect (DLD); active low. | | | | | | |
| | | | Holdover active (active low). | | | | | | |
| | | | Not available. Do not use. | | | | | | |
| 0x01B | 7 | VCO frequency monitor | Enables or disables VCO frequency monitor. 0: disables VCO frequency monitor (default). 1: enables VCO frequency monitor. | | | | | | |
| | 6 | REF2 (REFIN) frequency monitor | Enables or disables REF2 frequency monitor. 0: disables REF2 frequency monitor (default). 1: enables REF2 frequency monitor. | | | | | | |
| | 5 | REF1 (REFIN) frequency monitor | REF1 (REFIN) frequency monitor enable; this is for both REF1 (single-ended) and REFIN (differential) inputs (as selected by differential reference mode). 0: disables REF1 (REFIN) frequency monitor (default). 1: enables REF1 (REFIN) frequency monitor. | | | | | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | | | | |
|------------------|-------|-----------------------------|--|---|-----|---|---|-------------------------|---|
| 0x01B | [4:0] | REFMON pin control | Selects the signal that is connected to the REFMON pin. | | | | | | |
| | | | | | | | | Level or Dynamic Signal | |
| | | | 4 | 3 | 2 | 1 | 0 | | Signal at REFMON Pin |
| | | | 0 | 0 | 0 | 0 | 0 | LVL | Ground (dc) (default). |
| | | | 0 | 0 | 0 | 0 | 1 | DYN | REF1 clock (differential reference when in differential mode). |
| | | | 0 | 0 | 0 | 1 | 0 | DYN | REF2 clock (not available in differential mode). |
| | | | 0 | 0 | 0 | 1 | 1 | DYN | Selected reference to PLL (differential reference when in differential mode). |
| | | | 0 | 0 | 1 | 0 | 0 | DYN | Unselected reference to PLL (not available in differential mode). |
| | | | 0 | 0 | 1 | 0 | 1 | LVL | Status of selected reference (status of differential reference); active high. |
| | | | 0 | 0 | 1 | 1 | 0 | LVL | Status of unselected reference (not available in differential mode); active high. |
| | | | 0 | 0 | 1 | 1 | 1 | LVL | Status REF1 frequency (active high). |
| | | | 0 | 1 | 0 | 0 | 0 | LVL | Status REF2 frequency (active high). |
| | | | 0 | 1 | 0 | 0 | 1 | LVL | (Status REF1 frequency) AND (status REF2 frequency). |
| | | | 0 | 1 | 0 | 1 | 0 | LVL | (DLD) AND (status of selected reference) AND (status of VCO). |
| | | | 0 | 1 | 0 | 1 | 1 | LVL | Status of VCO frequency (active high). |
| | | | 0 | 1 | 1 | 0 | 0 | LVL | Selected reference (low = REF1, high = REF2). |
| | | | 0 | 1 | 1 | 0 | 1 | LVL | Digital lock detect (DLD); active low. |
| | | | 0 | 1 | 1 | 1 | 0 | LVL | Holdover active (active high). |
| | | | 0 | 1 | 1 | 1 | 1 | LVL | LD pin comparator output (active high). |
| | | | 1 | 0 | 0 | 0 | 0 | LVL | VS (PLL supply). |
| | | | 1 | 0 | 0 | 0 | 1 | DYN | REF1 clock (differential reference when in differential mode). |
| | | | 1 | 0 | 0 | 1 | 0 | DYN | REF2 clock (not available in differential mode). |
| | | | 1 | 0 | 0 | 1 | 1 | DYN | Selected reference to PLL (differential reference when in differential mode). |
| | | | 1 | 0 | 1 | 0 | 0 | DYN | Unselected reference to PLL (not available when in differential mode). |
| | | | 1 | 0 | 1 | 0 | 1 | LVL | Status of selected reference (status of differential reference); active low. |
| | | | 1 | 0 | 1 | 1 | 0 | LVL | Status of unselected reference (not available in differential mode); active low. |
| | | | 1 | 0 | 1 | 1 | 1 | LVL | Status of REF1 frequency (active low). |
| | | | 1 | 1 | 0 | 0 | 0 | LVL | Status of REF2 frequency (active low). |
| | | | 1 | 1 | 0 | 0 | 1 | LVL | (Status of REF1 frequency) AND (Status of REF2 frequency). |
| | | | 1 | 1 | 0 | 1 | 0 | LVL | (DLD) AND (Status of selected reference) AND (Status of VCO). |
| 1 | 1 | 0 | 1 | 1 | LVL | Status of VCO frequency (active low). | | | |
| 1 | 1 | 1 | 0 | 0 | LVL | Selected reference (low = REF2, high = REF1). | | | |
| 1 | 1 | 1 | 0 | 1 | LVL | Digital lock detect (DLD); active low. | | | |
| 1 | 1 | 1 | 1 | 0 | LVL | Holdover active (active low). | | | |
| 1 | 1 | 1 | 1 | 1 | LVL | LD pin comparator output (active low). | | | |
| 0x01C | 7 | Disable switchover deglitch | Disables or enables the switchover deglitch circuit. 0: enables switchover deglitch circuit (default). 1: disables switchover deglitch circuit. | | | | | | |
| | 6 | Select REF2 | If Register 0x01C, Bit 5 = 0, select reference for PLL. 0: selects REF1 (default). 1: selects REF2. | | | | | | |
| | 5 | Use REF_SEL pin | Sets method of PLL reference selection. 0: uses Register 0x01C, Bit 6 (default). 1: uses REF_SEL pin. | | | | | | |
| | 4 | Reserved | 0: (default). | | | | | | |
| | 3 | Reserved | 0: (default). | | | | | | |
| | 2 | REF2 power-on | This bit turns the REF2 power on. 0: REF2 power off (default). 1: REF2 power on. | | | | | | |
| | 1 | REF1 power-on | This bit turns the REF1 power on. 0: REF1 power off (default). 1: REF1 power on. | | | | | | |
| | 0 | Differential reference | Selects the PLL reference mode, differential or single-ended. Single-ended must be selected for the automatic switchover or REF1 and REF2 to work. 0: single-ended reference mode (default). 1: differential reference mode. | | | | | | |

| Reg. Addr. (Hex) | Bits | Name | Description |
|------------------|------|-----------------------------|---|
| 0x01D | 4 | PLL status register disable | Disables the PLL status register readback. 0: PLL status register enable (default). 1: PLL status register disable. |
| | 3 | LD pin comparator enable | Enables the LD pin voltage comparator. This function is used with the LD pin current source lock detect mode. When in the internal (automatic) holdover mode, this function enables the use of the voltage on the LD pin to determine if the PLL was previously in a locked state (see Figure 53). Otherwise, this function can be used with the REFMON and STATUS pins to monitor the voltage on this pin. 0: disables LD pin comparator; internal/automatic holdover controller treats this pin as true (high) (default). 1: enables LD pin comparator. |
| | 2 | Holdover enable | Along with Bit 0, enables the holdover function. Automatic holdover must be disabled during VCO calibration. 0: holdover disabled (default). 1: holdover enabled. |
| | 1 | External holdover control | Enables the external hold control through the $\overline{\text{SYNC}}$ pin. (This disables the internal holdover mode.) 0: automatic holdover mode—holdover controlled by automatic holdover circuit. (default) 1: external holdover mode—holdover controlled by $\overline{\text{SYNC}}$ pin. |
| | 0 | Holdover enable | Along with Bit 2, enables the holdover function. Automatic holdover must be disabled during VCO calibration. 0: holdover disabled (default). 1: holdover enabled. |
| | | | |
| 0x01F | 6 | VCO cal finished | Read-only register. Indicates status of the VCO calibration. 0: VCO calibration not finished. 1: VCO calibration finished. |
| | 5 | Holdover active | Read-only register. Indicates if the part is in the holdover state (see Figure 53). This is not the same as holdover enabled. 0: not in holdover. 1: holdover state active. |
| | 4 | REF2 selected | Read-only register. Indicates which PLL reference is selected as the input to the PLL. 0: REF1 selected (or differential reference if in differential mode). 1: REF2 selected. |
| | 3 | VCO frequency > threshold | Read-only register. Indicates if the VCO frequency is greater than the threshold (see Table 16, REF1, REF2, and VCO frequency status monitor). 0: VCO frequency is less than the threshold. 1: VCO frequency is greater than the threshold. |
| | 2 | REF2 frequency > threshold | Read-only register. Indicates if the frequency of the signal at REF2 is greater than the threshold frequency set by Register 0x01A, Bit 6. 0: REF2 frequency is less than threshold frequency. 1: REF2 frequency is greater than threshold frequency. |
| | 1 | REF1 frequency > threshold | Read-only register. Indicates if the frequency of the signal at REF2 is greater than the threshold frequency set by Register 0x01A, Bit 6. 0: REF1 frequency is less than threshold frequency. 1: REF1 frequency is greater than threshold frequency. |
| | 0 | Digital lock detect | Read-only register. Digital lock detect. 0: PLL is not locked. 1: PLL is locked. |

Table 55. Fine Delay Adjust—OUT6 to OUT9

| Reg. Addr. (Hex) | Bits | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|-------|----------------------|---|---|---|---|----------------------|---|---|---|---------------|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|------|---|---|---|------|---|---|---|------|---|
| 0x0A0 | 0 | OUT6 delay bypass | Bypasses or uses the delay function. 0: uses delay function. 1: bypasses delay function (default). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0A1 | [5:3] | OUT6 ramp capacitors | Selects the number of ramp capacitors used by the delay function. The combination of the number of the capacitors and the ramp current sets the delay full scale. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table><tr><th>5</th><th>4</th><th>3</th><th>Number of Capacitors</th></tr><tr><td>0</td><td>0</td><td>0</td><td>4 (default)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>3</td></tr><tr><td>0</td><td>1</td><td>0</td><td>3</td></tr><tr><td>0</td><td>1</td><td>1</td><td>2</td></tr><tr><td>1</td><td>0</td><td>0</td><td>3</td></tr><tr><td>1</td><td>0</td><td>1</td><td>2</td></tr><tr><td>1</td><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> | 5 | 4 | 3 | Number of Capacitors | 0 | 0 | 0 | 4 (default) | 0 | 0 | 1 | 3 | 0 | 1 | 0 | 3 | 0 | 1 | 1 | 2 | 1 | 0 | 0 | 3 | 1 | 0 | 1 | 2 | 1 | 1 | 0 | 2 | 1 |
| 5 | 4 | 3 | Number of Capacitors | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 4 (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | [2:0] | OUT6 ramp current | Ramp current for the delay function. The combination of the number of capacitors and the ramp current sets the delay full scale. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table><tr><th>2</th><th>1</th><th>0</th><th>Current (μA)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>200 (default)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>400</td></tr><tr><td>0</td><td>1</td><td>0</td><td>600</td></tr><tr><td>0</td><td>1</td><td>1</td><td>800</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1000</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1200</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1400</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1600</td></tr></table> | 2 | 1 | 0 | Current (μA) | 0 | 0 | 0 | 200 (default) | 0 | 0 | 1 | 400 | 0 | 1 | 0 | 600 | 0 | 1 | 1 | 800 | 1 | 0 | 0 | 1000 | 1 | 0 | 1 | 1200 | 1 | 1 | 0 | 1400 | 1 |
| 2 | 1 | 0 | Current (μA) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 200 (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 400 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 600 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 800 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1400 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1600 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0A2 | [5:0] | OUT6 delay fraction | Selects the fraction of the full-scale delay desired (6-bit binary). A setting of 000000 gives zero delay. Only delay values up to 47 decimals (101111b; 0x2F) are supported (default = 0x00). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0A3 | 0 | OUT7 delay bypass | Bypasses or uses the delay function. 0: use delay function. 1: bypass delay function (default). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0A4 | [5:3] | OUT7 ramp capacitors | Selects the number of ramp capacitors used by the delay function. The combination of the number of the capacitors and the ramp current sets the delay full scale. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table><tr><th>5</th><th>4</th><th>3</th><th>Number of Capacitors</th></tr><tr><td>0</td><td>0</td><td>0</td><td>4 (default)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>3</td></tr><tr><td>0</td><td>1</td><td>0</td><td>3</td></tr><tr><td>0</td><td>1</td><td>1</td><td>2</td></tr><tr><td>1</td><td>0</td><td>0</td><td>3</td></tr><tr><td>1</td><td>0</td><td>1</td><td>2</td></tr><tr><td>1</td><td>1</td><td>0</td><td>2</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> | 5 | 4 | 3 | Number of Capacitors | 0 | 0 | 0 | 4 (default) | 0 | 0 | 1 | 3 | 0 | 1 | 0 | 3 | 0 | 1 | 1 | 2 | 1 | 0 | 0 | 3 | 1 | 0 | 1 | 2 | 1 | 1 | 0 | 2 | 1 |
| 5 | 4 | 3 | Number of Capacitors | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 4 (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | |
|------------------|-------|----------------------|--|---|------|----------------------|
| 0x0A4 | [2:0] | OUT7 ramp current | Ramp current for the delay function. The combination of the number of capacitors and the ramp current sets the delay full scale. | | | |
| | | | 2 | 1 | 0 | Current (μA) |
| | | | 0 | 0 | 0 | 200 (default) |
| | | | 0 | 0 | 1 | 400 |
| | | | 0 | 1 | 0 | 600 |
| | | | 0 | 1 | 1 | 800 |
| | | | 1 | 0 | 0 | 1000 |
| | | | 1 | 0 | 1 | 1200 |
| | | | 1 | 1 | 0 | 1400 |
| 1 | 1 | 1 | 1600 | | | |
| 0x0A5 | [5:0] | OUT7 delay fraction | Selects the fraction of the full-scale delay desired (6-bit binary). A setting of 000000 gives zero delay. Only delay values up to 47 decimals (101111b; 0x2F) are supported (default = 0x00). | | | |
| 0x0A6 | 0 | OUT8 delay bypass | Bypasses or uses the delay function. 0: uses delay function. 1: bypasses delay function (default). | | | |
| 0x0A7 | [5:3] | OUT8 ramp capacitors | Selects the number of ramp capacitors used by the delay function. The combination of the number of capacitors and the ramp current sets the delay full scale. | | | |
| | | | 5 | 4 | 3 | Number of Capacitors |
| | | | 0 | 0 | 0 | 4 (default) |
| | | | 0 | 0 | 1 | 3 |
| | | | 0 | 1 | 0 | 3 |
| | | | 0 | 1 | 1 | 2 |
| | | | 1 | 0 | 0 | 3 |
| | | | 1 | 0 | 1 | 2 |
| | | | 1 | 1 | 0 | 2 |
| | 1 | 1 | 1 | 1 | | |
| | [2:0] | OUT8 ramp current | Ramp current for the delay function. The combination of the number of capacitors and the ramp current sets the delay full scale. | | | |
| | | | 2 | 1 | 0 | Current (μA) |
| | | | 0 | 0 | 0 | 200 (default) |
| | | | 0 | 0 | 1 | 400 |
| | | | 0 | 1 | 0 | 600 |
| | | | 0 | 1 | 1 | 800 |
| | | | 1 | 0 | 0 | 1000 |
| 1 | | | 0 | 1 | 1200 | |
| 1 | 1 | 0 | 1400 | | | |
| 1 | 1 | 1 | 1600 | | | |
| 0x0A8 | [5:0] | OUT8 delay fraction | Selects the fraction of the full-scale delay desired (6-bit binary). A setting of 000000 gives zero delay. Only delay values up to 47 decimals (101111b; 0x2F) are supported (default = 0x00). | | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|-------|----------------------|--|---|---|---|----------------------|---|---|---|---------------|---|---|---|-----|---|---|---|-----|---|---|---|-----|---|---|---|------|---|---|---|------|---|---|---|------|---|
| 0x0A9 | 0 | OUT9 delay bypass | Bypasses or uses the delay function. 0: uses delay function. 1: bypasses delay function (default). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0AA | [5:3] | OUT9 ramp capacitors | Selects the number of ramp capacitors used by the delay function. The combination of the number of capacitors and the ramp current sets the delay full scale. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table> <tr> <th>5</th><th>4</th><th>3</th><th>Number of Capacitors</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>4 (default)</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>3</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>3</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>2</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>3</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>2</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>2</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td></tr> </table> | 5 | 4 | 3 | Number of Capacitors | 0 | 0 | 0 | 4 (default) | 0 | 0 | 1 | 3 | 0 | 1 | 0 | 3 | 0 | 1 | 1 | 2 | 1 | 0 | 0 | 3 | 1 | 0 | 1 | 2 | 1 | 1 | 0 | 2 | 1 |
| 5 | 4 | 3 | Number of Capacitors | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 4 (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | [2:0] | OUT9 ramp current | Ramp current for the delay function. The combination of the number of capacitors and the ramp current sets the delay full scale. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | <table> <tr> <th>2</th><th>1</th><th>0</th><th>Current Value (μA)</th></tr> <tr><td>0</td><td>0</td><td>0</td><td>200 (default)</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>400</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>600</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>800</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1000</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1200</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1400</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1600</td></tr> </table> | 2 | 1 | 0 | Current Value (μA) | 0 | 0 | 0 | 200 (default) | 0 | 0 | 1 | 400 | 0 | 1 | 0 | 600 | 0 | 1 | 1 | 800 | 1 | 0 | 0 | 1000 | 1 | 0 | 1 | 1200 | 1 | 1 | 0 | 1400 | 1 |
| 2 | 1 | 0 | Current Value (μA) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 200 (default) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 400 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 600 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 800 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1000 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1200 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1400 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1600 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0AB | [5:0] | OUT9 delay fraction | Selects the fraction of the full-scale delay desired (6-bit binary). A setting of 000000 gives zero delay. Only delay values up to 47 decimals (101111b; 0x2F) are supported (default = 0x00). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 56. LVPECL Outputs

| Reg. Addr. (Hex) | Bits | Name | Description | | | |
|------------------|-------|----------------------------------|--|---|-----------------------------|--------|
| 0x0F0 | 4 | OUT0 invert | Sets the output polarity. 0: noninverting (default). 1: inverting. | | | |
| | [3:2] | OUT0 LVPECL differential voltage | Sets the LVPECL output differential voltage (V _{OD}). | | | |
| | | | 3 | 2 | V _{OD} (mV) | |
| | | | 0 | 0 | 400 | |
| | | | 0 | 1 | 600 | |
| | | | 1 | 0 | 780 (default) | |
| | | 1 | 1 | 960 | | |
| | [1:0] | OUT0 power-down | LVPECL power-down modes. | | | |
| | | | 1 | 0 | Mode | Output |
| | | | 0 | 0 | Normal operation (default). | On |
| 0 | | | 1 | Partial power-down, reference on; use only if there are no external load resistors. | Off | |
| 1 | | | 0 | Partial power-down, reference on, safe LVPECL power-down. | Off | |
| | 1 | 1 | Total power-down, reference off; use only if there are no external load resistors. | Off | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | |
|------------------|-------|--|--|---|---|--------|
| 0x0F1 | 4 | OUT1 invert | Sets the output polarity. 0: noninverting (default). 1: inverting. | | | |
| | [3:2] | OUT1 LVPECL differential voltage | Sets the LVPECL output differential voltage (V _{OD}). | | | |
| | | | 3 | 2 | V _{OD} (mV) | |
| | | | 0 | 0 | 400 | |
| | | | 0 | 1 | 600 | |
| | | | 1 | 0 | 780 (default) | |
| | 1 | 1 | 960 | | | |
| | | | LVPECL power-down modes. | | | |
| | | | 1 | 0 | Mode | Output |
| | | | 0 | 0 | Normal operation. | On |
| 0 | | | 1 | Partial power-down, reference on; use only if there are no external load resistors. | Off | |
| 1 | 0 | Partial power-down, reference on, safe LVPECL power-down (default). | | Off | | |
| | | Total power-down, reference off; use only if there are no external load resistors. | | Off | | |
| | | 0x0F2 | | | | |
| | | 4 | OUT2 invert | Sets the output polarity. 0: noninverting (default). 1: inverting. | | |
| 0x0F2 | [3:2] | OUT2 LVPECL differential voltage | Sets the LVPECL output differential voltage (V _{OD}). | | | |
| | | | 3 | 2 | V _{OD} (mV) | |
| | | | 0 | 0 | 400 | |
| | | | 0 | 1 | 600 | |
| | | | 1 | 0 | 780 (default) | |
| | 1 | 1 | 960 | | | |
| | | | LVPECL power-down modes. | | | |
| | | | 1 | 0 | Mode | Output |
| | | | 0 | 0 | Normal operation (default). | On |
| | | | 0 | 1 | Partial power-down, reference on; use only if there are no external load resistors. | Off |
| 1 | 0 | Partial power-down, reference on, safe LVPECL power-down. | | Off | | |
| | | Total power-down, reference off; use only if there are no external load resistors. | | Off | | |
| | | 0x0F3 | | | | |
| | | 4 | OUT3 invert | Sets the output polarity. 0: noninverting (default). 1: inverting. | | |
| 0x0F3 | [3:2] | OUT3 LVPECL differential voltage | Sets the LVPECL output differential voltage (V _{OD}). | | | |
| | | | 3 | 2 | V _{OD} (mV) | |
| | | | 0 | 0 | 400 | |
| | | | 0 | 1 | 600 | |
| | | | 1 | 0 | 780 (default) | |
| | 1 | 1 | 960 | | | |
| | | | LVPECL power-down modes. | | | |
| | | | 1 | 0 | Mode | Output |
| | | | 0 | 0 | Normal operation. | On |
| | | | 0 | 1 | Partial power-down, reference on; use only if there are no external load resistors. | Off |
| 1 | 0 | Partial power-down, reference on, safe LVPECL power-down (default). | | Off | | |
| | | Total power-down, reference off; use only if there are no external load resistors. | | Off | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | |
|------------------|-------|----------------------------------|--|---|---|--------|
| 0x0F4 | 4 | OUT4 invert | Sets the output polarity. 0: noninverting (default). 1: inverting. | | | |
| | [3:2] | OUT4 LVPECL differential voltage | Sets the LVPECL output differential voltage (V _{OD}). | | | |
| | | | 3 | 2 | V _{OD} (mV) | |
| | | | 0 | 0 | 400 | |
| | | | 0 | 1 | 600 | |
| | | | 1 | 0 | 780 (default) | |
| | [1:0] | OUT4 power-down | 1 | 1 | 960 | |
| | | | LVPECL power-down modes. | | | |
| | | | 1 | 0 | Mode | Output |
| | | | 0 | 0 | Normal operation (default). | On |
| | | | 0 | 1 | Partial power-down, reference on; use only if there are no external load resistors. | Off |
| | [1:0] | OUT4 power-down | 1 | 0 | Partial power-down, reference on, safe LVPECL power-down. | Off |
| | | | 1 | 1 | Total power-down, reference off; use only if there are no external load resistors. | Off |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| 0x0F5 | 4 | OUT5 invert | Sets the output polarity. 0: noninverting (default). 1: inverting. | | | |
| | [3:2] | OUT5 LVPECL differential voltage | Sets the LVPECL output differential voltage (V _{OD}). | | | |
| | | | 3 | 2 | V _{OD} (mV) | |
| | | | 0 | 0 | 400 | |
| | | | 0 | 1 | 600 | |
| | | | 1 | 0 | 780 (default) | |
| | [1:0] | OUT5 power-down | 1 | 1 | 960 | |
| | | | LVPECL power-down modes. | | | |
| | | | 1 | 0 | Mode | Output |
| | | | 0 | 0 | Normal operation. | On |
| | | | 0 | 1 | Partial power-down, reference on; use only if there are no external load resistors. | Off |
| | [1:0] | OUT5 power-down | 1 | 0 | Partial power-down, reference on, safe LVPECL power-down (default). | Off |
| | | | 1 | 1 | Total power-down, reference off; use only if there are no external load resistors. | Off |
| | | | | | | |
| | | | | | | |
| | | | | | | |

Table 57. LVDS/CMOS Outputs

| Reg. Addr. (Hex) | Bits | Name | Description | | | | | | |
|------------------|-----------------|---|---|--------------|--------------|--------------|-----------------------------|------------------------|--|
| 0x140 | [7:5] | OUT6 output polarity | In CMOS mode, Bits[7:5] select the output polarity of each CMOS output. In LVDS mode, only Bit 5 determines LVDS polarity. | | | | | | |
| | | | 7 | 6 | 5 | OUT4A (CMOS) | OUT4B (CMOS) | OUT4 (LVDS) | |
| | | | 0 | 0 | 0 | Noninverting | Inverting | Noninverting | |
| | | | 0 | 1 | 0 | Noninverting | Noninverting | Noninverting (default) | |
| | | | 1 | 0 | 0 | Inverting | Inverting | Noninverting | |
| | | | 1 | 1 | 0 | Inverting | Noninverting | Noninverting | |
| | | | 0 | 0 | 1 | Inverting | Noninverting | Inverting | |
| | | | 0 | 1 | 1 | Inverting | Inverting | Inverting | |
| | | | 1 | 0 | 1 | Noninverting | Noninverting | Inverting | |
| | 1 | 1 | 1 | Noninverting | Inverting | Inverting | | | |
| | 4 | OUT6 CMOS B | In CMOS mode, turns on/off the CMOS B output. There is no effect in LVDS mode. 0: turns off the CMOS B output (default). 1: turns on the CMOS B output. | | | | | | |
| | 3 | OUT6 select LVDS/CMOS | Selects LVDS or CMOS logic levels. 0: LVDS (default). 1: CMOS. | | | | | | |
| | [2:1] | OUT6 LVDS output current | Set output current level in LVDS mode. This has no effect in CMOS mode. | | | | | | |
| | | | 2 | 1 | Current (mA) | | Recommended Termination (Ω) | | |
| | | | 0 | 0 | 1.75 | | 100 | | |
| | | | 0 | 1 | 3.5 | | 100 (default) | | |
| | | | 1 | 0 | 5.25 | | 50 | | |
| 1 | 1 | 7 | | 50 | | | | | |
| 0 | OUT6 power-down | Power-down output (LVDS/CMOS). 0: power on (default). 1: power off. | | | | | | | |
| 0x141 | [7:5] | OUT7 output polarity | In CMOS mode, Bits[7:5] select the output polarity of each CMOS output. In LVDS mode, only Bit 5 determines LVDS polarity. | | | | | | |
| | | | 7 | 6 | 5 | OUT5A (CMOS) | OUT5B (CMOS) | OUT5 (LVDS) | |
| | | | 0 | 0 | 0 | Noninverting | Inverting | Noninverting | |
| | | | 0 | 1 | 0 | Noninverting | Noninverting | Noninverting (default) | |
| | | | 1 | 0 | 0 | Inverting | Inverting | Noninverting | |
| | | | 1 | 1 | 0 | Inverting | Noninverting | Noninverting | |
| | | | 0 | 0 | 1 | Inverting | Noninverting | Inverting | |
| | | | 0 | 1 | 1 | Inverting | Inverting | Inverting | |
| | | | 1 | 0 | 1 | Noninverting | Noninverting | Inverting | |
| | 1 | 1 | 1 | Noninverting | Inverting | Inverting | | | |
| | 4 | OUT7 CMOS B | In CMOS mode, turns on/off the CMOS B output. There is no effect in LVDS mode. 0: turns off the CMOS B output (default). 1: turns on the CMOS B output. | | | | | | |
| | 3 | OUT7 select LVDS/CMOS | Select LVDS or CMOS logic levels. 0: LVDS (default). 1: CMOS. | | | | | | |
| | [2:1] | OUT7 LVDS output current | Sets output current level in LVDS mode. This has no effect in CMOS mode. | | | | | | |
| | | | 2 | 1 | Current (mA) | | Recommended Termination (Ω) | | |
| | | | 0 | 0 | 1.75 | | 100 | | |
| | | | 0 | 1 | 3.5 | | 100 (default) | | |
| | | | 1 | 0 | 5.25 | | 50 | | |
| 1 | 1 | 7 | | 50 | | | | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | | | |
|------------------|-----------------|---|---|--------------|--------------|-----------------------------|--------------|------------------------|
| 0x141 | 0 | OUT7 power-down | Power-down output (LVDS/CMOS). 0: power on. 1: power off (default). | | | | | |
| 0x142 | [7:5] | OUT8 output polarity | In CMOS mode, Bits[7:5] select the output polarity of each CMOS output. In LVDS mode, only Bit 5 determines LVDS polarity. | | | | | |
| | | | 7 | 6 | 5 | OUT6A (CMOS) | OUT6B (CMOS) | OUT6 (LVDS) |
| | | | 0 | 0 | 0 | Noninverting | Inverting | Noninverting |
| | | | 0 | 1 | 0 | Noninverting | Noninverting | Noninverting (default) |
| | | | 1 | 0 | 0 | Inverting | Inverting | Noninverting |
| | | | 1 | 1 | 0 | Inverting | Noninverting | Noninverting |
| | | | 0 | 0 | 1 | Inverting | Noninverting | Inverting |
| | | | 0 | 1 | 1 | Inverting | Inverting | Inverting |
| | | | 1 | 0 | 1 | Noninverting | Noninverting | Inverting |
| | 1 | 1 | 1 | Noninverting | Inverting | Inverting | | |
| | 4 | OUT8 CMOS B | In CMOS mode, turns on/off the CMOS B output. There is no effect in LVDS mode. 0: turn off the CMOS B output (default). 1: turn on the CMOS B output. | | | | | |
| | 3 | OUT8 select LVDS/CMOS | Selects LVDS or CMOS logic levels. 0: LVDS (default). 1: CMOS. | | | | | |
| | [2:1] | OUT8 LVDS output current | Sets output current level in LVDS mode. This has no effect in CMOS mode. | | | | | |
| | | | 2 | 1 | Current (mA) | Recommended Termination (Ω) | | |
| | | | 0 | 0 | 1.75 | 100 | | |
| | | | 0 | 1 | 3.5 | 100 (default) | | |
| | | | 1 | 0 | 5.25 | 50 | | |
| 1 | 1 | 7 | 50 | | | | | |
| 0 | OUT8 power-down | Power-down output (LVDS/CMOS). 0: power on (default). 1: power off. | | | | | | |
| 0x143 | [7:5] | OUT9 output polarity | In CMOS mode, Bits[7:5] select the output polarity of each CMOS output. In LVDS mode, only Bit 5 determines LVDS polarity. | | | | | |
| | | | 7 | 6 | 5 | OUT7A (CMOS) | OUT7B (CMOS) | OUT7 (LVDS) |
| | | | 0 | 0 | 0 | Noninverting | Inverting | Noninverting |
| | | | 0 | 1 | 0 | Noninverting | Noninverting | Noninverting (default) |
| | | | 1 | 0 | 0 | Inverting | Inverting | Noninverting |
| | | | 1 | 1 | 0 | Inverting | Noninverting | Noninverting |
| | | | 0 | 0 | 1 | Inverting | Noninverting | Inverting |
| | | | 0 | 1 | 1 | Inverting | Inverting | Inverting |
| | | | 1 | 0 | 1 | Noninverting | Noninverting | Inverting |
| | 1 | 1 | 1 | Noninverting | Inverting | Inverting | | |
| | 4 | OUT9 CMOS B | In CMOS mode, turns on/off the CMOS B output. There is no effect in LVDS mode. 0: turn off the CMOS B output (default). 1: turn on the CMOS B output. | | | | | |
| | 3 | OUT9 select LVDS/CMOS | Selects LVDS or CMOS logic levels. 0: LVDS (default). 1: CMOS. | | | | | |

| Reg. Addr. (Hex) | Bits | Name | Description | | | |
|------------------|-------|--------------------------|---|----|--------------|-----------------------------|
| 0x143 | [2:1] | OUT9 LVDS output current | Sets output current level in LVDS mode. This has no effect in CMOS mode. | | | |
| | | | 2 | 1 | Current (mA) | Recommended Termination (Ω) |
| | | | 0 | 0 | 1.75 | 100 |
| | | | 0 | 1 | 3.5 | 100 (default) |
| | | | 1 | 0 | 5.25 | 50 |
| | 1 | 1 | 7 | 50 | | |
| | 0 | OUT9 power-down | Power-down output (LVDS/CMOS). 0: power on. 1: power off (default). | | | |

Table 58. LVPECL Channel Dividers

| Reg. Addr. (Hex) | Bits | Name | Description |
|------------------|-------|----------------------------|---|
| 0x190 | [7:4] | Divider 0 low cycles | Number of clock cycles (minus 1) of the divider input during which divider output stays low. A value of 0x0 means that the divider is low for one input clock cycle (default = 0x0). |
| | [3:0] | Divider 0 high cycles | Number of clock cycles (minus 1) of the divider input during which divider output stays high. A value of 0x0 means that the divider is high for one input clock cycle (default = 0x0). |
| 0x191 | 7 | Divider 0 bypass | Bypasses and powers down the divider; routes input to divider output. 0: uses divider. 1: bypasses divider (default). |
| | 6 | Divider 0 nosync | Nosync. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal. |
| | 5 | Divider 0 force high | Forces divider output to high. This requires that nosync (Bit 6) also be set. 0: divider output forced to low (default). 1: divider output forced to high. |
| | 4 | Divider 0 start high | Selects clock output to start high or start low. 0: starts low (default). 1: starts high. |
| | [3:0] | Divider 0 phase offset | Phase offset (default = 0x0). |
| | | | |
| 0x192 | 1 | Divider 0 direct to output | Connect OUT0 and OUT1 to Divider 0 or directly to VCO or CLK. 0: OUT0 and OUT1 are connected to Divider 0 (default). 1: If Register 0x1E1[1:0] = 10b, the VCO is routed directly to OUT0 and OUT1. If Register 0x1E1[1:0] = 00b, the CLK is routed directly to OUT0 and OUT1. If Register 0x1E1[1:0] = 01b, there is no effect. |
| | 0 | Divider 0 DCCOFF | Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction. |
| 0x193 | [7:4] | Divider 1 low cycles | Number of clock cycles of the divider input during which divider output stays low. A value of 0x0 means that the divider is low for one input clock cycle (default = 0x0). |
| | [3:0] | Divider 1 high cycles | Number of clock cycles (minus 1) of the divider input during which divider output stays high. A value of 0x0 means that the divider is high for one input clock cycle (default = 0x0). |
| 0x194 | 7 | Divider 1 bypass | Bypasses and powers down the divider; routes input to divider output. 0: uses divider (default). 1: bypasses divider. |
| | 6 | Divider 1 nosync | Nosync. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal. |
| | 5 | Divider 1 force high | Forces divider output to high. This requires that nosync (Bit 6) also be set. 0: divider output forced to low (default). 1: divider output forced to high. |

| Reg. Addr. (Hex) | Bits | Name | Description |
|------------------|-------|----------------------------|--|
| 0x194 | 4 | Divider 1 start high | Selects clock output to start high or start low. 0: starts low (default). 1: starts high. |
| | [3:0] | Divider 1 phase offset | Phase offset (default = 0x0). |
| 0x195 | 1 | Divider 1 direct to output | Connects OUT2 and OUT3 to Divider 1 or directly to VCO or CLK. 0: OUT2 and OUT3 are connected to Divider 1 (default). 1: If Register 0x1E1[1:0] = 10b, the VCO is routed directly to OUT2 and OUT3. If Register 0x1E1[1:0] = 00b, the CLK is routed directly to OUT2 and OUT3. If Register 0x1E1[1:0] = 01b, there is no effect. |
| | 0 | Divider 1 DCCOFF | Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction. |
| 0x196 | [7:4] | Divider 2 low cycles | Number of clock cycles (minus 1) of the divider input during which divider output stays low. A value of 0x0 means that the divider is low for one input clock cycle (default = 0x0). |
| | [3:0] | Divider 2 high cycles | Number of clock cycles (minus 1) of the divider input during which divider output stays high. A value of 0x0 means that the divider is high for one input clock cycle (default = 0x0). |
| 0x197 | 7 | Divider 2 bypass | Bypasses and powers down the divider; routes input to divider output. 0: uses divider. 1: bypasses divider (default). |
| | 6 | Divider 2 nosync | Nosync. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal. |
| | 5 | Divider 2 force high | Forces divider output to high. This requires that nosync (Bit 6) also be set. 0: divider output forced to low (default). 1: divider output forced to high. |
| | 4 | Divider 2 start high | Selects clock output to start high or start low. 0: starts low (default). 1: starts high. |
| | [3:0] | Divider 2 phase offset | Phase offset (default = 0x0). |
| 0x198 | 1 | Divider 2 direct to output | Connects OUT4 and OUT5 to Divider 2 or directly to VCO or CLK. 0: OUT4 and OUT5 are connected to Divider 2 (default). 1: If Register 0x1E1[1:0] = 10b, the VCO is routed directly to OUT4 and OUT5. If Register 0x1E1[1:0] = 00b, the CLK is routed directly to OUT4 and OUT5. If Register 0x1E1[1:0] = 01b, there is no effect. |
| | 0 | Divider 2 DCCOFF | Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction. |

Table 59. LVDS/CMOS Channel Dividers

| Reg. Addr. (Hex) | Bits | Name | Description |
|------------------|-------|--------------------------|--|
| 0x199 | [7:4] | Low Cycles Divider 3.1 | Number of clock cycles (minus 1) of 3.1 divider input during which 3.1 output stays low. A value of 0x0 means that the divider is low for one input clock cycle (default = 0x0). |
| | [3:0] | High Cycles Divider 3.1 | Number of clock cycles (minus 1) of 3.1 divider input during which 3.1 output stays high. A value of 0x0 means that the divider is high for one input clock cycle (default = 0x0). |
| 0x19A | [7:4] | Phase Offset Divider 3.2 | Refer to LVDS/CMOS channel divider function description (default = 0x0). |
| | [3:0] | Phase Offset Divider 3.1 | Refer to LVDS/CMOS channel divider function description (default = 0x0). |
| 0x19B | [7:4] | Low Cycles Divider 3.2 | Number of clock cycles (minus 1) of 3.2 divider input during which 3.2 output stays low. A value of 0x0 means that the divider is low for one input clock cycle (default = 0x0). |
| | [3:0] | High Cycles Divider 3.2 | Number of clock cycles (minus 1) of 3.2 divider input during which 3.2 output stays high. A value of 0x0 means that the divider is high for one input clock cycle (default = 0x0). |

| Reg. Addr. (Hex) | Bits | Name | Description |
|------------------|-------|--------------------------|--|
| 0x19C | 5 | Bypass Divider 3.2 | Bypasses (and powers down) 3.2 divider logic, routes clock to 3.2 output. 0: does not bypass (default). 1: bypasses. |
| | 4 | Bypass Divider 3.1 | Bypasses (and powers down) 3.1 divider logic, routes clock to 3.1 output. 0: does not bypass 3.1 divider logic (default). 1: bypasses 3.1 divider logic. |
| | 3 | Divider 3 nosync | Nosync. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal. |
| | 2 | Divider 3 force high | Force Divider 3 output high. Requires that nosync also be set. 0: forces low (default). 1: forces high. |
| | 1 | Start High Divider 3.2 | Divider 3.2 starts high/low. 0: starts low (default). 1: starts high. |
| | 0 | Start High Divider 3.1 | Divider 3.1 starts high/low. 0: starts low (default). 1: starts high. |
| 0x19D | 0 | Divider 3 DCCOFF | Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction. |
| 0x19E | [7:4] | Low Cycles Divider 4.1 | Number of clock cycles (minus 1) of 4.1 divider input during which 4.1 output stays low. A value of 0x0 means that the divider is low for one input clock cycle (default = 0x0). |
| | [3:0] | High Cycles Divider 4.1 | Number of clock cycles (minus 1) of 4.1 divider input during which 4.1 output stays high. A value of 0x0 means that the divider is high for one input clock cycle (default = 0x0). |
| 0x19F | [7:4] | Phase Offset Divider 4.2 | Refer to LVDS/CMOS channel divider function description (default = 0x0). |
| | [3:0] | Phase Offset Divider 4.1 | Refer to LVDS/CMOS channel divider function description (default = 0x0). |
| 0x1A0 | [7:4] | Low Cycles Divider 4.2 | Number of clock cycles (minus 1) of 4.2 divider input during which 4.2 output stays low. A value of 0x0 means that the divider is low for one input clock cycle (default = 0x0). |
| | [3:0] | High Cycles Divider 4.2 | Number of clock cycles (minus 1) of 4.2 divider input during which 4.2 output stays high. A value of 0x0 means that the divider is high for one input clock cycle (default = 0x0). |
| 0x1A1 | 5 | Bypass Divider 4.2 | Bypasses (and powers down) 4.2 divider logic; route clock to 4.2 output. 0: does not bypass 4.2 divider logic (default). 1: bypasses 4.2 divider logic. |
| | 4 | Bypass Divider 4.1 | Bypasses (and powers down) 4.1 divider logic; route clock to 4.1 output. 0: does not bypass 4.1 divider logic (default). 1: bypasses 4.1 divider logic. |
| | 3 | Divider 4 nosync | Nosync. 0: obeys chip-level SYNC signal (default). 1: ignores chip-level SYNC signal. |
| | 2 | Divider 4 force high | Forces Divider 4 output high. Requires that nosync also be set. 0: forces low (default). 1: forces high. |
| | 1 | Start High Divider 4.2 | Divider 4.2 starts high/low. 0: starts low (default). 1: starts high. |
| | 0 | Start High Divider 4.1 | Divider 4.1 starts high/low. 0: starts low (default). 1: starts high. |
| 0x1A2 | 0 | Divider 4 DCCOFF | Duty-cycle correction function. 0: enables duty-cycle correction (default). 1: disables duty-cycle correction. |

Table 60. VCO Divider and CLK Input

| Reg. Addr (Hex) | Bits | Name | Description | | | |
|-----------------|-------|--------------------------------|--|---|---|--|
| 0x1E0 | [2:0] | VCO divider | 2 | 1 | 0 | Divide |
| | | | 0 | 0 | 0 | 2. |
| | | | 0 | 0 | 1 | 3. |
| | | | 0 | 1 | 0 | 4 (default). |
| | | | 0 | 1 | 1 | 5. |
| | | | 1 | 0 | 0 | 6. |
| | | | 1 | 0 | 1 | Output static. Note that setting the VCO divider static should occur only after VCO calibration. |
| | | | 1 | 1 | 0 | Output static. Note that setting the VCO divider static should occur only after VCO calibration. |
| | | | 1 | 1 | 1 | Output static. Note that setting the VCO divider static should occur only after VCO calibration. |
| 0x1E1 | 4 | Power down clock input section | Powers down the clock input section (including CLK buffer, VCO divider, and CLK tree). 0: normal operation (default). 1: power-down. | | | |
| | 3 | Power down VCO clock interface | Powers down the interface block between VCO and clock distribution. 0: normal operation (default). 1: power-down. | | | |
| | 2 | Power down VCO and CLK | Powers down both VCO and CLK input. 0; normal operation (default). 1: power-down. | | | |
| 0x1E1 | 1 | Select VCO or CLK | Selects either the VCO or the CLK as the input to VCO divider. 0: selects external CLK as input to VCO divider (default). 1: selects VCO as input to VCO divider; cannot bypass VCO divider when this is selected. | | | |
| | 0 | Bypass VCO divider | Bypasses or uses the VCO divider. 0: uses VCO divider (default). 1: bypasses VCO divider; cannot select VCO as input when this is selected. | | | |

Table 61. System

| Reg. Addr (Hex) | Bits | Name | Description |
|-----------------|------|-----------------------------------|--|
| 0x230 | 2 | Power down SYNC | Powers down the SYNC function. 0: normal operation of the SYNC function (default). 1: powers down SYNC circuitry. |
| | 1 | Power down distribution reference | Powers down the reference for distribution section. 0: normal operation of the reference for the distribution section (default). 1: powers down the reference for the distribution section. |
| | 0 | Soft SYNC | The soft SYNC bit works the same as the $\overline{\text{SYNC}}$ pin, except that the polarity of the bit is reversed. That is, a high level forces selected channels into a predetermined static state, and a 1-to-0 transition triggers a SYNC. 0: same as $\overline{\text{SYNC}}$ high (default). 1: same as $\overline{\text{SYNC}}$ low. |

Table 62. Update All Registers

| Reg. Addr (Hex) | Bits | Name | Description |
|-----------------|------|----------------------|---|
| 0x232 | 0 | Update all registers | This bit must be set to 1 to transfer the contents of the buffer registers into the active registers. This bit is self-clearing; that is, it does not have to be set back to 0. 1 (self-clearing): updates all active registers to the contents of the buffer registers. |

APPLICATIONS INFORMATION

FREQUENCY PLANNING USING THE AD9516

The AD9516 is a highly flexible PLL. When choosing the PLL settings and version of the AD9516, keep in mind the following guidelines.

The AD9516 has the following four frequency dividers: the reference (or R) divider, the feedback (or N) divider, the VCO divider, and the channel divider. When trying to achieve a particularly difficult frequency divide ratio requiring a large amount of frequency division, some of the frequency division can be done by either the VCO divider or the channel divider, thus allowing a higher phase detector frequency and more flexibility in choosing the loop bandwidth.

Within the AD9516 family, lower VCO frequencies generally result in slightly lower jitter. The difference in integrated jitter (from 12 kHz to 20 MHz offset) for the same output frequency is usually less than 150 fs over the entire VCO frequency range (1.45 GHz to 2.95 GHz) of the AD9516 family. If the desired frequency plan can be achieved with a version of the AD9516 that has a lower VCO frequency, choosing the lower frequency part results in the lowest phase noise and the lowest jitter. However, choosing a higher VCO frequency may result in more flexibility in frequency planning.

Choosing a nominal charge pump current in the middle of the allowable range as a starting point allows the designer to increase or decrease the charge pump current and, thus, allows the designer to fine-tune the PLL loop bandwidth in either direction.

ADIsimCLK is a powerful PLL modeling tool that can be downloaded from www.analog.com. It is a very accurate tool for determining the optimal loop filter for a given application.

USING THE AD9516 OUTPUTS FOR ADC CLOCK APPLICATIONS

Any high speed ADC is extremely sensitive to the quality of its sampling clock. An ADC can be thought of as a sampling mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the analog-to-digital output. Clock integrity requirements scale with the analog input frequency and resolution, with higher analog input frequency applications at ≥ 14 -bit resolution being the most stringent. The theoretical SNR of an ADC is limited by the ADC resolution and the jitter on the sampling clock.

Considering an ideal ADC of infinite resolution, where the step size and quantization error can be ignored, the available SNR can be expressed approximately by

$$\text{SNR(dB)} = 20 \times \log \left(\frac{1}{2\pi f_A t_j} \right)$$

where:

f_A is the highest analog frequency being digitized.

t_j is the rms jitter on the sampling clock.

Figure 70 shows the required sampling clock jitter as a function of the analog frequency and effective number of bits (ENOB).

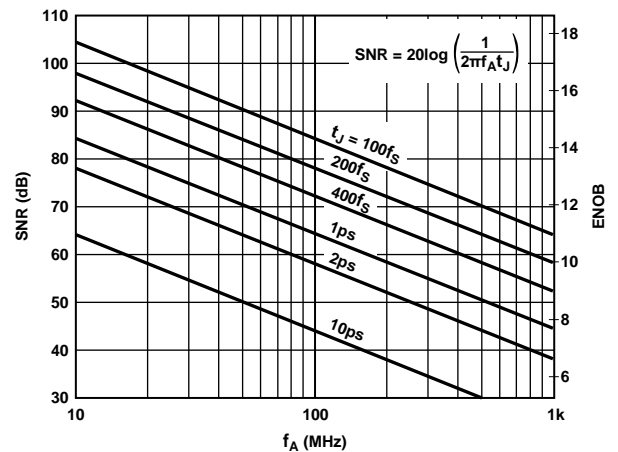


Figure 70. SNR and ENOB vs. Analog Input Frequency

See the [AN-756 Application Note, Sampled Systems and the Effects of Clock Phase Noise and Jitter](#), and the [AN-501 Application Note, Aperture Uncertainty and ADC System Performance](#), at www.analog.com.

Many high performance ADCs feature differential clock inputs to simplify the task of providing the required low jitter clock on a noisy PCB. (Distributing a single-ended clock on a noisy PCB may result in coupled noise on the sample clock. Differential distribution has inherent common-mode rejection that can provide superior clock performance in a noisy environment.) The AD9516 features both LVPECL and LVDS outputs that provide differential clock outputs, which enable clock solutions that maximize converter SNR performance. The input requirements of the ADC (differential or single-ended, logic level, termination) should be considered when selecting the best clocking/converter solution.

LVPECL CLOCK DISTRIBUTION

The LVPECL outputs of the AD9516 provide the lowest jitter clock signals that are available from the AD9516. The LVPECL outputs (because they are open emitter) require a dc termination to bias the output transistors. The simplified equivalent circuit in Figure 59 shows the LVPECL output stage.

In most applications, an LVPECL far-end Thevenin termination (see Figure 71) or Y-termination (see Figure 72) is recommended. In each case, the V_S of the receiving buffer should match the V_{S_LVPECL} . If it does not, ac coupling is recommended (see Figure 73).

The resistor network is designed to match the transmission line impedance ($50\ \Omega$) and the switching threshold ($V_S - 1.3\ \text{V}$).

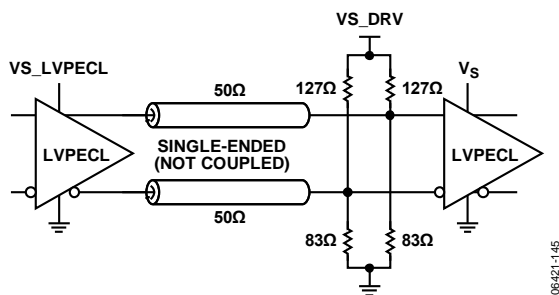


Figure 71. DC-Coupled 3.3 V LVPECL, Far-End Thevenin Termination

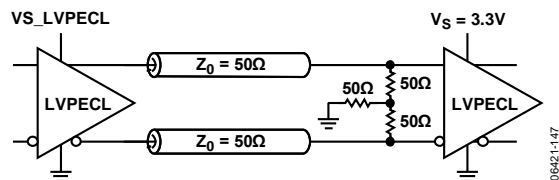


Figure 72. DC-Coupled 3.3 V LVPECL, Y-Termination

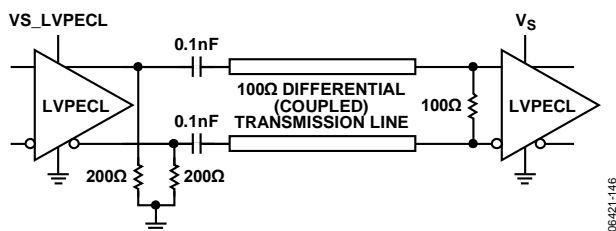


Figure 73. AC-Coupled LVPECL with Parallel Transmission Line

LVPECL Y-termination is an elegant termination scheme that uses the fewest components and offers both odd- and even-mode impedance matching. Even-mode impedance matching is an important consideration for closely coupled transmission lines at high frequencies. Its main drawback is that it offers limited flexibility for varying the drive strength of the emitter-follower LVPECL driver. This can be an important consideration when driving long trace lengths but is usually not an issue. In the case shown in Figure 72, where $V_{S_LVPECL} = 2.5\ \text{V}$, the $50\ \Omega$ termination resistor that is connected to ground should be changed to $19\ \Omega$.

Thevenin-equivalent termination uses a resistor network to provide $50\ \Omega$ termination to a dc voltage that is below V_{OL} of the LVPECL driver. In this case, V_{S_LVPECL} on the AD9516 should equal V_S of the receiving buffer. Although the resistor combination shown in Figure 72 results in a dc bias point of $V_{S_LVPECL} - 2\ \text{V}$, the actual common-mode voltage is $V_{S_LVPECL} - 1.3\ \text{V}$ because additional current flows from the AD9516 LVPECL driver through the pull-down resistor.

The circuit is identical when $V_{S_LVPECL} = 2.5\ \text{V}$, except that the pull-down resistor is $62.5\ \Omega$ and the pull-up resistor is $250\ \Omega$.

LVDS CLOCK DISTRIBUTION

The AD9516 provides four clock outputs (OUT6 to OUT9) that are selectable as either CMOS or LVDS level outputs. LVDS is a differential output option that uses a current mode output stage. The nominal current is $3.5\ \text{mA}$, which yields $350\ \text{mV}$ output swing across a $100\ \Omega$ resistor. An output current of $7\ \text{mA}$ is also available in cases where a larger output swing is required. The LVDS output meets or exceeds all ANSI/TIA/EIA-644 specifications.

A recommended termination circuit for the LVDS outputs is shown in Figure 74.

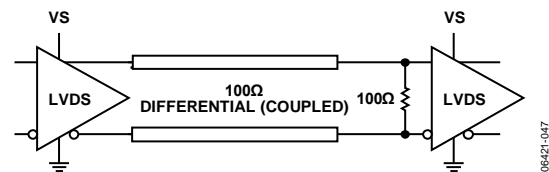


Figure 74. LVDS Output Termination

See the [AN-586 Application Note, LVDS Data Outputs for High-Speed Analog-to-Digital Converters](#) for more information on LVDS.

CMOS CLOCK DISTRIBUTION

The AD9516 provides four clock outputs (OUT6 to OUT9) that are selectable as either CMOS or LVDS level outputs. When selected as CMOS, each output becomes a pair of CMOS outputs, each of which can be individually turned on or off and set as noninverting or inverting. These outputs are 3.3 V CMOS compatible.

Whenever single-ended CMOS clocking is used, some of the following general guidelines should be used.

Point-to-point nets should be designed such that a driver has only one receiver on the net, if possible. This allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver. The value of the resistor is dependent on the board design and timing requirements (typically $10\ \Omega$ to $100\ \Omega$ is used). CMOS outputs are also limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 3 inches are recommended to preserve signal rise/fall times and preserve signal integrity.

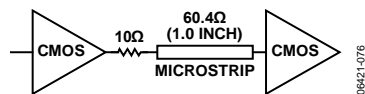


Figure 75. Series Termination of CMOS Output

Termination at the far-end of the PCB trace is a second option. The CMOS outputs of the AD9516 do not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 76. The far-end termination network should match the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

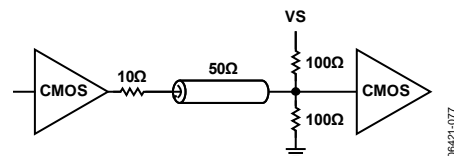
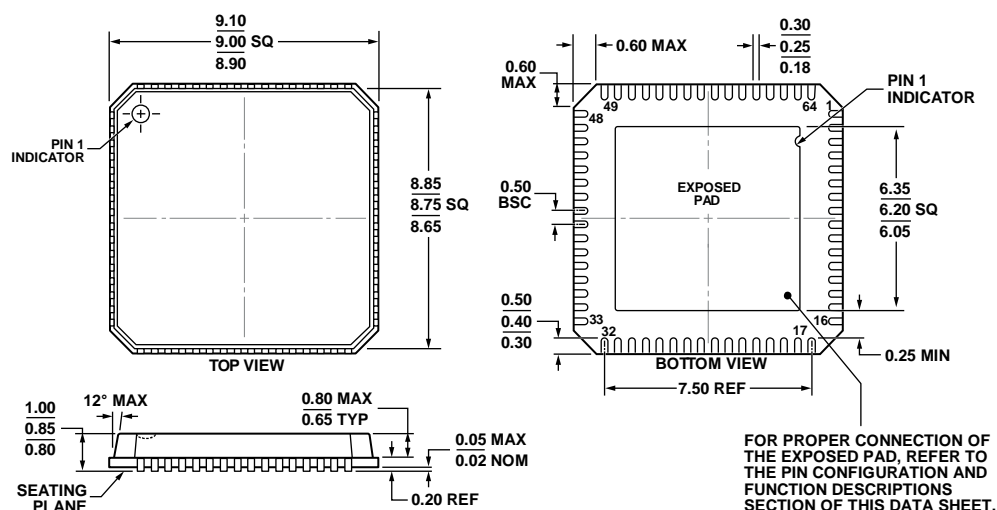


Figure 76. CMOS Output with Far-End Termination

Because of the limitations of single-ended CMOS clocking, consider using differential outputs when driving high speed signals over long traces. The AD9516 offers both LVPECL and LVDS outputs that are better suited for driving long traces where the inherent noise immunity of differential signaling provides superior performance for clocking converters.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 77. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]

9 mm × 9 mm Body, Very Thin Quad

CP-64-4

Dimensions shown in millimeters

06-12-2012-C

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| AD9516-2BCPZ | −40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9516-2BCPZ-REEL7 | −40°C to +85°C | 64-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-64-4 |
| AD9516-2/PCBZ | | Evaluation Board | |

¹ Z = RoHS Compliant Part.