AD8138* Product Page Quick Links

Last Content Update: 11/01/2016

Comparable Parts

View a parametric search of comparable parts

Evaluation Kits

- Universal Evaluation Board for Single Differential Amplifiers

Documentation

Application Notes

- AN-0990: Terminating a Differential Amplifier in Single-Ended Input Applications
- AN-0992: Active Filter Evaluation Board for Differential Amplifiers
- AN-1026: High Speed Differential ADC Driver Design Considerations
- AN-1363: Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers
- AN-584: Using the AD813X Differential Amplifier
- AN-589: Ways to Optimize the Performance of a Difference Amplifier
- AN-649: Using the Analog Devices Active Filter Design Tool

Data Sheet

- AD8138-DSCC: Military Data Sheet
- AD8138-EP: Enhanced Product Data Sheet
- AD8138: Low Distortion Differential ADC Driver Data Sheet

User Guides

- UG-474: Evaluation Board for Differential Amplifiers Offered in 8-Lead SOIC Packages
- UG-888: Evaluation Board for Differential Amplifiers Offered in 8-Lead MSOP Packages

Tools and Simulations

- ADI DiffAmpCalc™
- AD8138 SPICE Macro-Model

Reference Designs

- CN0040
- CN0041
- CN0061

Reference Materials

Product Selection Guide

- High Speed Amplifiers Selection Table

Technical Articles

- Maximize Performance When Driving Differential ADCs

Tutorials

- MT-075: Differential Drivers for High Speed ADCs Overview
- MT-076: Differential Driver Analysis
- MT-218: Multiple Feedback Band-Pass Design Example
- MT-230: Noise Considerations in High Speed Converter Signal Chains

Design Resources

- AD8138 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

Discussions

View all AD8138 EngineerZone Discussions

Sample and Buy

Visit the product page to see pricing options

Technical Support

Submit a technical question or find your regional support number

* This page was dynamically generated by Analog Devices, Inc. and inserted into this data sheet. Note: Dynamic changes to the content on this page does not constitute a change to the revision number of the product data sheet. This content may be frequently modified.

TABLE OF CONTENTS

REVISION HISTORY

3/16—Rev. F to Rev. G
Changes to Setting the Closed-Loop Gain Section ... 17
Changes to Figure 46 ... 21
Changes to Figure 47 ... 22

1/06—Rev. E to Rev. F
Changes to Features ... 1
Added Thermal Resistance Section and Maximum Power Dissipation Section ... 7
Changes to Balanced Transformer Driver Section ... 20
Changes to Ordering Guide ... 23

3/03—Rev. D to Rev. E
Changes to Specifications ... 2
Changes to Ordering Guide ... 4
Changes to TPC 16 ... 6
Changes to Table I ... 9
Added New Paragraph after Table I ... 10
Updated Outline Dimensions ... 14

7/02—Rev. C to Rev. D
Addition of TPC 35 and TPC 36 ... 8

6/01—Rev. B to Rev. C
Edits to Specifications ... 2
Edits to Ordering Guide ... 4

12/00—Rev. A to Rev. B

9/99—Rev. 0 to Rev. A

3/99—Rev. 0: Initial Version

SPECIFICATIONS

±D_{IN} TO ±OUT SPECIFICATIONS

At 25°C, V_S = ±5 V, V_{OCM} = 0, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. Refer to Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.5 V p-p, C_F = 0 pF	290	320		MHz
	V_{OUT} = 0.5 V p-p, C_F = 1 pF		225		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, C_F = 0 pF		30		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, C_F = 0 pF		265		MHz
Slew Rate	V_{OUT} = 2 V p-p, C_F = 0 pF		1150		V/µs
Settling Time	0.01%, V_{OUT} = 2 V p-p, C_F = 1 pF		16		ns
Overdrive Recovery Time	V_{IN} = 5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE[1]					
Second Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−94		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−87		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		−62		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−114		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−85		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		−57		dBc
IMD	20 MHz		−77		dBc
IP3	20 MHz		37		dBm
Voltage Noise (RTI)	f = 100 kHz to 40 MHz		5		nV/√Hz
Input Current Noise	f = 100 kHz to 40 MHz		2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm} = V_{OUT, dm}/2$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	−2.5	±1	+2.5	mV
	T_{MIN} to T_{MAX} variation		±4		µV/°C
Input Bias Current			3.5	7	µA
	T_{MIN} to T_{MAX} variation		−0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			−4.7 to +3.4		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V		−77	−70	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output		7.75		V p-p
Output Current			95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−66		dB

[1] Harmonic distortion performance is equal or slightly worse with higher values of $R_{L, dm}$. See Figure 17 and Figure 18 for more information.

V_{OCM} TO ±OUT SPECIFICATIONS

At 25°C, V_S = ±5 V, V_{OCM} = 0, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. Refer to Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth			250		MHz
Slew Rate			330		V/µs
INPUT VOLTAGE NOISE (RTI)	f = 0.1 MHz to 100 MHz		17		nV/√Hz
DC PERFORMANCE					
Input Voltage Range			±3.8		V
Input Resistance			200		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	−3.5	±1	+3.5	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−75		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.9955	1	1.0045	V/V
POWER SUPPLY					
Operating Range		±1.4		±5.5	V
Quiescent Current		18	20	23	mA
	T_{MIN} to T_{MAX} variation		40		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ±1 V		−90	−70	dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

±D_{IN} TO ±OUT SPECIFICATIONS

At 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. Refer to Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential output, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	V_{OUT} = 0.5 V p-p, C_F = 0 pF	280	310		MHz
	V_{OUT} = 0.5 V p-p, C_F = 1 pF		225		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, C_F = 0 pF		29		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p, C_F = 0 pF		265		MHz
Slew Rate	V_{OUT} = 2 V p-p, C_F = 0 pF		950		V/µs
Settling Time	0.01%, V_{OUT} = 2 V p-p, C_F = 1 pF		16		ns
Overdrive Recovery Time	V_{IN} = 2.5 V to 0 V step, G = +2		4		ns
NOISE/HARMONIC PERFORMANCE[1]					
Second Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−90		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−79		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		−60		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 5 MHz, $R_{L, dm}$ = 800 Ω		−100		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L, dm}$ = 800 Ω		−82		dBc
	V_{OUT} = 2 V p-p, 70 MHz, $R_{L, dm}$ = 800 Ω		−53		dBc
IMD	20 MHz		−74		dBc
IP3	20 MHz		35		dBm
Voltage Noise (RTI)	f = 100 kHz to 40 MHz		5		nV/√Hz
Input Current Noise	f = 100 kHz to 40 MHz		2		pA/√Hz
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm} = V_{OUT, dm}/2$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	−2.5	±1	+2.5	mV
	T_{MIN} to T_{MAX} variation		±4		µV/°C
Input Bias Current			3.5	7	µA
	T_{MIN} to T_{MAX} variation		−0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			−0.3 to +3.2		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = 1 V		−77	−70	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output		2.9		V p-p
Output Current			95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V		−65		dB

[1] Harmonic distortion performance is equal or slightly worse with higher values of $R_{L, dm}$. See Figure 17 and Figure 18 for more information.

V_{OCM} TO ±OUT SPECIFICATIONS

At 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = +1, $R_{L, dm}$ = 500 Ω, unless otherwise noted. Refer to Figure 39 for test setup and label descriptions. All specifications refer to single-ended input and differential output, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth			220		MHz
Slew Rate			250		V/µs
INPUT VOLTAGE NOISE (RTI)	f = 0.1 MHz to 100 MHz		17		nV/√Hz
DC PERFORMANCE					
Input Voltage Range			1.0 to 3.8		V
Input Resistance			100		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = V_{OCM}$ = 0 V	−5	±1	+5	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 V ±1 V		−70		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 V ±1 V	0.9968	1	1.0032	V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current		15	20	21	mA
	T_{MIN} to T_{MAX} variation		40		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = ± 1 V		−90	−70	dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Ratings
Supply Voltage	±5.5 V
V_{OCM}	$\pm V_S$
Internal Power Dissipation	550 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 6.

Package Type	θ_{JA}	Unit
8-Lead SOIC/4-Layer	121	°C/W
8-Lead MSOP/4-Layer	145	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8138 packages is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8138. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The load current consists of the differential and common-mode currents flowing to the load, as well as currents flowing through the external feedback networks and internal common-mode feedback loop. The internal resistor tap used in the common-mode feedback loop places a negligible differential load on the output. RMS voltages and currents should be considered when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 8-lead SOIC (121°C/W) and 8-lead MSOP (θ_{JA} = 145°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

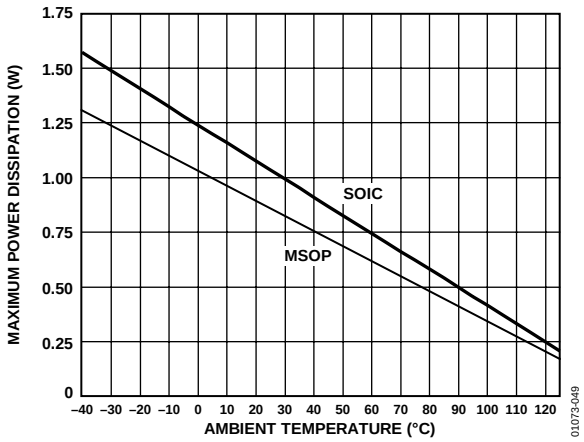

Figure 3. Maximum Power Dissipation vs. Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

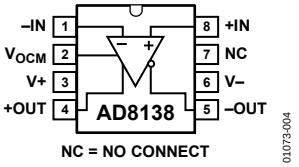

Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN	Negative Input Summing Node.
2	V_{OCM}	Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on V_{OCM} sets the dc bias level on +OUT and –OUT to 1 V.
3	V+	Positive Supply Voltage.
4	+OUT	Positive Output. Note that the voltage at $-D_{IN}$ is inverted at +OUT (see Figure 42).
5	–OUT	Negative Output. Note that the voltage at $+D_{IN}$ is inverted at –OUT (see Figure 42).
6	V–	Negative Supply Voltage.
7	NC	No Connect.
8	+IN	Positive Input Summing Node.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, Gain = 1, $R_G = R_F = R_{L, dm}$ = 499 V, T_A = 25°C; refer to Figure 39 for test setup.

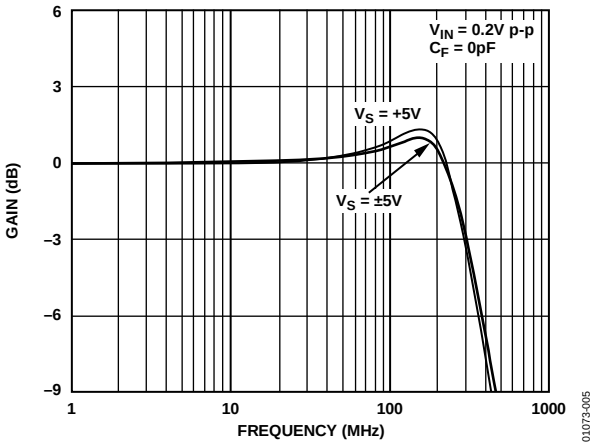

Figure 5. Small Signal Frequency Response

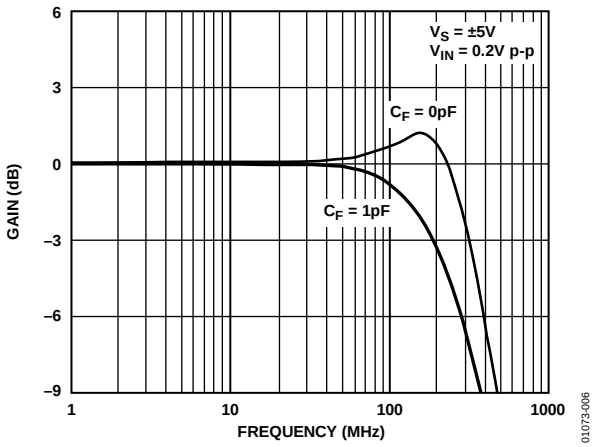

Figure 6. Small Signal Frequency Response

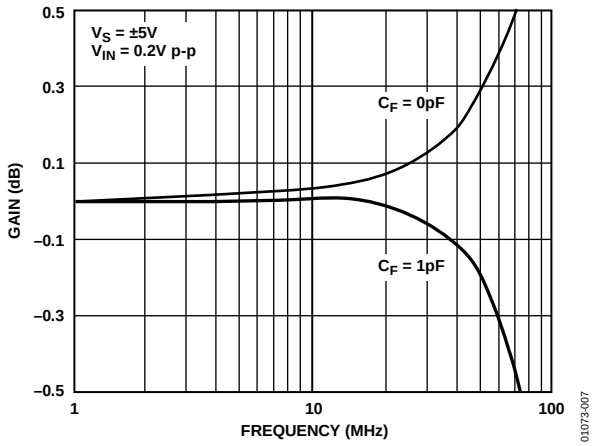

Figure 7. 0.1 dB Flatness vs. Frequency

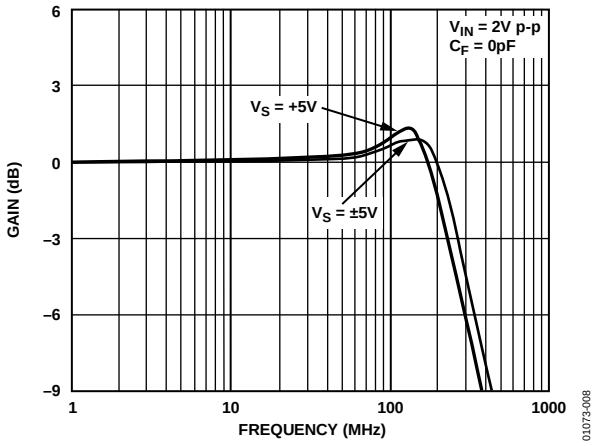

Figure 8. Large Signal Frequency Response

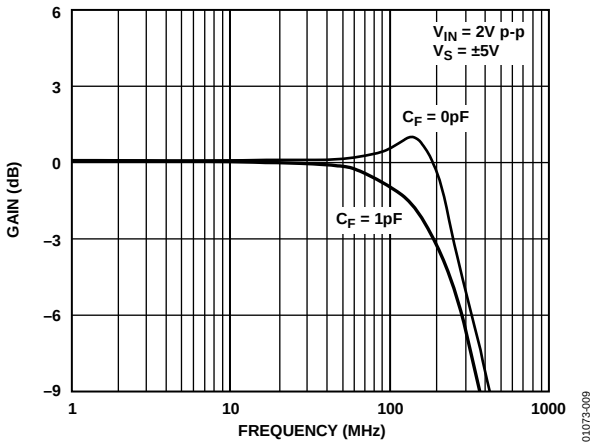

Figure 9. Large Signal Frequency Response

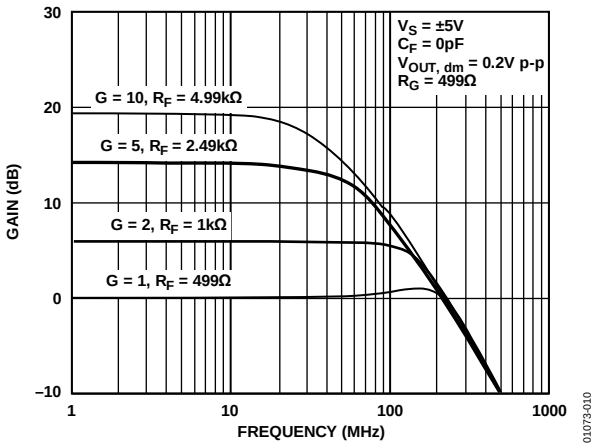

Figure 10. Small Signal Frequency Response for Various Gains

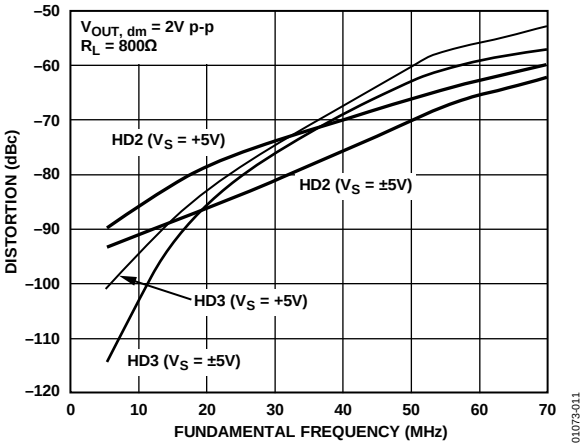

Figure 11. Harmonic Distortion vs. Frequency

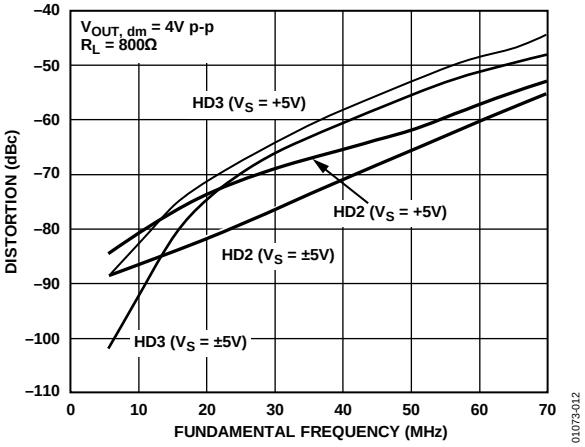

Figure 12. Harmonic Distortion vs. Frequency

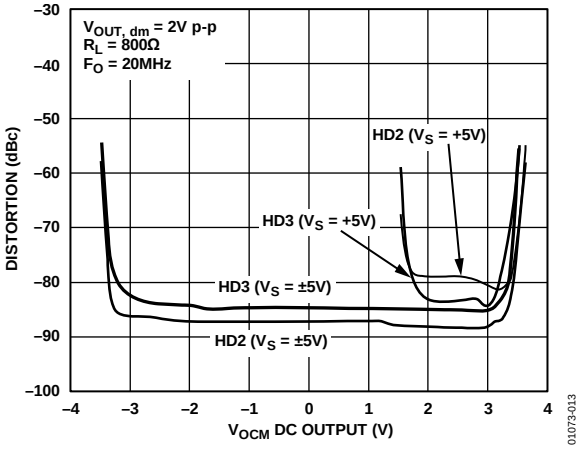

Figure 13. Harmonic Distortion vs. V_{OCM}

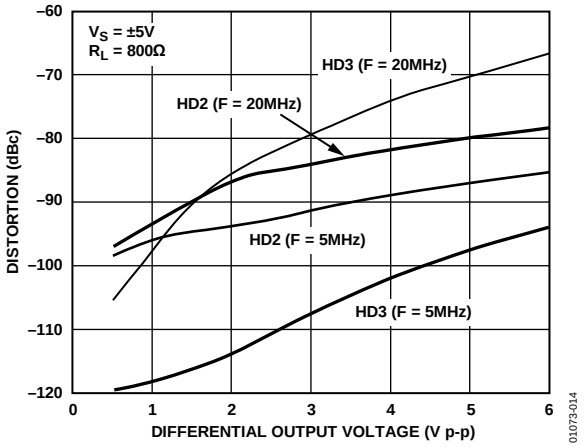

Figure 14. Harmonic Distortion vs. Differential Output Voltage

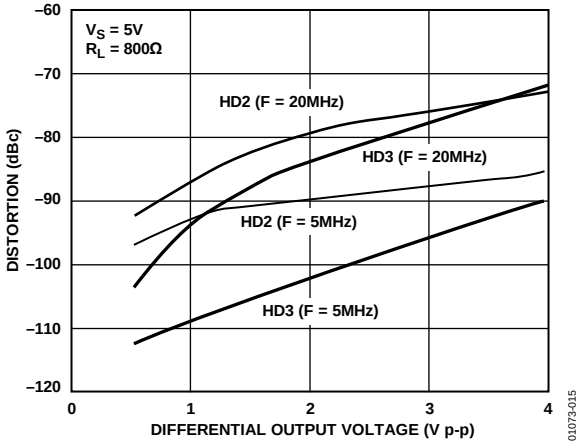

Figure 15. Harmonic Distortion vs. Differential Output Voltage

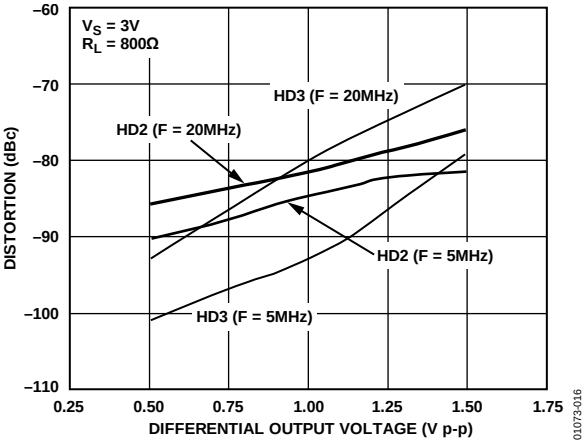

Figure 16. Harmonic Distortion vs. Differential Output Voltage

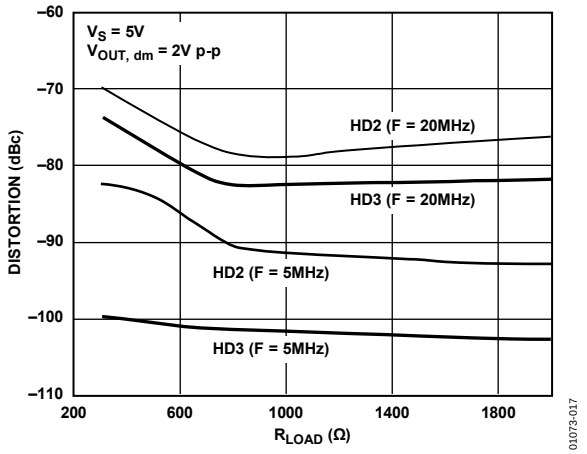

Figure 17. Harmonic Distortion vs. R_{LOAD}

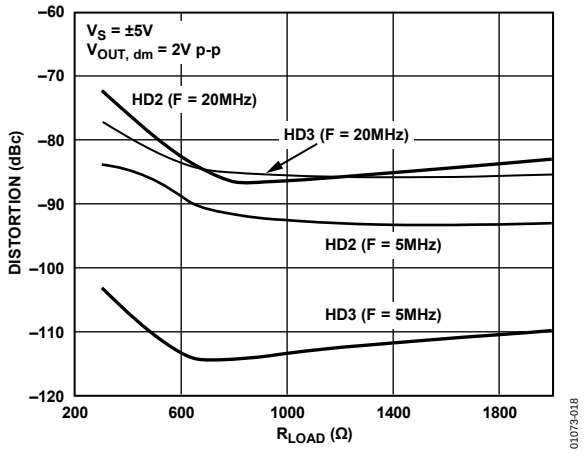

Figure 18. Harmonic Distortion vs. R_{LOAD}

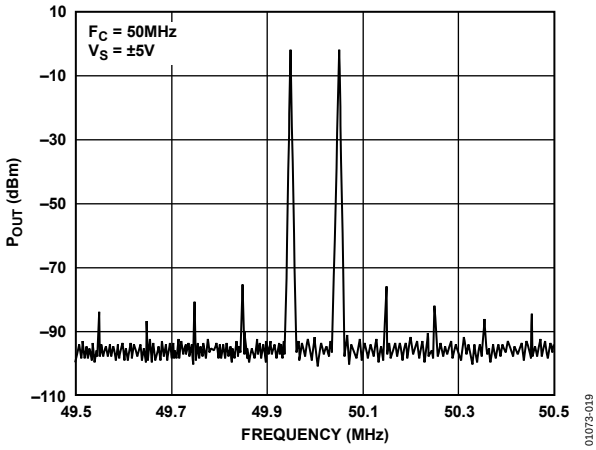

Figure 19. Intermodulation Distortion

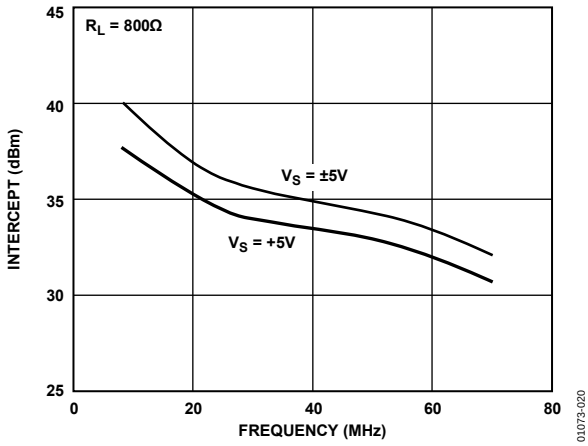

Figure 20. Third-Order Intercept vs. Frequency

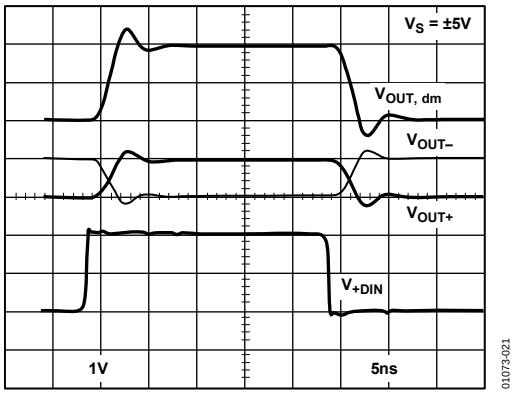

Figure 21. Large Signal Transient Response

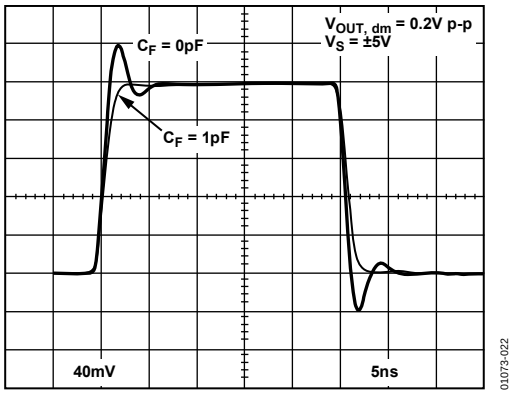

Figure 22. Small Signal Transient Response

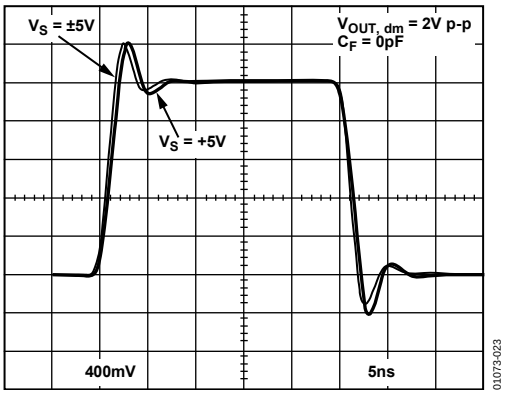

Figure 23. Large Signal Transient Response

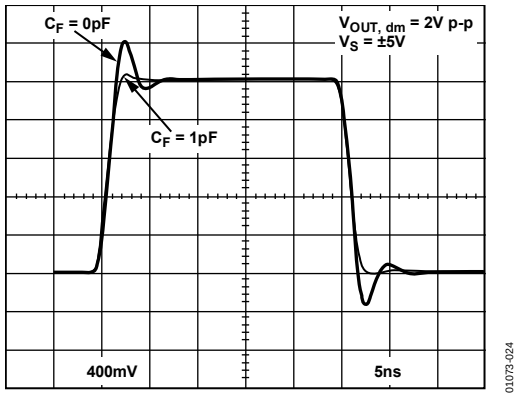

Figure 24. Large Signal Transient Response

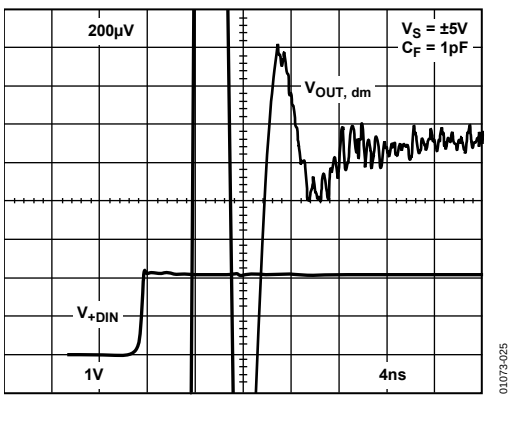

Figure 25. Settling Time

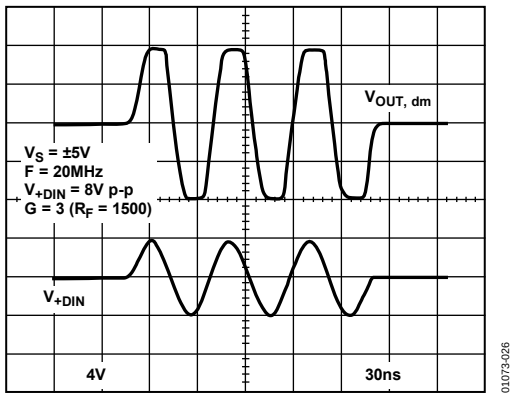

Figure 26. Output Overdrive

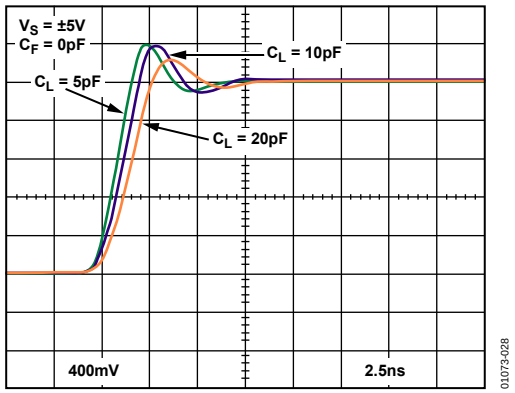

Figure 27. Large Signal Transient Response for Various Cap Loads (See Figure 40)

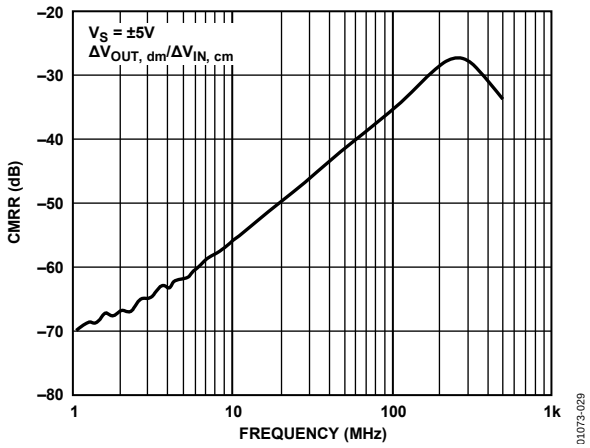

Figure 28. CMRR vs. Frequency

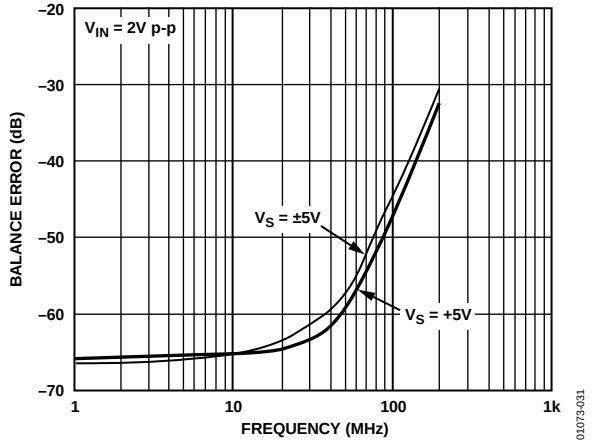

Figure 29. Output Balance Error vs. Frequency (See Figure 41)

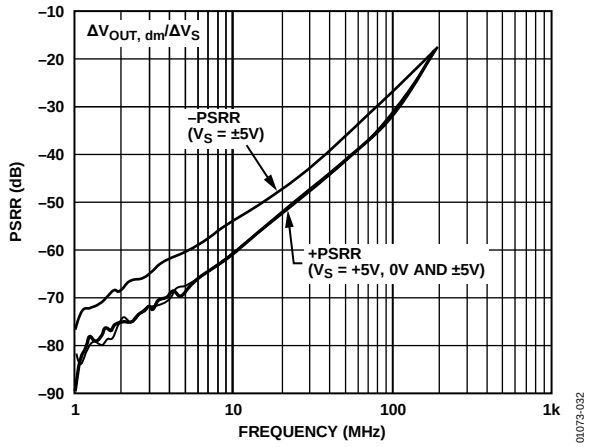

Figure 30. PSRR vs. Frequency

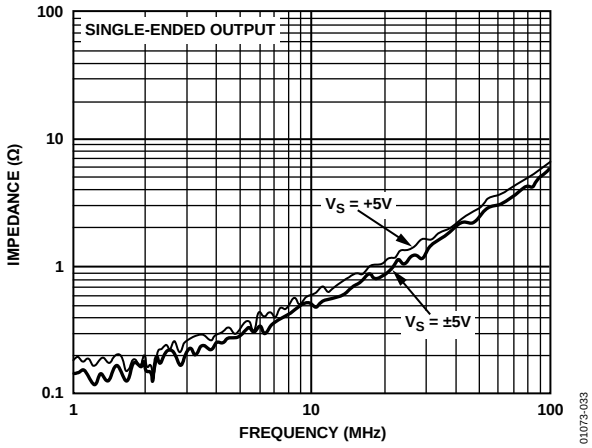

Figure 31. Output Impedance vs. Frequency

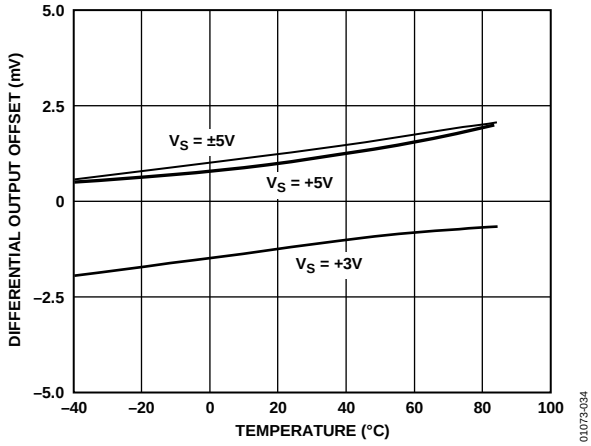

Figure 32. Output Referred Differential Offset Voltage vs. Temperature

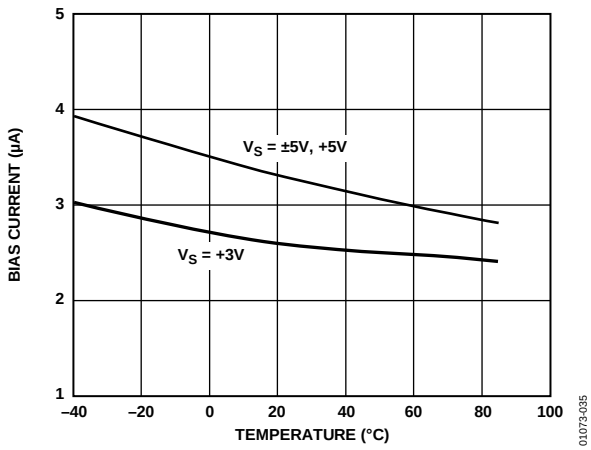

Figure 33. Input Bias Current vs. Temperature

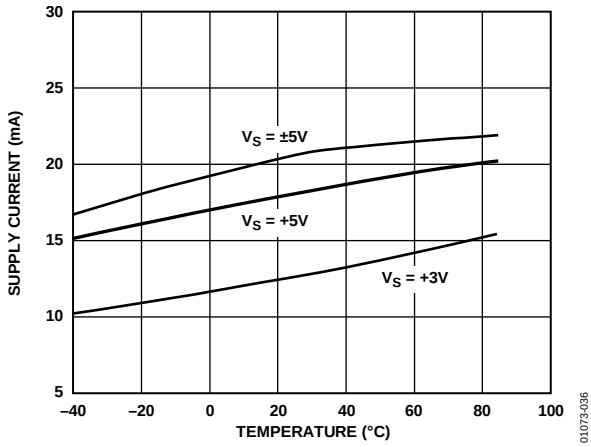

Figure 34. Supply Current vs. Temperature

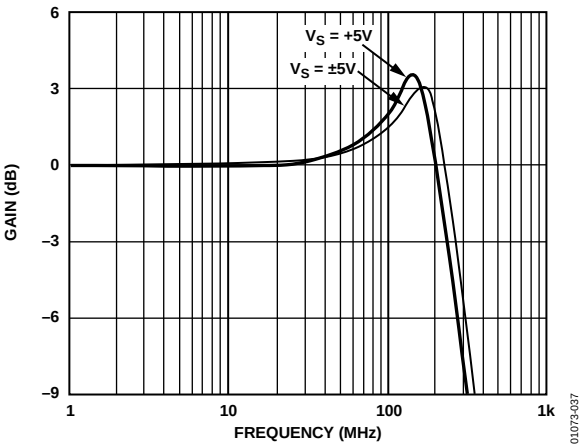

Figure 35. V_{OCM} Frequency Response

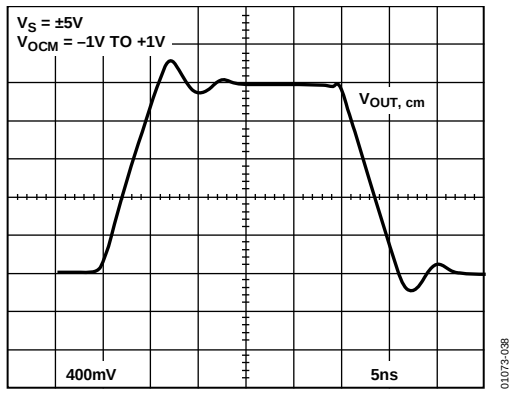

Figure 36. V_{OCM} Transient Response

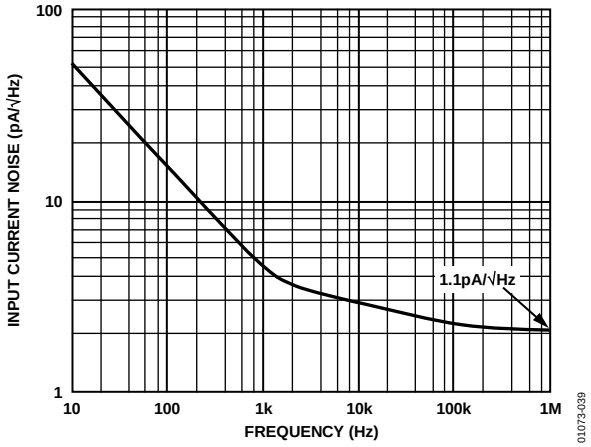

Figure 37. Current Noise (RTI)

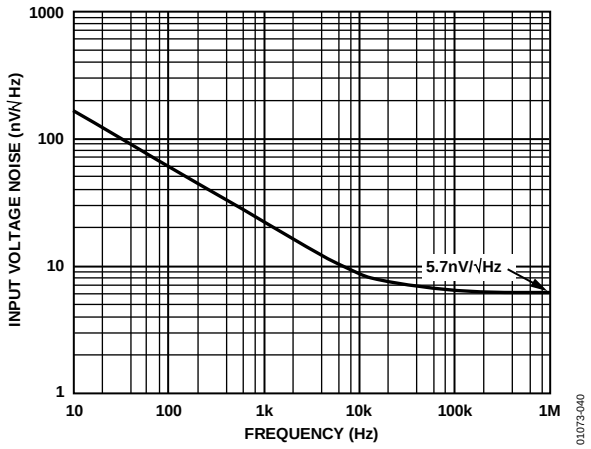

Figure 38. Voltage Noise (RTI)

TEST CIRCUITS

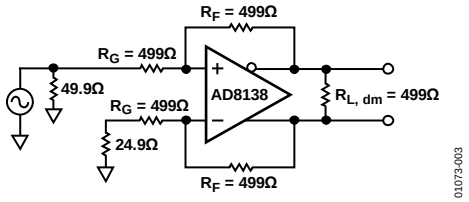

Figure 39. Basic Test Circuit

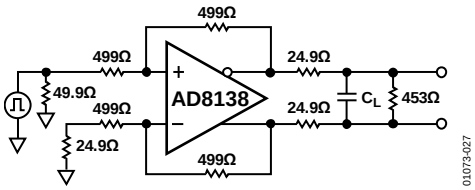

Figure 40. Test Circuit for Cap Load Drive

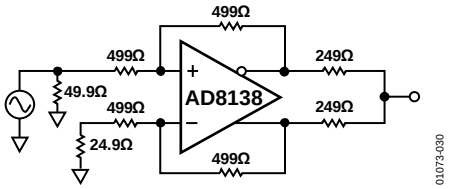

Figure 41. Test Circuit for Output Balance

OPERATIONAL DESCRIPTION

DEFINITION OF TERMS

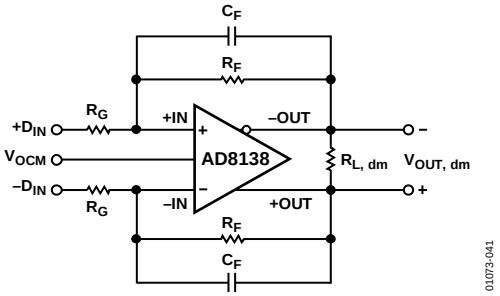

Figure 42. Circuit Definitions

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance is a measure of how well differential signals are matched in amplitude and exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the midpoint of the divider with the magnitude of the differential signal (see Figure 41). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage:

$$Output\ Balance\ Error = \left| \frac{V_{OUT,\,cm}}{V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

The AD8138 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on high open-loop gain and negative feedback to force these outputs to the desired voltages. The AD8138 behaves much like a standard voltage feedback op amp and makes it easy to perform single-ended-to-differential conversion, common-mode level-shifting, and amplification of differential signals. Also like an op amp, the AD8138 has high input impedance and low output impedance.

Previous differential drivers, both discrete and integrated designs, have been based on using two independent amplifiers and two independent feedback loops, one to control each of the outputs. When these circuits are driven from a single-ended source, the resulting outputs are typically not well balanced. Achieving a balanced output has typically required exceptional matching of the amplifiers and feedback networks.

DC common-mode level-shifting has also been difficult with previous differential drivers. Level-shifting has required the use of a third amplifier and feedback loop to control the output common-mode level. Sometimes the third amplifier has also been used to attempt to correct an inherently unbalanced circuit. Excellent performance over a wide frequency range has proven difficult with this approach.

The AD8138 uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The AD8138 architecture results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to be zeroed. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly 180°apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The AD8138 uses high open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN in Figure 42. For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

Neglecting the capacitors C_F, the differential-mode gain of the circuit in Figure 42 can be determined to be described by

$$\left|\frac{V_{OUT,\,dm}}{V_{IN,\,dm}}\right| = \frac{R_F{}^S}{R_G{}^S}$$

This assumes the input resistors, $R_G{}^S$, and feedback resistors, $R_F{}^S$, on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at +IN and −IN, by the circuit noise gain. The noise gain is defined as

$$G_N = 1 + \left(\frac{R_F}{R_G}\right)$$

To compute the total output referred noise for the circuit of Figure 42, consideration must also be given to the contribution of the Resistors R_F and R_G. Refer to Table 8 for the estimated output noise voltage densities at various closed-loop gains.

Table 8.

Gain	R_G (Ω)	R_F (Ω)	Bandwidth −3 dB	Output Noise AD8138 Only	Output Noise AD8138 + R_G, R_F
1	499	499	320 MHz	10 nV/√Hz	11.6 nV/√Hz
2	499	1.0 k	180 MHz	15 nV/√Hz	18.2 nV/√Hz
5	499	2.49 k	70 MHz	30 nV/√Hz	37.9 nV/√Hz
10	499	4.99 k	30 MHz	55 nV/√Hz	70.8 nV/√Hz

When using the AD8138 in gain configurations where R_F/R_G of one feedback network is unequal to R_F/R_G of the other network, there is a differential output noise due to input-referred voltage in the V_{OCM} circuitry. The output noise is defined in terms of the following feedback terms (refer to Figure 42):

$$\beta_1 = \frac{R_G}{R_F + R_G}$$

for −OUT to +IN loop, and

$$\beta_2 = \frac{R_G}{R_F + R_G}$$

for +OUT to −IN loop. With these defined,

$$V_{nOUT,\,dm} = 2V_{nIN,V_{OCM}}\left[\frac{\beta_1 - \beta_2}{\beta_1 + \beta_2}\right]$$

where $V_{nOUT,\,dm}$ is the output differential noise, and $V_{nIN,V_{COM}}$ is the input-referred voltage noise in V_{OCM}.

THE IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remains equal and 180° out of phase. The input-to-output differential-mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

Ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential-mode output offset voltage. For the G = 1 case, with a ground referenced input signal and the output common-mode level set for 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, worst-case differential mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION

The effective input impedance of a circuit such as the one in Figure 42, at +DIN and −DIN, depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN,\,dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply

$$R_{IN,\,dm} = 2 \times R_G$$

In the case of a single-ended input signal (for example if $-D_{IN}$ is grounded and the input signal is applied to $+D_{IN}$), the input impedance becomes

$$R_{IN,\,dm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}}\right)$$

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The AD8138 is optimized for level-shifting, ground-referenced input signals. For a single-ended input, this would imply, for example, that the voltage at $-D_{IN}$ in Figure 42 would be 0 V when the negative power supply voltage of the amplifier (at V−) is also set to 0 V.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the AD8138 is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V−). Relying on this internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (made up of 10 kΩ resistors), be used. The output common-mode offset listed in the Specifications section assumes the V_{OCM} input is driven by a low impedance voltage source.

DRIVING A CAPACITIVE LOAD

A purely capacitive load can react with the pin and bondwire inductance of the AD8138, resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance should be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the outputs of the amplifier, as shown in Figure 40.

LAYOUT, GROUNDING, AND BYPASSING

As a high speed device, the AD8138 is sensitive to the PCB environment in which it has to operate. Realizing its superior specifications requires attention to various details of good high speed PCB design.

The first requirement is for a good solid ground plane that covers as much of the board area around the AD8138 as possible. The only exception to this is that the two input pins (Pin 1 and Pin 8) should be kept a few millimeters from the ground plane, and ground should be removed from inner layers and the opposite side of the board under the input pins. This minimizes the stray capacitance on these nodes and helps preserve the gain flatness vs. frequency.

The power supply pins should be bypassed as close as possible to the device to the nearby ground plane. Good high frequency ceramic chip capacitors should be used. This bypassing should be done with a capacitance value of 0.01 µF to 0.1 µF for each supply. Further away, low frequency bypassing should be provided with 10 µF tantalum capacitors from each supply to ground.

The signal routing should be short and direct to avoid parasitic effects. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on the PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This reduces the radiated energy and makes the circuit less susceptible to interference.

BALANCED TRANSFORMER DRIVER

Transformers are among the oldest devices used to perform a single-ended-to-differential conversion (and vice versa). Transformers can also perform the additional functions of galvanic isolation, step-up or step-down of voltages, and impedance transformation. For these reasons, transformers always find uses in certain applications.

However, when driving the transformer in a single-ended manner, there is an imbalance at the output due to the parasitics inherent in the transformer. The primary (or driven) side of the transformer has one side at dc potential (usually ground), while the other side is driven. This can cause problems in systems that require good balance of the differential output signals of the transformer.

If the interwinding capacitance (C_{STRAY}) is assumed to be uniformly distributed, a signal from the driving source couples to the secondary output terminal that is closest to the driven side of the primary. On the other hand, no signal is coupled to the opposite terminal of the secondary because its nearest primary terminal is not driven (see Figure 43). The exact amount of this imbalance depends on the particular parasitics of the trans-former, but is mostly a problem at higher frequencies.

The balance of a differential circuit can be measured by connecting an equal-valued resistive voltage divider across the differential outputs and then measuring the center point of the circuit with respect to ground. Since the two differential outputs are supposed to be of equal amplitude, but 180° opposite phase, there should be no signal present for perfectly balanced outputs.

The circuit in Figure 43 shows a Mini-Circuits® T1-6T transformer connected with its primary driven single-endedly and the secondary connected with a precision voltage divider across its terminals. The voltage divider is made up of two 500 Ω, 0.005% precision resistors. The voltage V_{UNBAL}, which is also equal to the ac common-mode voltage, is a measure of how closely the outputs are balanced.

Figure 45 compares the transformer being driven single-endedly by a signal generator and being driven differentially using an AD8138. The top signal trace of Figure 45 shows the balance of the single-ended configuration, while the bottom shows the differentially driven balance response. The 100 MHz balance is 35 dB better when using the AD8138.

The well-balanced outputs of the AD8138 provide a drive signal to each of the primary inputs of the transformer that are of equal amplitude and 180° out of phase. Therefore, depending on how the polarity of the secondary is connected, the signals that conduct across the interwinding capacitance either both assist the secondary signal of the transformer equally, or both buck the secondary signals. In either case, the parasitic effect is symmetrical and provides a well-balanced transformer output (see Figure 45).

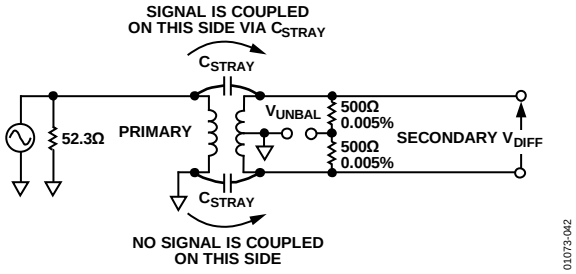

Figure 43. Transformer Single-Ended-to-Differential Converter Is Inherently Imbalanced

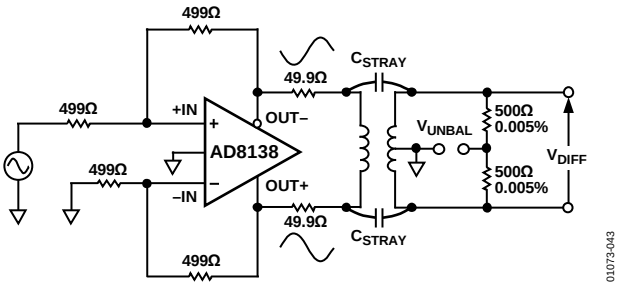

Figure 44. AD8138 Forms a Balanced Transformer Driver

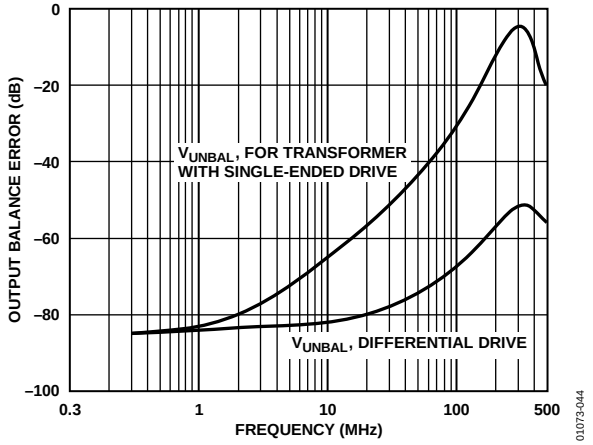

Figure 45. Output Balance Error for Circuits of Figure 43 and Figure 44

HIGH PERFORMANCE ADC DRIVING

The circuit in Figure 46 shows a simplified front-end connection for an AD8138 driving an AD9224, a 12-bit, 40 MSPS ADC. The ADC works best when driven differentially, which minimizes its distortion. The AD8138 eliminates the need for a transformer to drive the ADC and performs single-ended-to-differential conversion, common-mode level-shifting, and buffering of the driving signal.

The positive and negative outputs of the AD8138 are connected to the respective differential inputs of the AD9224 via a pair of 49.9 Ω resistors to minimize the effects of the switched-capacitor front end of the AD9224. For best distortion performance, it runs from supplies of ±5 V.

The AD8138 is configured with unity gain for a single-ended, input-to-differential output. The additional 23 Ω, 523 Ω total, at the input to −IN is to balance the parallel impedance of the 50 Ω source and its 50 Ω termination that drives the noninverting input.

The signal generator has a ground-referenced, bipolar output, that is, it drives symmetrically above and below ground. Connecting V_{OCM} to the CML pin of the AD9224 sets the output common-mode of the AD8138 at 2.5 V, which is the midsupply level for the AD9224. This voltage is bypassed by a 0.1 µF capacitor.

The full-scale analog input range of the AD9224 is set to 4 V p-p, by shorting the SENSE terminal to AVSS. This has been determined to be the scaling to provide minimum harmonic distortion.

For the AD8138 to swing at 4 V p-p, each output swings 2 V p-p while providing signals that are 180° out of phase. With a common-mode voltage at the output of 2.5 V, each AD8138 output swings between 1.5 V and 3.5 V.

A ground-referenced 4 V p-p, 5 MHz signal at D_{IN}+ was used to test the circuit in Figure 46. When the combined-device circuit was run with a sampling rate of 20 MSPS, the spurious-free dynamic range (SFDR) was measured at −85 dBc.

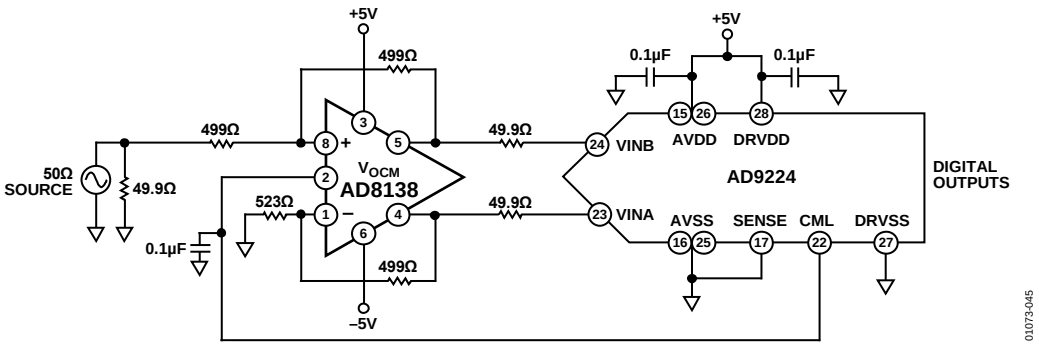

Figure 46. AD8138 Driving an AD9224, a 12-Bit, 40 MSPS ADC

3 V OPERATION

The circuit in Figure 47 shows a simplified front-end connection for an AD8138 driving an AD9203, a 10-bit, 40 MSPS ADC that is specified to work on a single 3 V supply. The ADC works best when driven differentially to make the best use of the signal swing available within the 3 V supply. The appropriate outputs of the AD8138 are connected to the appropriate differential inputs of the AD9203 via a low-pass filter.

The AD8138 is configured for unity gain for a single-ended input to differential output. The additional 23 Ω at the input to −IN is to balance the impedance of the 50 Ω source and its 50 Ω termination that drives the noninverting input.

The signal generator has ground-referenced, bipolar output, that is, it can drive symmetrically above and below ground. Even though the AD8138 has ground as its negative supply, it can still function as a level-shifter with such an input signal.

The output common mode is raised up to midsupply by the voltage divider that biases V_{OCM}. In this way, the AD8138 provides dc coupling and level-shifting of a bipolar signal, without inverting the input signal.

The low-pass filter between the AD8138 and the AD9203 provides filtering that helps to improve the signal-to-noise ratio (SNR). Lower noise can be realized by lowering the pole frequency, but the bandwidth of the circuit is lowered.

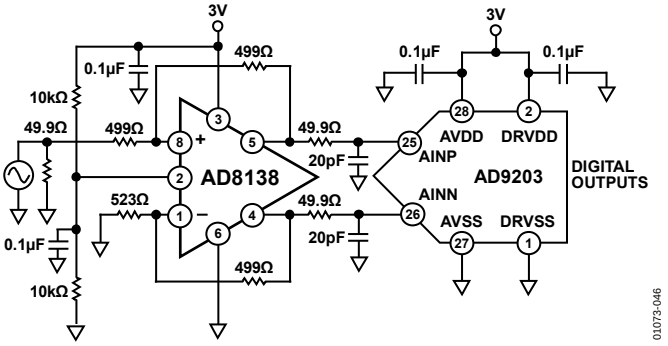

Figure 47. AD8138 Driving an AD9203, a 10-Bit, 40 MSPS Analog-to-Digital Converter

The circuit was tested with a −0.5 dBFS signal at various frequencies. Figure 48 shows a plot of the total harmonic distortion (THD) vs. frequency at signal amplitudes of 1 V and 2 V differential drive levels.

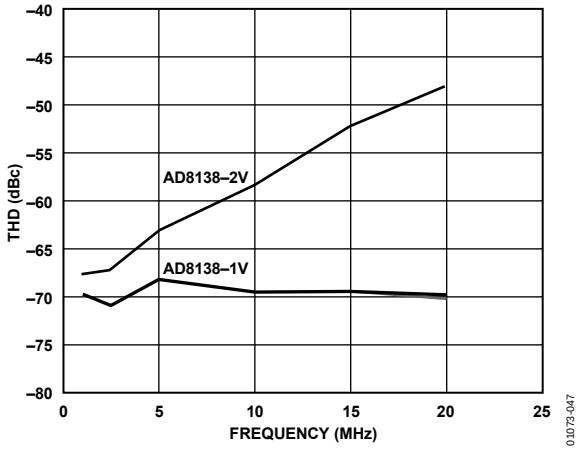

Figure 48. AD9203 THD at −0.5 dBFS AD8138

Figure 49 shows the signal-to-noise-and-distortion (SINAD) under the same conditions as above. For the smaller signal swing, the AD8138 performance is quite good, but its performance degrades when trying to swing too close to the supply rails.

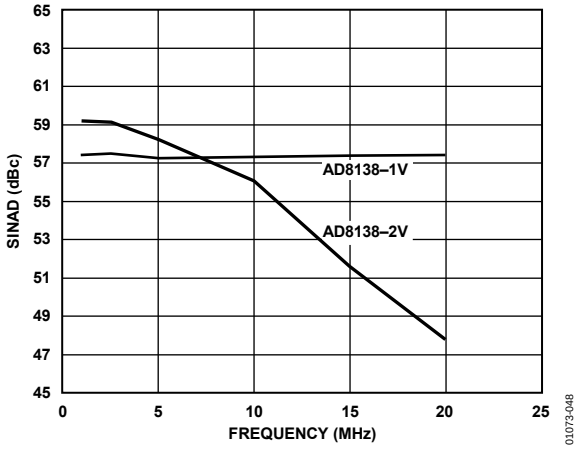

Figure 49. AD9203 SINAD at −0.5 dBFS AD8138

OUTLINE DIMENSIONS

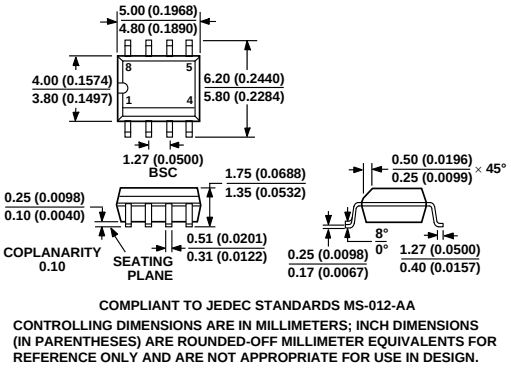

Figure 50. 8-Lead Standard Small Outline Package [SOIC]
(R-8)
Dimensions shown in millimeters and (inches)

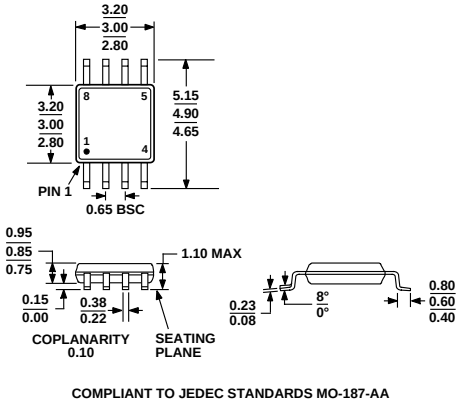

Figure 51. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8138AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD8138AR-REEL	−40°C to +85°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD8138AR-REEL7	−40°C to +85°C	8-Lead SOIC, 7" Tape and Reel	R-8	
AD8138ARZ	−40°C to +85°C	8-Lead SOIC	R-8	
AD8138ARZ-RL	−40°C to +85°C	8-Lead SOIC, 13" Tape and Reel	R-8	
AD8138ARZ-R7	−40°C to +85°C	8-Lead SOIC, 7" Tape and Reel	R-8	
AD8138ARM	−40°C to +85°C	8-Lead MSOP	RM-8	HBA
AD8138ARM-REEL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HBA
AD8138ARM-REEL7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HBA
AD8138ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8	HBA#
AD8138ARMZ-REEL	−40°C to +85°C	8-Lead MSOP, 13" Tape and Reel	RM-8	HBA#
AD8138ARMZ-REEL7	−40°C to +85°C	8-Lead MSOP, 7" Tape and Reel	RM-8	HBA#

[1] Z = RoHS Compliant Part. # denotes RoHS compliant part may be top or bottom marked.

NOTES