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SPECIFICATIONS

At T_A = 25°C, V_S = ±5 V, R_L = 100 Ω, R_F = 0 Ω, gain = +1, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p		325		MHz
	G = –1, V_O = 0.2 V p-p		95		MHz
	G = +1, V_O = 2 V p-p		175		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_O = 0.2 V p-p		30		MHz
Slew Rate	G = +1, V_O = 2 V step, R_L = 2 kΩ		850		V/µs
	G = +1, V_O = 4 V step, R_L = 2 kΩ		1150		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		30		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–85		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–62		dBc
SFDR	f = 5 MHz, V_O = 2 V p-p, R_L = 150 Ω		–68		dB
Third-Order Intercept	f = 5 MHz, V_O = 2 V p-p		–35		dBm
Crosstalk, Output to Output	f = 5 MHz, G = +2		–60		dB
Input Voltage Noise	f = 100 kHz		7		nV/√Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01		%
	NTSC, G = +2, R_L = 1 kΩ		0.02		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.15		Degrees
	NTSC, G = +2, R_L = 1 kΩ		0.01		Degrees
Overload Recovery	V_{IN} = 200 mV p-p, G = +1		30		ns
DC PERFORMANCE					
Input Offset Voltage			1	5	mV
	T_{MIN} to T_{MAX}		2.5		mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current			0.5	2.5	µA
	T_{MIN} to T_{MAX}		3.0		µA
Input Offset Current				±0.75	µA
Open-Loop Gain	V_O = ±2.5 V, R_L = 2 kΩ	50	55		dB
	V_O = ±2.5 V, R_L = 150 Ω	50	52		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance	+Input		2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ	–4.0		+4.0	V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	48	60		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 2 kΩ	–4.0		+4.0	V
	R_L = 150 Ω		±3.9		V
Capacitive Load Drive	30% overshoot		30		pF
POWER SUPPLY					
Operating Range		±1.5	±5.0	±6	V
Quiescent Current for AD8057			6.0	7.5	mA
Quiescent Current for AD8058			14.0	15	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±1.5 V	54	59		dB

At T_A = 25°C, V_S = 5 V, R_L = 100 Ω, R_F = 0 Ω, gain = +1, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p		300		MHz
	G = +1, V_O = 2 V p-p		155		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		28		MHz
Slew Rate	G = +1, V_O = 2 V step, R_L = 2 kΩ		700		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		35		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−75		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		−54		dBc
Crosstalk, Output to Output	f = 5 MHz, G = +2		−60		dB
Input Voltage Noise	f = 100 kHz		7		nV/√Hz
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.05		%
	NTSC, G = +2, R_L = 1 kΩ		0.05		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.10		Degrees
	NTSC, G = +2, R_L = 1 kΩ		0.02		Degrees
DC PERFORMANCE					
Input Offset Voltage			1	5	mV
	T_{MIN} to T_{MAX}		2.5		mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current			0.5	2.5	µA
	T_{MIN} to T_{MAX}		3.0		µA
Input Offset Current				0.75	µA
Open-Loop Gain	V_O = ±1.5 V, R_L = 2 kΩ to midsupply	50	55		dB
	V_O = ±1.5 V, R_L = 150 Ω to midsupply	45	52		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance	+Input		2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		0.9 to 3.4		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	48	60		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 2 kΩ		0.9 to 3.8		V
	R_L = 150 Ω		1.2 to 3.4		V
Capacitive Load Drive	30% overshoot		30		pF
POWER SUPPLY					
Operating Range		3	5.0	10	V
Quiescent Current for AD8057			5.4	7.0	mA
Quiescent Current for AD8058			13.5	14	mA
Power Supply Rejection Ratio		54	58		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage ($+V_S$ to $-V_S$)	12.6 V
Internal Power Dissipation[1]	
SOIC Package (R)	0.8 W
SOT-23-5 Package (RT)	0.5 W
MSOP Package (RM)	0.6 W
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	±4.0 V
Output Short-Circuit Duration	Observe power derating curves
Storage Temperature Range (R)	−65°C to +125°C
Operating Temperature Range (A Grade)	−40°C to +85°C
Lead Temperature (Soldering 10sec)	300°C

[1] Specification is for device in free air:
8-lead SOIC package: θ_{JA} = 160°C/W
5-lead SOT-23-5 package: θ_{JA} = 240°C/W
8-Lead MSOP package: θ_{JA} = 200°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8057/AD8058 is limited by the associated rise in junction temperature. Exceeding a junction temperature of 175°C for an extended period can result in device failure. Although the AD8057/AD8058 is internally short-circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

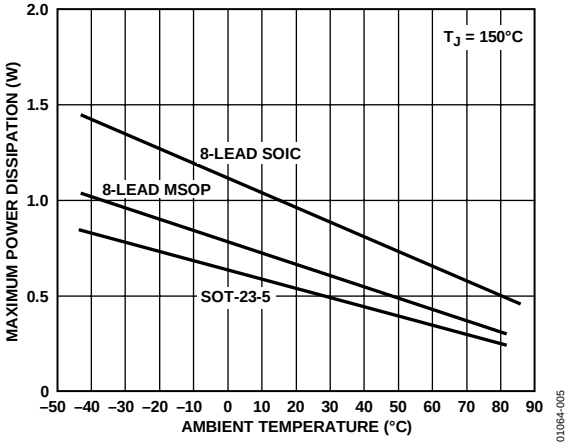


Figure 5. Maximum Power Dissipation vs. Ambient Temperature

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

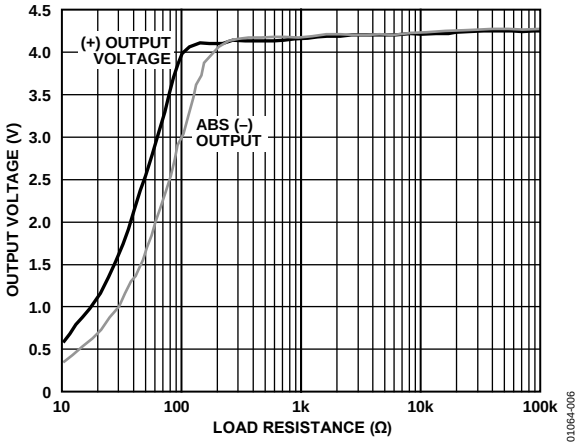


Figure 6. Output Swing vs. Load Resistance

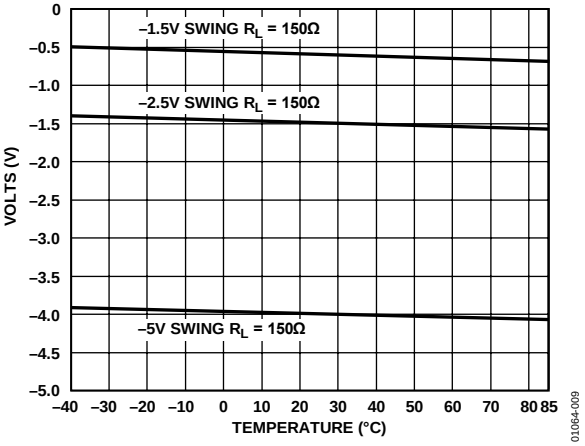


Figure 9. Negative Output Voltage Swing vs. Temperature

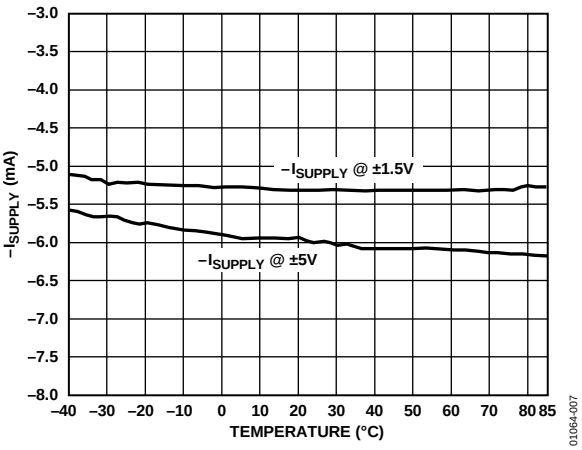


Figure 7. $-I_{SUPPLY}$ vs. Temperature

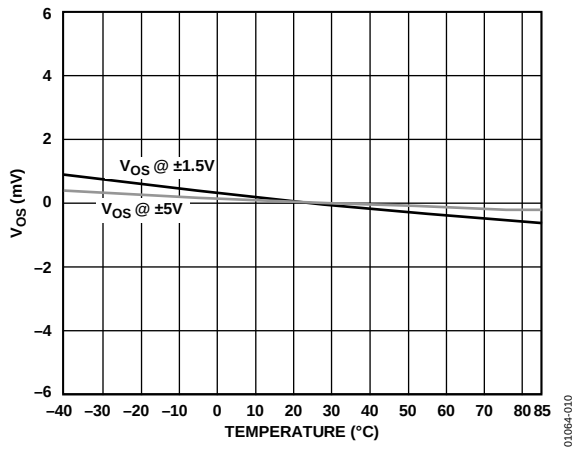


Figure 10. V_{OS} vs. Temperature

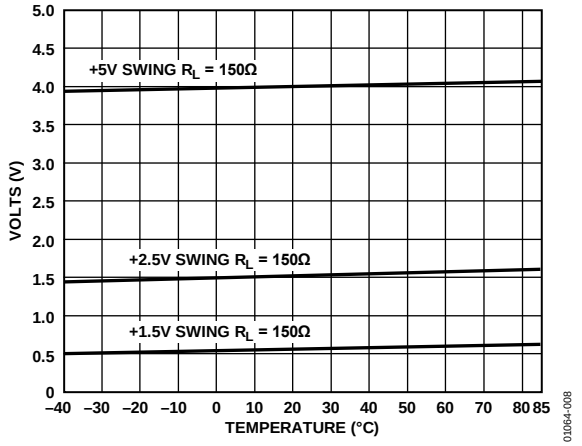


Figure 8. Positive Output Voltage Swing vs. Temperature

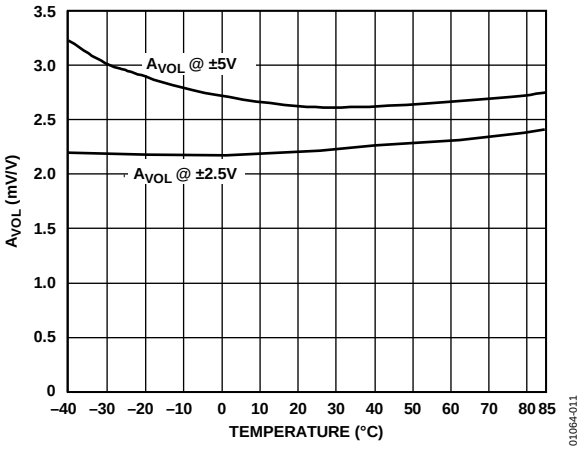


Figure 11. Open-Loop Gain vs. Temperature

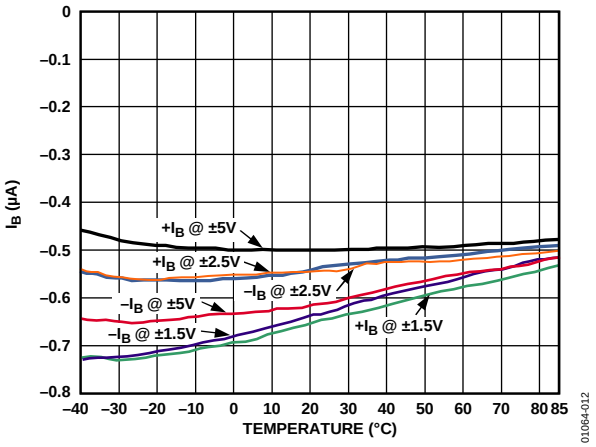


Figure 12. Input Bias Current vs. Temperature

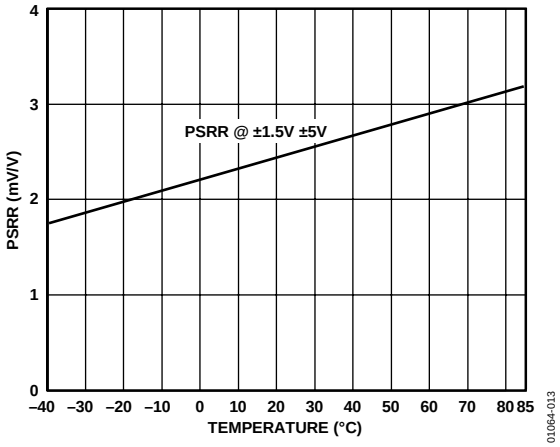


Figure 13. PSRR vs. Temperature

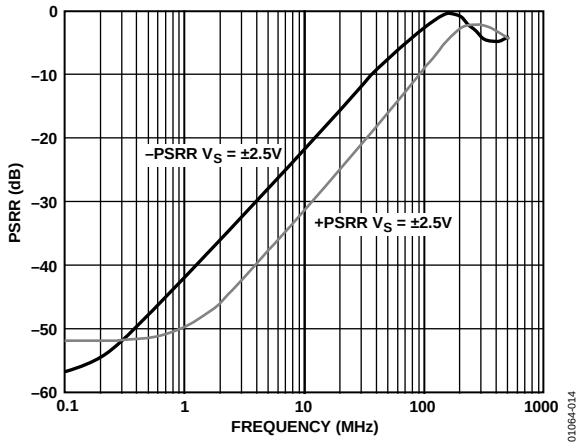


Figure 14. PSRR vs. Frequency

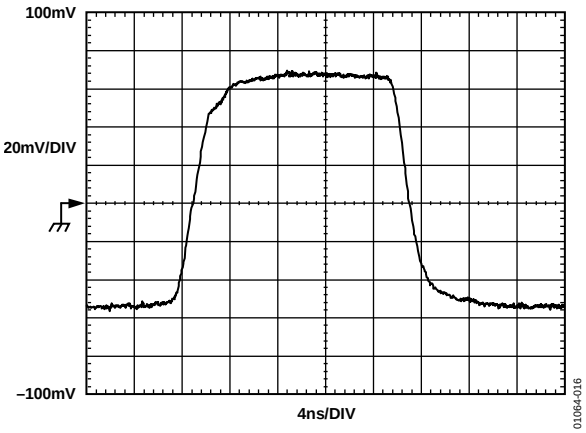


Figure 15. Small Signal Step Response G = +1, R_L = 1 kΩ, V_S = ±5 V, See Figure 41 for Test Circuit

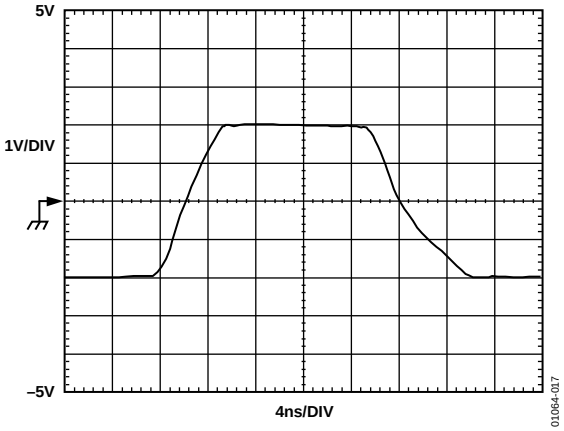


Figure 16. Large Signal Step Response G = +1,RL = 1 kΩ, V_S = ±5.0 V, See Figure 41 for Test Circuit

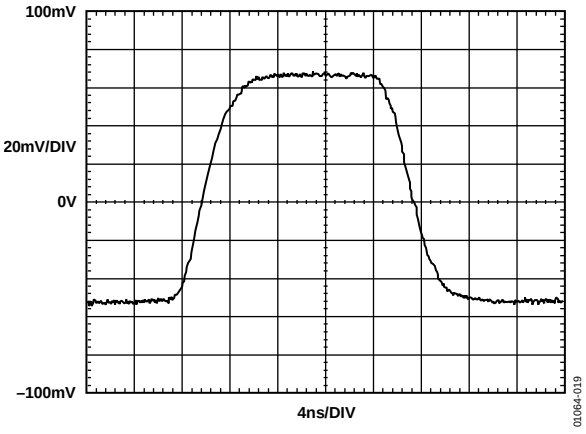


Figure 17. Small Signal Step Response G = –1, R_L = 1 kΩ, See Figure 42 for Test Circuit

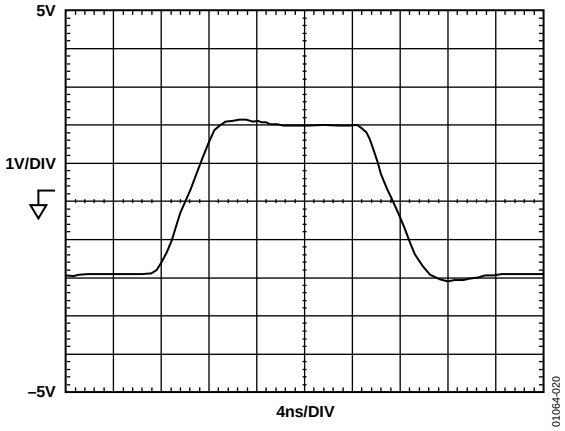


Figure 18. Large Signal Step Response G = –1, R_L = 1 kΩ, See Figure 42 for Test Circuit

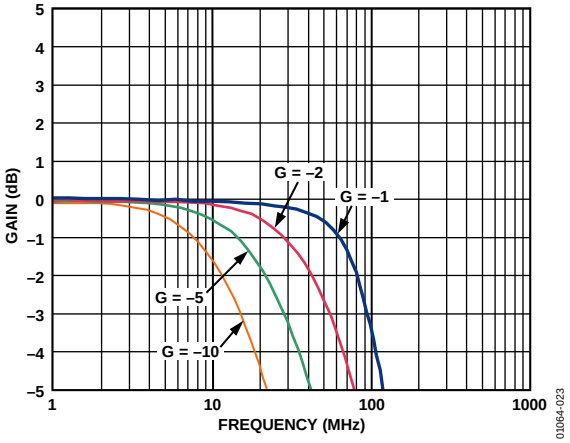


Figure 21. Large Signal Frequency Response

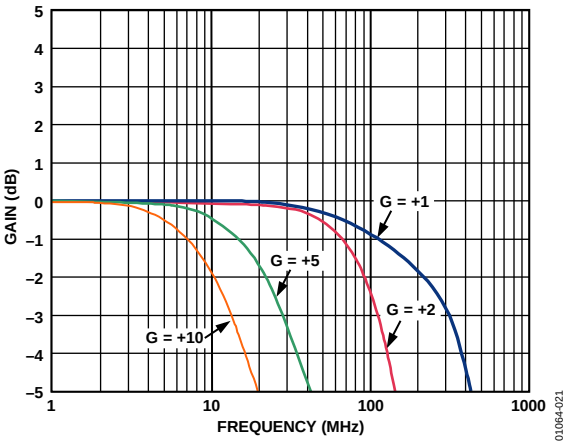


Figure 19. Small Signal Frequency Response, V_{OUT} = 0.2 V p-p

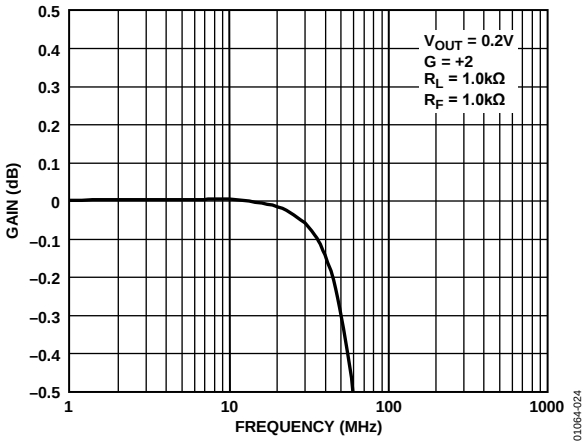


Figure 22. 0.1 dB Flatness G = +2

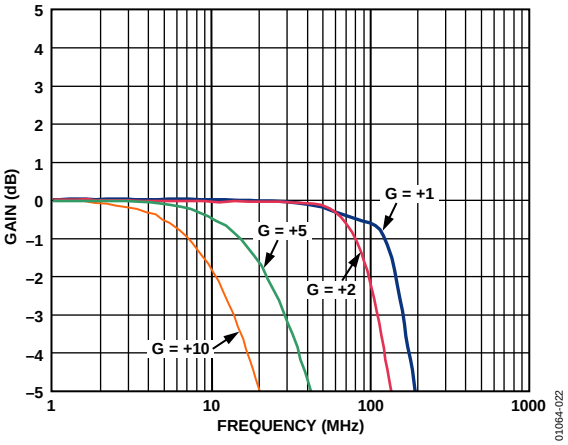


Figure 20. Large Signal Frequency Response, V_{OUT} = 2 V p-p

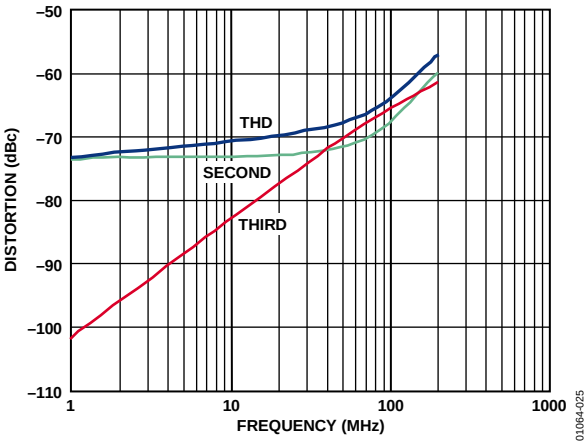


Figure 23. Distortion vs. Frequency, R_L = 150 Ω

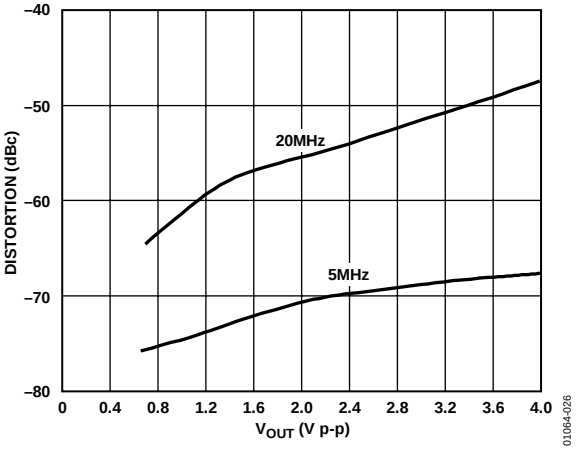


Figure 24. Distortion vs. V_{OUT} at 20 MHz, 5 MHz, R_L = 150 Ω, V_S = ±5.0 V

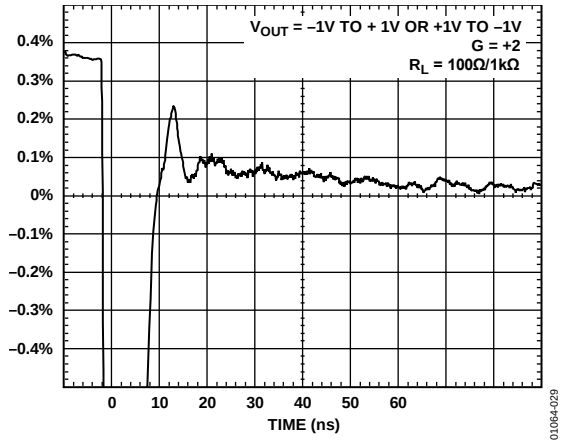


Figure 27. Settling Time

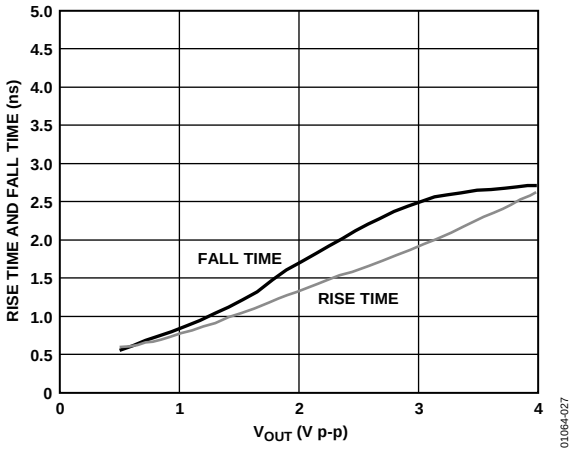


Figure 25. Rise Time and Fall Time vs. V_{OUT}, G = +1, R_L = 1 kΩ, R_F = 0 Ω

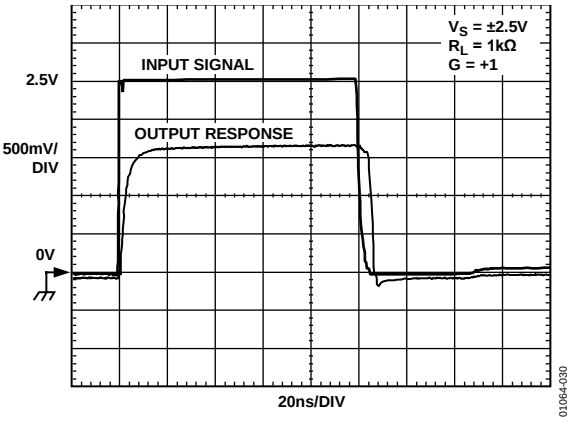


Figure 28. Input Overload Recovery, V_S = ±2.5 V

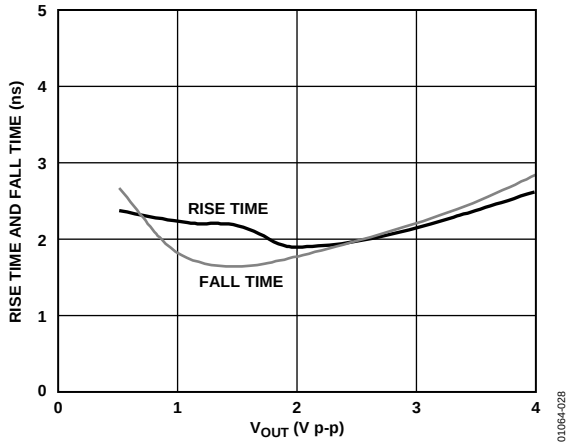


Figure 26. Rise Time and Fall Time vs. V_{OUT}, G = +2, R_L = 100 Ω, R_F = 402 Ω

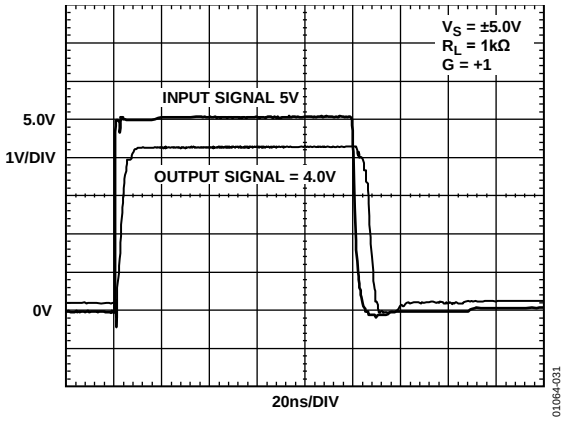


Figure 29. Output Overload Recovery, V_S = ±5.0 V

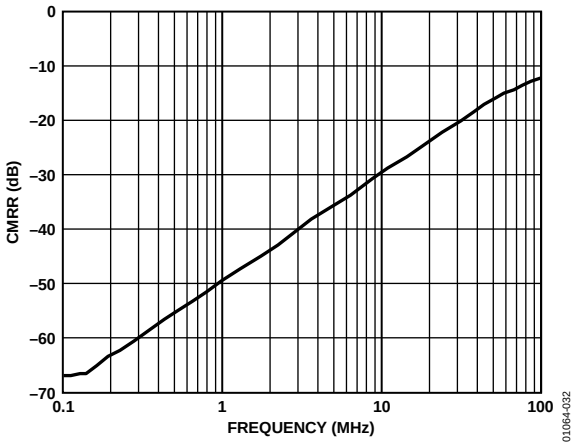


Figure 30. CMRR vs. Frequency

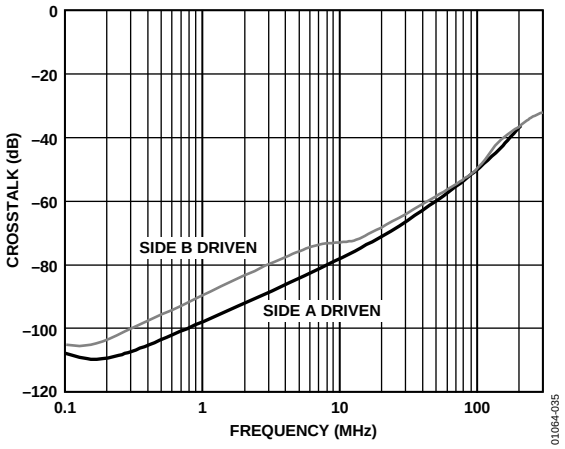


Figure 33. Crosstalk (Output-to-Output) vs. Frequency

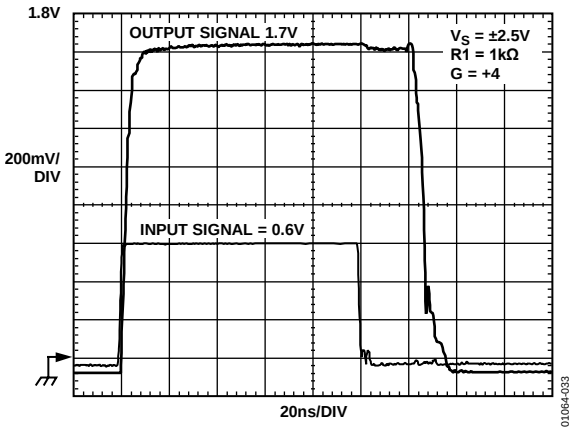


Figure 31. Output Overload Recovery, V_S = ±2.5 V

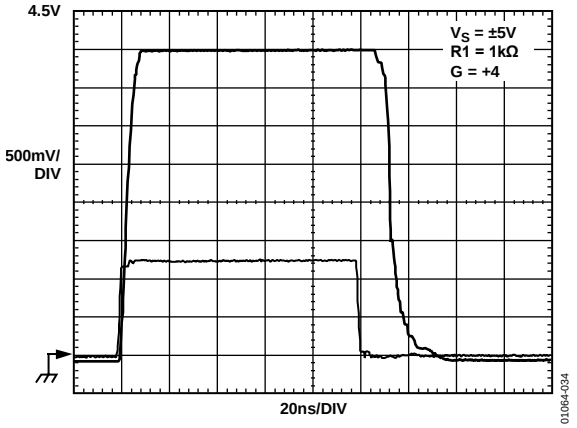


Figure 32. Output Overload Recovery, V_S = ±5.0 V

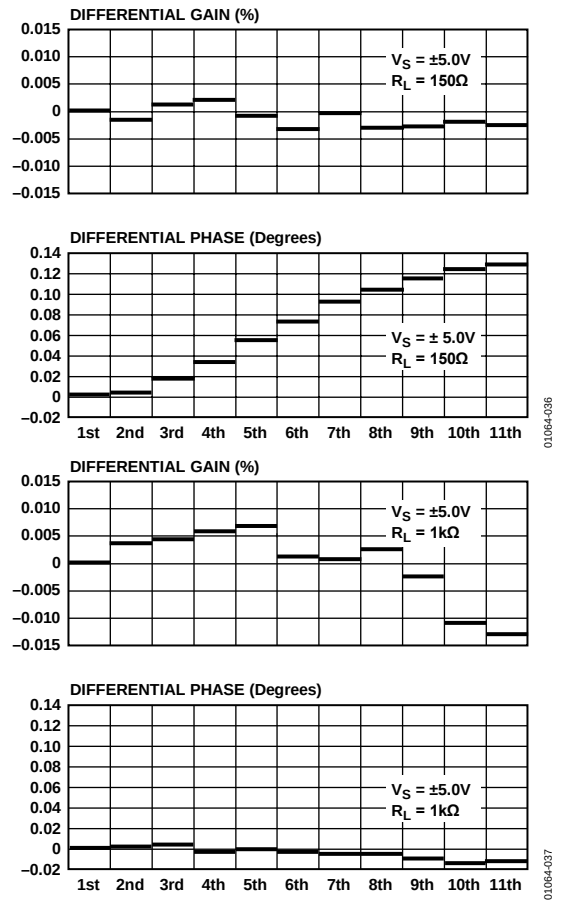


Figure 34. Differential Gain and Differential Phase One Back Terminated Load (150 Ω) (Video Op Amps Only)

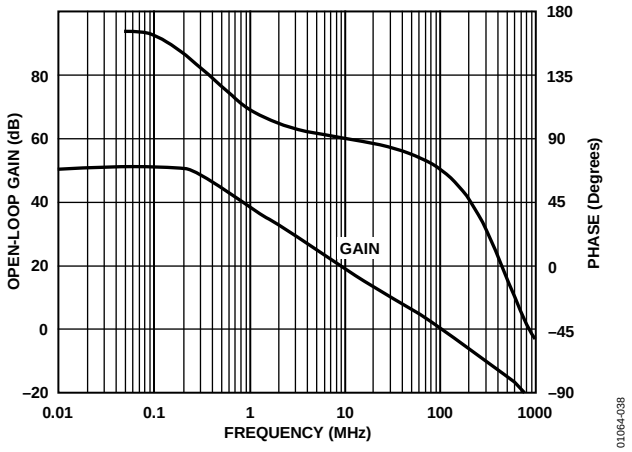


Figure 35. Open-Loop Gain and Phase vs. Frequency

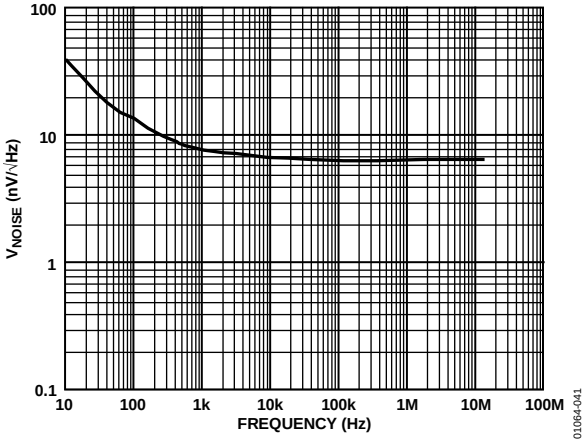


Figure 38. Voltage Noise vs. Frequency

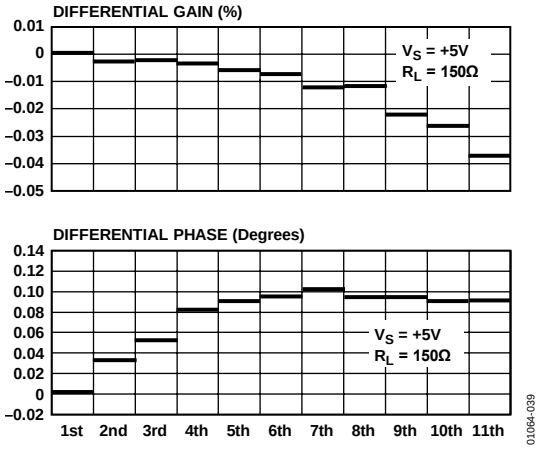


Figure 36. Differential Gain and Differential Phase, R_L = 150 Ω

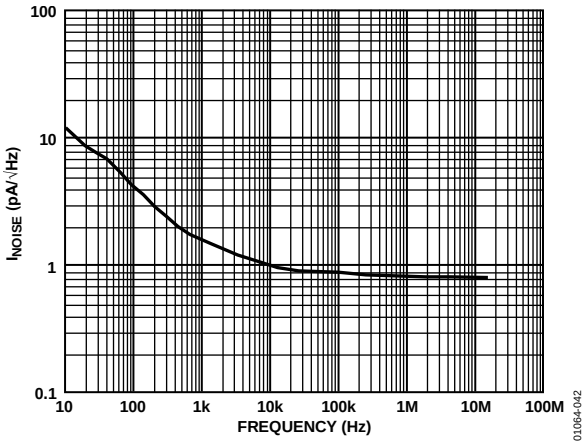


Figure 39. Current Noise vs. Frequency

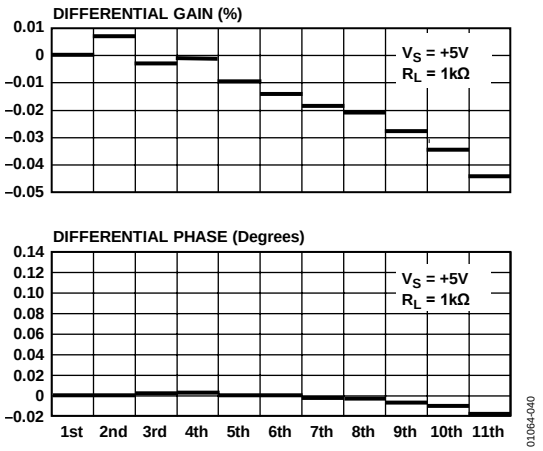


Figure 37. Differential Gain and Differential Phase, R_L = 1 kΩ

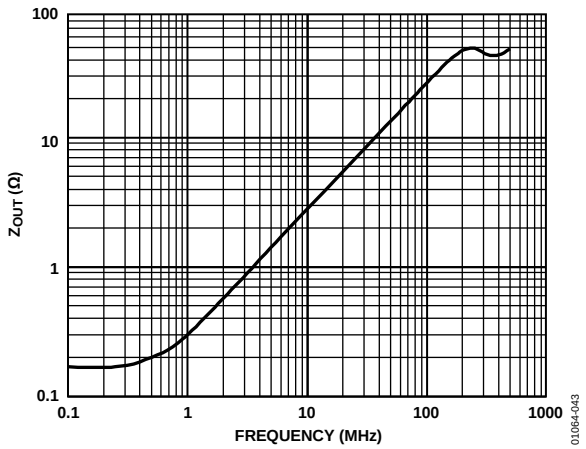


Figure 40. Output Impedance vs. Frequency

TEST CIRCUITS

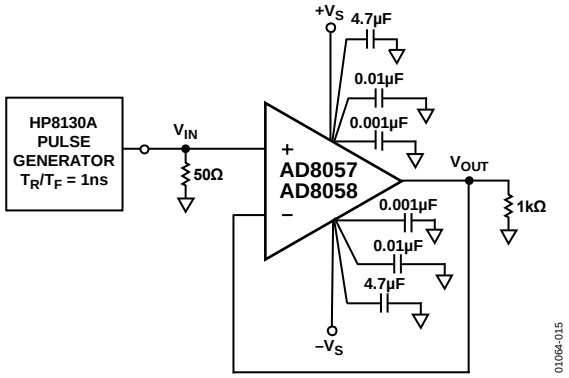


Figure 41. Test Circuit, G = +1, R_L = 1 kΩ

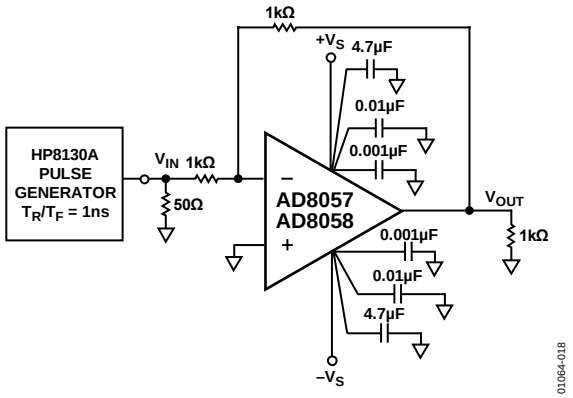


Figure 42. Test Circuit, G = −1, R_L = 1 kΩ

APPLICATIONS INFORMATION

DRIVING CAPACITIVE LOADS

When driving a capacitive load, most op amps exhibit overshoot in their pulse response. Figure 43 shows the relationship between the capacitive load that results in 30% overshoot and the closed-loop gain of an AD8058. It can be seen that, under the gain = +2 condition, the device is stable with capacitive loads of up to 69 pF.

In general, to minimize peaking or to ensure device stability for larger values of capacitive loads, a small series resistor (R_S) can be added between the op amp output and the load capacitor (C_L) as shown in Figure 44.

For the setup shown in Figure 44, the relationship between R_S and C_L was empirically derived and is shown in Table 4.

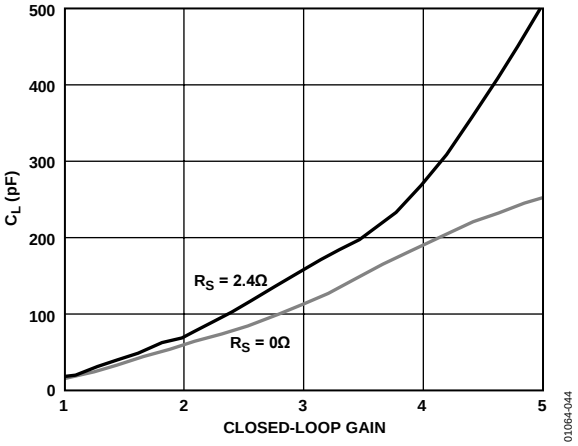


Figure 43. Capacitive Load Drive vs. Closed-Loop Gain

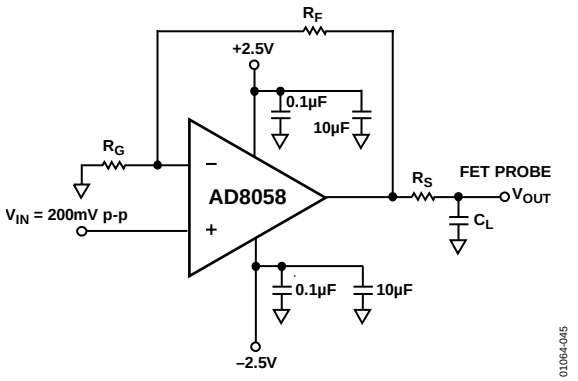


Figure 44. Capacitive Load Drive Circuit

Table 4. Recommended Value for Resistors R_S, R_F, R_G vs. Capacitive Load, C_L, Which Results in 30% Overshoot

Gain	R_F	R_G	C_L (R_S = 0 Ω)	C_L (R_S = 2.4 Ω)
1	100 Ω		11 pF	13 pF
2	100 Ω	100 Ω	51 pF	69 pF
3	100 Ω	50 Ω	104 pF	153 pF
4	100 Ω	33.2 Ω	186 pF	270 pF
5	100 Ω	25 Ω	245 pF	500 pF
10	100 Ω	11 Ω	870 pF	1580 pF

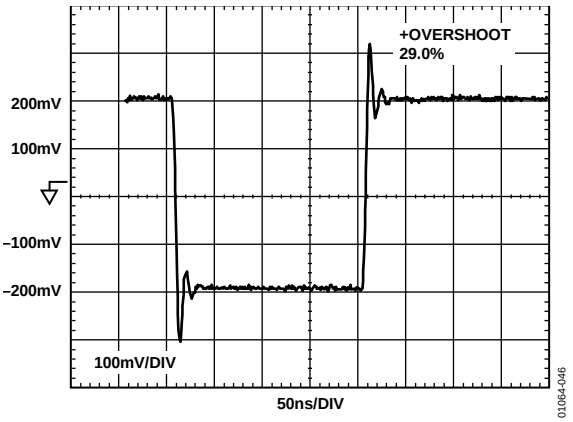


Figure 45. Typical Pulse Response with C_L = 65 pF, Gain = +2, and V_S = ±2.5

VIDEO FILTER

Some composite video signals that are derived from a digital source contain some clock feedthrough that can cause problems with downstream circuitry. This clock feedthrough is usually at 27 MHz, which is a standard clock frequency for both NTSC and PAL video systems. A filter that passes the video band and rejects frequencies at 27 MHz can be used to remove these frequencies from the video signal.

Figure 46 shows a circuit that uses an AD8057 to create a single 5 V supply, 3-pole Sallen-Key filter. This circuit uses a single RC pole in front of a standard 2-pole active section. To shift the dc operating point to midsupply, ac coupling is provided by R4, R5, and C4.

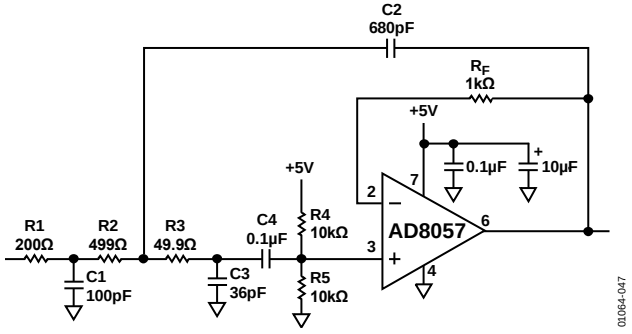


Figure 46. Low-Pass Filter for Video

Figure 47 shows a frequency sweep of this filter. The response is down 3 dB at 5.7 MHz; therefore, it passes the video band with little attenuation. The rejection at 27 MHz is 42 dB, which provides more than a factor of 100 in suppression of the clock components at this frequency.

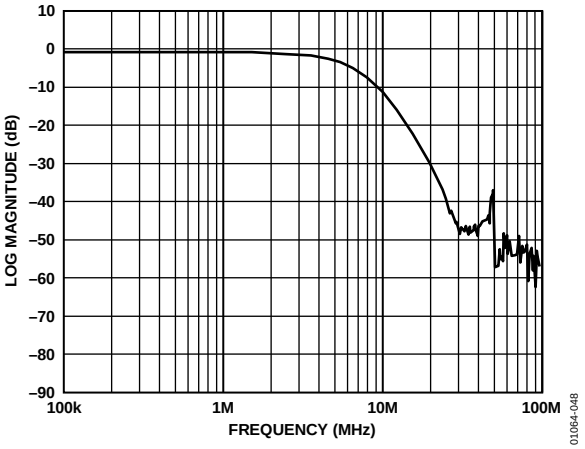


Figure 47. Video Filter Response

DIFFERENTIAL ANALOG-TO-DIGITAL DRIVER

As system supply voltages are dropping, many ADCs provide differential analog inputs to increase the dynamic range of the input signal while still operating on a low supply voltage. Differential driving can also reduce second and other even-order distortion products.

Analog Devices, Inc., offers an assortment of 12- and 14-bit high speed converters that have differential inputs and can be run from a single 5 V supply. These include the AD9220, AD9221, AD9223, AD9224, and AD9225 at 12 bits, and the AD9240, AD9241, and AD9243 at 14 bits. Although these devices can operate over a range of common-mode voltages at their analog inputs, they work best when the common-mode voltage at the input is at the midsupply or 2.5 V.

Op amp architectures that require upwards of 2 V of headroom at the output have significant problems when trying to drive such ADCs while operating with a 5 V positive supply. The low headroom output design of the AD8057 and AD8058 make them ideal for driving these types of ADCs.

The AD8058 can be used to make a dc-coupled, single-ended-to-differential driver for one of these ADCs. Figure 48 is a schematic of such a circuit for driving an AD9225, 12-bit, 25 MSPS ADC.

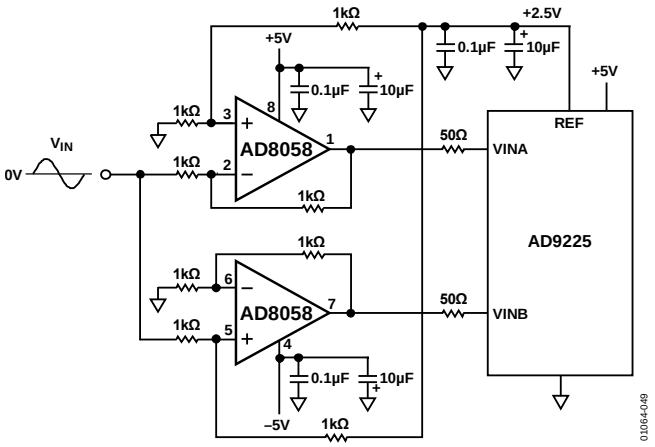


Figure 48. Schematic Circuit for Driving AD9225

In this circuit, one of the op amps is configured in the inverting mode whereas the other is in the noninverting mode. However, to provide better bandwidth matching, each op amp is configured for a noise gain of +2. The inverting op amp is configured for a gain of −1 and the noninverting op amp is configured for a gain of +2. Each of these produces a noise gain of +2, which is determined only by the inverse of the feedback ratio. The input signal to the noninverting op amp is divided by two to normalize its level and make it equal to the inverting output.

For 0 V input, the outputs of the op amps want to be at 2.5 V, which is the midsupply level of the ADCs. This is accomplished by first taking the 2.5 V reference output of the ADC and dividing it by two by a pair of 1 kΩ resistors. The resulting 1.25 V is applied to the positive input of each op amp. This voltage is then multiplied by the gain of +2 of the op amps to provide a 2.5 V level at each output.

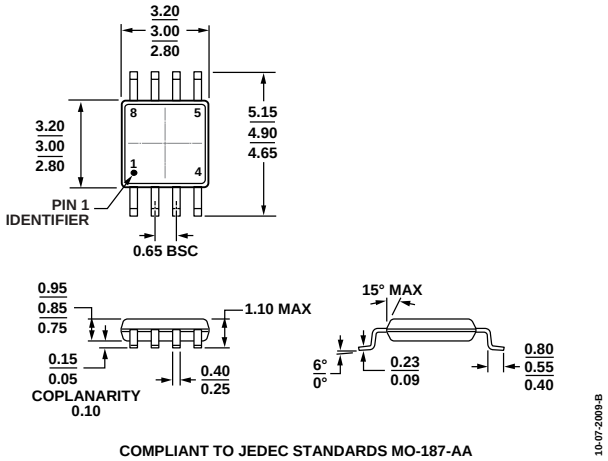
The assumption for this circuit is that the input signal is bipolar with respect to ground and the circuit must be dc-coupled thereby implying the existence of a negative supply elsewhere in the system. This circuit uses −5 V as the negative supply for the AD8058.

Tying the negative supply of the AD8058 to ground causes a problem at the input of the noninverting op amp. The input common-mode voltage can only go to within 1 V of the negative rail. Because this circuit requires that the positive inputs operate with a 1.25 V bias, there is not enough room to swing this voltage in the negative direction. The inverting stage does not have this problem because its common-mode input voltage remains fixed at 1.25 V. If dc coupling is not required, various ac coupling techniques can be used to eliminate this problem.

LAYOUT

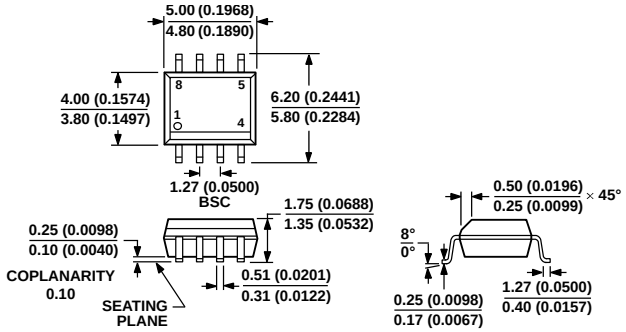
The AD8057 and AD8058 are high speed op amps for use in a board layout that follows standard high speed design rules. Make all signal traces as short and direct as possible. In particular, keep the parasitic capacitance on the inverting input of each device to a minimum to avoid excessive peaking and other undesirable performance. Bypass the power supplies very close to the power pins of the package with a 0.1 µF capacitor in parallel with a larger (approximately 10 µF) tantalum capacitor. Connect these capacitors to a ground plane that either is on an inner layer or fills the area of the board that is not used for other signals.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

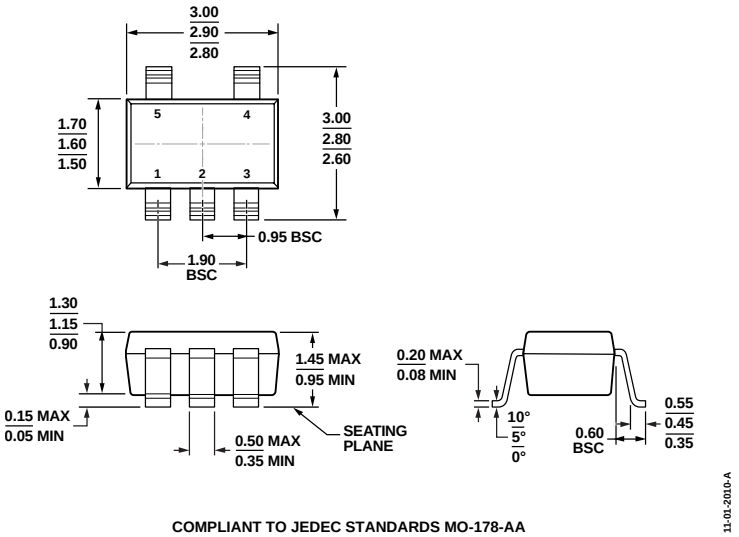
Figure 49. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 50. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 51. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option	Branding
AD8057AR		−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8057AR-REEL		−40°C to +85°C	8-Lead SOIC_N, 13″Tape and Reel	R-8	
AD8057AR-REEL7		−40°C to +85°C	8-Lead SOIC_N, 7″Tape and Reel	R-8	
AD8057ARZ		−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8057ARZ-REEL		−40°C to +85°C	8-Lead SOIC_N, 13″Tape and Reel	R-8	
AD8057ARZ-REEL7		−40°C to +85°C	8-Lead SOIC_N, 7″Tape and Reel	R-8	
AD8057ACHIPS		−40°C to +85°C	Die	Waffle Pak	
AD8057ART-R2		−40°C to +85°C	5-Lead SOT-23	RJ-5	H7A
AD8057ART-REEL7		−40°C to +85°C	5-Lead SOT-23	RJ-5	H7A
AD8057ARTZ-R2		−40°C to +85°C	5-Lead SOT-23	RJ-5	H08
AD8057ARTZ-REEL		−40°C to +85°C	5-Lead SOT-23	RJ-5	H08
AD8057ARTZ-REEL7		−40°C to +85°C	5-Lead SOT-23	RJ-5	H08
AD8057AR-EBZ		−40°C to +85°C	8-Lead SOIC_N Evaluation Board		
AD8057ART-EBZ		−40°C to +85°C	5-Lead SOT-23 Evaluation Board		
AD8058AR		−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8058AR-REEL7		−40°C to +85°C	8-Lead SOIC_N, 7″Tape and Reel	R-8	
AD8058ARZ		−40°C to +85°C	8-Lead SOIC_N	R-8	
AD8058ARZ-REEL		−40°C to +85°C	8-Lead SOIC_N, 13″Tape and Reel	R-8	
AD8058ARZ-REEL7		−40°C to +85°C	8-Lead SOIC_N, 7″Tape and Reel	R-8	
AD8058ACHIPS		−40°C to +85°C	Die	Waffle Pak	
AD8058ARM		−40°C to +85°C	8-Lead MSOP	RM-8	H8A
AD8058ARM-REEL7		−40°C to +85°C	8-Lead MSOP	RM-8	H8A
AD8058ARMZ-REEL7	[2]	−40°C to +85°C	8-Lead MSOP	RM-8	H8A
AD8058ARMZ	[2]	−40°C to +85°C	8-Lead MSOP	RM-8	H8A
AD8058ARMZ-REEL	[2]	−40°C to +85°C	8-Lead MSOP	RM-8	H8A
AD8058AR-EBZ		−40°C to +85°C	8-Lead SOIC_N Evaluation Board		
AD8058ARM-EBZ		−40°C to +85°C	8-Lead MSOP Evaluation Board		

[1] Z = RoHS Compliant Part.

[2] Bottom mark has # sign before date code.

D01064-0-3/14(E)