TABLE OF CONTENTS

REVISION HISTORY

12/14—Rev. D to Rev. E

Changes to Shift Register Section and Table 11 ... 22

9/10—Rev. C to Rev. D

Changes to SDO Pin and Daisy-Chain Operation Section ... 25

3/10—Rev. B to Rev. C

Changes to Revision History ... 2
Changes to Figure 3 and Figure 4 Captions ... 9

3/10—Rev. A to Rev. B

Changes to Data Sheet Title ... 1
Changes to General Description Section ... 1
Changes to Theory of Operation Section ... 22

12/09—Rev. 0 to Rev. A

Added 50 kΩ and 100 kΩ specifications ... Universal
Changes to Features Section ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Added Table 3 ... 5
Changes to Table 4 ... 6
Changes to Table 5 ... 7
Added Table 6 ... 8
Change to Table 7 ... 8
Changes to Absolute Maximum Rating Section ... 10
Changes Table 9 ... 11
Changes to Typical Performance Characteristics Section ... 12
Changes to Ordering Guide ... 30

4/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5291

V_{DD} = 21 V to 33 V, V_{SS} = 0 V; V_{DD} = 10.5 V to 16.5 V, V_{SS} = −10.5 V to −16.5 V; V_{LOGIC} = 2.7 V to 5.5 V, $V_A = V_{DD}$, $V_B = V_{SS}$, −40°C < T_A < +105°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		8			Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC	−1		+1	LSB
Resistor Integral Nonlinearity[2]	R-INL		−1		+1	LSB
Nominal Resistor Tolerance (R-Perf Mode)[3]	$\Delta R_{AB}/R_{AB}$	See Table 2, Table 3	−1	±0.5	+1	%
Nominal Resistor Tolerance (Normal Mode)	$\Delta R_{AB}/R_{AB}$			±7		%
Resistance Temperature Coefficient[4]	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full-scale; See Figure 38		35		ppm/°C
Wiper Resistance	R_W	Code= zero scale		60	100	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Resolution	N		8			Bits
Differential Nonlinearity[5]	DNL		−0.5		+0.5	LSB
Integral Nonlinearity[5]	INL		−0.5		+0.5	LSB
Voltage Divider Temperature Coefficient[4]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half-scale; See Figure 41		1.5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−2		+0.25	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		2	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[6]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[4]	C_A, C_B	f = 1 MHz, measured to GND, code = half-scale		85		pF
Capacitance W[4]	C_W	f = 1 MHz, measured to GND, code = half-scale		65		pF
Common-Mode Leakage Current[4]	I_{CM}	$V_A = V_B = V_W$		±1		nA
DIGITAL INPUTS		JEDEC compliant				
Input Logic High[4]	V_{IH}	V_{LOGIC} = 2.7 V to 5.5 V	2.0			V
Input Logic Low[4]	V_{IL}	V_{LOGIC} = 2.7 V to 5.5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{LOGIC}			±1	µA
Input Capacitance[4]	C_{IL}			5		pF
DIGITAL OUTPUTS (SDO and RDY)						
Output High Voltage[4]	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}	V_{LOGIC} − 0.4			V
Output Low Voltage[4]	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}			GND + 0.4 V	V
Three-State Leakage Current			−1		+1	µA
Output Capacitance[4]	C_{OL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	9		33	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±9		±16.5	V
Positive Supply Current	I_{DD}	V_{DD}/V_{SS} = ±16.5 V		0.1	2	µA
Negative Supply Current	I_{SS}	V_{DD}/V_{SS} = ±16.5 V	−2	−0.1		µA
Logic Supply Range	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V; V_{IH} = 5 V or V_{IL} = GND		1	10	µA
OTP Store Current[4, 7]	I_{LOGIC_PROG}	V_{IH} = 5 V or V_{IL} = GND		25		mA
OTP Read Current[4, 8]	$I_{LOGIC\_FUSE\_READ}$	V_{IH} = 5 V or V_{IL} = GND		25		mA
Power Dissipation[9]	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND		8	110	µW
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10%				%/%
		R_{AB} = 20 kΩ		0.103		
		R_{AB} = 50 kΩ		0.039		
		R_{AB} = 100 kΩ		0.021		

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[5, 10]						
Bandwidth	BW	−3 dB, code = half-scale				kHz
		R_{AB} = 20 kΩ		520		
		R_{AB} = 50 kΩ		210		
		R_{AB} = 100 kΩ		105		
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz				dB
		R_{AB} = 20 kΩ		−93		
		R_{AB} = 50 kΩ		−101		
		R_{AB} = 100 kΩ		−106		
V_W Settling Time	t_S	V_A = 30 V, V_B = 0 V, ±0.5 LSB error band, initial code = zero scale, board capacitance = 170 pF				
		Code = full-scale, normal mode		750		ns
		Code = full-scale, R-Perf mode		2.5		µs
		Code = half-scale, normal mode				µs
		R_{AB} = 20 kΩ		2.5		
		R_{AB} = 50 kΩ		7		
		R_{AB} = 100 kΩ		14		
		Code = half-scale, R-Perf mode				µs
		R_{AB} = 20 kΩ		5		
		R_{AB} = 50 kΩ		9		
		R_{AB} = 100 kΩ		16		
Resistor Noise Density	e_{N_WB}	Code = half-scale, T_A = 25°C, 0 kHz to 200 kHz				nV/√Hz
		R_{AB} = 20 kΩ		10		
		R_{AB} = 50 kΩ		18		
		R_{AB} = 100 kΩ		27		

[1] Typical values represent average readings at 25°C, V_{DD} = 15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between the R_{WB} at code 0x02 to code 0xFF or between R_{WA} at code 0xFD to code 0x00. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode, with a wiper current of 1 mA for V_A < 12 V and 1.2 mA for V_A ≥ 12 V.
[3] Resistor performance mode (see the Resistor Performance Mode section). The terms resistor performance mode and R-Perf mode are used interchangeably.
[4] Guaranteed by design and characterization, not subject to production test.
[5] INL and DNL are measured at V_{WB} with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[7] Different from operating current; supply current for fuse program lasts approximately 550 µs.
[8] Different from operating current; supply current for fuse read lasts approximately 550 µs.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$) + ($I_{LOGIC} \times V_{LOGIC}$).
[10] All dynamic characteristics use V_{DD} = 15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.

RESISTOR PERFORMANCE MODE CODE RANGE

Table 2.

Resistor Tolerance per Code	R_{AB} = 20 kΩ							
	$\|V_{DD} - V_{SS}\|$ = 30 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 26 V to 30 V		$\|V_{DD} - V_{SS}\|$ = 22 V to 26 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 22 V	
	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}
1% R-Tolerance	From 0x5A to 0xFF	From 0x00 to 0xA5	From 0x7D to 0xFF	From 0x00 to 0x82	From 0x7D to 0xFF	From 0x00 to 0x82	N/A	N/A
2% R-Tolerance	From 0x23 to 0xFF	From 0x00 to 0xDC	From 0x2D to 0xFF	From 0x00 to 0xD2	From 0x23 to 0xFF	From 0x00 to 0xDC	From 0x23 to 0xFF	From 0x00 to 0xDC
3% R-Tolerance	From 0x1E to 0xFF	From 0x00 to 0xE1	From 0x19 to 0xFF	From 0x00 to 0xE6	From 0x17 to 0xFF	From 0x00 to 0xE8	From 0x17 to 0xFF	From 0x00 to 0xE8

Table 3.

Resistor Tolerance per Code	R_{AB} = 50 kΩ				R_{AB} = 100 kΩ			
	$\|V_{DD} - V_{SS}\|$ = 26 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 26 V		$\|V_{DD} - V_{SS}\|$ = 26 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 26 V	
	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}
1% R-Tolerance	From 0x2A to 0xFF	From 0x00 to 0xD5	From 0x37 to 0xFF	From 0x00 to 0xC8	From 0x1E to 0xFF	From 0x00 to 0xE1	From 0x14 to 0xFF	From 0x00 to 0xEB
2% R-Tolerance	From 0x11 to 0xFF	From 0x00 to 0xEE	From 0x16 to 0xFF	From 0x00 to 0xE9	From 0x0A to 0xFF	From 0x00 to 0xF5	From 0x0A to 0xFF	From 0x00 to 0xF5
3% R-Tolerance	From 0x0A to 0xFF	From 0x00 to 0xF5	From 0x0D to 0xFF	From 0x00 to 0xF2	From 0x07 to 0xFF	From 0x00 to 0xF8	From 0x07 to 0xFF	From 0x00 to 0xF8

ELECTRICAL CHARACTERISTICS—AD5292

V_{DD} = 21 V to 33 V, V_{SS} = 0 V; V_{DD} = 10.5 V to 16.5 V, V_{SS} = −10.5 V to −16.5 V; V_{LOGIC} = 2.7 V to 5.5 V, $V_A = V_{DD}$, $V_B = V_{SS}$, −40°C < T_A < +105°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution	N		10			Bits
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC	−1		+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{AB} =50 kΩ, 100 kΩ	−2		+2	LSB
	R-INL	R_{AB} =20 kΩ , $\|V_{DD} - V_{SS}\|$ = 26 V to 33 V	−2		+2	LSB
	R-INL	R_{AB} =20 kΩ , $\|V_{DD} - V_{SS}\|$ = 21 V to 26 V	−3		+3	LSB
Nominal Resistor Tolerance (R-Perf Mode)[3]	$\Delta R_{AB}/R_{AB}$	See Table 5 and Table 6	−1	±0.5	+1	%
Nominal Resistor Tolerance (Normal Mode)[4]	$\Delta R_{AB}/R_{AB}$			±7		%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB})/\Delta T \times 10^6$	Code = full scale; See Figure 38		35		ppm/°C
Wiper Resistance	R_W	Code= zero scale		60	100	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity[5]	DNL		−1		+1	LSB
Integral Nonlinearity[5]	INL		−1.5		+1.5	LSB
Voltage Divider Temperature Coefficient[4]	$(\Delta V_W/V_W)/\Delta T \times 10^6$	Code = half scale; See Figure 41		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = full scale	−8		+1	LSB
Zero-Scale Error	V_{WZSE}	Code = zero scale	0		8	LSB
RESISTOR TERMINALS						
Terminal Voltage Range[4]	V_A, V_B, V_W		V_{SS}		V_{DD}	V
Capacitance A, Capacitance B[6]	C_A, C_B	f = 1 MHz, measured to GND, code = half scale		85		pF
Capacitance W[5]	C_W	f = 1 MHz, measured to GND, code = half scale		65		pF
Common-Mode Leakage Current[4]	I_{CM}	$V_A = V_B = V_W$		±1		nA
DIGITAL INPUTS		JEDEC compliant				
Input Logic High[4]	V_{IH}	V_{LOGIC} = 2.7 V to 5.5 V	2.0			V
Input Logic Low[4]	V_{IL}	V_{LOGIC} = 2.7 V to 5.5 V			0.8	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{LOGIC}			±1	μA
Input Capacitance[4]	C_{IL}			5		pF
DIGITAL OUTPUTS (SDO and RDY)						
Output High Voltage[4]	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}	V_{LOGIC} − 0.4			V
Output Low Voltage[4]	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}			GND + 0.4	V
Three-State Leakage Current			−1		+1	μA
Output Capacitance[4]	C_{OL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	9		33	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±9		±16.5	V
Positive Supply Current	I_{DD}	V_{DD}/V_{SS} = ±16.5 V		0.1	2	μA
Negative Supply Current	I_{SS}	V_{DD}/V_{SS} = ±16.5 V	−2	−0.1		μA
Logic Supply Range	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{LOGIC} = 5 V; V_{IH} = 5 V or V_{IL} = GND		1	10	μA
OTP Store Current[6, 7]	I_{LOGIC_PROG}	V_{IH} = 5 V or V_{IL} = GND		25		mA
OTP Read Current[6, 8]	$I_{LOGIC\_FUSE\_READ}$	V_{IH} = 5 V or V_{IL} = GND		25		mA
Power Dissipation[9]	P_{DISS}	V_{IH} = 5 V or V_{IL} = GND		8	110	μW
Power Supply Rejection Ratio[6]	PSSR	$\Delta V_{DD}/\Delta V_{SS}$ = ±15 V ± 10%				%/%
		R_{AB} = 20 kΩ		0.103		
		R_{AB} = 50 kΩ		0.039		
		R_{AB} = 100 kΩ		0.021		

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[5, 10]						
Bandwidth	BW	−3 dB				kHz
		R_{AB} = 20 kΩ		520		
		R_{AB} = 50 kΩ		210		
		R_{AB} = 100 kΩ		105		
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz				dB
		R_{AB} = 20 kΩ		−93		
		R_{AB} = 50 kΩ		−101		
		R_{AB} = 100 kΩ		−106		
V_W Settling Time	t_S	V_A = 30 V, V_B = 0 V, ±0.5 LSB error band, initial code = zero scale, board capacitance = 170 pF				
		Code = full-scale, normal mode		750		ns
		Code = full-scale, R-Perf mode		2.5		µs
		Code = half-scale, normal mode				µs
		R_{AB} = 20 kΩ		2.5		
		R_{AB} = 50 kΩ		7		
		R_{AB} = 100 kΩ		14		
		Code = half-scale, R-Perf mode				µs
		R_{AB} = 20 kΩ		5		
		R_{AB} = 50 kΩ		9		
		R_{AB} = 100 kΩ		16		
Resistor Noise Density	e_{N_WB}	Code = half-scale, T_A = 25°C, 0 kHz to 200 kHz				nV/√Hz
		R_{AB} = 20 kΩ		10		
		R_{AB} = 50 kΩ		18		
		R_{AB} = 100 kΩ		27		

[1] Typical values represent average readings at 25°C, V_{DD} = 15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.
[2] Resistor position nonlinearity error. R-INL is the deviation from an ideal value measured between the R_{WB} at code 0x00B to code 0x3FF or between R_{WA} at code 0x3F3 to code 0x000. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode, with a wiper current of 1 mA for V_A < 12 V and 1.2 mA for V_A ≥ 12 V.
[3] Resistor performance mode (see the Resistor Performance Mode section). The terms resistor performance mode and R-Perf mode are used interchangeably.
[4] Guaranteed by design and characterization, not subject to production test.
[5] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V_A = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[6] Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[7] Different from operating current; supply current for fuse program lasts approximately 550 µs.
[8] Different from operating current; supply current for fuse read lasts approximately 550 µs.
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$) + ($I_{LOGIC} \times V_{LOGIC}$).
[10] All dynamic characteristics use V_{DD} = 15 V, V_{SS} = −15 V, and V_{LOGIC} = 5 V.

RESISTOR PERFORMANCE MODE CODE RANGE

Table 5.

Resistor Tolerance per Code	R_{AB} = 20 kΩ							
	$\|V_{DD} - V_{SS}\|$ = 30 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 26 V to 30 V		$\|V_{DD} - V_{SS}\|$ = 22 V to 26 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 22 V	
	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}
1% R-Tolerance	From 0x15E to 0x3FF	From 0x000 to 0x2A1	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	From 0x1F4 to 0x3FF	From 0x000 to 0x20B	N/A	N/A
2% R-Tolerance	From 0x8C to 0x3FF	From 0x000 to 0x373	From 0xB4 to 0x3FF	From 0x000 to 0x34B	From 0xFA to 0x3FF	From 0x000 to 0x305	From 0xFA to 0x3FF	From 0x000 to 0x305
3% R-Tolerance	From 0x5A to 0x3FF	From 0x000 to 0x3A5	From 0x64 to 0x3FF	From 0x000 to 0x39B	From 0x78 to 0x3FF	From 0x000 to 0x387	From 0x78 to 0x3FF	From 0x000 to 0x387

Table 6.

Resistor Tolerance per Code	R_{AB} = 50 kΩ				R_{AB} = 100 kΩ			
	$\|V_{DD} - V_{SS}\|$ = 26 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 26 V		$\|V_{DD} - V_{SS}\|$ = 26 V to 33 V		$\|V_{DD} - V_{SS}\|$ = 21 V to 26 V	
	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}	R_{WB}	R_{WA}
1% R-Tolerance	From 0x08C to 0x3FF	From 0x000 to 0x35F	From 0x0B4 to 0x3FF	From 0x000 to 0x31E	From 0x04B to 0x3FF	From 0x000 to 0x3B4	From 0x064 to 0x3FF	From 0x000 to 0x39B
2% R-Tolerance	From 0X03C to 0x3FF	From 0x000 to 0x3C3	From 0x050 to 0x3FF	From 0x000 to 0x3AF	From 0x028 to 0x3FF	From 0x000 to 0x3D7	From 0x028 to 0x3FF	From 0x000 to 0x3D7
3% R-Tolerance	From 0X028 to 0x3FF	From 0x000 to 0x3D7	From 0x032 to 0x3FF	From 0x000 to 0x3CD	From 0x019 to 0x3FF	From 0x000 to 0x3E6	From 0x019 to 0x3FF	From 0x000 to 0x3E6

INTERFACE TIMING SPECIFICATIONS

V_{DD}/V_{SS} = ±15 V, V_{LOGIC} = 2.7 V to 5.5 V, −40°C < T_A < +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 7.

Parameter	Limit[1]	Unit	Description
t_1[2]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	1	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	400[3]	ns min	Minimum $\overline{SYNC}$ high time
t_9	14	ns min	$\overline{SYNC}$ rising edge to next SCLK fall ignore
t_{10}[4]	1	ns min	RDY rising edge to $\overline{SYNC}$ falling edge
t_{11}[4]	40	ns max	$\overline{SYNC}$ rising edge to RDY fall time
t_{12}[4]	2.4	µs max	RDY low time, RDAC register write command execute time (R-Perf mode)
t_{12}[4]	410	ns max	RDY low time, RDAC register write command execute time (normal mode)
t_{12}[4]	8	ms max	RDY low time, memory program execute time
t_{12}[4]	1.5	ms min	Software/hardware reset
t_{13}[4]	450	ns max	RDY low time, RDAC register readback execute time
t_{13}[4]	1.3	ms max	RDY low time, memory readback execute time
t_{14}[4]	450	ns max	SCLK rising edge to SDO valid
t_{RESET}	20	ns min	Minimum $\overline{RESET}$ pulse width (asynchronous)
$t_{POWER-UP}$[5]	2	ms max	Power-on OTP restore time

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Maximum SCLK frequency is 50 MHz.
[3] Refer to t_{12} and t_{13} for RDAC register and memory commands operations.
[4] R_{PULL_UP} = 2.2 kΩ to V_{LOGIC}, with a capacitance load of 168 pF.
[5] Maximum time after V_{LOGIC} is equal to 2.5 V.

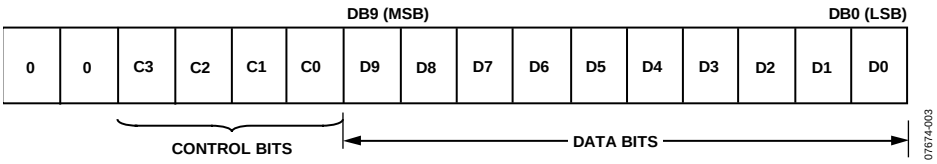

Figure 2. Shift Register Content

Timing Diagrams

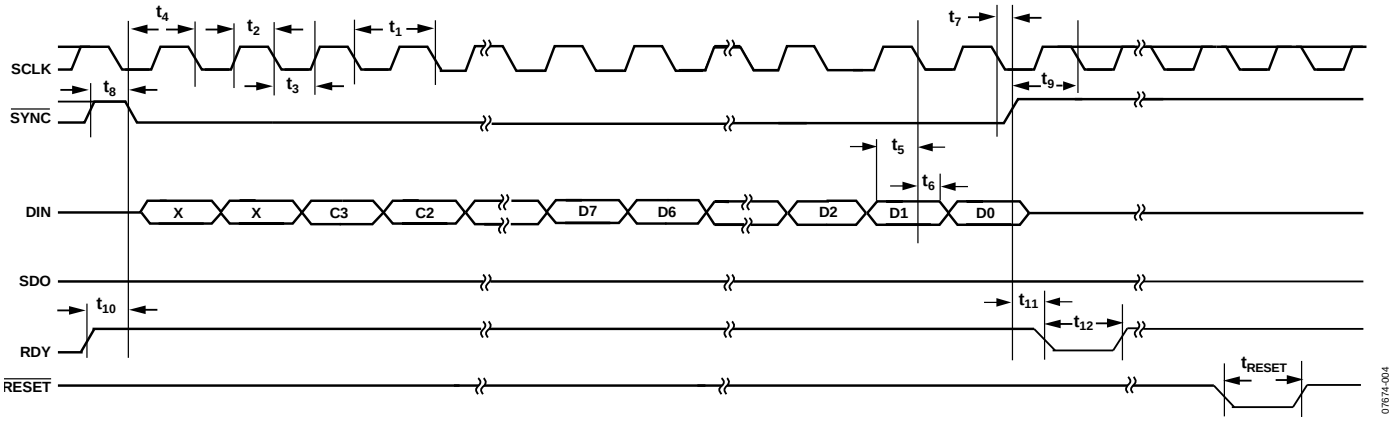

Figure 3. Write Timing Diagram, CPOL = 0, CPHA = 1

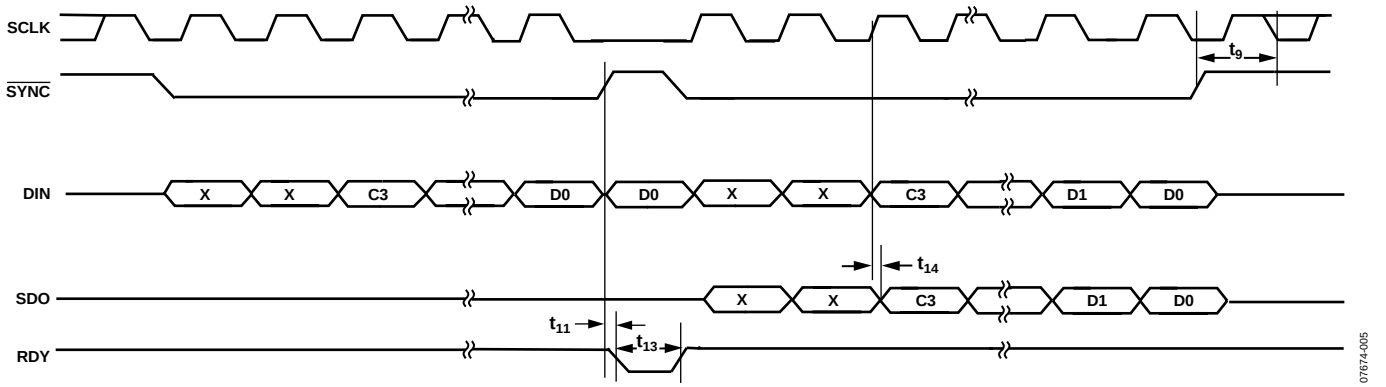

Figure 4. Read Timing Diagram, CPOL = 0, CPHA = 1

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
V_{DD} to GND	−0.3 V to +35 V
V_{SS} to GND	+0.3 V to − 25 V
V_{LOGIC} to GND	−0.3 V to + 7 V
V_{DD} to V_{SS}	35 V
V_A, V_B, V_W to GND	V_{SS} − 0.3 V, V_{DD}+ 0.3 V
Digital Input and Output Voltage to GND	−0.3 V to V_{LOGIC} + 0.3 V
EXT_CAP Voltage to GND	−0.3 V to +7 V
I_A, I_B, I_W	
Continuous	
R_{AB} = 20 kΩ	±3 mA
R_{AB} = 50 kΩ, 100 kΩ	±2mA
Pulsed[1]	
Frequency > 10 kHz	MCC^2/d^3
Frequency ≤ 10 kHz	$MCC^2/\sqrt{d^3}$
Operating Temperature Range[4]	−40°C to +105°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Maximum continuous current
[3] Pulse duty factor.
[4] Includes programming of OTP memory.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead TSSOP	93[1]	20	°C/W

[1] JEDEC 2S2P test board, still air (0 m/sec to 1 m/sec airflow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

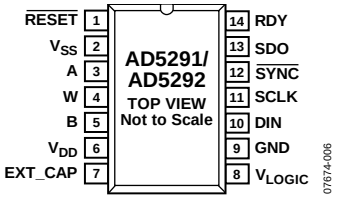

Figure 5. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Hardware Reset Pin. Refreshes the RDAC register with the contents of the 20-TP memory register. Factory default loads midscale until the first 20-TP wiper memory location is programmed. $\overline{\text{RESET}}$ is activated at the logic high transition. Tie $\overline{\text{RESET}}$ to V_{LOGIC} if not used.
2	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
3	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$.
4	W	Wiper Terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$.
5	B	Terminal B of RDAC. $V_{SS} \le V_B \le V_{DD}$.
6	V_{DD}	Positive Power Supply. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
7	EXT_CAP	External Capacitor. Connect a 1 µF capacitor to EXT_CAP. This capacitor must have a voltage rating of ≥7 V.
8	V_{LOGIC}	Logic Power Supply; 2.7 V to 5.5 V. This pin should be decoupled with 0.1 µF ceramic capacitors and 10 µF capacitors.
9	GND	Ground Pin, Logic Ground Reference.
10	DIN	Serial Data Input. The AD5291 and AD5292 have a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
11	SCLK	Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.
12	$\overline{\text{SYNC}}$	Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the shift register and data is transferred in on the falling edges of the following clocks. The selected register is updated on the rising edge of $\overline{\text{SYNC}}$ following the 16th clock cycle. If $\overline{\text{SYNC}}$ is taken high before the 16th clock cycle, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt, and the write sequence is ignored by the DAC.
13	SDO	Serial Data Output. This open-drain output requires an external pull-up resistor. SDO can be used to clock data from the shift register in daisy-chain mode or in readback mode.
14	RDY	Ready Pin. This active-high open-drain output identifies the completion of a write or read operation to or from the RDAC register or memory.

TYPICAL PERFORMANCE CHARACTERISTICS

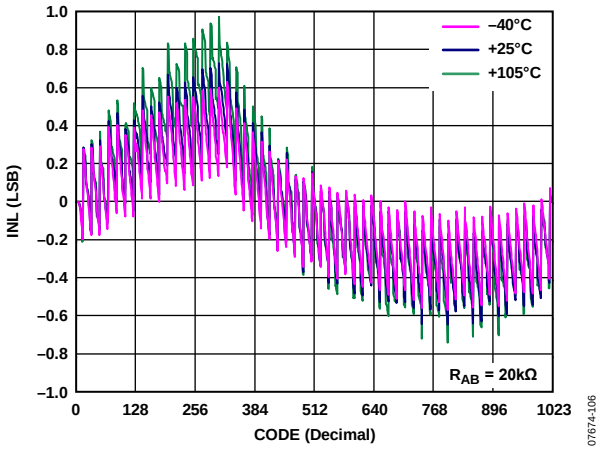

Figure 6. R-INL in R-Perf Mode vs. Code vs. Temperature (AD5292)

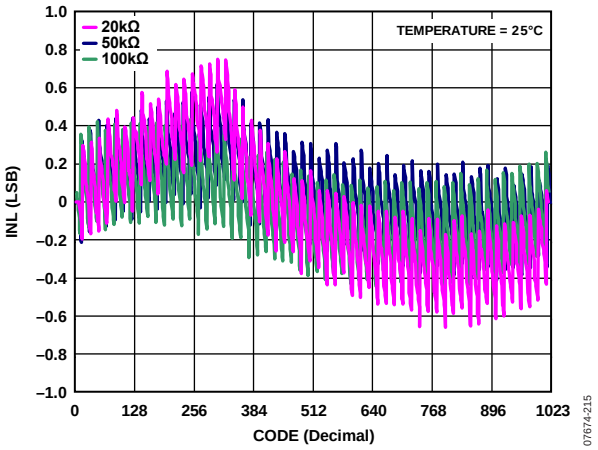

Figure 9. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

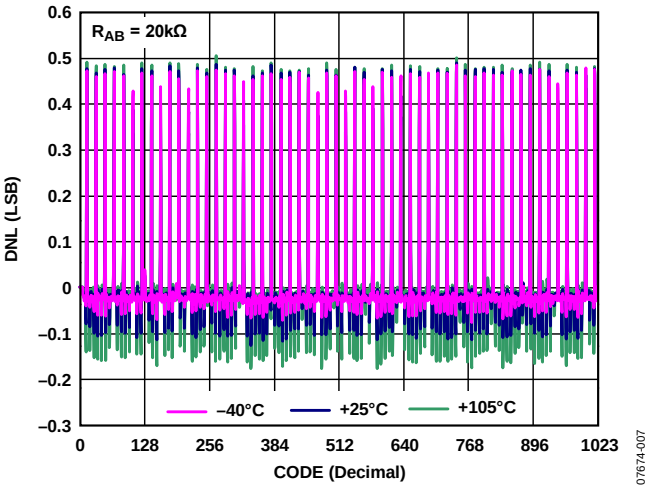

Figure 7. R-DNL in R-Perf Mode vs. Code vs. Temperature (AD5292)

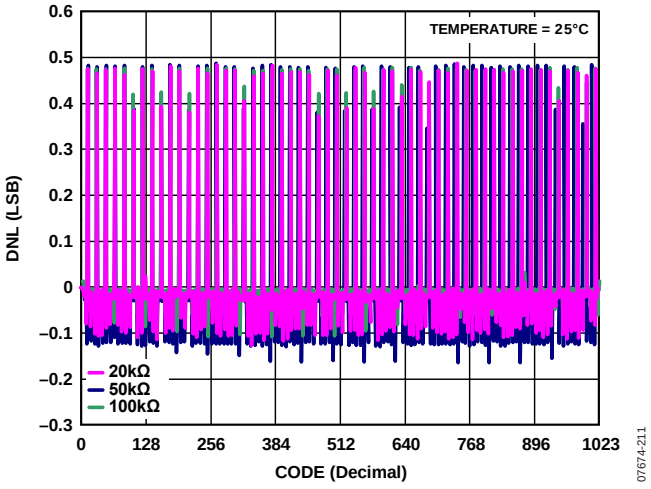

Figure 10. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

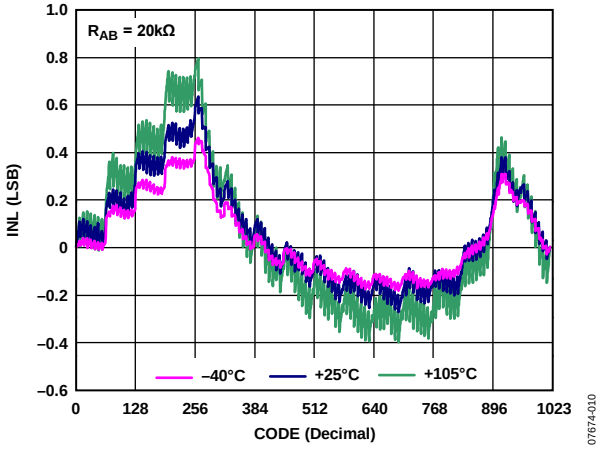

Figure 8. R-INL in Normal Mode vs. Code vs. Temperature (AD5292)

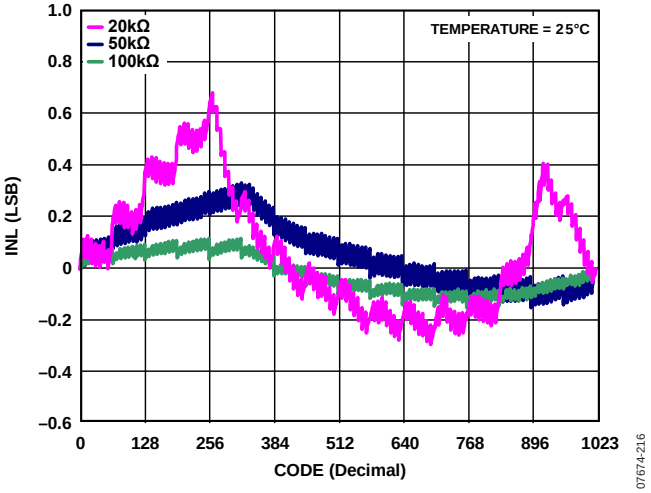

Figure 11. R-INL in Normal Mode vs. Code vs. Nominal Resistance (AD5292)

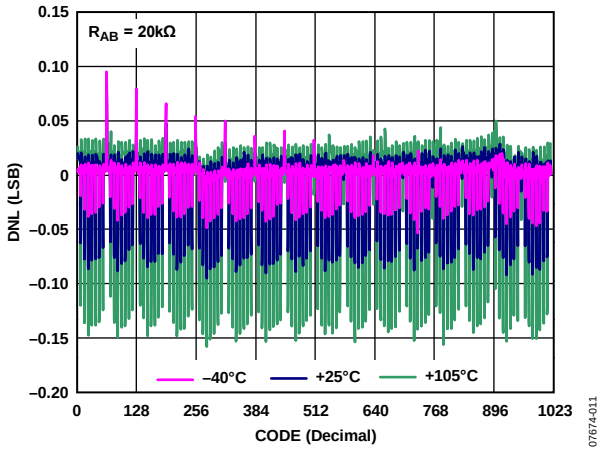

Figure 12. R-DNL in Normal Mode vs. Code vs. Temperature (AD5292)

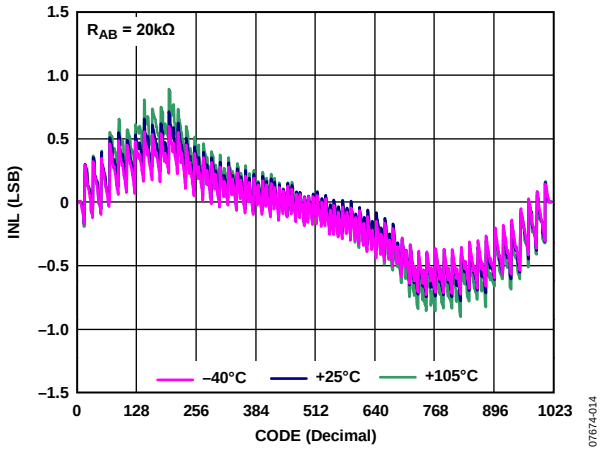

Figure 13. INL in R-Perf Mode vs. Code vs. Temperature (AD5292)

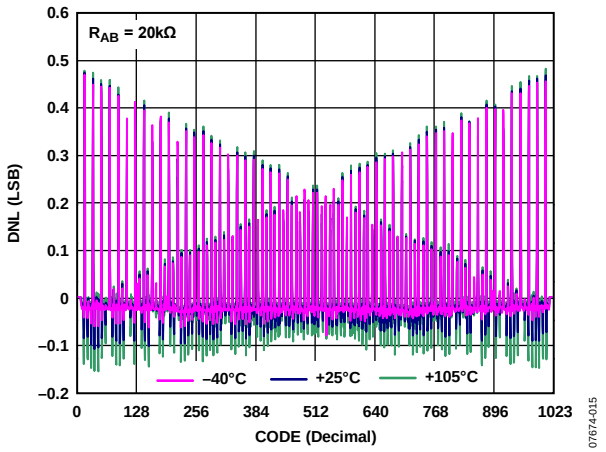

Figure 14. DNL in R-Perf Mode vs. Code vs. Temperature (AD5292)

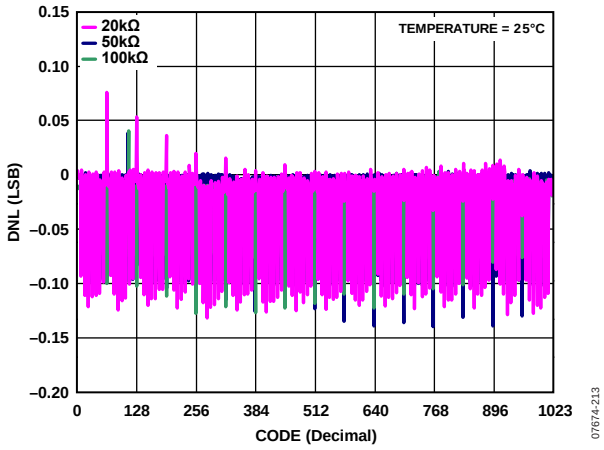

Figure 15. R-DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5292)

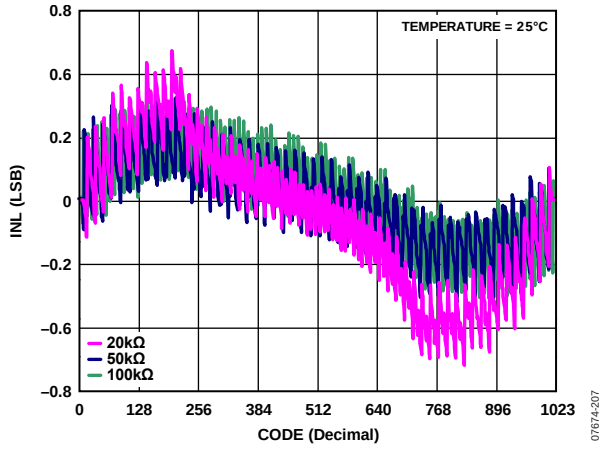

Figure 16. INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

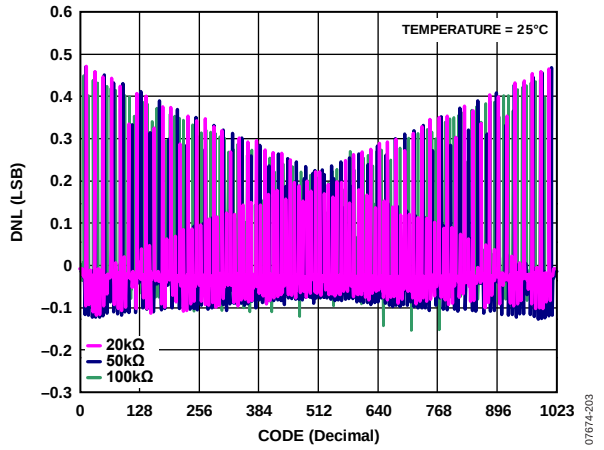

Figure 17. DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5292)

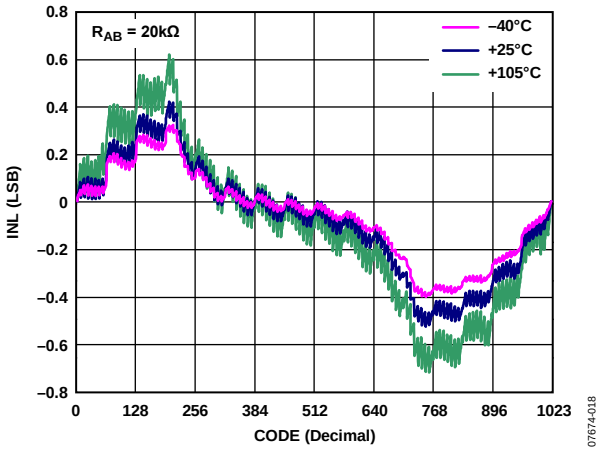

Figure 18. INL in Normal Mode vs. Code vs. Temperature (AD5292)

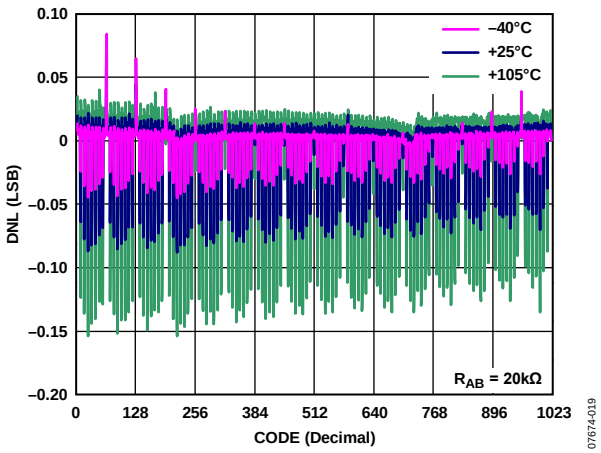

Figure 19. DNL in Normal Mode vs. Code vs. Temperature (AD5292)

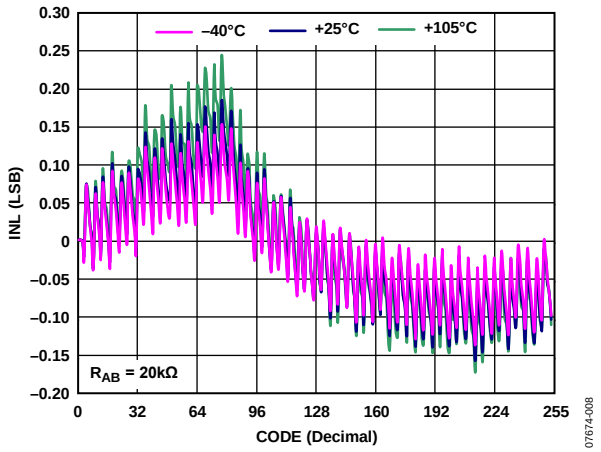

Figure 20. R-INL in R-Perf Mode vs. Code vs. Temperature (AD5291)

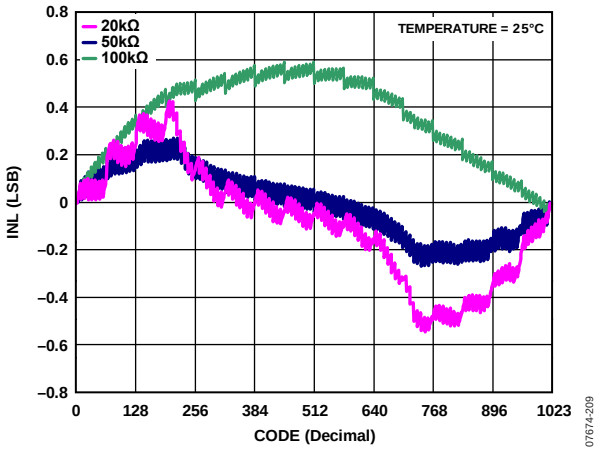

Figure 21. INL in Normal Mode vs. Code vs. Nominal Resistance (AD5292)

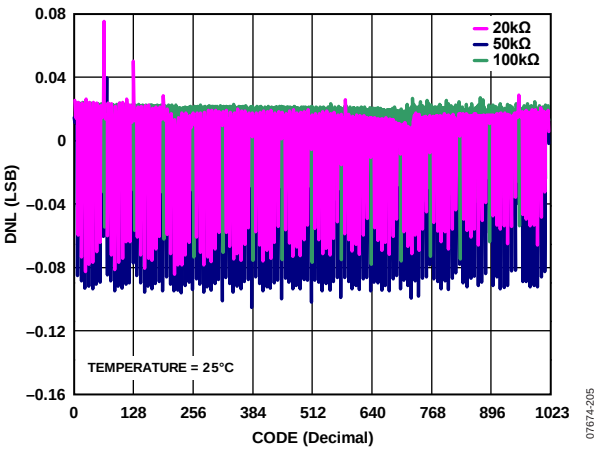

Figure 22. DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5292)

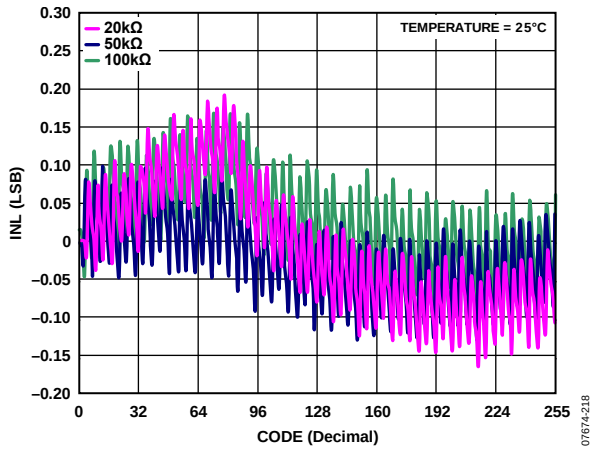

Figure 23. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5291)

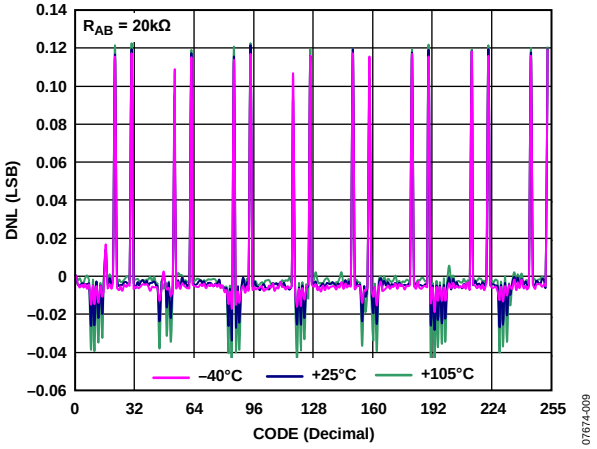

Figure 24. R-DNL in R-Perf Mode vs. Code vs. Temperature (AD5291)

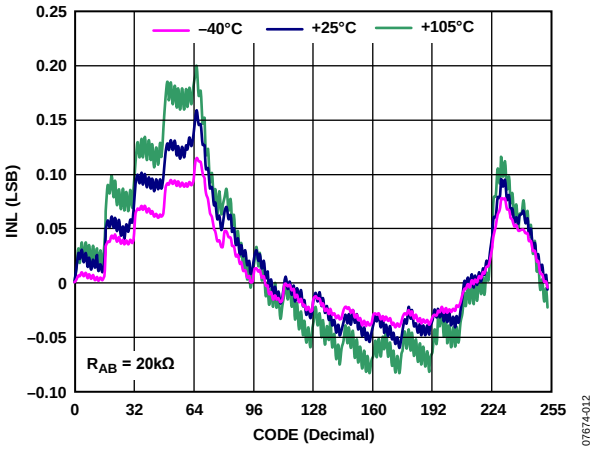

Figure 25. R-INL in Normal Mode vs. Code vs. Temperature (AD5291)

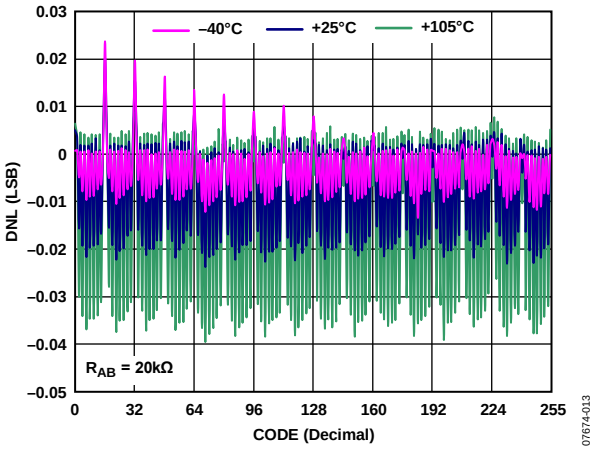

Figure 26. R-DNL in Normal Mode vs. Code vs. Temperature (AD5291)

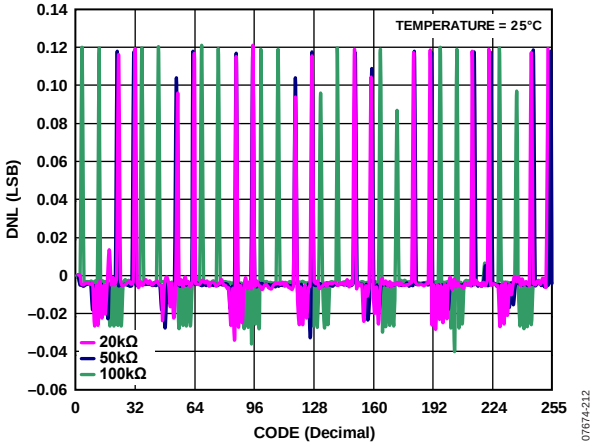

Figure 27. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5291)

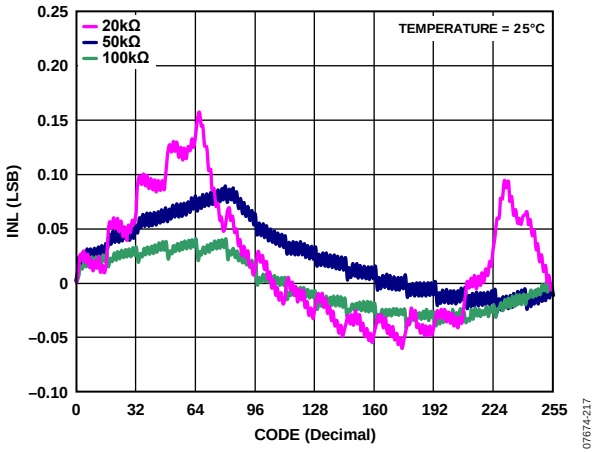

Figure 28. R-INL in Normal Mode vs. Code vs. Nominal Resistance (AD5291)

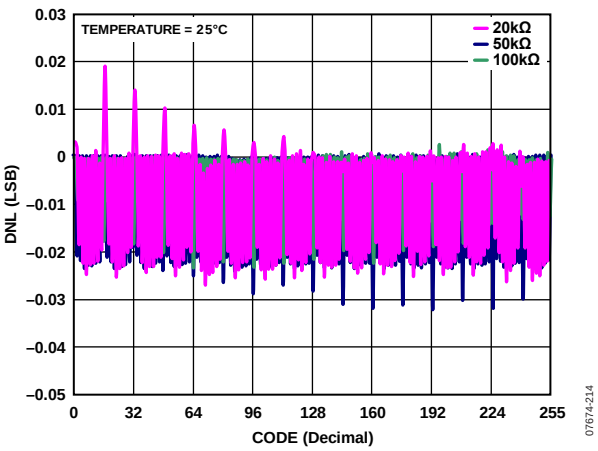

Figure 29. R-DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5291)

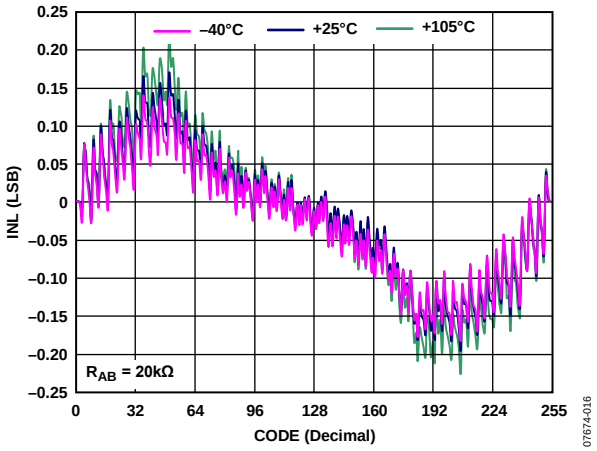

Figure 30. INL in R-Perf Mode vs. Code vs. Temperature (AD5291)

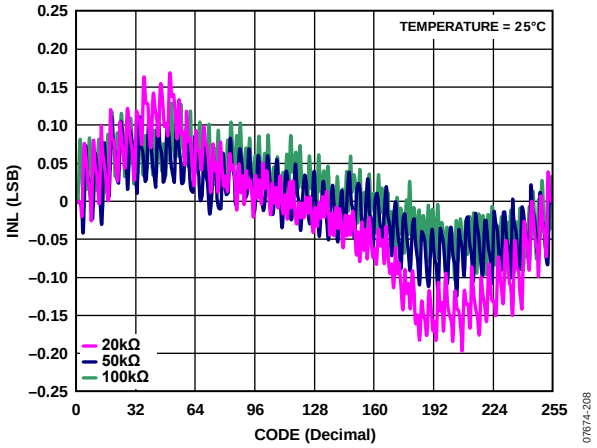

Figure 33. INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5291)

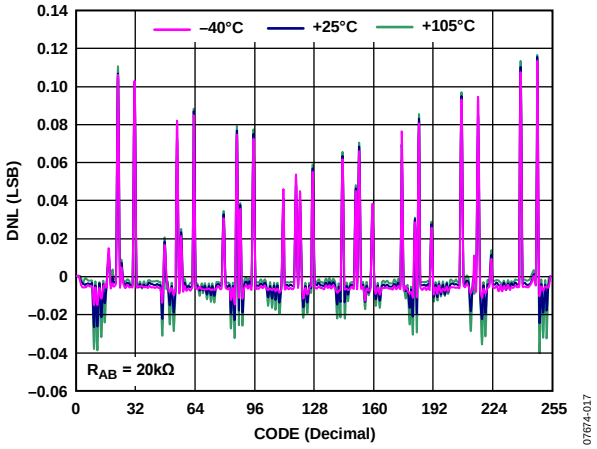

Figure 31. DNL in R-Perf Mode vs. Code vs. Temperature (AD5291)

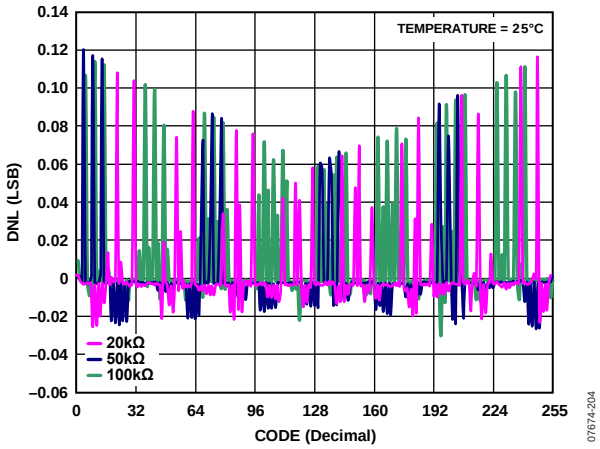

Figure 34. DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5291)

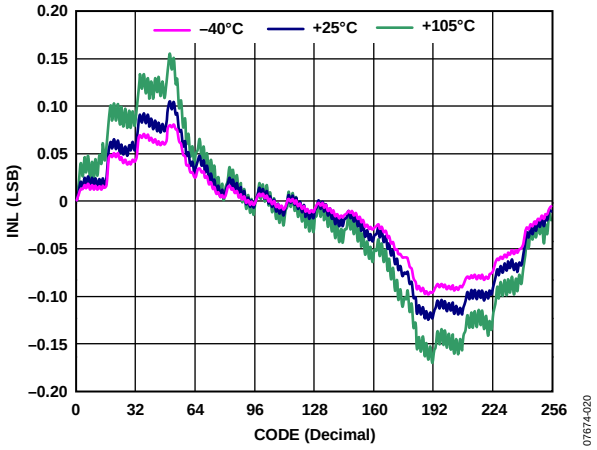

Figure 32. INL in Normal Mode vs. Code vs. Temperature (AD5291)

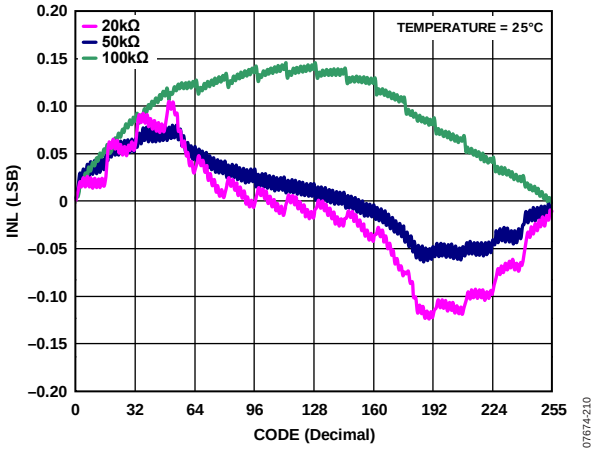

Figure 35. INL in Normal Mode vs. Code vs. Nominal Resistance (AD5291)

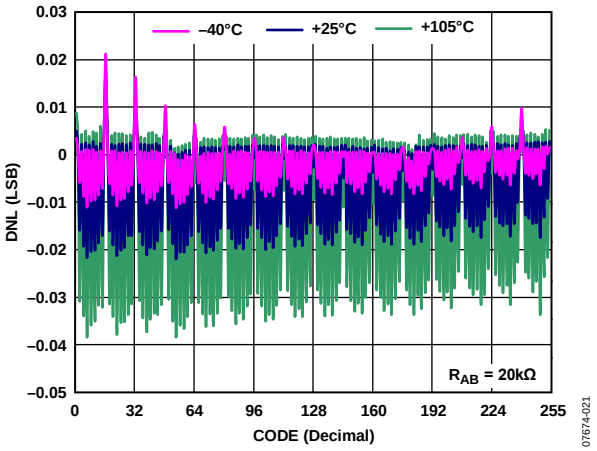

Figure 36. DNL in Normal Mode vs. Code vs. Temperature (AD5291)

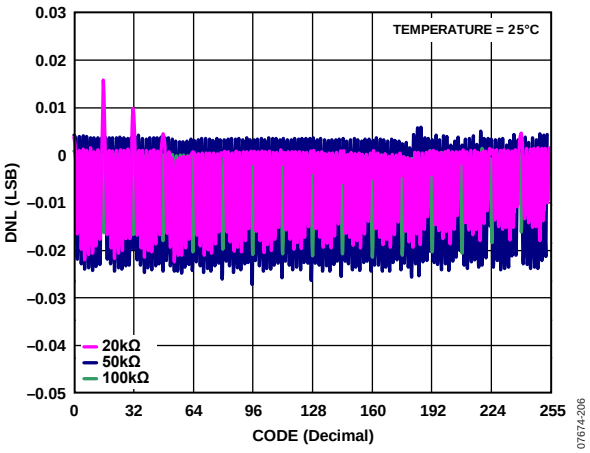

Figure 39. DNL in Normal Mode vs. Code vs. Temperature (AD5291)

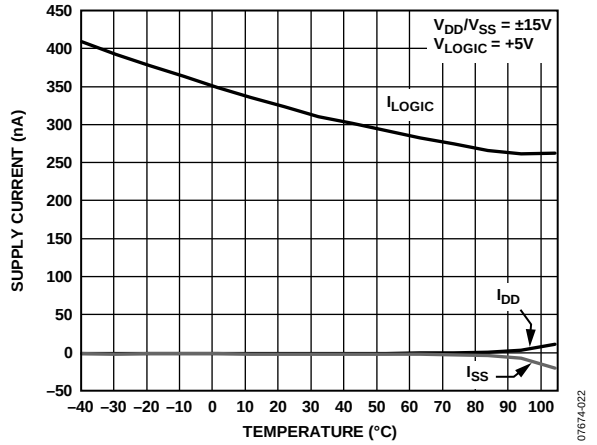

Figure 37. Supply Current (I_{DD}, I_{SS}, I_{LOGIC}) vs. Temperature

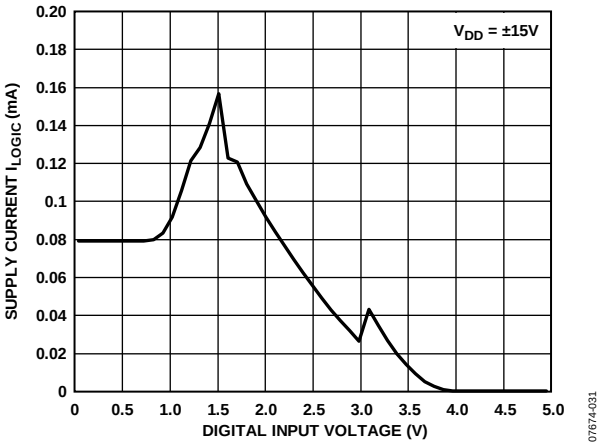

Figure 40. Supply Current I_{LOGIC} vs. Digital Input Voltage

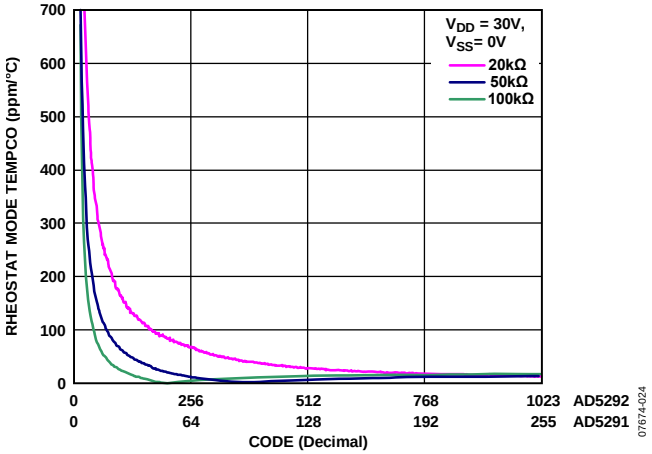

Figure 38. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

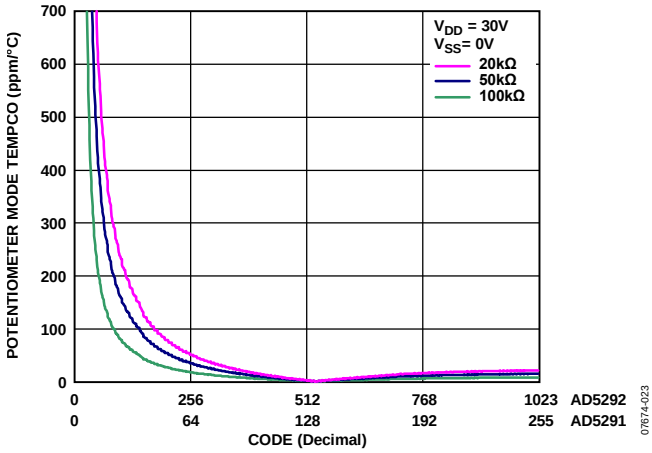

Figure 41. Potentiometer Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

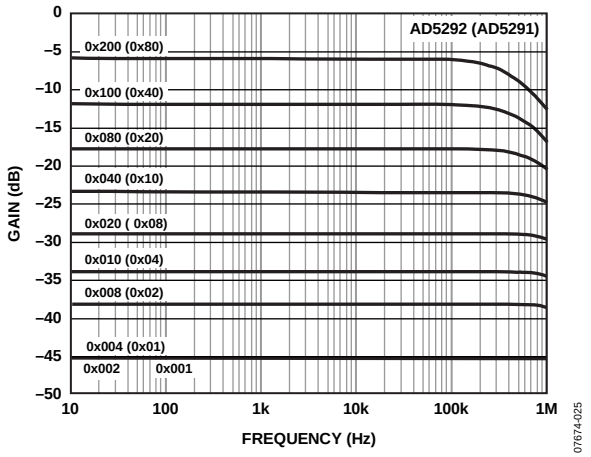

Figure 42. 20 kΩ Gain vs. Frequency vs. Code

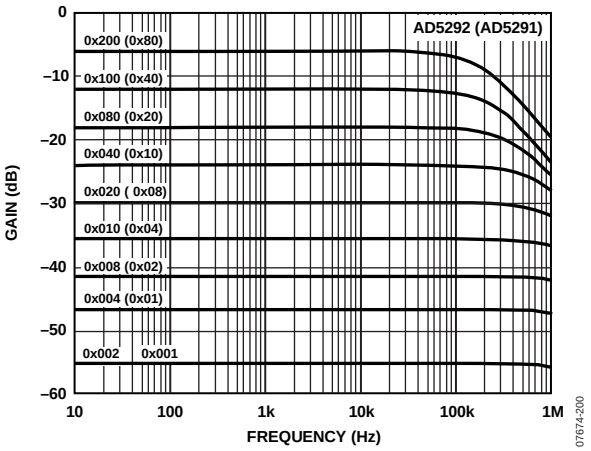

Figure 43. 50 kΩ Gain vs. Frequency vs. Code

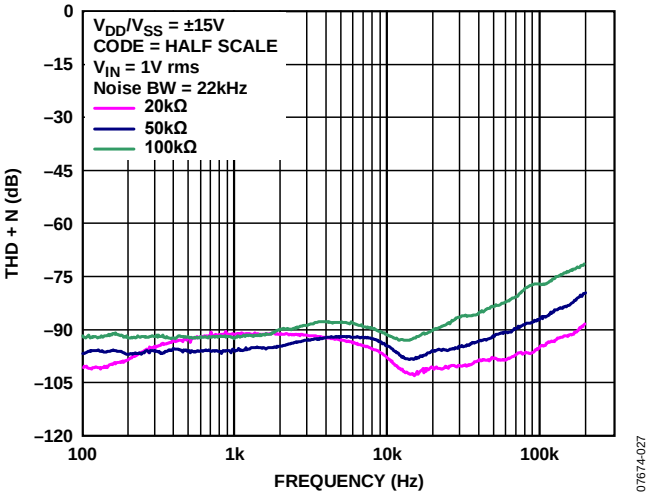

Figure 44. THD + Noise vs. Frequency

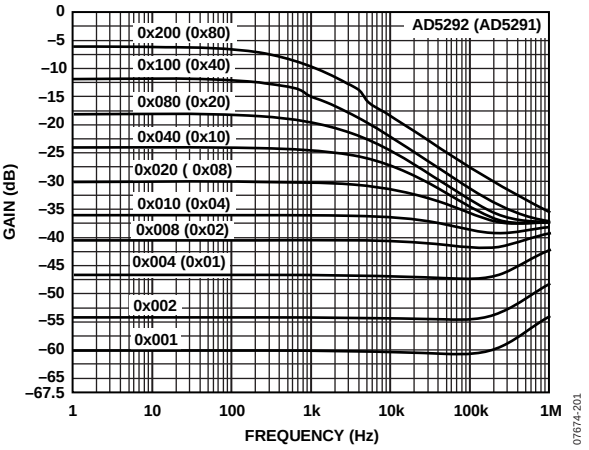

Figure 45. 100 kΩ Gain vs. Frequency vs. Code

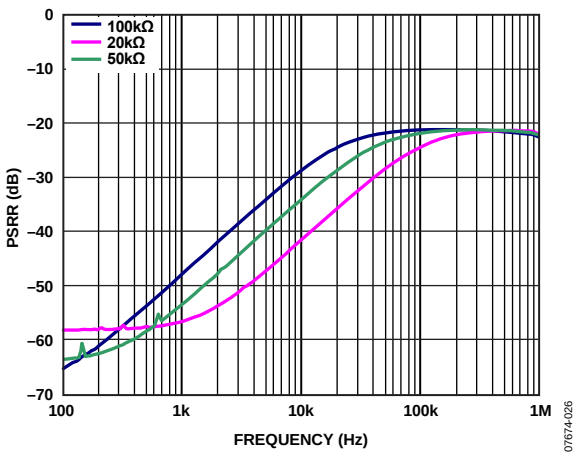

Figure 46. Power Supply Rejection Ratio vs. Frequency

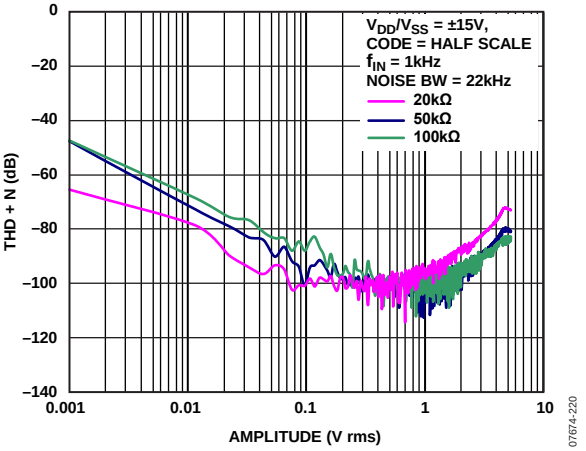

Figure 47. THD + Noise vs. Amplitude

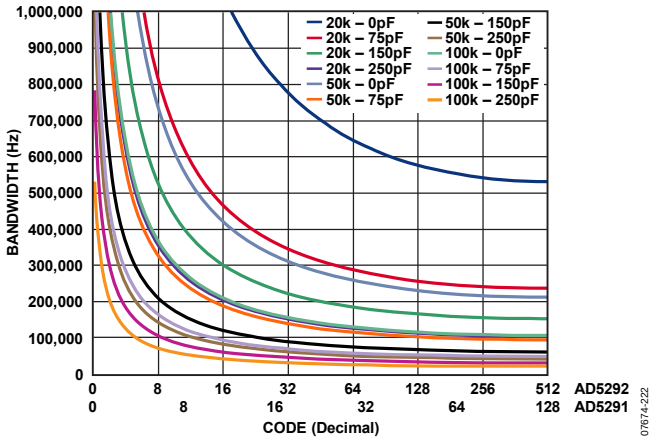

Figure 48. Bandwidth vs Code vs Net Capacitance

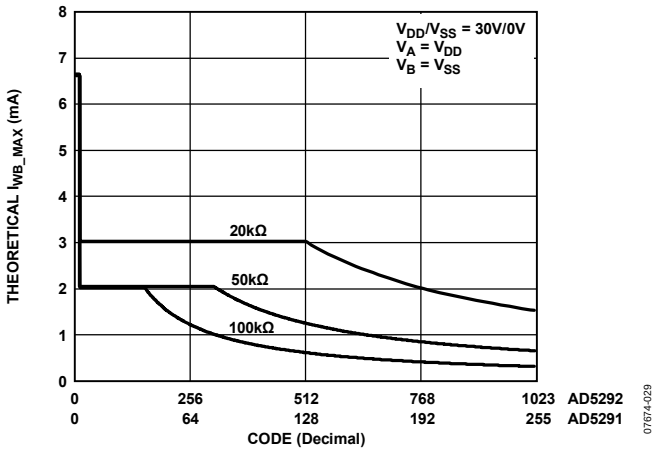

Figure 51. Theoretical Maximum Current vs. Code

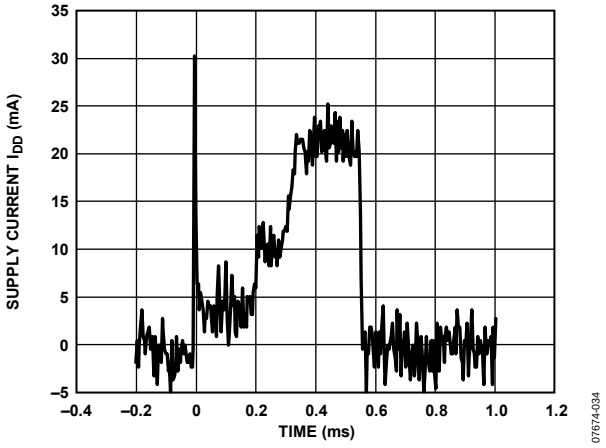

Figure 49. I_{DD} Waveform While Blowing/Reading Fuse

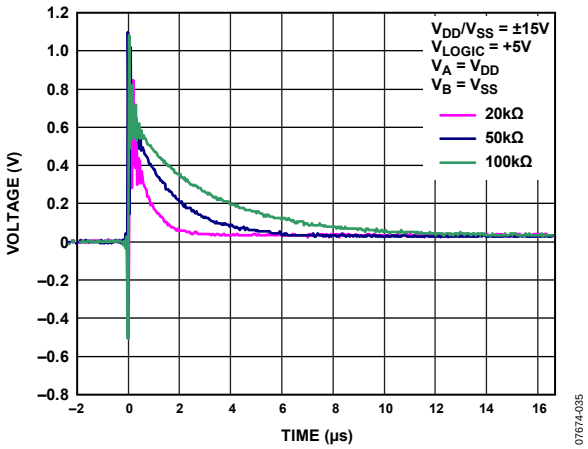

Figure 52. Maximum Transition Glitch

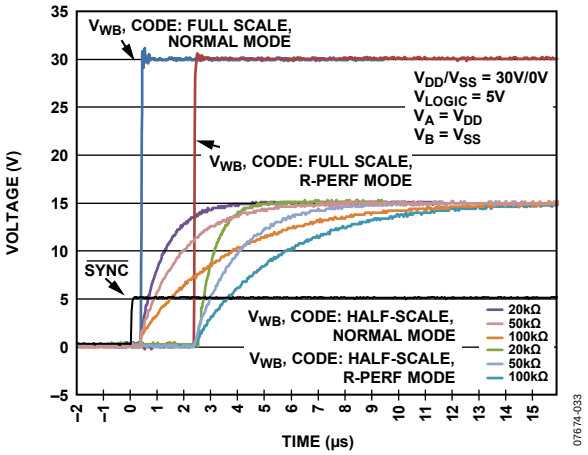

Figure 50. 20kΩ Large-Signal Settling Time from Code Zero Scale

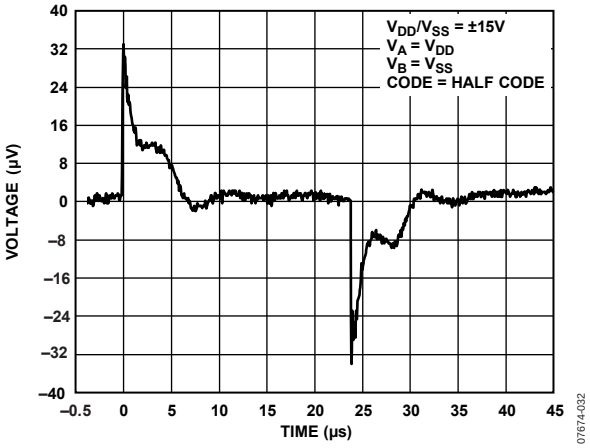

Figure 53. Digital Feedthrough

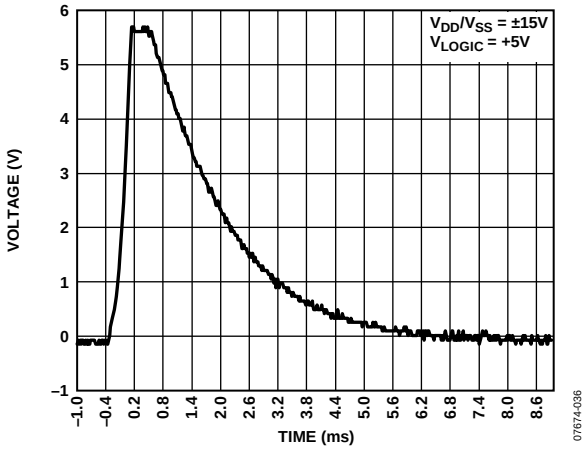

Figure 54. V_{EXT_CAP} Waveform While Reading Fuse Or Calibration

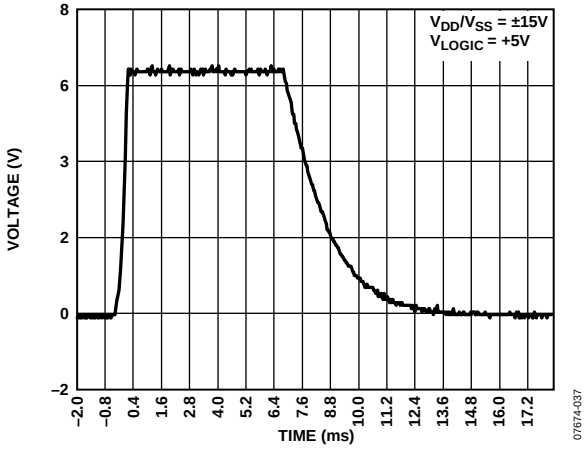

Figure 55. V_{EXT_CAP} Waveform While Writing Fuse

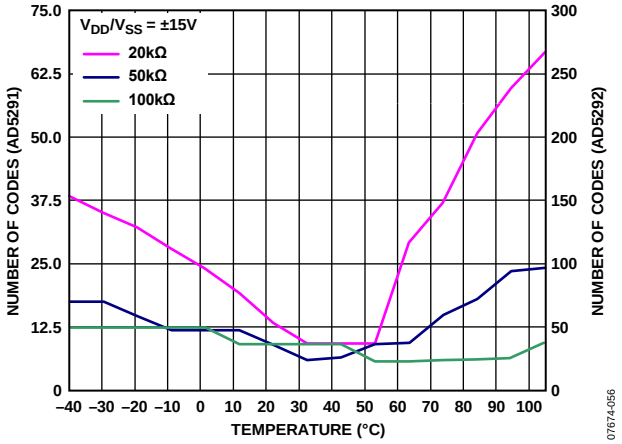

Figure 56. Code Range > 1% R-Tolerance Error vs. Temperature

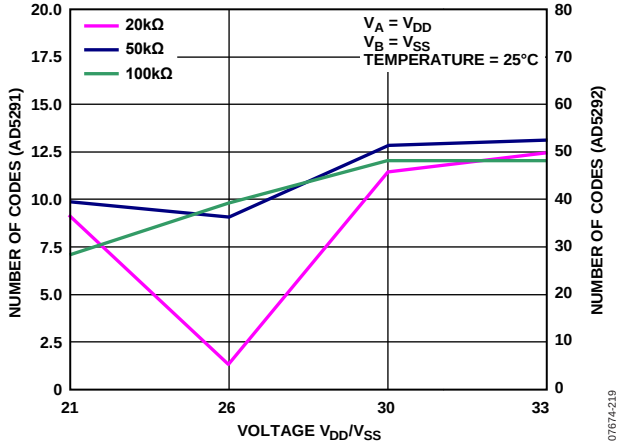

Figure 57. Code Range > 1% R-Tolerance Error vs. Voltage

TEST CIRCUITS

Figure 58 to Figure 63 define the test conditions used in the Specifications section.

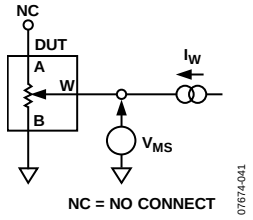

Figure 58. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

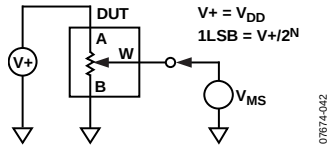

Figure 59. Potentiometer Divider Nonlinearity Error (INL, DNL)

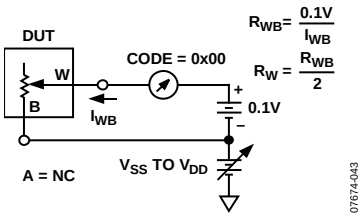

Figure 60. Wiper Resistance

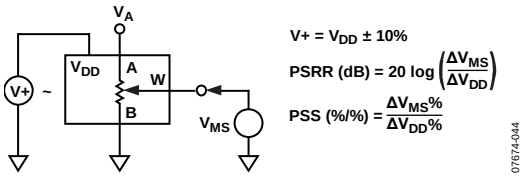

Figure 61. Power Supply Sensitivity (PSS, PSRR)

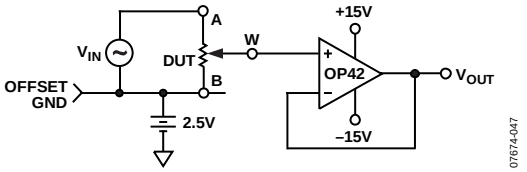

Figure 62. Gain vs. Frequency

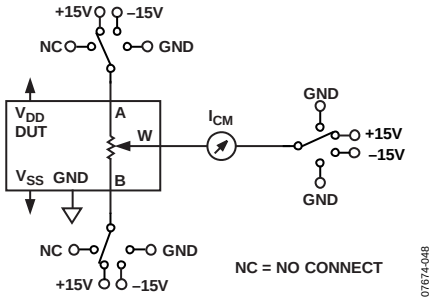

Figure 63. Common-Mode Leakage Current

THEORY OF OPERATION

The AD5291 and AD5292 digital potentiometers are designed to operate as true variable resistors for analog signals that remain within the terminal voltage range of VSS < VTERM < VDD. The patented ±1% resistor tolerance feature helps to minimize the total RDAC resistance error, which reduces the overall system error by offering better absolute matching and improved open-loop performance. The digital potentiometer wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register, allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The RDAC register can be programmed with any position setting using the standard SPI interface by loading the 16-bit data-word. Once a desirable position is found, this value can be stored in a 20-TP memory register. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of 20-TP data takes approximately 6 ms; during this time, the shift register is locked, preventing any changes from taking place. The RDY pin identifies the completion of this 20-TP storage.

SERIAL DATA INTERFACE

The AD5291 and AD5292 contain a serial interface ($\overline{\text{SYNC}}$, SCLK, DIN and SDO) that is compatible with SPI interface standards, as well as most DSPs. The part allows writing of data via the serial interface to every register.

SHIFT REGISTER

The AD5291 and AD5292 shift register is 16 bits wide (see Figure 2). The 16-bit input word consists of two zeros, followed by four control bits, and 10 RDAC data bits. For the AD5291, the lower two RDAC data bits are don't cares if the RDAC register is read from or written to. Data is loaded MSB first (Bit DB15). The four control bits determine the function of the software command (see Table 11). Figure 3 shows a timing diagram of a typical AD5291 and AD5292 write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. The $\overline{\text{SYNC}}$ pin must be held low until the complete data-word is loaded from the DIN pin. When $\overline{\text{SYNC}}$ returns high, the serial data-word is decoded according to the commands in Table 11. The command bits (Cx) control the operation of the digital potentiometer. The data bits (Dx) are the values that are loaded into the decoded register. The AD5291 and AD5292 have an internal counter that counts a multiple of 16 bits (a frame) for proper operation. For example, AD5291 and AD5292 work with a 32-bit word but does not work properly with a 31-bit or 33-bit word. The AD5291 and AD5292 do not require a continuous SCLK, when $\overline{\text{SYNC}}$ is high, and all serial interface pins should be operated at close to the VLOGIC supply rails to minimize power consumption in the digital input buffers.

RDAC REGISTER

The RDAC register directly controls the position of the digital potentiometer wiper. For example, when the RDAC register is loaded with all zeros, the wiper is connected to Terminal B of the variable resistor. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

Table 11. Command Operation Truth Table

			Command Bits[DB13:DB10]				Data Bits[DB9:DB0][1]										
Command	DB15	DB14	C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP command: do nothing.
1	0	0	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1[2]	D0[2]	Write contents of serial data to RDAC.
2	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Read RDAC wiper setting from the SDO output in the next frame.
3	0	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	Store wiper setting: store RDAC setting to 20-TP memory.
4	0	0	0	1	0	0	X	X	X	X	X	X	X	X	X	X	Reset: refresh RDAC with 20-TP stored value.
5	0	0	0	1	0	1	X	X	X	X	X	D4	D3	D2	D1	D0	Read contents of 20-TP memory, or status of 20-TP memory, from the SDO output in the next frame.
6	0	0	0	1	1	0	X	X	X	X	X	X	D3	D2	D1	D0	Write contents of serial data to control register.
7	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	Read control register from the SDO output in the next frame.
8	0	0	1	0	0	0	X	X	X	X	X	X	X	X	X	D0	Software shutdown. D0 = 0 (normal mode). D0 = 1 (device placed in shutdown mode).

[1] X = don't care.
[2] In the AD5291, this bit is a don't care.

20-TP MEMORY

Once a desirable wiper position is found, the contents of the RDAC register can be saved into a 20-TP memory register (see Table 12). Thereafter, the wiper position is always set at that position for any future on-off-on power supply sequence. The AD5291 and AD5292 have an array of 20 one-time programmable (OTP) memory registers. When the desired word is programmed to 20-TP memory, the device automatically verifies that the program command was successful. The verification process includes margin testing. Bit C3 of the control register can be polled to verify that the fuse program command was successful. Programming data to 20-TP memory consumes approximately 25 mA for 550 µs and takes approximately 8 ms to complete. During this time, the shift register is locked, preventing any changes from taking place. The RDY pin can be used to monitor the completion of the 20-TP memory program and verification. No change in supply voltage is required to program the 20-TP memory. However, a 1 µF capacitor on the EXT_CAP pin is required (see Figure 68). Prior to 20-TP activation, the AD5291 and AD5292 preset to midscale on power-up.

WRITE PROTECTION

On power-up, the shift register write commands for both the RDAC register and the 20-TP memory register are disabled. The RDAC write protect bit, C1 of the control register (see Table 13 and Table 14), is set to 0 by default. This disables any change of the RDAC register content regardless of the software commands, except that the RDAC register can be refreshed from the 20-TP memory using the software reset command (Command 4) or through hardware by the $\overline{\text{RESET}}$ pin. To enable programming of the variable resistor wiper position (programming the RDAC register), the write protect bit, C1 of the control register, must first be programmed. This is accomplished by loading the shift register with Command 6 (see Table 11). To enable programming of the 20-TP memory block bit, C0 of the control register (set to 0 by default) must first be set to 1.

Table 12. Write and Read to RDAC and 20-TP Memory

DIN	SDO	Action
0x1803	0xXXXX	Enable update of wiper position and 20-TP memory contents through digital interface.
0x0500	0x1803	Write 0x100 to the RDAC register; wiper moves to ¼ full-scale position.
0x0800	0x0500	Prepare data read from the RDAC register.
0x0C00	0x0100	Stores RDAC register content into 20-TP memory. The 16-bit word appears out of SDO, where the last 10 bits contain the contents of the RDAC register (0x100).
0x1C00	0x0C00	Prepare data read from the control register.
0x0000	0x000X	NOP Instruction 0 sends 16-bit word out of SDO, where the last four bits contain the contents of the control register. If Bit C3 = 1, the fuse program command is successful.

Table 13. Control Register Bit Map[1]

DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	X	X	X	X	C3	C2	C1	C0

[1] X = don't care.

Table 14. Control Register Function

Bit Name	Description
C0	20-TP program enable 0 = 20-TP program disabled (default) 1 = enable device for 20-TP program
C1	RDAC register write protect 0 = wiper position frozen to value in memory (default)[1] 1 = allow update of wiper position through digital Interface
C2	Calibration enable 0 = resistor performance mode enabled (default) 1 = normal mode enabled
C3	20-TP memory program success 0 = fuse program command unsuccessful (default) 1 = fuse program command successful

[1] Wiper position frozen to value last programmed in 20-TP memory. Wiper is frozen to midscale if 20-TP memory has not been previously programmed.

BASIC OPERATION

The basic mode of setting the variable resistor wiper position (programming the RDAC register) is accomplished by loading the shift register with Command 1 (see Table 11) and the desired wiper position data. When the desired wiper position is determined, the user can load the shift register with Command 3 (see Table 11), which stores the wiper position data in the 20-TP memory register. After 6 ms, the wiper position is permanently stored in the 20-TP memory. The RDY pin can be used to monitor the completion of this 20-TP program. Table 12 provides a programming example, listing the sequence of serial data input (DIN) words with the serial data output appearing at the SDO pin in hexadecimal format.

20-TP READBACK AND SPARE MEMORY STATUS

It is possible to read back the contents of any of the 20-TP memory registers through SDO by using Command 5 (see Table 11). The lower five LSB bits (D0 to D4) of the data byte select which memory location is to be read back (see Table 16). Data from the selected memory location are clocked out of the SDO pin during the next SPI operation, where the last 10 bits contain the contents of the specified memory location.

It is also possible to calculate the address of the most recently programmed memory location by reading back the contents of read-only Memory Address 0x14 and Memory Address 0x15 using Command 5. The data bytes read back from Memory Address 0x014 and Memory Address 0x015 are thermometer encoded versions of the address of the last programmed memory location.

For the example outlined in Table 15, the address of the last programmed location is calculated as

(*Number of Bits* = 1 *in Memory Address 0x14*) + (*Number of Bits* = 1 *in Memory Address 0x15*) − 1 = 10 + 8 − 1 = 17 (0x10)

If no memory location has been programmed, then the address generated is −1.

SHUTDOWN MODE

The AD5291 and AD5292 can be placed in shutdown mode by executing the software shutdown command, Command 8 (see Table 11), and setting the LSB, D0, to 1. This feature places the RDAC in a special state in which Terminal A is open-circuited, and Wiper W is connected to Terminal B. The contents of the RDAC register are unchanged by entering shutdown mode. However, all commands listed in Table 11 are supported while in shutdown mode. Execute Command 8 (see Table 11), and set the LSB, D0, to 0 to exit shutdown mode.

Table 15. Example 20-TP Memory Readback

DIN	SDO	Action
0x1414	0xXXXX	Prepares data read from Memory Address 0x14.
0x1415	0x03FF	Prepares data read from Memory Address 0x15. Sends 16-bit word out of SDO, where the last 10 bits contain the contents of Memory Address 0x14.
0x0000	0x00FF	NOP Command 0 sends 16-bit word out of SDO, where last 10-bits contain the contents of Memory Address 0x15.
0x1410	0x0000	Prepares data read from memory location 0x10.
0x0000	0xXXXX	NOP Instruction 0 sends 16-bit word out of SDO, where the last 10 bits contain the contents of Memory Address 0x10 (17).

Table 16. Memory Map of Command 5

Data Bits[DB9:DB0][1]										
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register Contents
X	X	X	X	X	0	0	0	0	0	1st programmed wiper location (0x00)
X	X	X	X	X	0	0	0	0	1	2nd programmed wiper location (0x01)
X	X	X	X	X	0	0	0	1	0	3rd programmed wiper location (0x02)
X	X	X	X	X	0	0	0	1	1	4th programmed wiper location (0x03)
X	X	X	X	X	0	0	1	0	0	5th programmed wiper location (0x04)
…	…	…	…	…	…	…	…	…	…	…
X	X	X	X	X	0	1	0	0	1	10th programmed wiper location (0x09)
X	X	X	X	X	0	1	1	1	0	15th programmed wiper location (0x0E)
X	X	X	X	X	1	0	0	1	1	20th programmed wiper location (0x13)
X	X	X	X	X	1	0	1	0	0	Programmed memory status (thermometer encoded)[2] (0x14)
X	X	X	X	X	1	0	1	0	1	Programmed memory status (thermometer encoded)[2] (0x15)

[1] X = don't care.
[2] Allows the user to calculate the remaining spare memory locations.

RESISTOR PERFORMANCE MODE

This mode activates a new, patented 1% end-to-end resistor tolerance that ensures a ±1% resistor tolerance on each code, that is, code = half scale, R_{WB} = 10 kΩ ± 100 Ω. See Table 2 (AD5291) or Table 5 (AD5292) to check which codes achieve ±1% resistor tolerance. The resistor performance mode is activated by programming Bit C2 of the control register (see Table 13 and Table 14). The typical settling time is shown in Figure 50.

RESET

A low-to-high transition of the hardware $\overline{\text{RESET}}$ pin loads the RDAC register with the contents of the most recently programmed 20-TP memory location. The AD5291 and AD5292 can also be reset through software by executing Command 4 (see Table 11). If no 20-TP memory location is programmed, then the RDAC register loads with midscale upon reset. The control register is restored with default bits; see Table 14.

SDO PIN AND DAISY-CHAIN OPERATION

The serial data output pin (SDO) serves two purposes: it can be used to read the contents of the wiper setting, 50-TP values and control register using Command 2, Command 5 and Command 7, respectively (see Table 11) or the SDO pin can be used in daisy-chain mode. Data is clocked out of SDO on the rising edge of SCLK. The SDO pin contains an open-drain N-channel FET that requires a pull-up resistor if this pin is used. To place the pin in high impedance and minimize the power dissipation when the pin is used, the 0x8001 data word followed by Command 0 should be sent to the part. Table 17 provides a sample listing for the sequence of the serial data input (DIN). Daisy chaining minimizes the number of port pins required from the controlling IC. As shown in Figure 64, users need to tie the SDO pin of one package to the DIN pin of the next package. Users may need to increase the clock period, because the pull-up resistor and the capacitive loading at the SDO-to-DIN interface may require additional time delay between subsequent devices.

When two AD5291 and AD5292 devices are daisy-chained, 32 bits of data are required. The first 16 bits go to U2, and the second 16 bits go to U1. Hold the $\overline{\text{SYNC}}$ pin low until all 32 bits are clocked into their respective shift registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

Keep the $\overline{\text{SYNC}}$ pin low until all 32 bits are clocked into their respective serial registers. The $\overline{\text{SYNC}}$ pin is then pulled high to complete the operation.

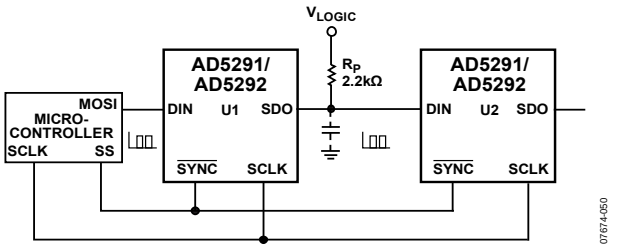

Figure 64. Daisy-Chain Configuration Using SDO

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5291 and AD5292 employ a three-stage segmentation approach, as shown in Figure 65. The AD5291 and AD5292 wiper switches are designed with the transmission gate CMOS topology and with the gate voltages derived from V_{DD} and V_{SS}.

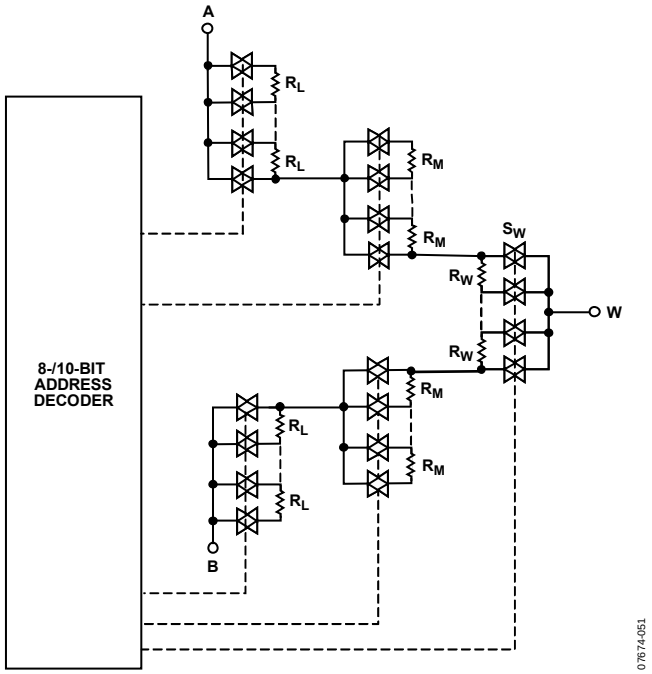

Figure 65. Simplified RDAC Circuit

Table 17. Minimize Power Dissipation at SDO Pin

DIN	SDO[1]	Action
0xXXXX	0xXXXX	Last user command sent to the digipot
0x8001	0xXXXX	Prepares the SDO pin to be placed in high impedance mode
0x0000	High impedance	The SDO pin is placed in high impedance

[1] X is don't care.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—1% Resistor Tolerance

The AD5291 and AD5292 operate in rheostat mode when only two terminals are used as a variable resistor. The unused terminal can be left floating or tied to the W terminal, as shown in Figure 66.

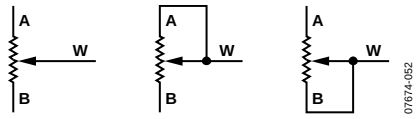

Figure 66. Rheostat Mode Configuration

The nominal resistance between Terminal A and Terminal B, R_{AB}, is available in 20 kΩ, 50 kΩ, and 100 kΩ, and 256 or 1024 tap points accessed by the wiper terminal. The 8-/10-bit data in the RDAC latch is decoded to select one of the 256/1024 possible wiper settings. The AD5291 and AD5292 contain an internal ±1% resistor performance mode that can be disabled or enabled (this is enabled by default), by programming Bit C2 of the control register (see Table 13 and Table 14). The digitally programmed output resistance between the W terminal and the A terminal, R_{WA}, and between the W terminal and B terminal, R_{WB}, is internally calibrated to give a maximum of ±1% absolute resistance error across a wide code range. As a result, the general equations for determining the digitally programmed output resistance between the W terminal and B terminal are

AD5291:

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} \quad (1)$$

AD5292:

$$R_{WB}(D) = \frac{D}{1024} \times R_{AB} \quad (2)$$

where:

D is the decimal equivalent of the binary code loaded in the 8-/10-bit RDAC register.
R_{AB} is the end-to-end resistance.

Similar to the mechanical potentiometer, the resistance of the RDAC between the W terminal and the A terminal also produces a digitally controlled complementary resistance, R_{WA}. R_{WA} is also calibrated to give a maximum of 1% absolute resistance error. R_{WA} starts at the maximum resistance value and decreases as the data loaded into the latch increases. The general equations for this operation are

AD5291:

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} \quad (3)$$

AD5292:

$$R_{WA}(D) = \frac{1024 - D}{1024} \times R_{AB} \quad (4)$$

where:

D is the decimal equivalent of the binary code loaded in the 8-/10-bit RDAC register.
R_{AB} is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of 120 Ω is present. Regardless of which setting the part is operating in, take care to limit the current between Terminal A and Terminal B, between Terminal W and Terminal A, and between Terminal W and Terminal B, to the maximum continuous current of ±3 mA or to the pulse current specified in Table 8. Otherwise, degradation or possible destruction of the internal resistors may occur.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at the wiper to B and at the wiper to A that is proportional to the input voltage at A to B, as shown in Figure 67. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A to B, W to A, and W to B can be at either polarity.

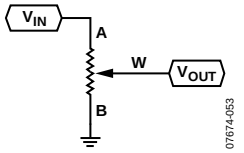

Figure 67. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for simplicity, connecting the A terminal to 30 V and the B terminal to ground produces an output voltage at the Wiper W to Terminal B ranging from 0 V to 1 LSB less than 30 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B, divided by the 256/1024 positions of the potentiometer divider. The general equations defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B are

AD5291:

$$V_W(D) = \frac{D}{256} \times V_A + \frac{256 - D}{256} \times V_B \quad (5)$$

AD5292:

$$V_W(D) = \frac{D}{1024} \times V_A + \frac{1024 - D}{1024} \times V_B \quad (6)$$

If using the AD5291 and AD5292 in voltage divider mode as shown in Figure 67, then the ±1% resistor tolerance calibration feature reduces the error when matching with discrete resistors. However, it is recommended to disable the internal ±1% resistor tolerance calibration feature by programming Bit C2 of the control register (see Table 13 and Table 14) to optimize wiper position update rate. In this configuration, the RDAC is ratiometric and resistor tolerance error does not affect performance.

Operation of the digital potentiometer in the voltage divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors, R_{WA} and R_{WB}, and not the absolute values. Therefore, the temperature drift reduces to 5 ppm/°C.

EXT_CAP CAPACITOR

A 1 µF capacitor to GND must be connected to the EXT_CAP pin (see Figure 68) on power-up and throughout the operation of the AD5291 and AD5292.

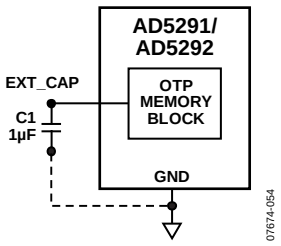

Figure 68. Hardware Setup for EXT_CAP Pin

TERMINAL VOLTAGE OPERATING RANGE

The positive V_{DD} and negative V_{SS} power supplies of the AD5291 and AD5292 define the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 69).

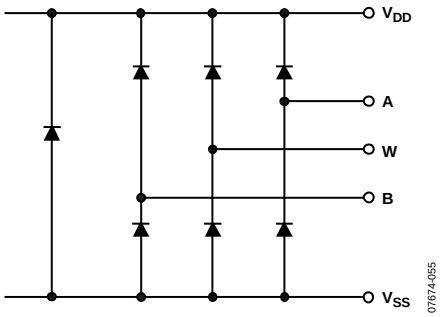

Figure 69. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pins of the AD5291 and AD5292 devices are primarily used as a digital ground reference. To minimize the digital ground bounce, the AD5291 and AD5292 ground terminals should be joined remotely to the common ground. The digital input control signals to the AD5291 and AD5292 must be referenced to the device ground pin (GND), and satisfy the logic level defined in the Specifications section.

Power-Up Sequence

To ensure that the AD5291 and AD5292 power up correctly, a 1 µF capacitor must be connected to the EXT_CAP pin. Because there are diodes to limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 69), it is important to power V_{DD} and V_{SS} first before applying any voltage to Terminal A, Terminal B, and Terminal W. Otherwise, the diode is forward-biased such that V_{DD} and V_{SS} are powered up unintentionally. The ideal power-up sequence is GND, V_{SS}, V_{LOGIC} and V_{DD}, the digital inputs, and then V_A, V_B, and V_W. The order of powering up V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}, V_{SS}, and V_{LOGIC}.

Regardless of the power-up sequence and the ramp rates of the power supplies, after V_{LOGIC} is powered, the power-on preset activates, restoring the 20-TP memory value to the RDAC register.

APPLICATIONS INFORMATION

HIGH VOLTAGE DAC

The AD5292 can be configured as a high voltage DAC, with output voltage as high as 33 V. The circuit is shown in Figure 70. The output is

$$V_{OUT}(D) = \frac{D}{1024} \times \left[1.2\ \text{V} \times \left(1 + \frac{R_2}{R_1} \right) \right] \quad (7)$$

where D is the decimal code from 0 to 1023.

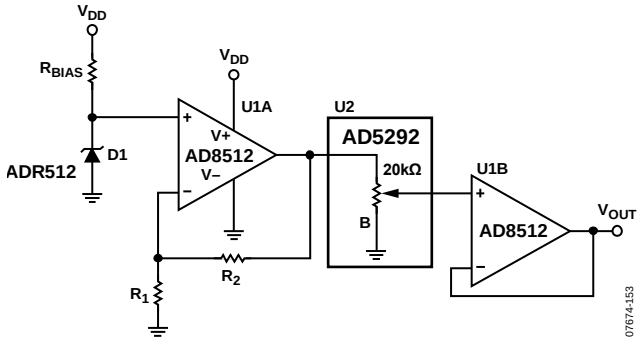

Figure 70. High Voltage DAC

PROGRAMMABLE VOLTAGE SOURCE WITH BOOSTED OUTPUT

For applications that require high current adjustments such as a laser diode or tunable laser, a boosted voltage source can be considered; see Figure 71.

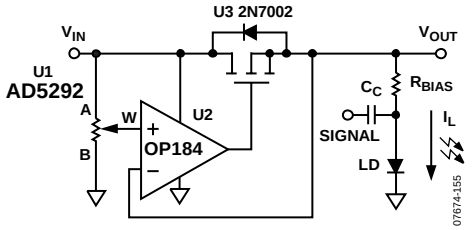

Figure 71. Programmable Boosted Voltage Source

In this circuit, the inverting input of the op amp forces V_{OUT} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET (U3). The N-Channel FET power handling must be adequate to dissipate $(V_{IN} - V_{OUT}) \times I_L$ power. This circuit can source a maximum of 100 mA with a 33 V supply.

HIGH ACCURACY DAC

It is possible to configure the AD5292 as a high accuracy DAC by optimizing the resolution of the device over a specific reduced voltage range. This is achieved by placing external resistors on either side of the RDAC, as shown in Figure 72. The improved ±1% R-Tolerance specification greatly reduces error associated with matching to discrete resistors.

$$V_{OUT}(D) = \frac{R_3 + (D/1024 \times R_{AB}) \times V_{DD}}{R_1 + ((1024-D)/1024) \times R_{AB} + R_3} \quad (8)$$

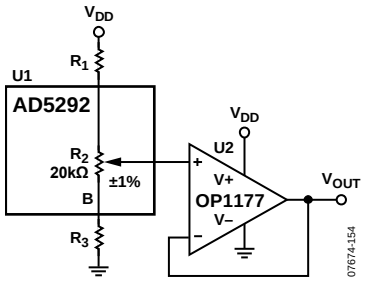

Figure 72. Optimizing Resolution

VARIABLE GAIN INSTRUMENTATION AMPLIFIER

The AD8221 in conjunction with the AD5291 and AD5292 and the ADG1207, as shown in Figure 73, make an excellent instrumentation amplifier for use in data acquisition systems. The data acquisition system's low distortion and low noise enable it to condition signals in front of a variety of ADCs.

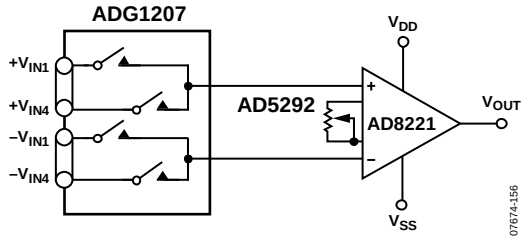

Figure 73. Data Acquisition System

The gain can be calculated by using Equation 9.

$$G(D) = 1 + \frac{49.4\ \text{k}\Omega}{(D/1024) \times R_{AB}} \quad (9)$$

AUDIO VOLUME CONTROL

The excellent THD performance and high voltage capability make the AD5291 and AD5292 ideal for a digital volume control as an audio attenuator or gain amplifier. A typical problem in these systems is that a large step change in the volume level at any arbitrary time can lead to an abrupt discontinuity of the audio signal causing an audible zipper noise. To prevent this, a zero-crossing window detector can be inserted to the $\overline{\text{SYNC}}$ line to delay the device update until the audio signal crosses the window. Because the input signal can operate on top of any dc level rather than absolute zero volt level, zero-crossing in this case means the signal is ac-coupled, and the dc offset level is the signal zero reference point.

The configuration to reduce zipper noise is shown in Figure 74, and the results of using this configuration is shown in Figure 75. The input is ac-coupled by C1 and attenuated down before feeding into the window comparator formed by U2, U3, and U4B. U6 is used to establish the signal zero reference. The upper limit of the comparator is set above its offset and, therefore, the output pulses high whenever the input falls between 2.502 V and 2.497 V (or 0.005 V window) in this example. This output is AND'ed with the $\overline{\text{SYNC}}$ signal such that the AD5291 and AD5292 updates whenever the signal crosses the window. To avoid a constant update of the device, the $\overline{\text{SYNC}}$ signal should be programmed as two pulses, rather than as one.

In Figure 75, the lower trace shows that the volume level changes from a quarter-scale to full-scale when a signal change occurs near the zero-crossing window.

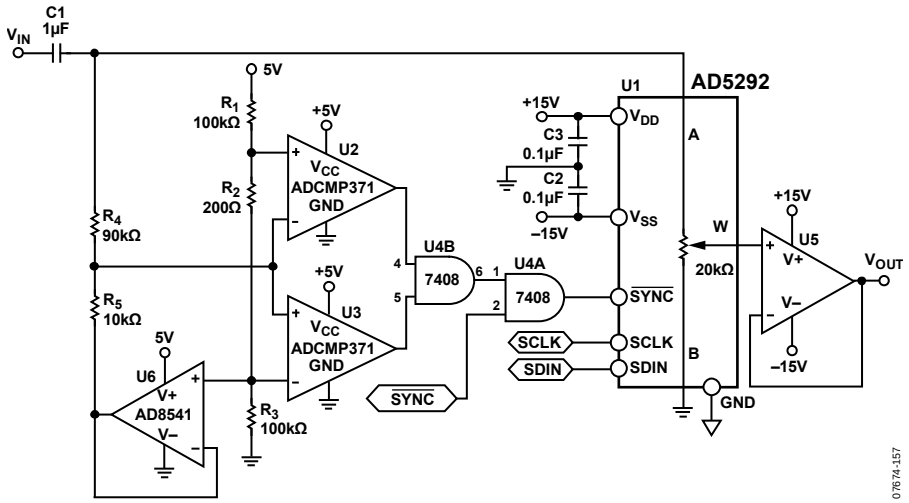

Figure 74. Audio Volume Control with Zipper Noise Reduction

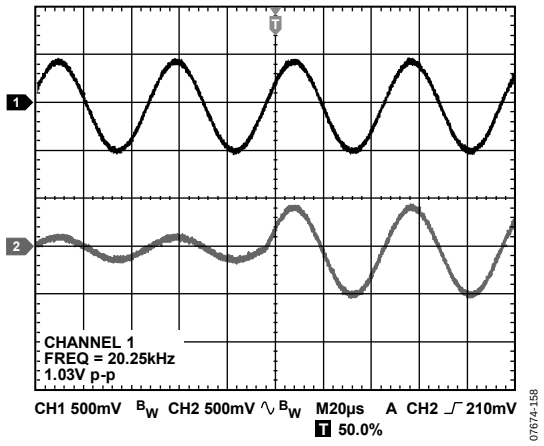

Figure 75. Zipper Noise Detector

OUTLINE DIMENSIONS

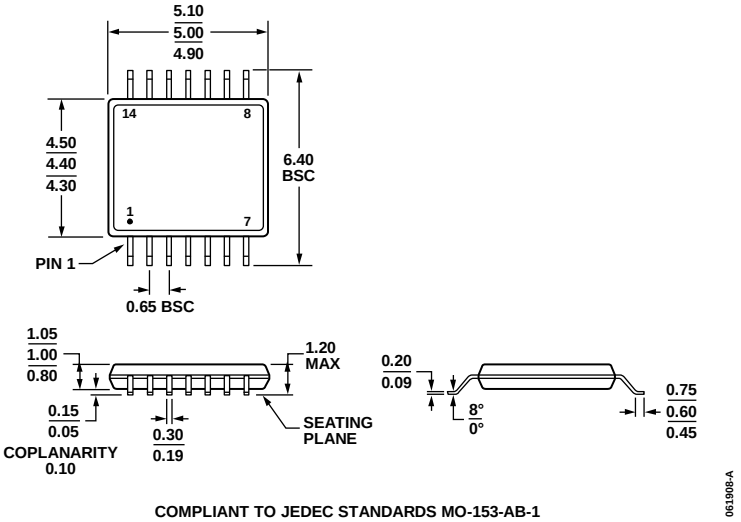

Figure 76. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Resolution	Memory	Temperature Range	Package Description	Package Option
AD5291BRUZ-20	20	256	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5291BRUZ-20-RL7	20	256	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5291BRUZ-50	50	256	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5291BRUZ-50-RL7	50	256	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5291BRUZ-100	100	256	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5291BRUZ-100-RL7	100	256	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5292BRUZ-20	20	1,024	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5292BRUZ-20-RL7	20	1,024	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5292BRUZ-50	50	1,024	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5292BRUZ-50-RL7	50	1,024	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5292BRUZ-100	100	1,024	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
AD5292BRUZ-100-RL7	100	1,024	20-TP	−40°C to +105°C	14-Lead TSSOP	RU-14
EVAL-AD5292EBZ					Evaluation Board	

[1] Z = RoHS Compliant Part.

D07674-0-12/14(E)