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9/03—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 kΩ VERSION

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$, −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}		−30		+30	%
Resistance Temperature Coefficient[3]	$\Delta R_{AB}/\Delta T$			45		ppm/°C
Output Resistance	R_{WB}	Code = 0x00		75	300	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x40		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0x7F	−3	−2	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_W		GND		V_{DD}	V
Capacitance A[6]	C_A	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x40		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
Output Logic Low (SDA)	V_{OL}	I_{OL} = 3 mA			0.4	V
		I_{OL} = 6 mA			0.6	V
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{DD} = 5.5 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		3	7	µA
		V_{DD} = 5 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		2.5	5.2	µA
		V_{DD} = 3.3 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		0.9	2	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			40	µW
Power Supply Sensitivity	PSSR	V_{DD} = 5 V ± 10%, code = midscale		±0.003	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 8]						
Bandwidth −3 dB	BW_5 K	R_{AB} = 5 kΩ, code = 0x40		1.2		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A = 5 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ, R_S = 0 Ω		6		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic under operating conditions.
[5] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, AND 100 kΩ VERSIONS

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$, −40°C < T_A < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}		−20		+20	%
Resistance Temperature Coefficient[3]	$\Delta R_{AB}/\Delta T$			45		ppm/°C
Output Resistance	R_{WB}	Code = 0x00		75	300	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x40		15		ppm/°C
Full-Scale Error (50 kΩ, 100 kΩ)	V_{WFSE}	Code = 0x7F	−1	−1	0	LSB
Zero-Scale Error (50 kΩ, 100 kΩ)	V_{WZSE}	Code = 0x00	0	0.4	1	LSB
Full-Scale Error (10 kΩ)	V_{WFSE}	Code = 0x7F	−2	−0.5	0	LSB
Zero-Scale Error (10 kΩ)	V_{WZSE}	V_{DD} = 4.5 V to 5.5 V, code = 0x00	0	0.5	1	LSB
		V_{DD} = 2.7 V to 4.4 V, code = 0x00	0	0.5	1.2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	V_A, V_W		GND		V_{DD}	V
Capacitance A[6]	C_A	f = 1 MHz, measured to GND, code = 0x40		45		pF
Capacitance W[6]	C_W	f = 1 MHz, measured to GND, code = 0x40		60		pF
Common-Mode Leakage	I_{CM}	$V_A = V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	μA
Input Capacitance[6]	C_{IL}			5		pF
Output Logic Low (SDA)	V_{OL}	I_{OL} = 3 mA			0.4	V
		I_{OL} = 6 mA			0.6	V
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{DD} = 5.5 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		3	7	μA
		V_{DD} = 5 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		2.5	5.2	μA
		V_{DD} = 3.3 V; $V_{IH} = V_{DD}$ or V_{IL} = GND		0.9	2	μA
Power Dissipation[7]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			40	μW
Power Supply Sensitivity	PSSR	V_{DD} = 5 V ± 10%, code = midscale		±0.01	±0.02	%/%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[6, 8]						
Bandwidth –3 dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, code = 0x40		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V ±1 LSB error band		2		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, R_S = 0		9		nV/√Hz

[1] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] $V_A = V_{DD}$, wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W, with the RDAC configured as a potentiometer divider similar to a voltage output DAC. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other.
[6] Guaranteed by design, not subject to production test.
[7] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[8] All dynamic characteristics use V_{DD} = 5 V.

TIMING CHARACTERISTICS—5 kΩ, 10 kΩ, 50 kΩ, AND 100 kΩ VERSIONS

V_{DD} = 5 V ± 10% or 3 V ± 10%, $V_A = V_{DD}$, −40°C < T_A < +125°C, unless otherwise noted.

Table 3.

Parameter[1, 2, 3]	Symbol	Min	Typ[4]	Max	Unit
SCL Clock Frequency	f_{SCL}			400	kHz
Bus Free Time Between Stop and Start, t_{BUF}	t_1	1.3			µs
Hold Time (Repeated Start), $t_{HD;STA}$[5]	t_2	0.6			µs
Low Period of SCL Clock, t_{LOW}	t_3	1.3			µs
High Period of SCL Clock, t_{HIGH}	t_4	0.6		50	µs
Setup Time for Repeated Start Condition, $t_{SU;STA}$	t_5	0.6			µs
Data Hold Time, $t_{HD;DAT}$	t_6			0.9	µs
Data Setup Time, $t_{SU;DAT}$	t_7	100			ns
Fall Time of Both SDA and SCL Signals, t_F	t_8			300	ns
Rise Time of Both SDA and SCL Signals, t_R	t_9			300	ns
Setup Time for Stop Condition, $t_{SU;STO}$	t_{10}	0.6			µs

[1] Specifications apply to all parts.
[2] Guaranteed by design, not subject to production test.
[3] See timing diagrams (Figure 2, Figure 33, and Figure 34) for locations of measured values.
[4] Typical specifications represent average readings at 25°C and V_{DD} = 5 V.
[5] After this period, the first clock pulse is generated.

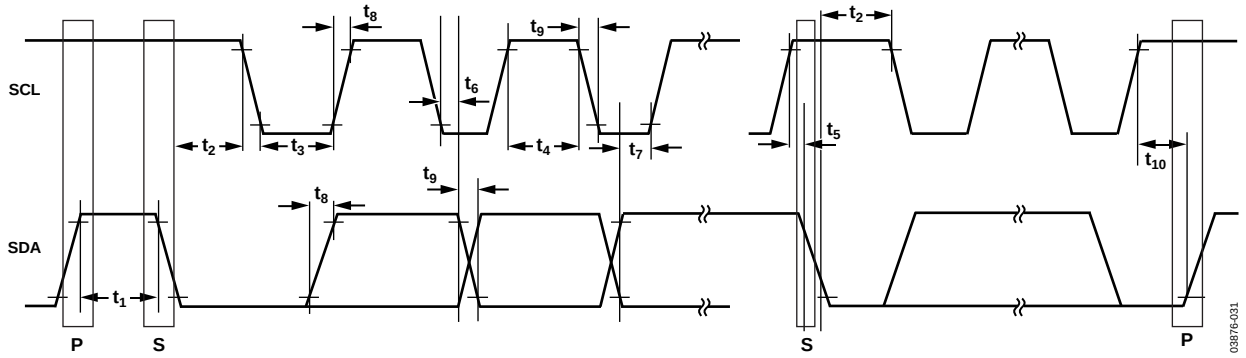

Figure 2. I²C Interface, Detailed Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_A, V_W to GND	V_{DD}
Terminal Current, Ax to Bx, Ax to Wx, Bx to Wx	
Pulsed[1]	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to V_{DD} + 0.3 V
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	−65°C to +150°C
Thermal Resistance θ_{JA}[2]: (SC70-6)	340°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb-Free	260°C

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_{JMAX} − T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

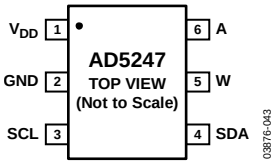

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply.
2	GND	Digital Ground and B Termination Voltage.
3	SCL	Serial Clock Input; Positive Edge Triggered.
4	SDA	Serial Data Input/Output.
5	W	Terminal W.
6	A	Terminal A.

TYPICAL PERFORMANCE CHARACTERISTICS

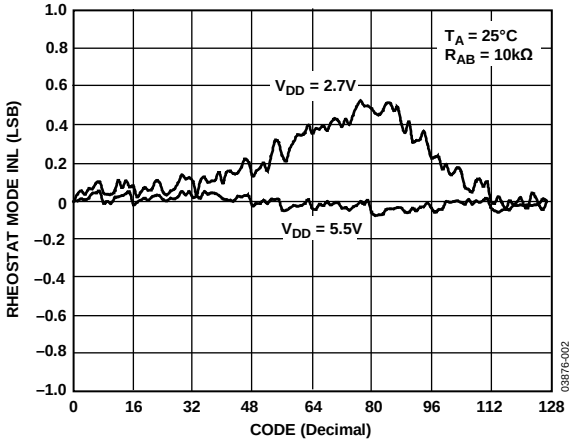

Figure 4. R-INL vs. Code vs. Supply Voltages

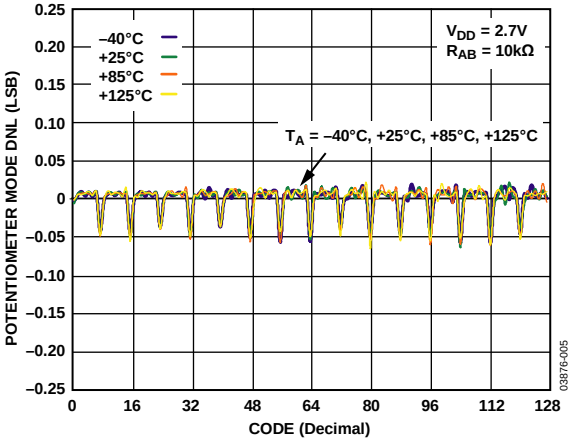

Figure 7. DNL vs. Code vs. Temperature

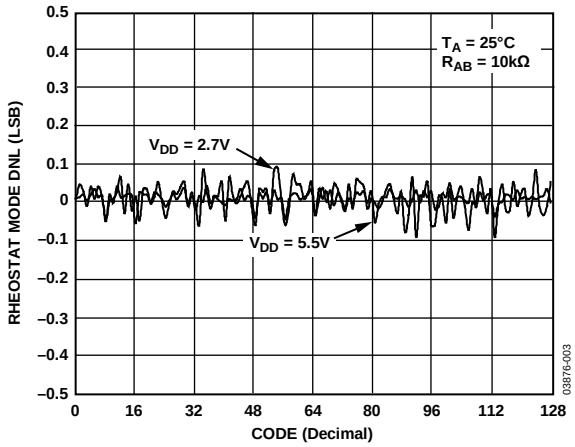

Figure 5. R-DNL vs. Code vs. Supply Voltages

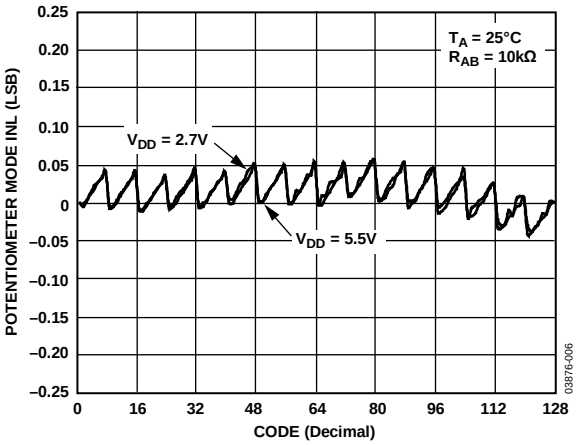

Figure 8. INL vs. Code vs. Supply Voltages

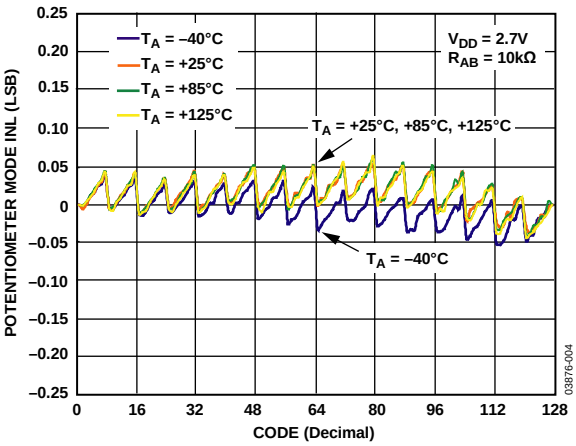

Figure 6. INL vs. Code vs. Temperature

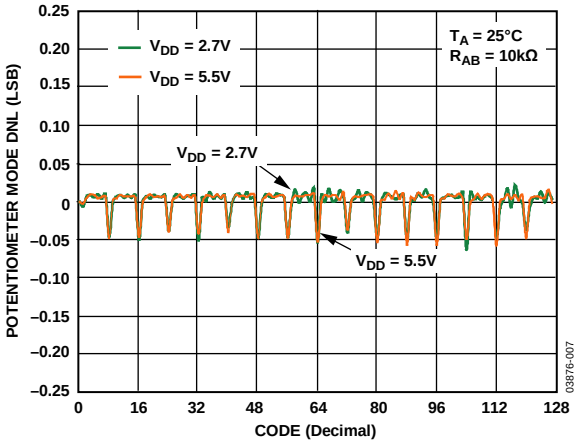

Figure 9. DNL vs. Code vs. Supply Voltages

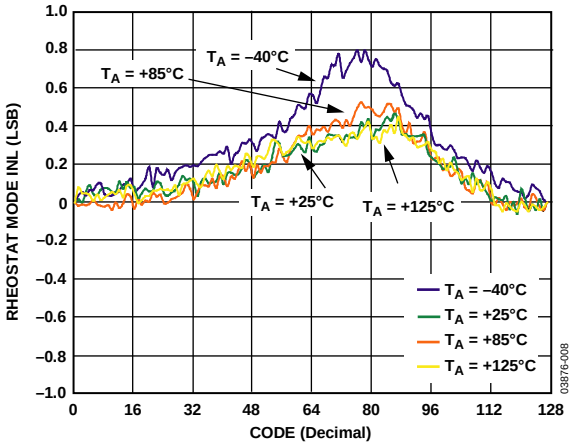

Figure 10. R-INL vs. Code vs. Temperature

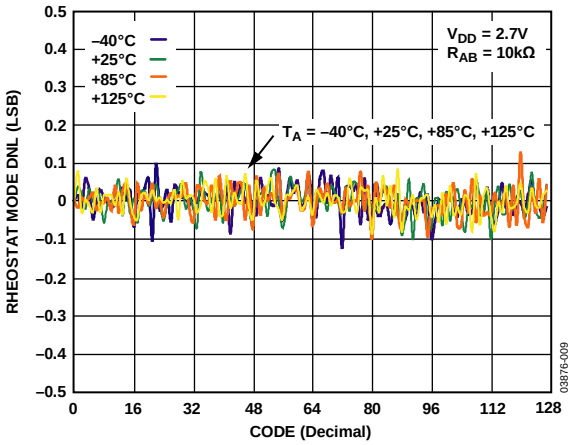

Figure 11. R-DNL vs. Code vs. Temperature

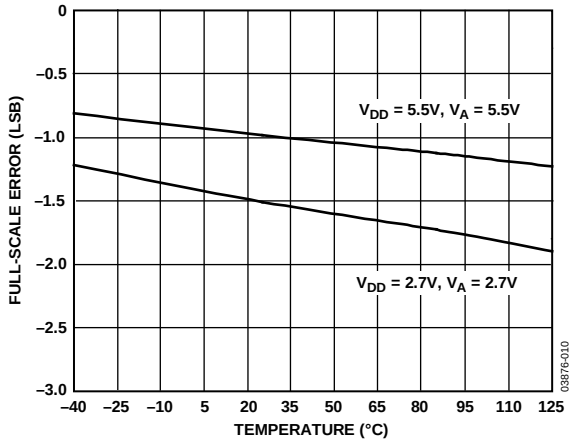

Figure 12. Full-Scale Error vs. Temperature

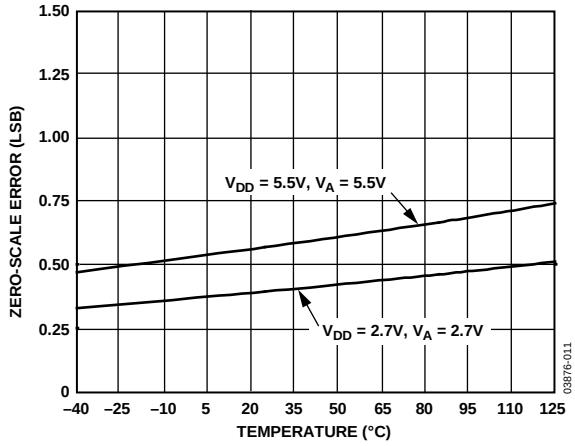

Figure 13. Zero-Scale Error vs. Temperature

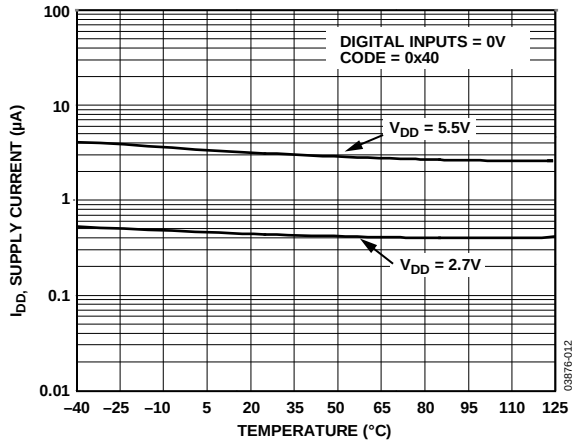

Figure 14. Supply Current vs. Temperature

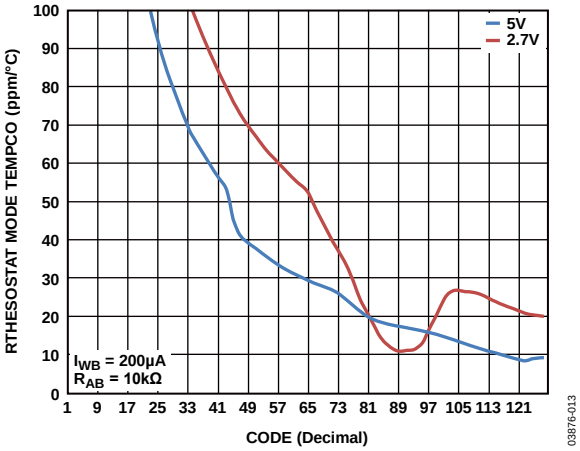

Figure 15. $\Delta R_{WB}/\Delta T$ vs. Code

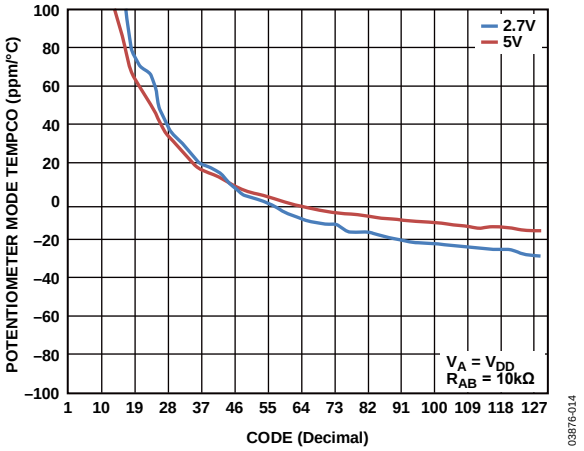

Figure 16. $\Delta V_{WB}/\Delta T$ vs. Code

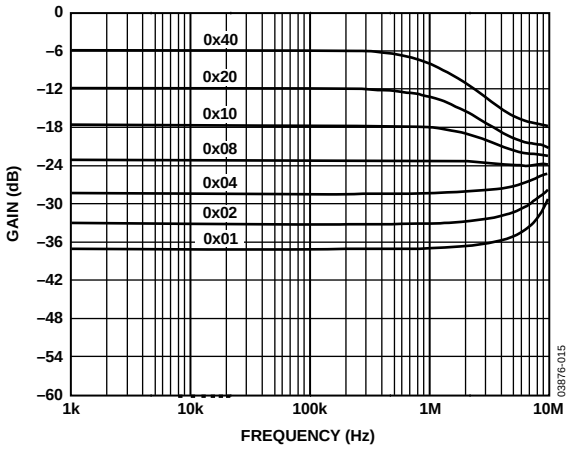

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

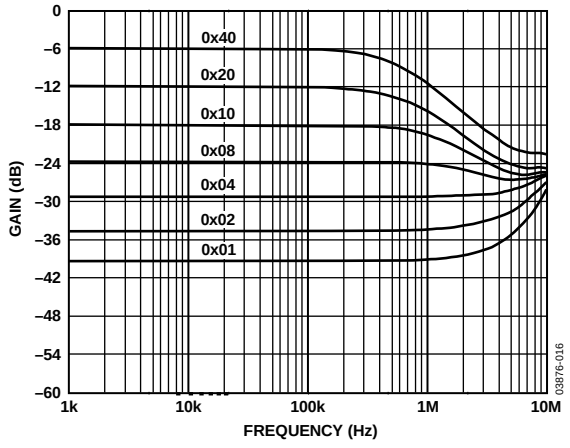

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

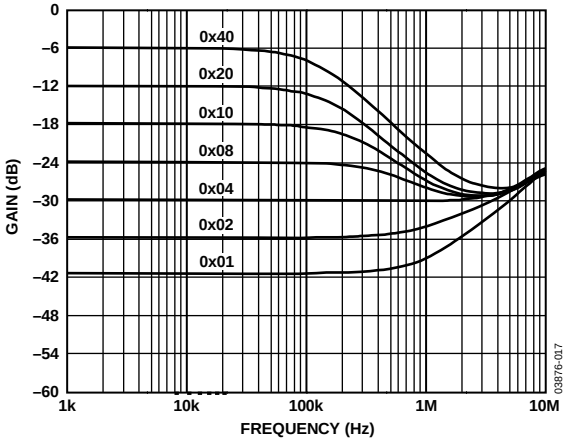

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

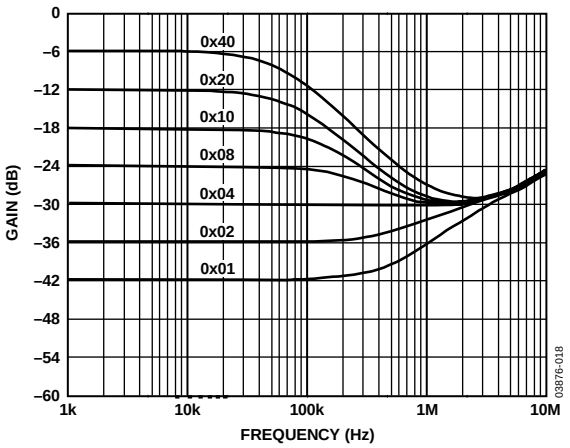

Figure 20. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

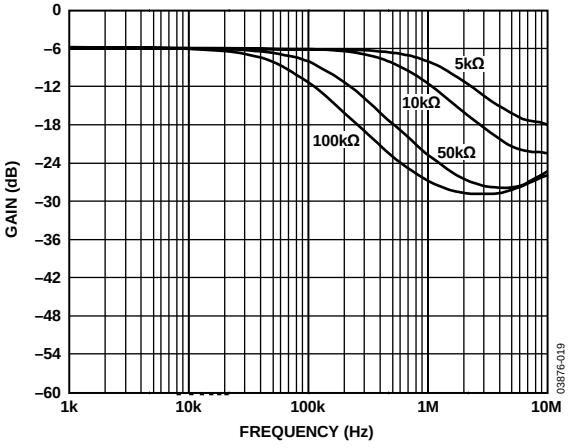

Figure 21. −3 dB Bandwidth @ Code = 0x80

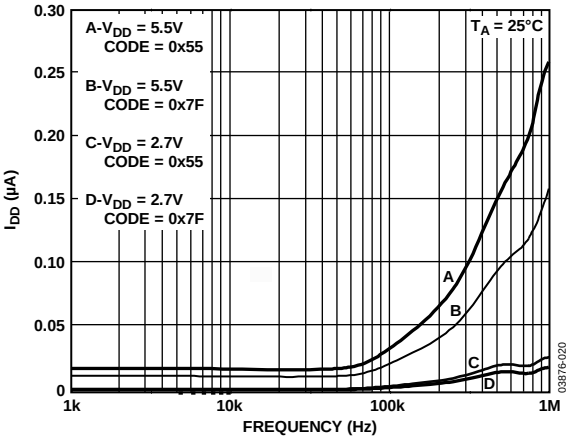

Figure 22. I_{DD} vs. Frequency

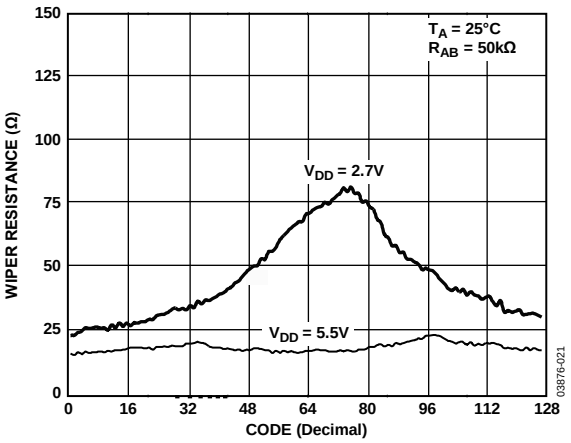

Figure 23. Wiper Resistance vs. Code vs. V_{DD}

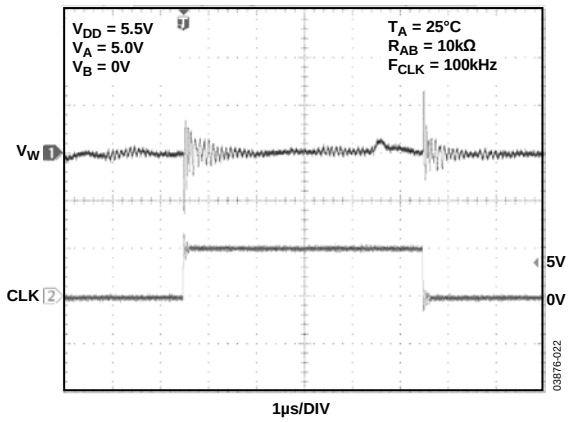

Figure 24. Digital Feedthrough

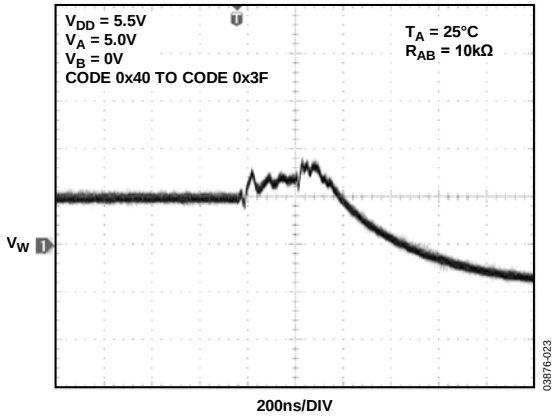

Figure 25. Midscale Glitch, Code 0x40 to Code 0x3F

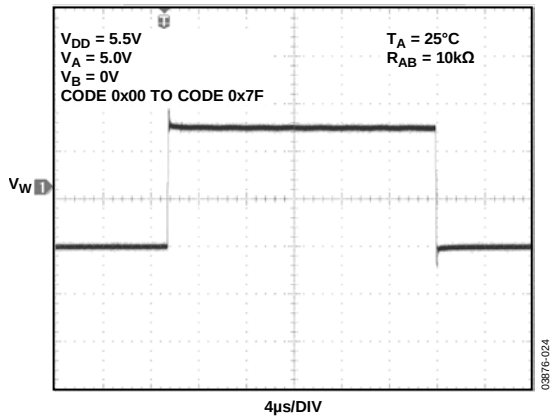

Figure 26. Large Signal Settling Time

TEST CIRCUITS

Figure 27 to Figure 32 define the test conditions used in the Specifications section.

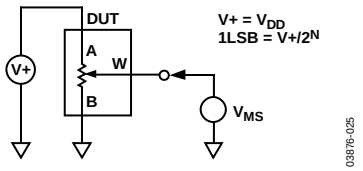

Figure 27. Potentiometer Divider Nonlinearity Error (INL, DNL)

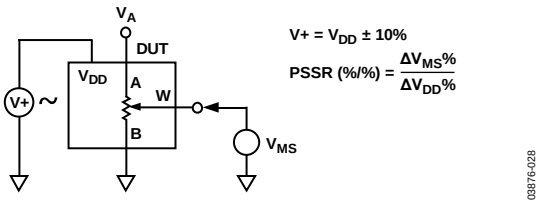

Figure 30. Power Supply Sensitivity (PSS, PSSR)

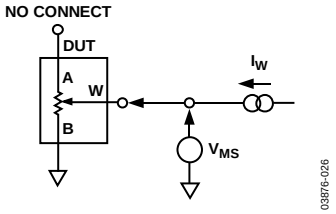

Figure 28. Resistor Position Nonlinearity Error (R-INL, R-DNL)

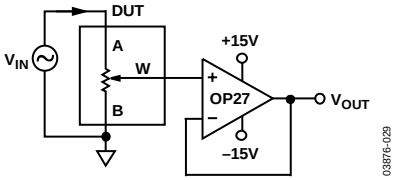

Figure 31. Gain vs. Frequency

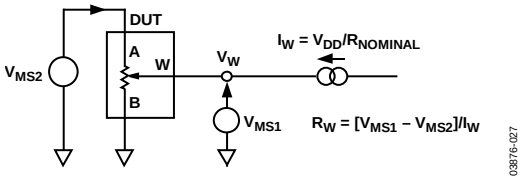

Figure 29. Wiper Resistance

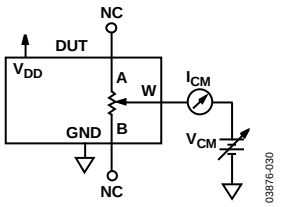

Figure 32. Common-Mode Leakage Current

I²C INTERFACE

The following abbreviations are used in this section:

- S = start condition
- P = stop condition
- A = acknowledge
- X = don't care
- $\overline{W}$ = write
- R = read
- A6, A5, A4, A3, A2, A1, A0 = address bits
- D6, D5, D4, D3, D2, D1, D0 = data bits

Table 6. Write Mode

S	A6	A5	A4	A3	A2	A1	A0	$\overline{W}$	A	X	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

Table 7. Read Mode

S	A6	A5	A4	A3	A2	A1	A0	R	A	0	D6	D5	D4	D3	D2	D1	D0	A	P
	Slave Address Byte									Data Byte									

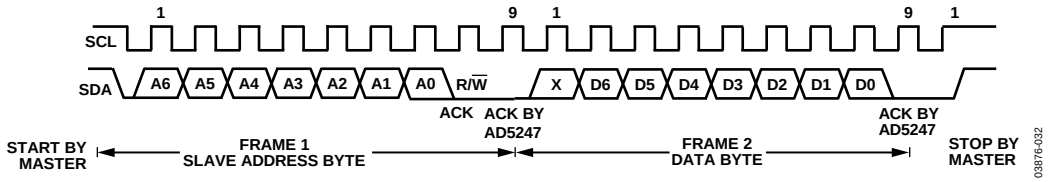

Figure 33. Writing to the RDAC Register

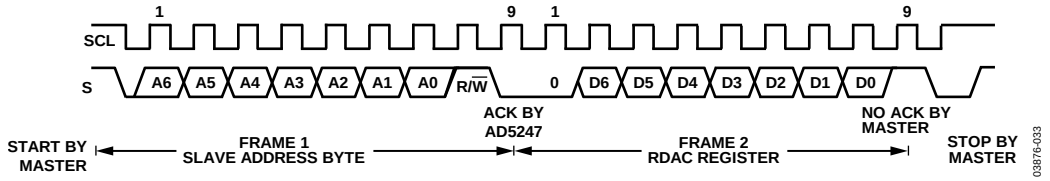

Figure 34. Reading from the RDAC Register

Table 8. I²C Slave Addresses

	Slave Addresses								Slave Address						
Model	A6	A5	A4	A3	A2	A1	A0	**Model**	A6	A5	A4	A3	A2	A1	A0
AD5247BKS5-R2	0	1	0	1	1	1	0	AD5247BKS50-RL7	0	1	0	1	1	1	0
AD5247BKS5-RL7	0	1	0	1	1	1	0	AD5247BKSZ50-RL7	0	1	0	1	1	1	0
AD5247BKSZ5-RL7	0	1	0	1	1	1	0	AD5247BKS100-R2	0	1	0	1	1	1	0
AD5247BKS10-R2	0	1	0	1	1	1	0	AD5247BKSZ100-R2	0	1	0	1	1	1	0
AD5247BKS10-RL7	0	1	0	1	1	1	0	AD5247BKS100-RL7	0	1	0	1	1	1	0
AD5247BKSZ10-RL7	0	1	0	1	1	1	0	AD5247BKSZ100-RL7	0	1	0	1	1	1	0
AD5247BKSZ10-1RL7	0	0	1	0	1	1	1	AD5247BKSZ100-1RL7	0	0	1	0	1	1	1
AD5247BKSZ10-2RL7	0	0	1	0	1	1	0	AD5247BKSZ100-2RL7	0	0	1	0	1	1	0
AD5247BKS50-R2	0	1	0	1	1	1	0								

THEORY OF OPERATION

The AD5247 is a 128-position, digitally-controlled variable resistor (VR) device. An internal power-on preset places the wiper at midscale during power-on, which simplifies the default condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance (R_{AB}) of the RDAC between Terminal A and Terminal B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final two or three digits of the part number determine the nominal resistance value; for example, 10 kΩ = 10 and 50 kΩ = 50. The R_{AB} of the VR has 128 contact points accessed by the wiper terminal, plus the B terminal contact. The 7-bit data in the RDAC latch is decoded to select one of the 128 possible settings.

Assuming a 10 kΩ part is used, the wiper's first connection starts at the B terminal for Data 0x00. Because there is a 50 Ω wiper contact resistance, such a connection yields a minimum of 100 Ω (2 × 50 Ω) resistance between Terminal W and Terminal B. The second connection is the first tap point, corresponding to 178 Ω (R_{WB} = R_{AB}/128 + R_W = 78 Ω + 2 × 50 Ω) for Data 0x01. The third connection is the next tap point, representing 256 Ω (2 × 78 Ω + 2 × 50 Ω) for Data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 10,100 Ω (R_{AB} + 2 × R_W).

Figure 35 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string is not accessed.

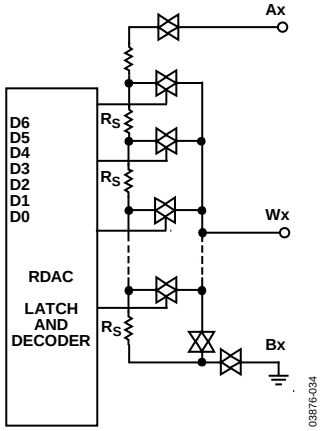

Figure 35. AD5247 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{128} \times R_{AB} + 2 \times R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 7-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and the Terminal A is open-circuited, the output resistance R_{WB}, shown in Table 9, is set for the indicated RDAC latch codes.

Table 9. Codes and Corresponding R_{WB} Resistance

D (Decimal)	R_{WB} (Ω)	Output State
127	10,072	Full scale (R_{AB} + 2 × R_W)
64	5150	Midscale
1	228	1 LSB
0	150	Zero scale (wiper contact resistance)

Note that in the zero-scale condition, a finite resistance of 100 Ω between Terminal W and Terminal B is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled complementary resistance, R_{WA}. When these terminals are used, the Terminal B can be opened. Set the resistance value for R_{WA} to start at a maximum value of resistance and to decrease the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{128 - D}{128} \times R_{AB} + 2 \times R_W \quad (2)$$

If R_{AB} = 10 kΩ and the B terminal is open-circuited, the output resistance, R_{WA}, shown in Table 10, is set for the indicated RDAC latch codes.

Table 10. Codes and Corresponding R_{WA} Resistance

D (Decimal)	R_{WA} (Ω)	Output State
127	228	Full scale
64	5150	Midscale
1	10,071	1 LSB
0	10,150	Zero scale

Typical device-to-device matching is process lot dependent and can vary by up to ±30%. Because the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 45 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A, proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A-to-B, W-to-A, and W-to-B can be at either polarity.

If ignoring the effect of the wiper resistance for approximation, connecting the Terminal A to 5 V and the Terminal B to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across Terminal A and Terminal B divided by the 128 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{128} \times V_A \quad (3)$$

A more accurate calculation that includes the effect of wiper resistance, V_W, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} \times V_A \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike rheostat mode, divider mode makes the output voltage mainly on the ratio of Internal Resistor R_{WA} to Internal Resistor R_{WB}, and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

I²C-COMPATIBLE 2-WIRE SERIAL BUS

The first byte of the AD5247 is a slave address byte (see the I²C Interface section). It has a 7-bit slave address and an R/$\overline{W}$ bit. The 5 kΩ and 50 kΩ options support one 7-bit slave address while the 10 kΩ and 100 kΩ options each have three hard-coded slave address options available (see Table 8 for a full list of slave address locations). The extra hard coded slave addresses on the 10 kΩ and 100 kΩ options allow users to employ up to three of these devices on one I²C bus. The seven MSBs of the slave address are followed by 0 for a write command or 1 to place the device in read mode.

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 33). The following byte is the slave address byte, consisting of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device). The slave, whose address corresponds to the transmitted address, responds by pulling the SDA line low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/$\overline{W}$ bit is high, the master reads from the slave device. If the R/$\overline{W}$ bit is low, the master writes to the slave device.
2. In write mode, after acknowledgement of the slave address byte, the next byte is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 33).
3. In read mode, after acknowledgment of the slave address byte, data is received over the serial bus in sequences of nine clock pulses (a slight difference from write mode, where eight data bits are followed by an acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 34).
4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 33). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, which goes high to establish a stop condition (see Figure 34).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing the part only once. For example, after the RDAC has acknowledged its slave address in the write mode, the RDAC output updates on each successive byte. If different instructions are needed, the write/read mode has to start again with a new slave address and data byte. Similarly, a repeated read function of the RDAC is also allowed.

LEVEL SHIFTING FOR BIDIRECTIONAL INTERFACE

While most legacy systems can be operated at one voltage, a new component can be optimized at another voltage. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, users can employ a 3.3 V E²PROM to interface with a 5 V digital potentiometer. A level shifting scheme is needed to enable a bidirectional communication so that the setting of the digital potentiometer can be stored in and retrieved from the E²PROM. Figure 36 shows one of the level-shifting implementations. M1 and M2 can be any N-channel signal FETs, or if V_{DD} falls below 2.5 V, M1 and M2 can be low threshold FETs such as the FDV301N.

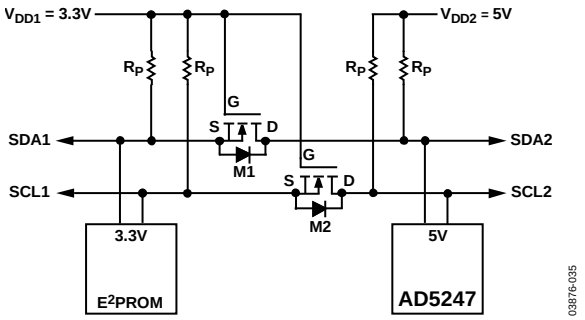

Figure 36. Level-Shifting for Operation at Different Potentials

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures as shown in Figure 37. This applies to digital input pins (SDA and SCL).

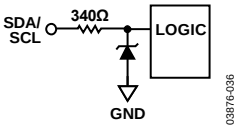

Figure 37. ESD Protection of Digital Pins

TERMINAL VOLTAGE OPERATING RANGE

The AD5247 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on Terminal A and Terminal W that exceed V_{DD} or GND are clamped by the internal forward biased diodes (see Figure 38).

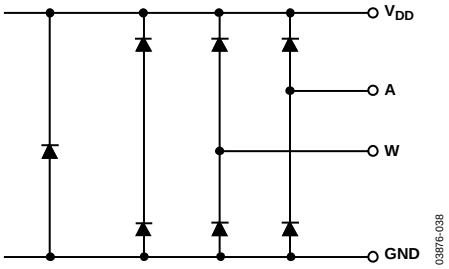

Figure 38. Maximum Terminal Voltages Set by V_{DD} and GND

MAXIMUM OPERATING CURRENT

At low code values, the user should be aware that, due to low resistance values, the current through the RDAC might exceed the 5 mA limit. In Figure 39, a 5 V supply is placed on the wiper, and the current through Terminal W and Terminal B is plotted with respect to code. A line is also drawn denoting the 5 mA current limit. Note that at low code values (particularly for the 5 kΩ and 10 kΩ options), the current level increases significantly. Care should be taken to limit the current flow between W and B in this state to a maximum continuous current of 5 mA and a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contacts can occur.

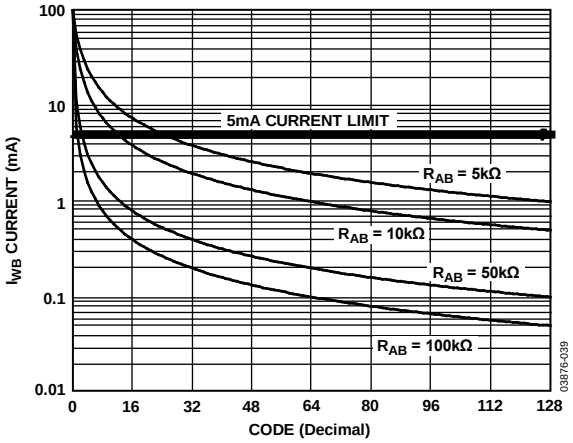

Figure 39. Maximum Operating Current

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A and Terminal W (see Figure 38), it is important to power V_{DD}/GND before applying any voltage to Terminal A and Terminal W; otherwise, the diode is forward-biased such that V_{DD} is powered unintentionally and can affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, V_A, and V_W. The relative order of powering V_A and V_W and the digital inputs is not important as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to employ a compact, minimum lead-length layout design. The leads to the inputs should be as direct as possible with minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF to 0.1 µF disc or chip ceramic capacitors. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 40). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

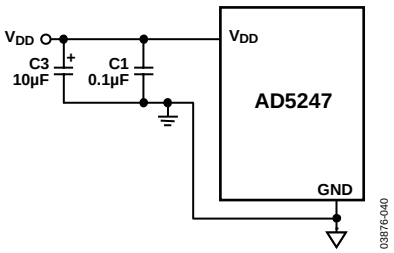

Figure 40. Power Supply Bypassing

CONSTANT BIAS TO RETAIN RESISTANCE SETTING

For users who desire nonvolatility but cannot justify the additional cost for the EEMEM, the AD5247 can be considered a low cost alternative because it maintains a constant bias to retain the wiper setting. The AD5247 is specifically designed with low power in mind, which allows low power consumption even in battery-operated systems.

Figure 41 demonstrates the power consumption from a 3.4 V 450 mA/hr Li-Ion cell phone battery, which is connected to the AD5247. The measurement over time shows that the device draws approximately 1.3 µA and consumes negligible power. Over a course of 30 days, the battery was depleted by less than 2%, the majority of which was due to the intrinsic leakage current of the battery itself.

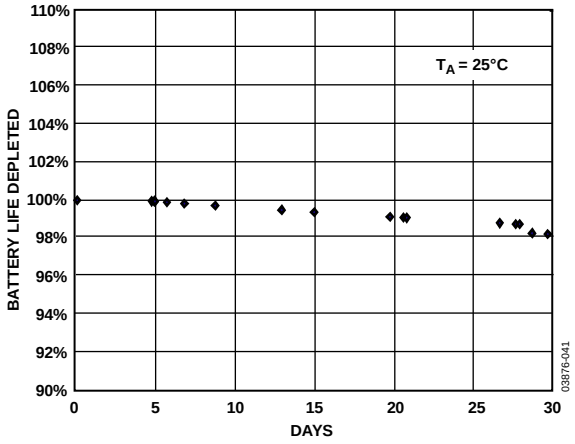

Figure 41. Battery Operating Life Depletion

This demonstrates that constantly biasing the potentiometer is a practical approach. Most portable devices do not require the removal of batteries for charging. Although the resistance setting of the AD5247 is lost when the battery needs replacement, such events occur rather infrequently. As a result, this inconvenience is justified by the lower cost and smaller size offered by the AD5247. If total power is lost, the user should be provided with a means to adjust the setting accordingly.

OUTLINE DIMENSIONS

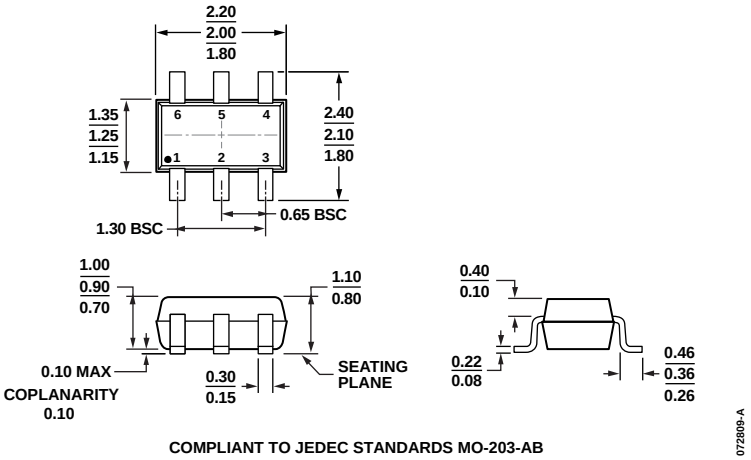

Figure 42. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AB} (kΩ)	Temperature Range	Package Description[2]	Package Option	Branding
AD5247BKSZ5-RL7	5	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D96
AD5247BKSZ10-RL7	10	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D95
AD5247BKSZ10-1RL7	10	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D5E
AD5247BKSZ10-2RL7	10	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	DAK
AD5247BKSZ50-RL7	50	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D97
AD5247BKSZ100-R2	100	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D98
AD5247BKSZ100-RL7	100	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D98
AD5247BKSZ100-1RL7	100	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	DAJ
AD5247BKSZ100-2RL7	100	−40°C to +125°C	6-lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	DAL
EVAL-AD5247DBZ			Evaluation Board		

[1] Z = RoHS compliant part.
[2] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D03876-0-5/12(F)