AD10242–SPECIFICATIONS

Electrical Characteristics (AV_{CC} = +5 V; AV_{EE} = –5.0 V; DV_{CC} = +5 V; applies to each ADC, unless otherwise noted.)

Parameter	Temp	Test Level	Mil Subgroup	AD10242BZ/TZ Min	Typ	Max	Unit
RESOLUTION					12		Bits
DC ACCURACY							
No Missing Codes	Full	VI	1, 2, 3		Guaranteed		
Offset Error	25°C	I	1	–0.5	±0.05	+0.5	% FS
	Full	VI	2, 3	–2.0	±1.0	+2.0	% FS
Offset Error Channel Match	Full	V			±0.1		%
Gain Error[1]	25°C	I	1	–1.0	±0.5	+1.0	% FS
	Full	VI	2, 3	–1.5	±0.8	+1.5	% FS
Gain Error Channel Match	Full	V			±0.1		%
ANALOG INPUT (A_{IN})							
Input Voltage Range							
$A_{IN}1$	Full	I			±0.5		V
$A_{IN}2$	Full	I			±1.0		V
$A_{IN}3$	Full	I			±2		V
Input Resistance							
$A_{IN}1$	Full	IV	12	99	100	101	Ω
$A_{IN}2$	Full	IV	12	198	200	202	Ω
$A_{IN}3$	Full	IV	12	396	400	404	Ω
Input Capacitance[2]	25°C	IV	12	0	4.0	7.0	pF
Analog Input Bandwidth[3]	Full	V			60		MHz
ENCODE INPUT[4, 5]							
Logic Compatibility					TTL/CMOS		
Logic "1" Voltage	Full	I	1, 2, 3	2.0		5.0	V
Logic "0" Voltage	Full	I	1, 2, 3	0		0.8	V
Logic "1" Current (V_{INH} = 5 V)	Full	I	1, 2, 3		625	800	µA
Logic "0" Current (V_{INL} = 0 V)	Full	I	1, 2, 3	–400	–300		µA
Input Capacitance	25°C	V	12			7.0	pF
SWITCHING PERFORMANCE							
Maximum Conversion Rate[6]	Full	VI	4, 5, 6	40	50		MSPS
Minimum Conversion Rate[6]	Full	V	12			5	MSPS
Aperture Delay (t_A)	25°C	V			1.0		ns
Aperture Delay Matching	25°C	V			±2.0		ns
Aperture Uncertainty (Jitter)	25°C	V			1		ps rms
ENCODE Pulsewidth High	25°C	IV	12	12	10		ns
ENCODE Pulsewidth Low	25°C	IV	12		10	41	ns
Output Delay (t_{OD})	Full	IV	12	10	12	14	ns
SNR[7]							
Analog Input @ 1.2 MHz	25°C	V			68		dB
@ 4.85 MHz	25°C	I	4	63	66		dB
	Full	II	5, 6	62	66		dB
@ 9.9 MHz	25°C	I	4	63	65		dB
	Full	II	5, 6	62	65		dB
@ 19.5 MHz	25°C	I	4	60	63		dB
	Full	II	5, 6	59	62		dB
SINAD[8]							
Analog Input @ 1.2 MHz	25°C	V			67		dB
@ 4.85 MHz	25°C	I	4	62	65		dB
	Full	II	5, 6	61	64		dB
@ 9.9 MHz	25°C	I	4	60	64		dB
	Full	II	5, 6	60	63		dB
@ 19.5 MHz	25°C	I	4	58	61		dB
	Full	II	5, 6	58	60		dB

Parameter	Temp	Test Level	Mil Subgroup	AD10242BZ/TZ Min	Typ	Max	Unit
SPURIOUS-FREE DYNAMIC RANGE[9]							
Analog Input @ 1.2 MHz	25°C	I			81		dBFS
@ 4.85 MHz	25°C	I	4	70	80		dBFS
	Full	II	5, 6	70	79		dBFS
@ 9.9 MHz	25°C	I	4	63	70		dBFS
	Full	II	5, 6	63	69		dBFS
@ 19.5 MHz	25°C	I	4	60	67		dBFS
	Full	II	5, 6	60	66		dBFS
TWO-TONE IMD REJECTION[10]							
F1, F2 @ –7 dBFS	Full	II	4, 5, 6	70	76		dBc
CHANNEL-TO-CHANNEL ISOLATION[11]	25°C	IV	12	75	80		dB
TRANSIENT RESPONSE	25°C	V			10		ns
LINEARITY							
Differential Nonlinearity	25°C	IV	12		0.3	1.0	LSB
(Encode = 20 MHz)	Full	IV	12		0.5	1.25	LSB
Integral Nonlinearity	25°C	V			0.3		LSB
(Encode = 20 MHz)	Full	V			0.5		LSB
OVERVOLTAGE RECOVERY TIME[12]							
V_{IN} = 2.0 × FS	Full	IV	12		50	100	ns
V_{IN} = 4.0 × FS	Full	IV	12		75	200	ns
DIGITAL OUTPUTS							
Logic Compatibility					CMOS		
Logic "1" Voltage[13]	Full	I	1, 2, 3	3.5	4.2		V
Logic "0" Voltage[14]	Full	I	1, 2, 3		0.45	0.65	V
Output Coding					Twos Complement		
POWER SUPPLY							
AV_{CC} Supply Voltage	Full	VI			5.0		V
I (AV_{CC}) Current	Full	V			260		mA
AV_{EE} Supply Voltage	Full	VI			–5.0		V
I (AV_{EE}) Current	Full	V			55		mA
DV_{CC} Supply Voltage	Full	VI			5.0		V
I (DV_{CC}) Current	Full	V			25		mA
I_{CC} (Total) Supply Current	Full	I	1, 2, 3		350	400	mA
Power Dissipation (Total)	Full	I	1, 2, 3		1.75	2.0	W
Power Supply Rejection Ratio (PSRR)	Full	I	7, 8		0.01	0.02	% FSR/% V_S
Pass-Band Ripple to 10 MHz	Full	IV	12			0.2	dB

NOTES

[1]Gain tests are performed on $A_{IN}3$ over specified input voltage range.

[2]Input capacitance specifications combine AD9632 die capacitance and ceramic package capacitance.

[3]Full power bandwidth is the frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

[4]ENCODE driven by single-ended source; $\overline{\text{ENCODE}}$ bypassed to ground through 0.01 µF capacitor.

[5]ENCODE may also be driven differentially in conjunction with $\overline{\text{ENCODE}}$; see Encoding the AD10242 section for details.

[6]Minimum and maximum conversion rates allow for variation in Encode Duty Cycle of 50% ± 5%.

[7]Analog Input signal power at –1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed). Encode = 40.0 MSPS.

[8]Analog Input signal power at –1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics. Encode = 40.0 MSPS.

[9]Analog Input signal equals –1 dBFS; SFDR is the ratio of converter full scale to worst spur.

[10]Both input tones at –7 dBFS; two-tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst third order intermod product. f1 = 10.0 MHz ± 100 kHz, 50 kHz ≤ f1 – f2 ≤ 300 kHz.

[11]Channel-to-channel isolation tested with A channel grounded and a full-scale signal applied to B channel ($A_{IN}1$).

[12]Input driven to 2× and 4× $A_{IN}1$ range for >4 clock cycles. Output recovers in band in specified time with Encode = 40 MSPS. No foldover guaranteed.

[13]Outputs are sourcing 10 µA.

[14]Outputs are sinking 10 µA.

All specifications guaranteed within 100 ms of initial power-up regardless of sequencing.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Unit
ELECTRICAL			
V_{CC} Voltage	0	7	V
V_{EE} Voltage	–7	0	V
Analog Input Voltage	V_{EE}	V_{CC}	V
Analog Input Current	–10	+10	mA
Digital Input Voltage (ENCODE)	0	V_{CC}	V
ENCODE, $\overline{\text{ENCODE}}$ Differential Voltage		4	V
Digital Output Current	–40	+40	mA
ENVIRONMENTAL[2]			
Operating Temperature (Case)	–55	+125	°C
Maximum Junction Temperature		175	°C
Lead Temperature (Soldering, 10 sec)		300	°C
Storage Temperature Range (Ambient)	–65	+150	°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances for ES-68-1 package: θ_{JC} = 11°C/W; θ_{JA} = 30°C/W.

Table I. Output Coding

MSB LSB	Base 10	Input
0111111111111	2047	+FS
0000000000001	+1	
0000000000000	0	0.0 V
1111111111111	–1, 4095	
1000000000000	–2047, 2048	–FS

EXPLANATION OF TEST LEVELS

Test Level

I – 100% Production Tested.

II – 100% production tested at 25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III – Sample Tested Only.

IV – Parameter is guaranteed by design and characterization testing.

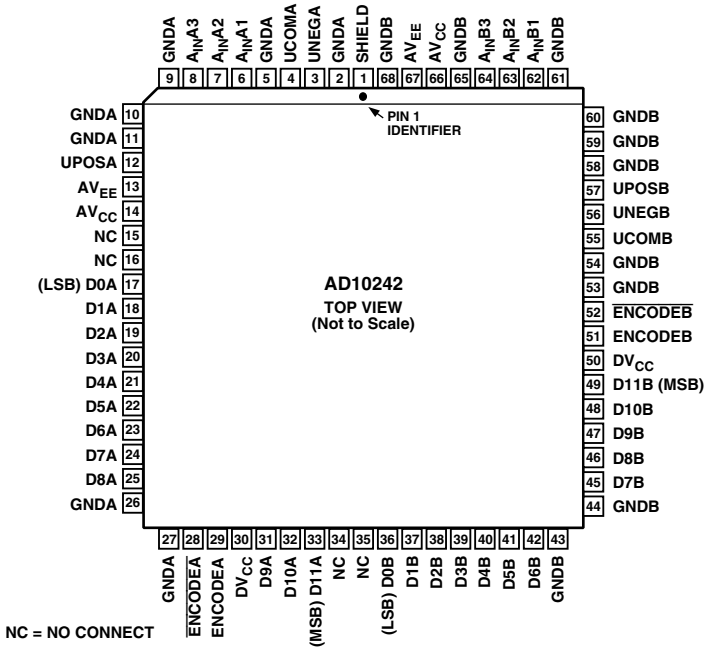
V – Parameter is a typical value only.

VI – All devices are 100% production tested at 25°C; sample tested at temperature extremes.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD10242 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
68-Lead Ceramic Leaded Chip Carrier



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	SHIELD	Internal Ground Shield between Channels.
2, 5, 9–11, 26–27	GNDA	A Channel Ground. A and B grounds should be connected as close to the device as possible.
3	UNEGA	Unipolar Negative.
4	UCOMA	Unipolar Common.
6	$A_{IN}A1$	Analog Input for A Side ADC (Nominally ±0.5 V).
7	$A_{IN}A2$	Analog Input for A Side ADC (Nominally ±1.0 V).
8	$A_{IN}A3$	Analog Input for A Side ADC (Nominally ±2.0 V).
12	UPOSA	Unipolar Positive.
13	AV_{EE}	Analog Negative Supply Voltage (Nominally –5.0 V or –5.2 V).
14	AV_{CC}	Analog Positive Supply Voltage (Nominally 5.0 V).
15, 16, 34, 35	NC	No Connect.
17–25, 31–33	D0A–D11A	Digital Outputs for ADC A. (D0 LSB.)
28	$\overline{\text{ENCODEA}}$	$\overline{\text{ENCODE}}$ is the complement of ENCODE.
29	ENCODEA	Data conversion is initiated on the rising edge of the ENCODE input.
30, 50	DV_{CC}	Digital Positive Supply Voltage (Nominally 5.0 V).
36–42, 45–49	D0B–D11B	Digital Outputs for ADC B. (D0 LSB.)
43–44, 53–54, 58–61, 65, 68	GNDB	B Channel Ground. A and B grounds should be connected as close to the device as possible.
51	ENCODEB	Data conversion is initiated on the rising edge of the ENCODE input.
52	$\overline{\text{ENCODEB}}$	$\overline{\text{ENCODE}}$ is the complement of ENCODE.
55	UCOMB	Unipolar Common.
56	UNEGB	Unipolar Negative.
57	UPOSB	Unipolar Positive.
62	$A_{IN}B1$	Analog Input for B Side ADC (Nominally ±0.5 V).
63	$A_{IN}B2$	Analog Input for B Side ADC (Nominally ±1.0 V).
64	$A_{IN}B3$	Analog Input for B Side ADC (Nominally ±2.0 V).
66	AV_{CC}	Analog Positive Supply Voltage (Nominally 5.0 V).
67	AV_{EE}	Analog Negative Supply Voltage (Nominally –5.0 V or –5.2 V).

DEFINITION OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Encode Pulsewidth/Duty Cycle
Pulsewidth high is the minimum amount of time that the ENCODE pulse should be left in Logic "1" state to achieve rated performance; pulsewidth low is the minimum time that the ENCODE pulse should be left in low state. At a given clock rate, these specifications define an acceptable encode duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the rising edge of the ENCODE command and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 0.02% accuracy after an analog input signal of the specified percentage of full scale is reduced to midscale.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise and Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (SNR, without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. SFDR may be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

Transient Response
The time required for the converter to achieve 0.02% accuracy when a one-half full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. Two-tone SFDR may be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

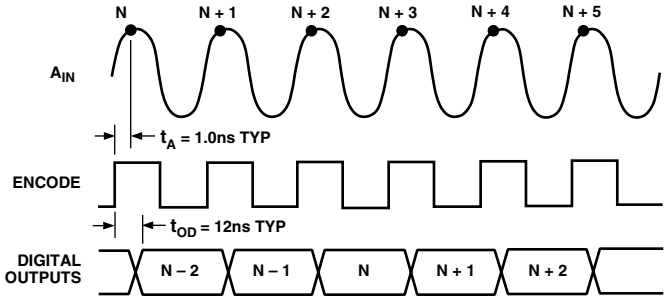


Figure 1. Timing Diagram

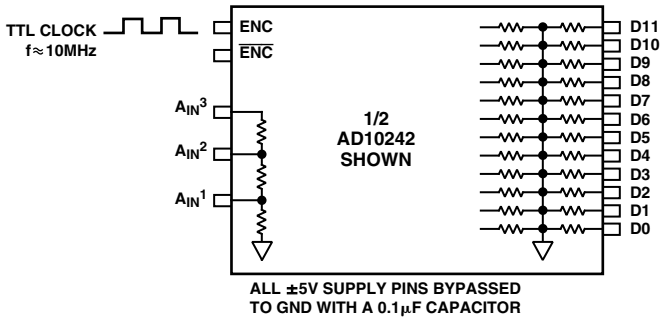


Figure 2. Equivalent Burn-In Circuit

EQUIVALENT CIRCUITS

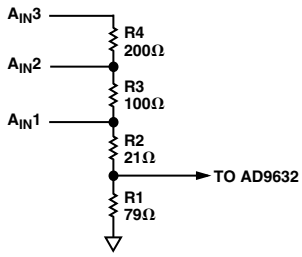


Figure 3. Analog Input Stage

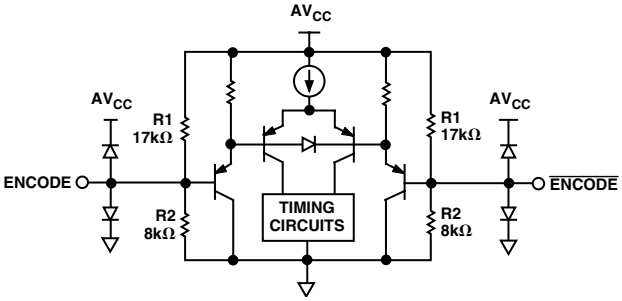


Figure 4. Encode Inputs

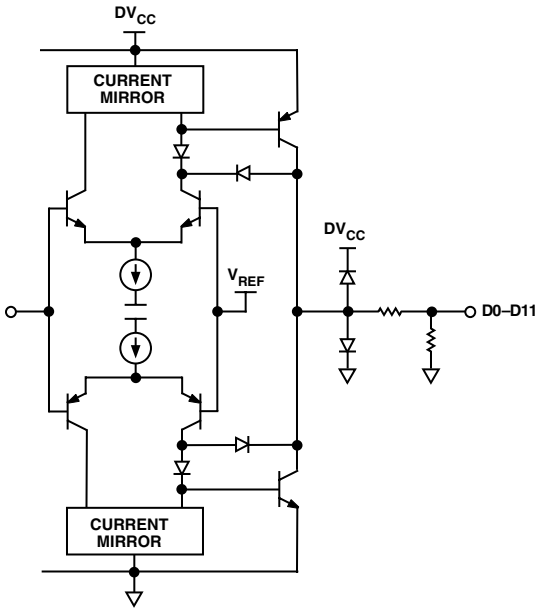
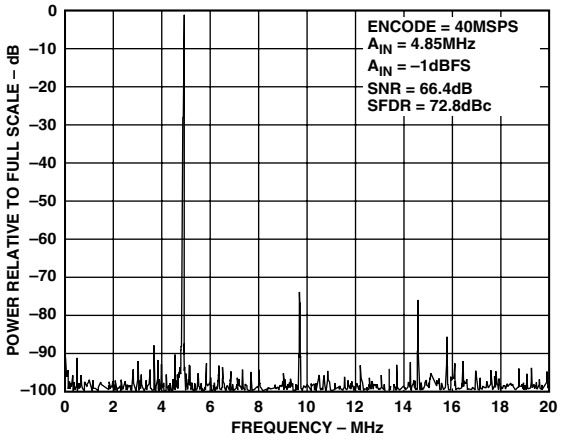
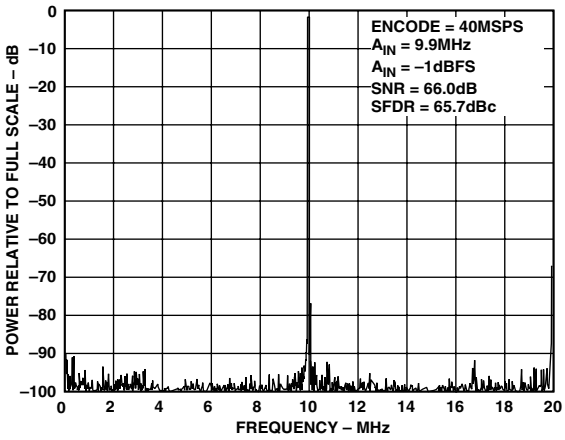


Figure 5. Digital Output Stage

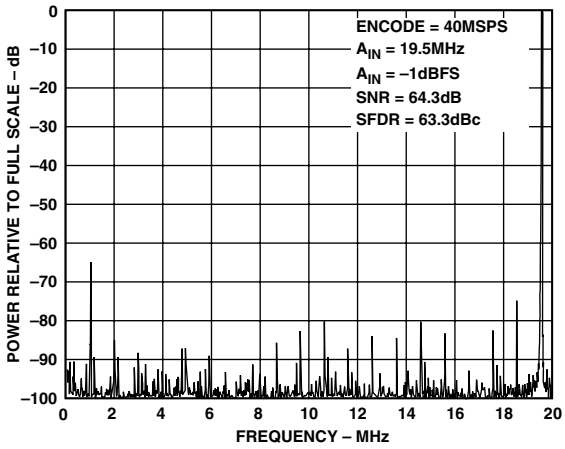
AD10242–Typical Performance Characteristics



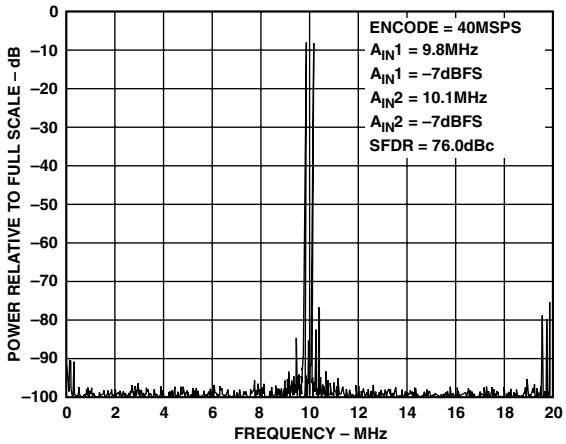
TPC 1. Single Tone @ 4.85 MHz



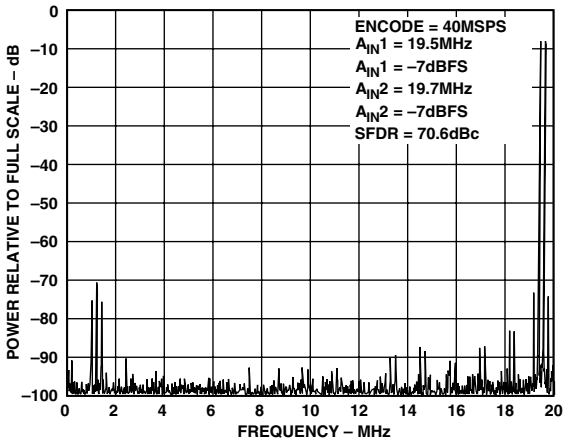
TPC 2. Single Tone @ 9.9 MHz



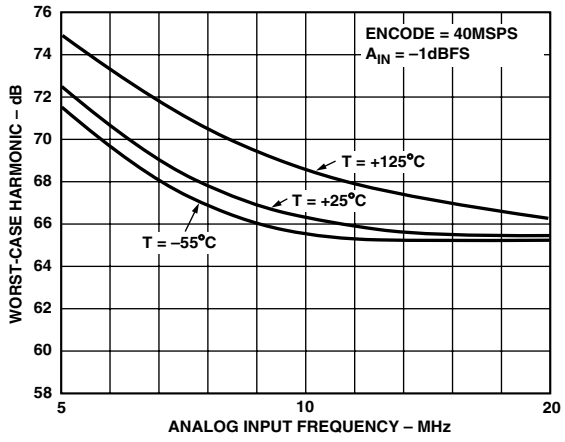
TPC 3. Single Tone @ 19.5 MHz



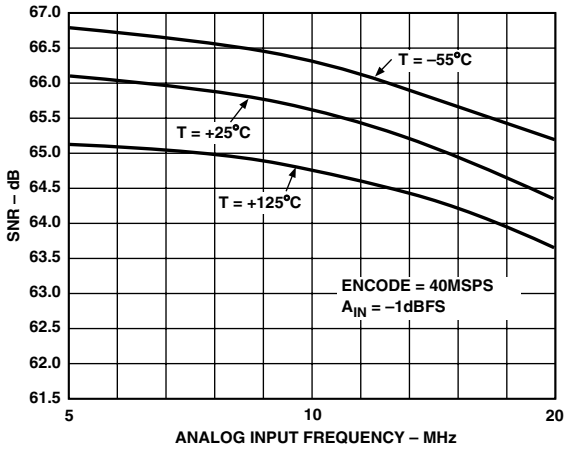
TPC 4. Two-Tone FFT @ 9.8 MHz/10.1 MHz



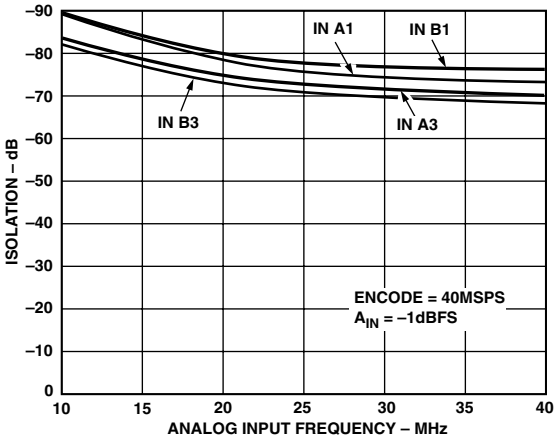
TPC 5. Two-Tone FFT @ 19.5 MHz/19.7 MHz



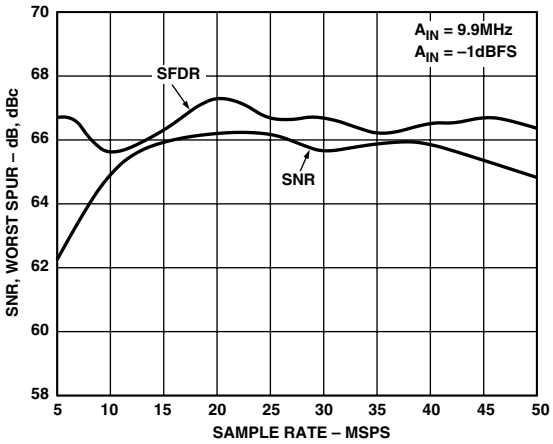
TPC 6. Harmonics vs. A_{IN}



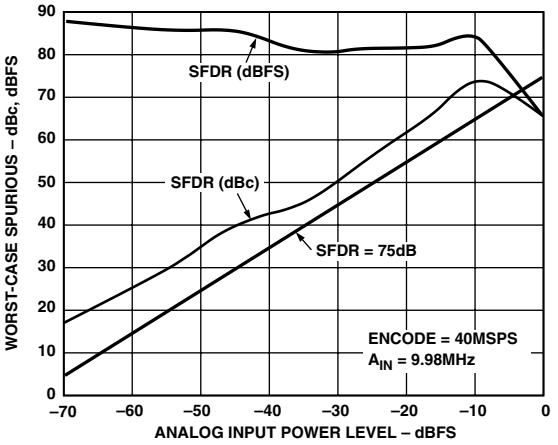
TPC 7. SNR vs. A_{IN}



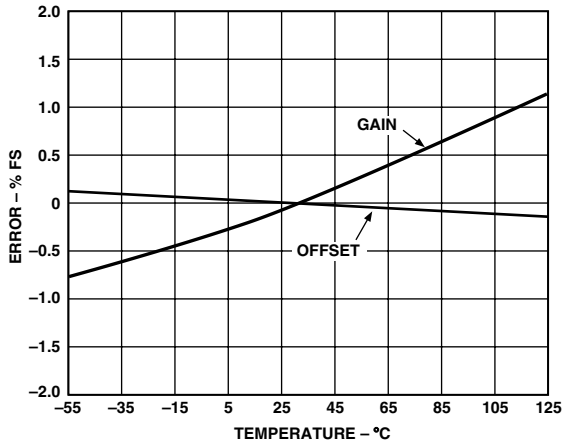
TPC 10. Isolation vs. Frequency



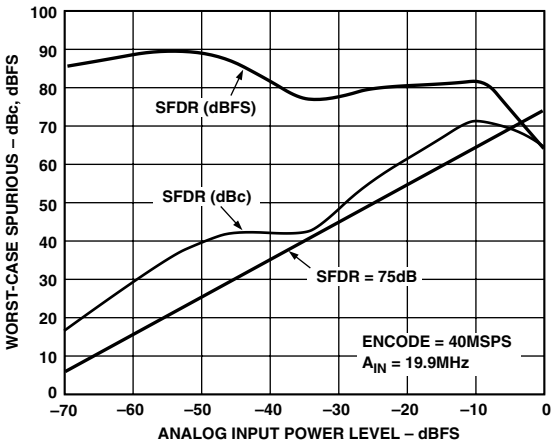
TPC 8. SNR and Harmonics vs. Encode Rate



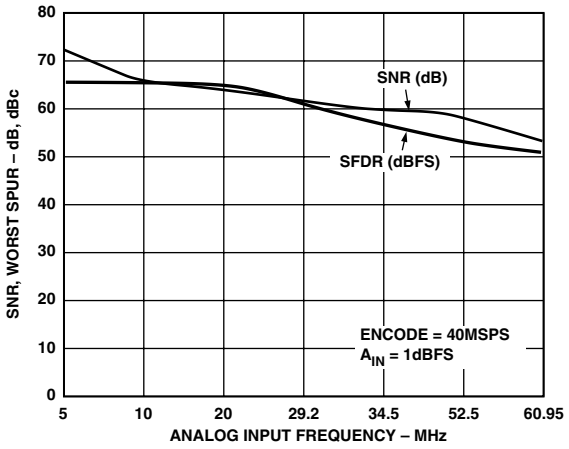
TPC 11. Single Tone SFDR (A_{IN} @ 9.98) vs. Power Level



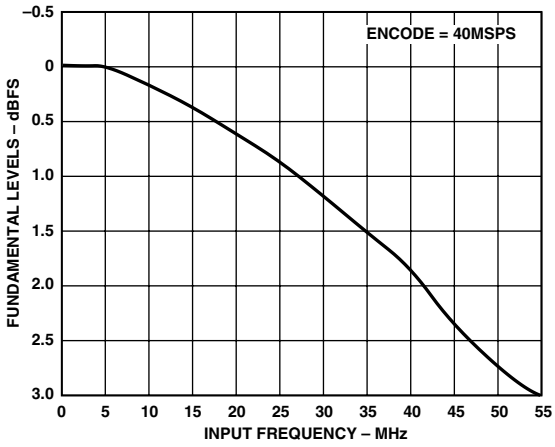
TPC 9. Offset and Gain Error vs. Temperature



TPC 12. Single Tone SFDR (A_{IN} @ 19.9) vs. Power Level



TPC 13. SNR/Harmonics to A_{IN} > Nyquist MSPS



TPC 14. Gain Flatness vs. Input Frequency

THEORY OF OPERATION

Refer to the functional block diagram. The AD10242 employs three monolithic ADI components per channel (AD9632, OP279, and AD9042), along with multiple passive resistor networks and decoupling capacitors to fully integrate a complete 12-bit analog-to-digital converter.

The input signal is first passed through a precision laser trimmed resistor divider, allowing the user to externally select operation with a full-scale signal of ±0.5 V, ±1.0 V, or ±2.0 V by choosing the proper input terminal for the application. The result of the resistor divider is to apply a full-scale input of approximately 0.4 V to the noninverting input of the internal AD9632 amplifier.

The AD9632 provides the dc-coupled level shift circuit required for operation with the AD9042 ADC. Configuring the amplifier in a noninverting mode, the ac signal gain can be trimmed to provide a constant input to the ADC centered around the internal reference voltage of the AD9042. This allows the converter to be used in multiple system applications without the need for external gain and level shift circuitry normally requiring trim. The AD9632 was chosen for its superior ac performance and input drive capabilities. These two specifications have limited the ability of many amplifiers to drive high performance ADCs. As new amplifiers are developed, pin compatible improvements are planned to incorporate the latest operational amplifier technology.

The OP279 provides the buffer and inversion of the internal reference of the AD9042 in order to supply the summing node of the AD9632 input amplifier. This dc voltage is then summed with the input voltage and applied to the input of the AD9042 ADC. The reference voltage of the AD9042 is designed to track internal offsets and drifts of the ADC and is used to ensure matching over an extended temperature range of operation.

APPLYING THE AD10242

Encoding the AD10242

The AD10242 is designed to interface with TTL and CMOS logic families. The source used to drive the ENCODE pin(s) must be clean and free from jitter. Sources with excessive jitter will limit SNR and overall performance.

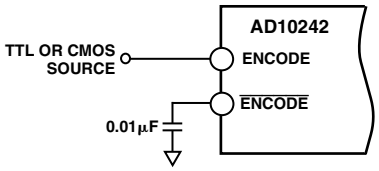


Figure 6. Single-Ended TTL/CMOS Encode

The AD10242 encode inputs are connected to a differential input stage (see Figure 4). With no input connected to either the ENCODE or $\overline{\text{ENCODE}}$ input, the voltage dividers bias the inputs to 1.6 V. For TTL or CMOS usage, the encode source should be connected to ENCODE (Pins 29 and/or 51). $\overline{\text{ENCODE}}$ (Pins 28 and/or 52) should be decoupled using a low inductance or microwave chip capacitor to ground. Devices such as AVX 05085C103MA15, a 0.01 µF capacitor, work well.

Performance Improvements

It is possible to improve the performance of the AD10242 slightly by taking advantage of the internal characteristics of the amplifier and converter combination. By increasing the 5 V supply slightly, the user may be able to gain up to a 5 dB improvement in SFDR over the entire frequency range of the converter. It is not recommended to exceed 5.5 V on the analog supplies since there are no performance benefits beyond that range and care should be taken to avoid the absolute maximum ratings.

If a logic threshold other than the nominal 1.6 V is required, the following equations show how to use an external resistor, *Rx*, to raise or lower the trip point (see Figure 4, R1 = 17 kΩ, R2 = 8 kΩ).

$$V_1 = \frac{5R2Rx}{R1R2 + R1Rx + R2Rx}$$ to lower logic threshold.

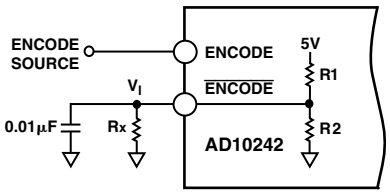


Figure 7. Lower Threshold for Encode

$$V_1 = \frac{5R2}{R2 + \frac{R1Rx}{R1 + Rx}}$$ to raise logic threshold.

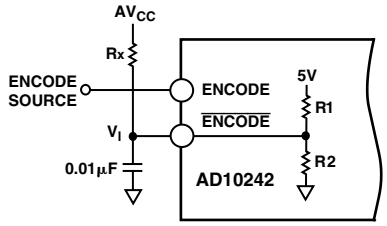


Figure 8. Raise Logic Threshold for Encode

While the single-ended encode will work well for many applications, driving the encode differentially will provide increased performance. Depending on circuit layout and system noise, a 1 dB to 3 dB improvement in SNR can be realized. It is recommended that the encode signal be ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins.

The simplest option is shown below. The low jitter TTL signal is coupled with a limiting resistor, typically 100 Ω, to the primary side of an RF transformer (these transformers are inexpensive and readily available; part number in Figures 9 and 10 is from Mini-Circuits). The secondary side is connected to the ENCODE and $\overline{\text{ENCODE}}$ pins of the converter. Since both encode inputs are self-biased, no additional components are required.

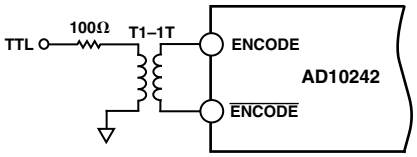


Figure 9. TTL Source—Differential Encode

If no TTL source is available, a clean sine wave may be substituted. In the case of the sine source, the matching network is shown below. Since the matching transformer specified is a 1:1 impedance ratio, the load resistor R should be selected to match the source impedance. The input impedance of the AD9042 is negligible in most cases.

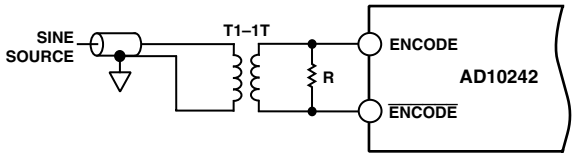


Figure 10. Sine Source—Differential Encode

If a low jitter ECL clock is available, another option is to ac-couple a differential ECL signal to the encode input pins, as shown in Figure 11. The capacitors shown here should be chip capacitors but do not need to be of the low inductance variety.

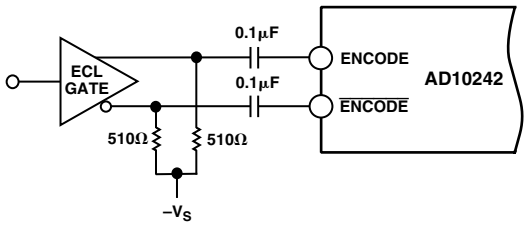


Figure 11. Differential ECL for Encode

As a final alternative, the ECL gate may be replaced by an ECL comparator. The input to the comparator could then be a logic signal or a sine signal.

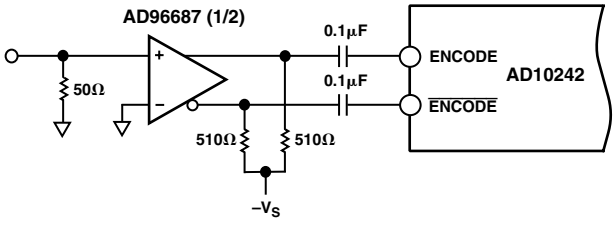


Figure 12. ECL Comparator for Encode

Care should be taken not to overdrive the encode input pin when ac-coupled. Although the input circuitry is electrically protected from overvoltage or undervoltage conditions, improper circuit operations may result from overdriving the encode input pin.

USING THE FLEXIBLE INPUT

The AD10242 has been designed with the user's ease of operation in mind. Multiple input configurations have been included on board to allow the user a choice of input signal levels and input impedance. While the standard inputs are ±0.5 V, ±1.0 V, and ±2.0 V, the user can select the input impedance of the AD10242 on any input by using the other inputs as alternate locations for GND or an external resistor. The following chart summarizes the impedance options available at each input location:

$A_{IN}1$ = 100 Ω when $A_{IN}2$ and $A_{IN}3$ are open.
$A_{IN}1$ = 75 Ω when $A_{IN}3$ is shorted to GND.
$A_{IN}1$ = 50 Ω when $A_{IN}2$ is shorted to GND.

$A_{IN}2$ = 200 Ω when $A_{IN}3$ is open.
$A_{IN}2$ = 100 Ω when $A_{IN}3$ is shorted to GND.
$A_{IN}2$ = 75 Ω when $A_{IN}2$ to $A_{IN}3$ has an external resistor of 300 Ω, with $A_{IN}3$ shorted to GND.
$A_{IN}2$ = 50 Ω when $A_{IN}2$ to $A_{IN}3$ has an external resistor of 100 Ω, with $A_{IN}3$ shorted to GND.

$A_{IN}3$ = 400 Ω.
$A_{IN}3$ = 100 Ω when $A_{IN}3$ has an external resistor of 133 Ω to GND.
$A_{IN}3$ = 75 Ω when $A_{IN}3$ has an external resistor of 92 Ω to GND.
$A_{IN}3$ = 50 Ω when $A_{IN}3$ has an external resistor of 57 Ω to GND.

While the analog inputs of the AD10242 are designed for dc- coupled bipolar inputs, the AD10242 has the ability to use unipolar inputs in a user selectable mode through the addition of an external resistor. This allows for 1 V, 2 V, and 4 V full-scale unipolar signals to be applied to the various inputs ($A_{IN}1$, $A_{IN}2$, and $A_{IN}3$, respectively). Placing a 2.43 kΩ resistor (typical, offset calibration required) between UPOS and UCOM shifts the reference voltage setpoint to allow a unipolar positive voltage to be applied at the inputs of the device. To calibrate offset, apply a midscale dc voltage to the converter while adjusting the unipolar resistor for a midscale output transition.

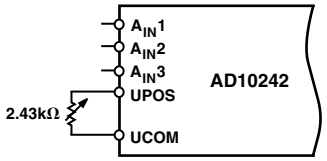


Figure 13. Unipolar Positive

To operate with –1 V, –2 V, or –4 V full-scale unipolar signals, place a 2.67 kΩ resistor (typical, offset calibration required) between UNEG and UCOM. This again shifts the reference voltage setpoint to allow a unipolar negative voltage to be applied at the inputs of the device. To calibrate offset, apply a midscale dc voltage to the converter while adjusting the unipolar resistor for a midscale output transition.

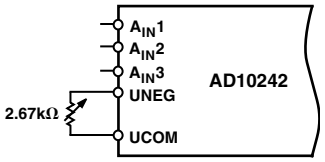


Figure 14. Unipolar Negative

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Proper grounding is essential in any high speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling to the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. The AD10242 does not distinguish between analog and digital ground pins as the AD10242 should always be treated like an analog component. All ground pins should be connected together directly under the AD10242. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance path and manage the power and ground currents. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

LAYOUT INFORMATION

The schematic of the evaluation board (Figure 15) represents a typical implementation of the AD10242. The pinout of the AD10242 is very straightforward and facilitates ease of use and the implementation of high frequency/high resolution design practices. It is recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. All capacitors except the one placed on $\overline{\text{ENCODE}}$ can be standard high quality ceramic chip capacitors. The capacitor used on the $\overline{\text{ENCODE}}$ pin must be a low inductance chip capacitor as referenced previously.

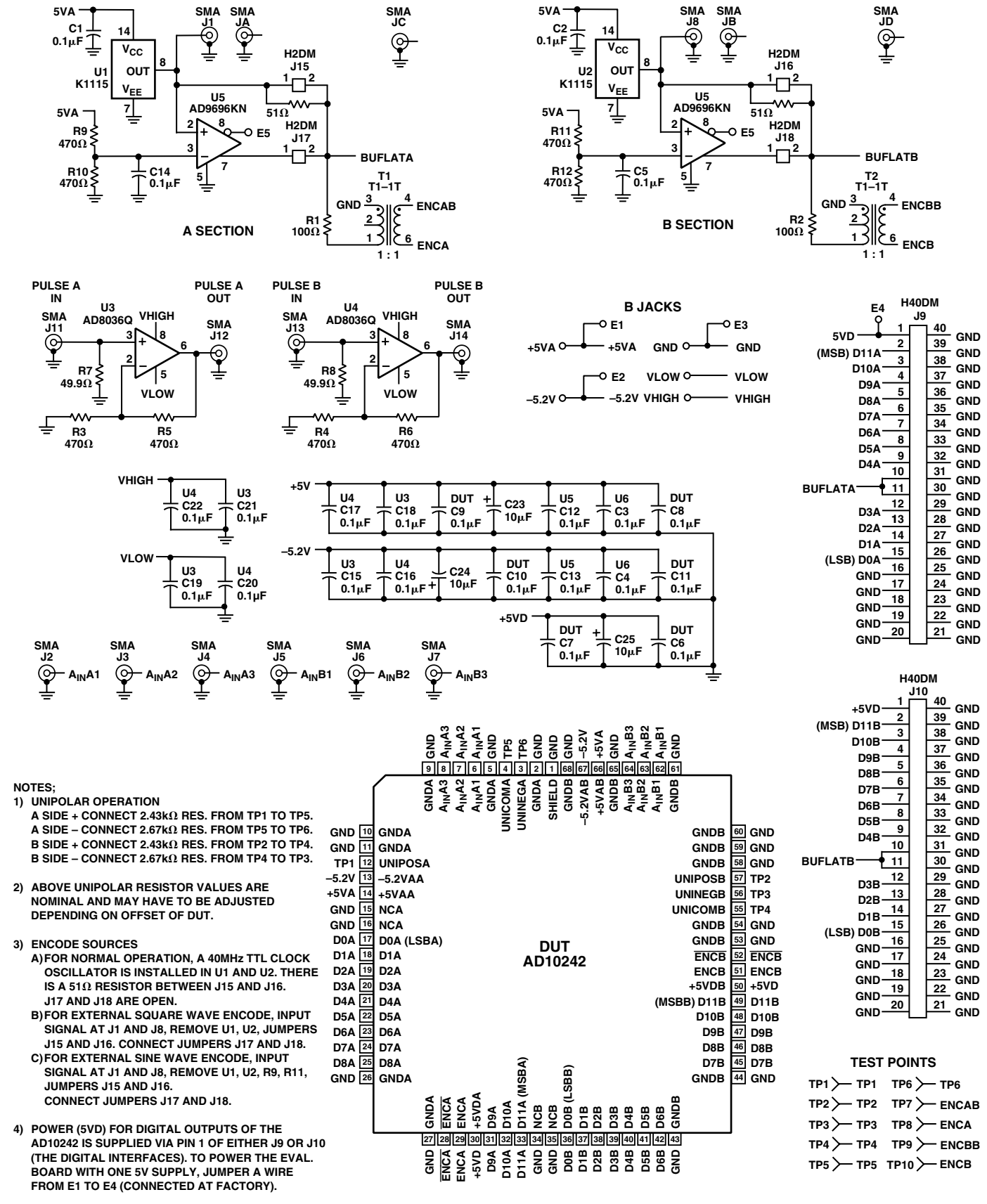


Figure 15. Evaluation Board Schematic

Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate. Internal circuitry buffers the outputs of the AD9042 ADC through a resistor network to eliminate the need to externally isolate the device from the receiving gate.

EVALUATION BOARD

The AD10242 evaluation board (see Figure 16) is designed to provide optimal performance for evaluation of the AD10242 analog-to-digital converter. The board encompasses everything needed to ensure the highest level of performance for evaluating the AD10242.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the crystal oscillator, the associated components and amplifiers, and the analog section of the AD10242. The digital outputs of the AD10242 are powered via Pin 1 of either J9 or J10 found on the digital interface connector. To power the evaluation board with one 5 V supply, a jumper wire is required from test point E1 to E4. Contact the factory if additional layout or applications assistance is required.

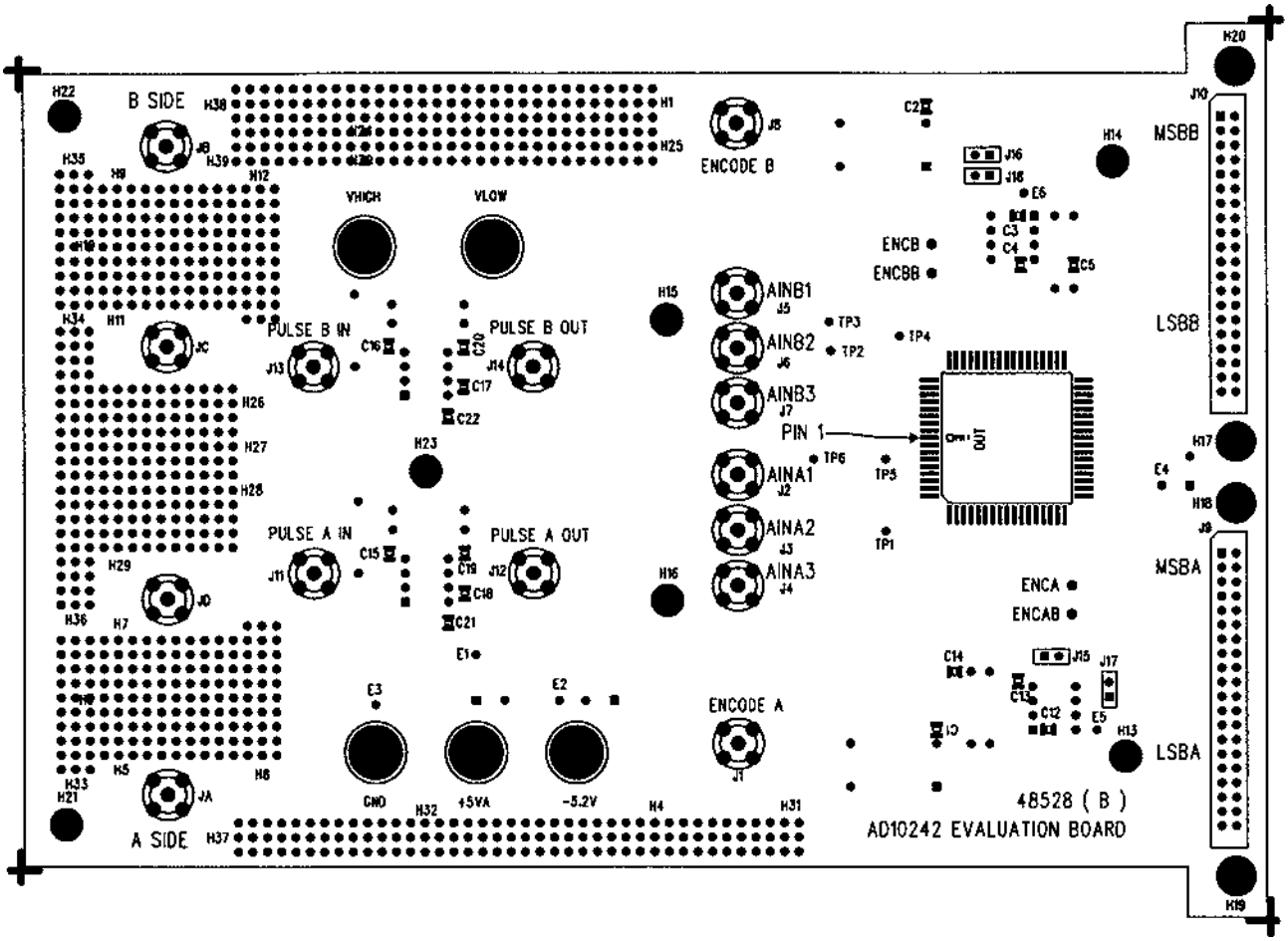
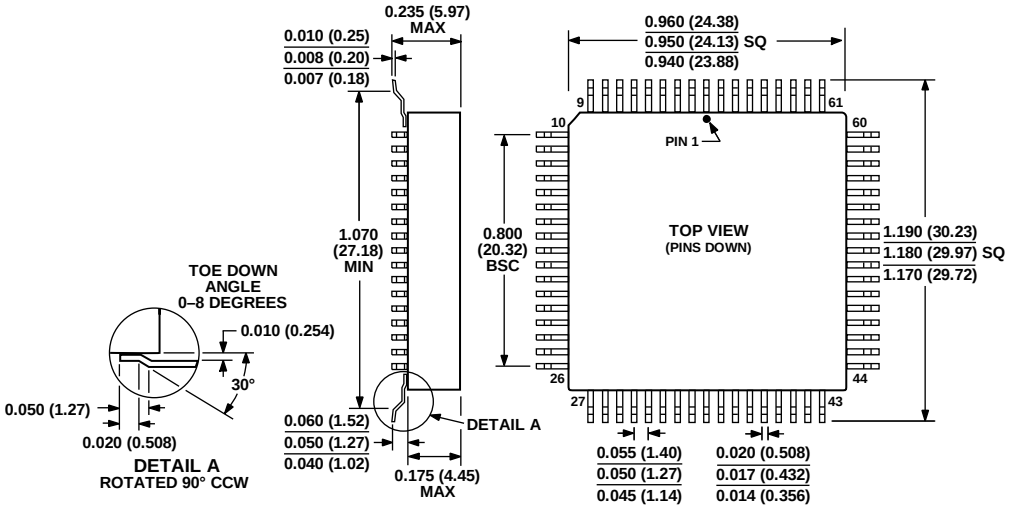


Figure 16. Evaluation Board Mechanical Layout

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

012908A

Figure 17. 68-Lead Ceramic Leaded Chip Carrier [CLCC]
(ES-68-1)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD10242BZ	–40°C to +85°C	68-Lead Ceramic Leaded Chip Carrier [CLCC]	ES-68-1
AD10242TZ	–55°C to +125°C	68-Lead Ceramic Leaded Chip Carrier [CLCC]	ES-68-1
AD10242TZ/883B	–55°C to +125°C	68-Lead Ceramic Leaded Chip Carrier [CLCC]	ES-68-1
5962-9581501HXA	–55°C to +125°C	68-Lead Ceramic Leaded Chip Carrier [CLCC]	ES-68-1

REVISION HISTORY

6/15—Rev. C to Rev. D

Change to Note 2 4
Updated Outline Dimensions 15
Changes to Ordering Guide 15

1/03—Rev. B to Rev. C

Changes to Functional Block Diagram 1
Changes to Table I 4
Changes to Pin Function Descriptions 5
Change to Encoding the AD10242 Section 10
Updated Outline Dimensions 15

6/01—Rev. A to Rev. B

AD9631 References Changed to AD9632 ..... Universal