encapsulations. The VSC8488-15 is a full dual-channel device, and the VSC8487-15 includes one serial port routed to one or both of the XAUI interfaces using the integrated crosspoint.

IEEE1588v2 timing integrated in the PHY is the quickest, lowest cost method of implementing the timing accuracy that is critical to maintaining existing timing-critical capabilities during the migration from TDM to packet-based architectures. Both devices support 1-step and 2-step PTP frames for ordinary clock, boundary clock, and transparent clock applications along with complete 1731 OAM performance monitoring capabilities.

The VSC8487-15 and VSC8488-15 devices integrate Microchip's world-class electronic dispersion compensation (EDC) performance across multiple data rates and applications including 10.3 Gbps Ethernet (GbE), 9.95 Gbps WAN traffic, and 10.5 Gbps SAN traffic. The devices also meet the SFP+ SR/LR host requirements in accordance with the SFF8431 specifications. The VSC8487-15 and VSC8488-15 devices compensate for optical impairments in SFP+ QSFP+ applications, along with degradations of the PCB, while providing wide system margin for SR and LR applications.

The VSC8487-15 and VSC8488-15 devices provide full KR support, including KR state machine, for autonegotiation and link optimization. The transmit path incorporates a multitap output driver to provide flexibility to meet the demanding 10GBASE-KR (IEEE 802.3ap) Tx output launch requirements.

A complete suite of BIST functionality includes line and client loopbacks along with pattern generation and error detection. Highly flexible clocking options support LAN and WAN operation using single or multiple, 1/64 or 1/66 REFCLK rate inputs, along with seamless Synchronous Ethernet support. The VSC8487-15 and VSC8488-15 devices include a failover switching capability for protection routing, along with selectable lane ordering.

Additional Features

- IEEE 1588v2 compliant
- Failover switching and lane ordering
- XAUI support
- SFP+ I/O with KR support
- 1 GbE support