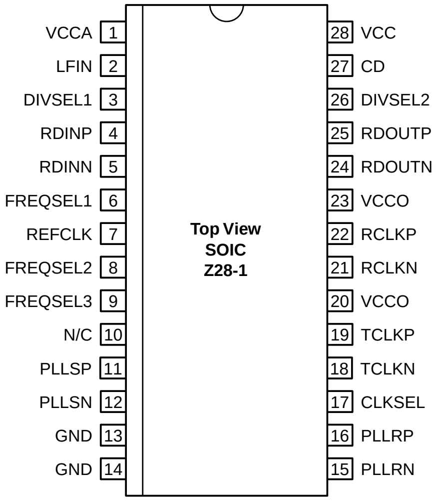
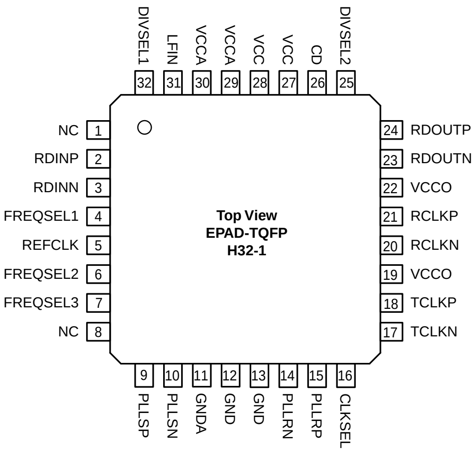
PACKAGE/ORDERING INFORMATION



28-Pin SOIC (Z28-1)



32-Pin EPAD TQFP (H32-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY87701VZC(3, 4)	Z28-1	Commercial	SY87701VZC	Sn-Pb
SY87701VZCTR(2, 3, 4)	Z28-1	Commercial	SY87701VZC	Sn-Pb
SY87701VHC(3)	H32-1	Commercial	SY87701VHC	Sn-Pb
SY87701VHCTR(2, 3)	H32-1	Commercial	SY87701VHC	Sn-Pb
SY87701VZH(3, 4)	Z28-1	Commercial	SY87701VZH with Pb-Free bar line indicator	NiPdAu Pb-Free
SY87701VZHTR(2, 3, 4)	Z28-1	Commercial	SY87701VZH with Pb-Free bar line indicator	NiPdAu Pb-Free
SY87701VHH(3)	H32-1	Commercial	SY87701VHH with Pb-Free bar line indicator	NiPdAu Pb-Free
SY87701VHHTR(2, 3)	H32-1	Commercial	SY87701VHH with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.
4. For optimum reliability, care should be taken when using the Z28-1 SOIC package to maintain the package case temperature at or below 70°C.

PIN DESCRIPTIONS

INPUTS

RDINP, RDINN [Serial Data Input] Differential PECL.

These built-in line receiver inputs are connected to the differential receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information. The incoming data rate can be within one of eight frequency ranges depending on the state of the FREQSEL pins. See "Frequency Selection" Table.

REFCLK [Reference Clock] TTL Input.

This input is used as the reference for the internal frequency synthesizer and the "training" frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN inputs.

CD [Carrier Detect] PECL Input.

This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW the data on the inputs RDIN will be internally forced to a constant LOW, the data outputs RDOUT will remain LOW, the Link Fault Indicator output LFIN forced LOW and the clock recovery PLL forced to lock onto the clock frequency generated from REFCLK.

FREQSEL1, ..., FREQSEL3 [Frequency Select] TTL Inputs.

These inputs select the output clock frequency range as shown in the *"Frequency Selection"* Table.

DIVSEL1, DIVSEL2 [Divider Select] TTL Inputs.

These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in the *"Reference Frequency Selection"* Table.

CLKSEL [Clock Select] TTL Input.

This input is used to select either the recovered clock of the receiver PLL (CLKSEL = HIGH) or the clock of the frequency synthesizer (CLKSEL = LOW) to the TCLK outputs.

OUTPUTS

LFIN [Link Fault Indicator] TTL Output.

This output indicates the status of the input data stream RDIN. Active HIGH signal is indicating when the internal clock recovery PLL has locked onto the incoming data stream. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (1000ppm). LFIN is an asynchronous output.

RDOUTP, RDOUTN [Receive Data Output] Differential PECL.

These ECL 100K outputs (+3.3V or +5V referenced) represent the recovered data from the input data stream (RDIN). This recovered data is sampled on the rising edge of RCLK.

RCLKP, RCLKN [Clock Output] Differential PECL.

These ECL 100K outputs (+3.3V or +5V referenced) represent the recovered clock used to sample the recovered data (RDOUT).

TCLKP, TCLKN [Clock Output] Differential PECL.

These ECL 100K outputs (+3.3V or +5V referenced) represent either the recovered clock (CLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (CLKSEL = LOW).

PLLSP, PLLSN [Clock Synthesis PLL Loop Filter]

External loop filter pins for the clock synthesis PLL.

PLLRP, PLLRN [Clock Recovery PLL Loop Filter]

External loop filter pins for the receiver PLL.

POWER & GROUND

V_{CC}	Supply Voltage(Note 1)
V_{CCA}	Analog Supply Voltage(Note 1)
V_{CCO}	Output Supply Voltage(Note 1)
GND	Ground
N/C	No Connect

Note 1. V_{CC}, V_{CCA}, V_{CCO} must be the same value.

FUNCTIONAL DESCRIPTION

Clock Recovery

Clock Recovery, as shown in the block diagram generates a clock that is at the same frequency as the incoming data bit rate at the Serial Data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency detector. Output pulses from the detector indicate the required direction of phase correction. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the Frequency of the incoming signal varies by greater than approximately 1000ppm with respect to the synthesizer frequency, the PLL will be declared out of lock, and the PLL will lock to the reference clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a 30µs data stream of continuous 1's or 0's for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL provides jitter tolerance which is better than the specified tolerance in GR-253-CORE.

Lock Detect

The SY87701V contains a link fault indication circuit which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than approximately 1000ppm, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within approximately 1000ppm, the PLL will be declared in lock and the lock detect output will go active.

CHARACTERISTICS

Performance

The SY87701V PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used with differential inputs and outputs.

Input Jitter Tolerance

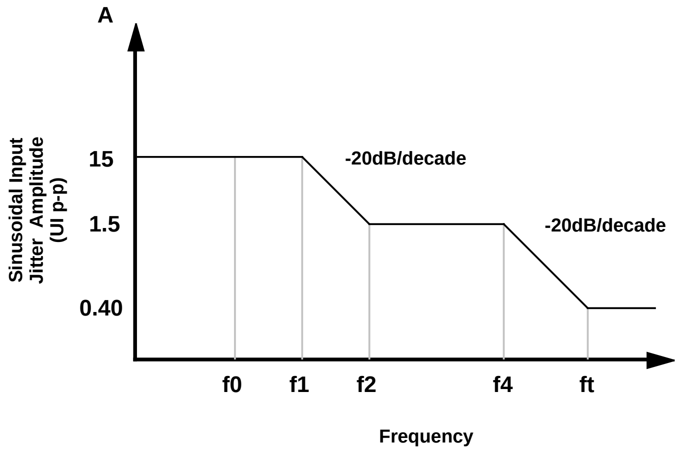
Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1dB optical/electrical power penalty. SONET input jitter tolerance requirement condition is the input jitter amplitude which causes an equivalent of 1dB power penalty.

Jitter Transfer

Jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 2.

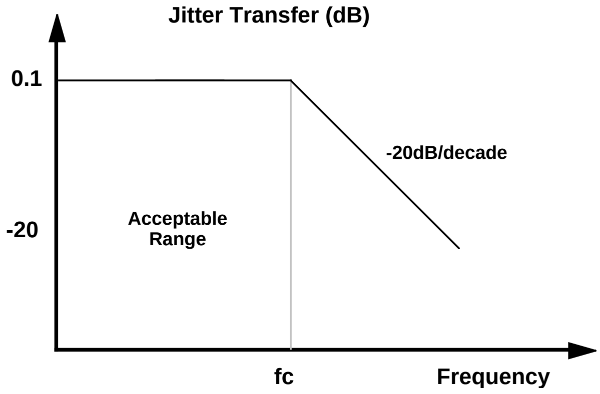
Jitter Generation

The jitter of the serial clock and serial data outputs shall not exceed .01 U.I. rms when a serial data input with no jitter is presented to the serial data inputs.



OC/STS-N Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
3	10	30	300	6.5	65
12	10	30	300	25	250

Figure 1. Input Jitter Tolerance



OC/STS-N Level	fc (kHz)	P (dB)
3	130	0.1
12	225	0.1

Figure 2. Jitter Transfer

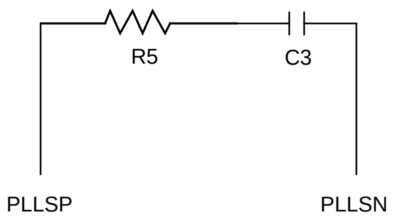
FREQUENCY SELECTION TABLE

FREQSEL1	FREQSEL2	FREQSEL3	f_{VCO}/f_{RCLK}	f_{RCLK} Data Rates (Mbps)
0	0	0	1	750 – 1250
0	0	1	2	375 – 625
0	1	0	4	188 – 313
0	1	1	6	125 – 208
1	0	0	8	94 – 157
1	0	1	12	63 – 104
1	1	0	16	47 – 78
1	1	1	24	32 – 52

REFERENCE FREQUENCY SELECTION

DIVSEL1	DIVSEL2	f_{RCLK}/f_{REFCLK}
0	0	8
0	1	10
1	0	16
1	1	20

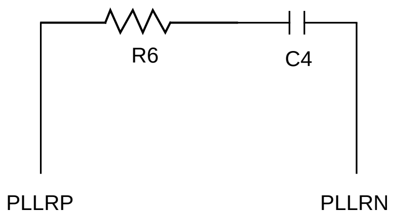
LOOP FILTER COMPONENTS[Note 1]



Wide Range

R5 = 350Ω

C3 = 1.0µF (X7R Dielectric)



Wide Range

R6 = 680Ω

C4 = 1.0µF (X7R Dielectric)

Note 1. Suggested Values. Values may vary for different applications.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_{IN}	Input Voltage	–0.5 to V_{CC}	V
I_{OUT}	Output Current – Continuous – Surge	 50 100	mA
T_{store}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +85	°C
T_C	Case Temperature	0 to +70	°C

Note 1. Permanent device damage may occur if *“Absolute Maximum Ratings”* are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to *“Absolute Maximum Ratings”* conditions for extended periods may affect device reliability.

PACKAGE THERMAL DATA[1]

θ_{JA} (°C/W) by Velocity (LFPM)

Package[1, 2]	0	200	500
28-Pin SOIC[1, 2]	80	—	—
32-Pin EPAD-TQFP[3]	27.6	22.6	20.7

Note 1. Case temperature not to exceed 70°C recommended for 28-pin SOIC.

Note 2. 28-pin SOIC package is NOT recommended for new designs.

Note 3. Using JEDEC standard test boards with die attach pad soldered to PCB. See www.amkor.com for additional package details.

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5% or 5.0V ±5%, T_A = 0°C to + 85°C for 32-TQFP, T_C = 0°C to 70°C for SOIC.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{CC}	Power Supply Voltage	3.15 4.75	3.3 5.0	3.45 5.25	V V	
I_{CC}	Power Supply Current	—	170	230	mA	

PECL 100K DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5% or 5.0V ±5%; T_A = 0°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	V_{CC} –1.165	—	V_{CC} –0.880	V	
V_{IL}	Input LOW Voltage	V_{CC} –1.810	—	V_{CC} –1.475	V	
V_{OH}	Output HIGH Voltage	V_{CC} –1.075	—	V_{CC} –0.830	V	50Ω to V_{CC} –2V
V_{OL}	Output LOW Voltage	V_{CC} –1.860	—	V_{CC} –1.570	V	50Ω to V_{CC} –2V
I_{IL}	Input LOW Current	0.5	—	—	µA	$V_{IN} = V_{IL}$(Min.)

TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5% or 5.0V ±5%; T_A = 0°C to + 85°C for 32-TQFP, T_C = 0°C to 70°C for SOIC.

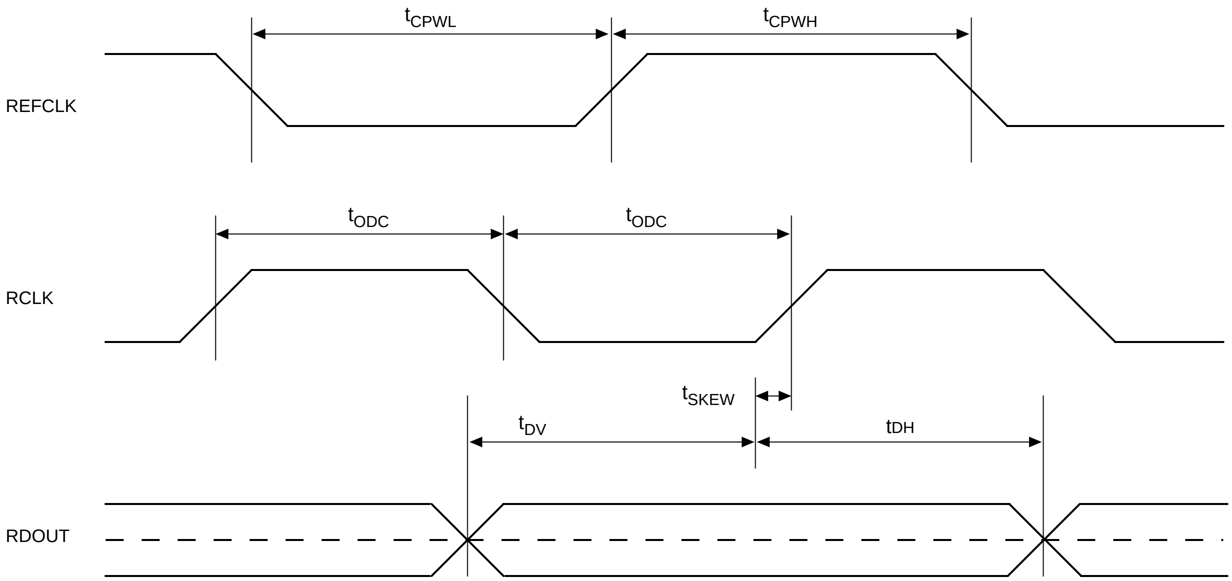
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0	—	V_{CC}	V	
V_{IL}	Input LOW Voltage	—	—	0.8	V	
V_{OH}	Output HIGH Voltage	2.0	—	—	V	I_{OH} = –0.4mA
V_{OL}	Output LOW Voltage	—	—	0.5	V	I_{OL} = 4mA
I_{IH}	Input HIGH Current	–175 —	— —	— +100	µA µA	V_{IN} = 2.7V, V_{CC} = Max. $V_{IN} = V_{CC}$, V_{CC} = Max.
I_{IL}	Input LOW Current	–300	—	—	µA	V_{IN} = 0.5V, V_{CC} = Max.
I_{OS}	Output Short Circuit Current	15	—	100	mA	V_{OUT} = 0V (maximum 1sec)

AC ELECTRICAL CHARACTERISTICS

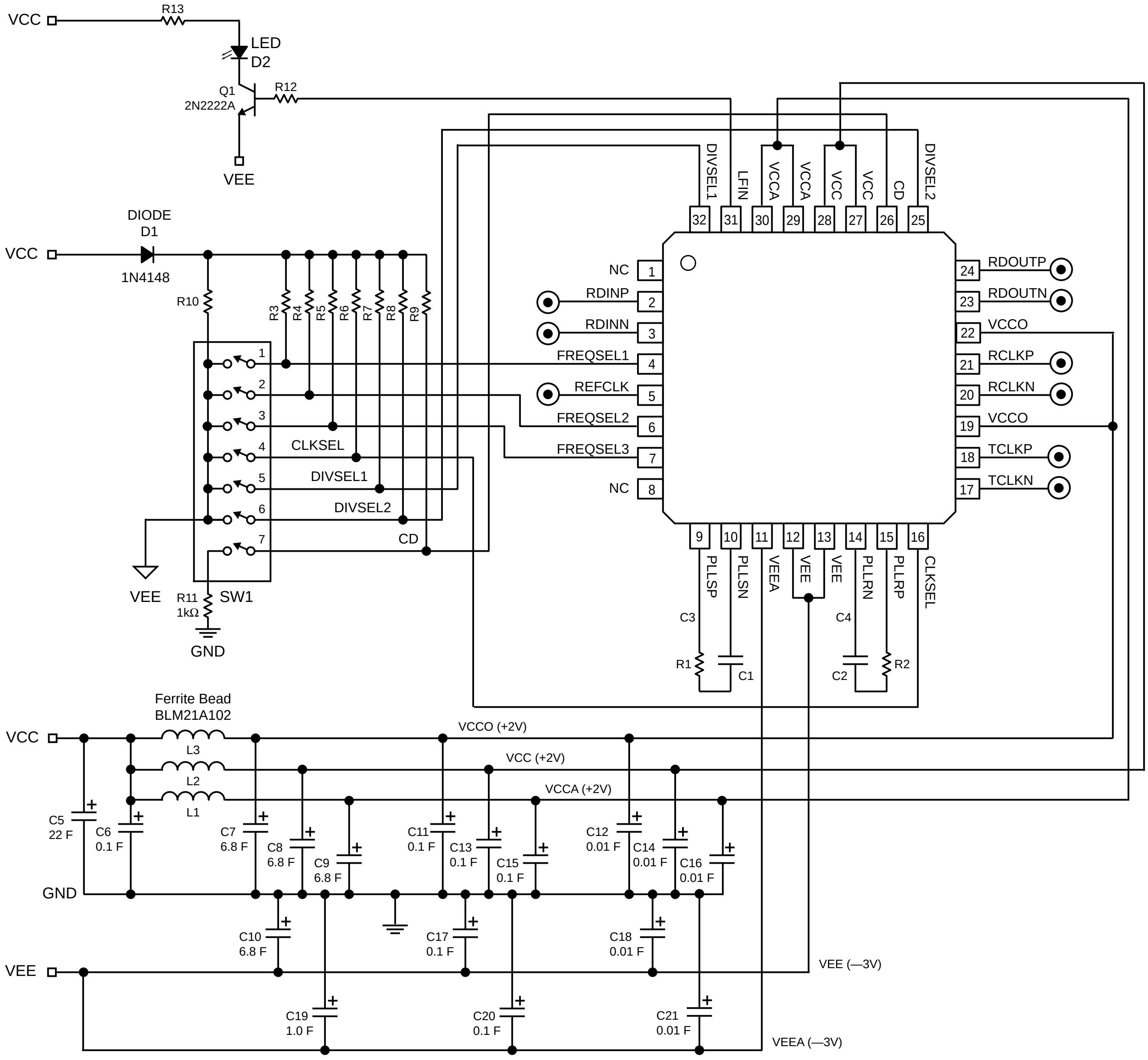
$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5% or 5.0V ±5%; T_A = 0°C to + 85°C for 32-TQFP, T_C = 0°C to 70°C for SOIC.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
f_{VCO}	VCO Center Frequency	750	—	1250	MHz	f_{REFCLK} × Byte Rate
Δf_{VCO}	VCO Center Frequency Tolerance	—	5	—	%	Nominal
t_{ACQ}	Acquisition Lock Time	—	—	15	µs	
t_{CPWH}	REFCLK Pulse Width HIGH	4	—	—	ns	
t_{CPWL}	REFCLK Pulse Width LOW	4	—	—	ns	
t_{ir}	REFCLK Input Rise Time	—	0.5	2	ns	
t_{ODC}	Output Duty Cycle (RCLK/TCLK)	45	—	55	% of UI	
t_r t_f	ECL Output Rise/Fall Time (20% to 80%)	100	—	500	ps	50Ω to V_{CC} –2
t_{SKEW}	Recovered Clock Skew	–200	—	+200	ps	
t_{DV}	Data Valid	$1/(2 \times f_{RCLK}) - 200$	—	—	ps	
t_{DH}	Data Hold	$1/(2 \times f_{RCLK}) - 200$	—	—	ps	

TIMING WAVEFORMS



32-PIN APPLICATION EXAMPLE

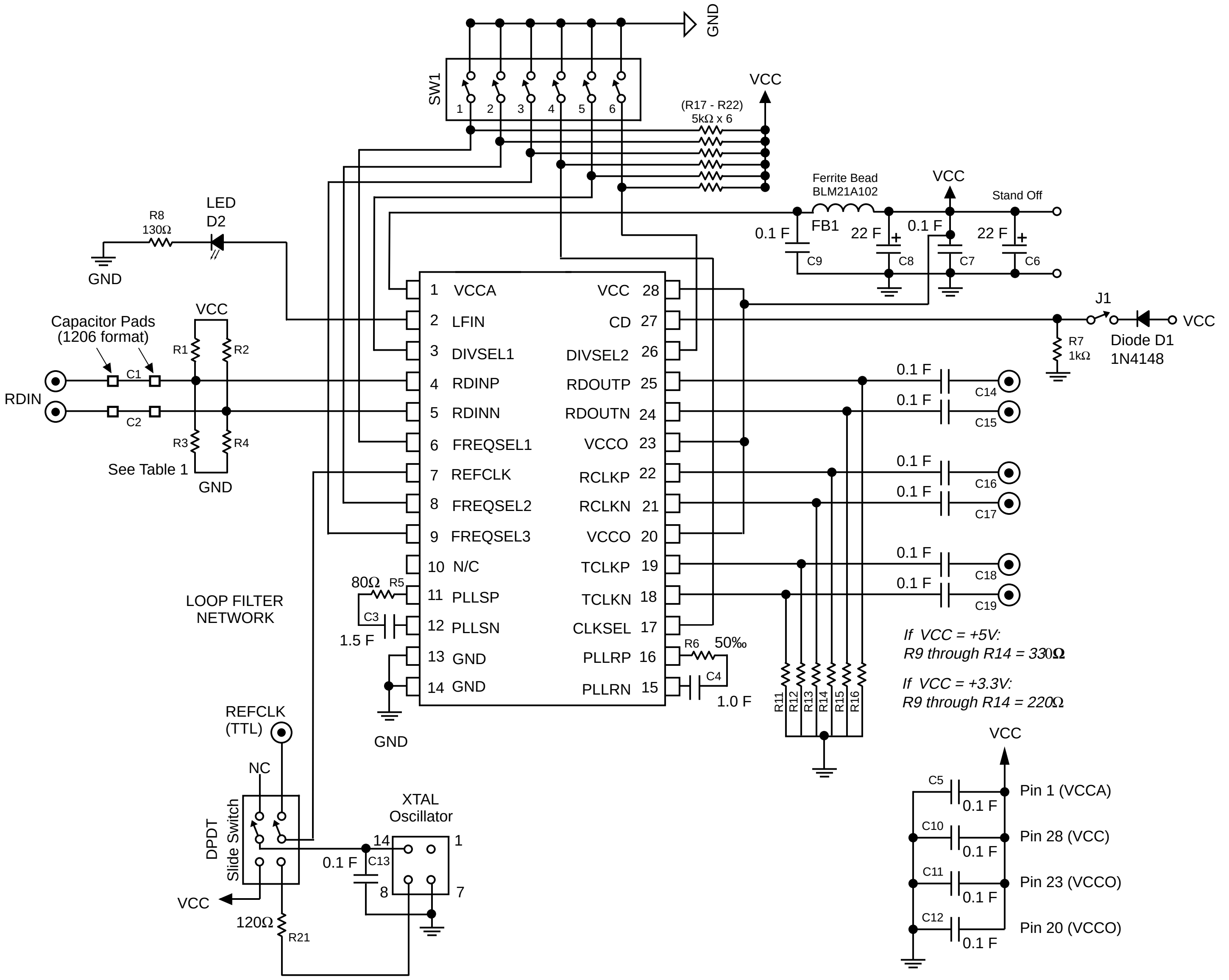


Note:

C3, C4 are optional

C1 = C2 = 1.0µF
R1 = 350Ω
R2 = 680Ω
R3 through R10 = 5kΩ
R12 = 12kΩ
R13 = 130Ω

28-PIN APPLICATION EXAMPLE



Note 1. C5 and C10–C12 are decoupling capacitors and should be kept as close to the power pins as possible.

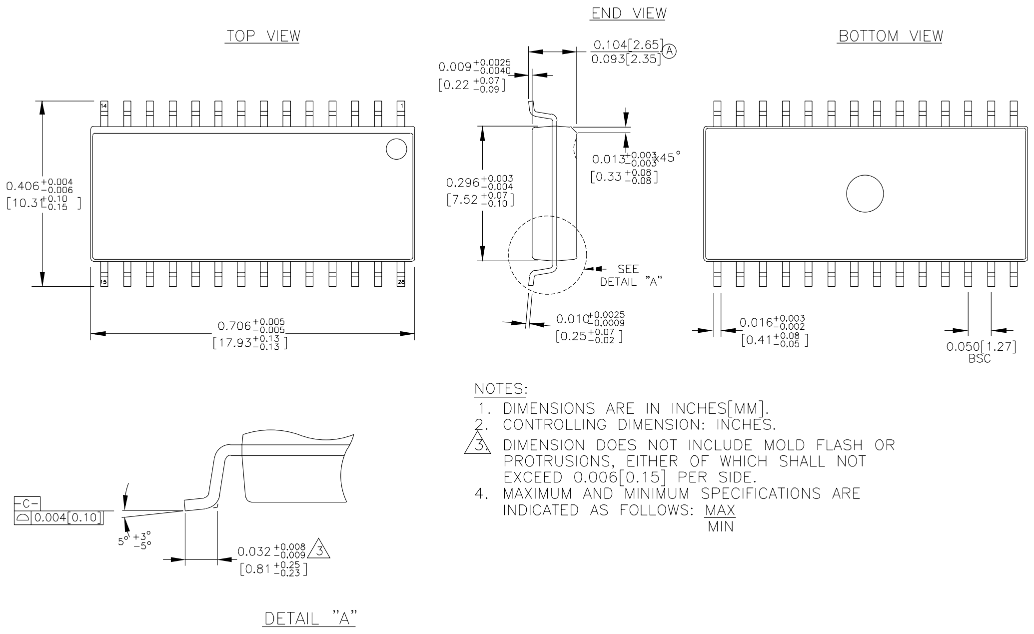
For AC-Coupling Only		For DC Mode Only	
when VCC = +5V	*when VCC = +3.3V*	*when VCC = +5V*	*when VCC = +3.3V*
C1 = C2 = 0.1µF	C1 = C2 = 0.1µF	C1 = C2 = Shorted	C1 = C2 = Shorted
R1 = R2 = 1.2kΩ	R1 = R2 = 680Ω	R1 = R2 = 82Ω	R1 = R2 = 130Ω
R3 = R4 = 3.4kΩ	R3 = R4 = 1kΩ	R3 = R4 = 130Ω	R3 = R4 = 82Ω

Table 1.

BILL OF MATERIALS (32-PIN EPAD-TQFP)

Item	Part Number	Manufacturer	Description	Qty.
C1, C2	VJ0603Y105JXJAT	Vishay	1.0µF Ceramic Capacitor, Size 0603 X7R Dielectric, Loop Filter, Critical	2
C3, C4	VJ0603Y105JXJAT	Vishay	1.0µF Ceramic Capacitor, Size 0603 X7R Dielectric, Loop Filter, Optional	2
C5	ECS-T1ED226R	Panasonic	22µF Tantalum Electrolytic Capacitor, Size D	1
C6	ECU-V1H104KBW	Panasonic	0.1µF Ceramic Capacitor, Size 1206 X7R Dielectric, Power Supply Decoupling	1
C7, C8, C9, C10	ECS-T1EC685R	Panasonic	6.8µF Tantalum Electrolytic Capacitor, Size C	4
C19	ECJ-3YB1E105K	Panasonic	1.0µF Ceramic Capacitor, Size 1206 X7R Dielectric, VEEA Decoupling	1
C11, C13	ECU-V1H104KBW	Panasonic	0.1µF Ceramic Capacitor, Size 1206 X7R Dielectric, VCCO/VCC Decoupling	1
C15, C17	ECU-V1H104KBW	Panasonic	0.1µF Ceramic Capacitor, Size 1206 X7R Dielectric, VCCA/VEEA Decoupling	1
C20	ECU-V1H104KBW	Panasonic	0.1µF Ceramic Capacitor, Size 1206 X7R Dielectric, VEEA Decoupling	1
C12, C14	ECU-V1H103KBW	Panasonic	0.01µF Ceramic Capacitor, Size 1206 X7R Dielectric, VCCO/VCC Decoupling	1
C16, C18	ECU-V1H103KBW	Panasonic	0.01µF Ceramic Capacitor, Size 1206 X7R Dielectric, VCCA/VEEA Decoupling	1
C21	ECU-V1H103KBW	Panasonic	0.01µF Ceramic Capacitor, Size 1206 X7R Dielectric, VEEA Decoupling	1
D1	1N4148		Diode	1
D2	P300-ND/P301-ND	Panasonic	T-1 3/4 Red LED	1
J1, J2, J3, J4, J5 J6, J7, J8, J9, J10, J11, J12	142-0701-851	Johnson Components	Gold Plated, Jack, SMA, PCB Mount	12
L1, L2, L3	BLM21A102F	Murata	Ferrite Beads, Power Noise Suppression	3
Q1	NTE123A	NTE	2N2222A Buffer/Driver Transistor, NPN	1
R1			350Ω Resistor, 2%, Size 0402 Loop Filter Component, Critical	1
R2			680Ω Resistor, 2%, Size 0402 Loop Filter Component, Critical	1
R3, R4, R5, R6 R7, R8, R9, R10			5kΩ Pullup Resistors, 2%, Size 1206	8
R11			1kΩ Pulldown Resistor, 2%, Size 1206	1
R12			12kΩ Resistor, 2%, Size 1206	1
R13			130Ω Pullup Resistor, 2%, Size 1206	1
SW1	206-7	CTS	SPST, Gold Finish, Sealed Dip Switch	1

28 LEAD SOIC .300" WIDE (Z28-1)



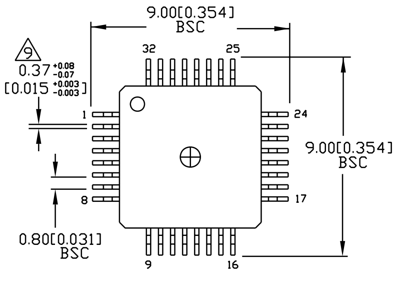
NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN

Rev. 02

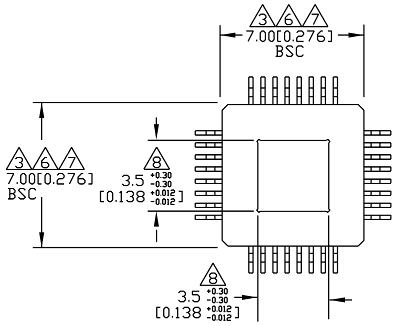
Note:

The 28 Lead SOIC package is NOT recommended for new designs.

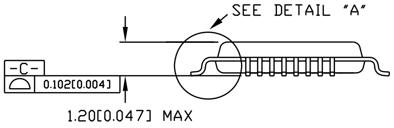
32 LEAD EPAD TQFP (DIE UP) (H32-1)



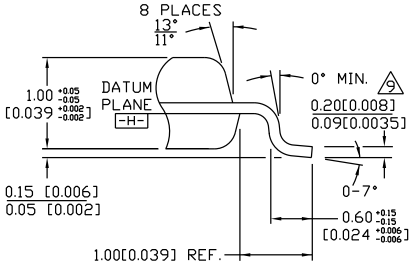
TOP VIEW



BOTTOM VIEW



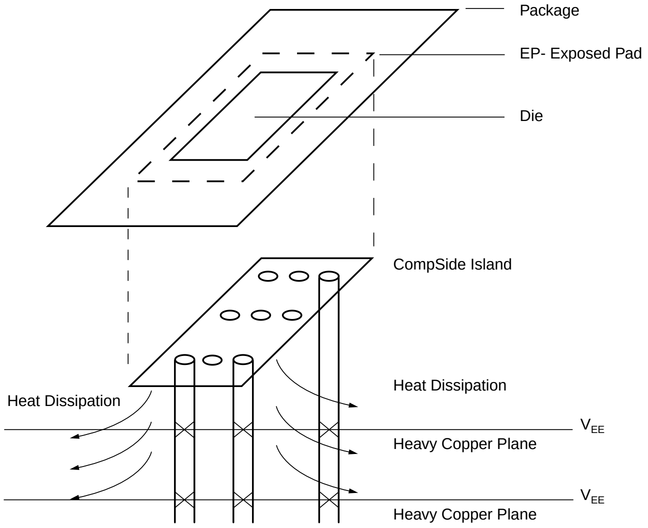
SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. △3 DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. △6 THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. △7 PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. △8 EXPOSED PAD SHALL BE COPLANAR WITH PACKAGE BOTTOM WITHIN 0.05mm EXPOSED PAD: Cu WITH Sn/Pb PLATING
9. △9 DIMENSION INCLUDES LEAD FINISH.



PCB Thermal Consideration for 32-Pin EPAD-TQFP Package

APPENDIX A

Layout and General Suggestions

1. Establish controlled impedance stripline, microstrip, or co-planar construction techniques.
2. Signal paths should have, approximately, the same width as the device pads.
3. All differential paths are critical timing paths, where skew should be matched to within ±10ps.
4. Signal trace impedance should not vary more than ±5%. If in doubt, perform TDR analysis of all high-speed signal traces.
5. Maintain compact filter networks as close to filter pins as possible. Provide ground plane relief under filter path to reduce stray capacitance. Be careful of crosstalk coupling into the filter network.
6. Maintain low jitter on the REFCLK input. Isolate the XTAL oscillator from power supply noise by adequately decoupling. Keep XTAL oscillator close to device, and minimize capacitive coupling from adjacent signals.
7. Higher speed operation may require use of fundamental-tone (third-overtone typically have more jitter) crystal based oscillator for optimum performance. Evaluate and compare candidates by measuring TXCLK jitter.
8. All unused outputs must be terminated. To conserve power, unused PECL outputs can be terminated with a 1kΩ resistor to V_{EE}.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com