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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	—	5.5	V
Interface Supply Voltage	V_{IO}		1.5	—	3.6	V
Digital Power Supply Powerup Rise Time	V_{DRISE}		10	—	—	µs
Interface Power Supply Powerup Rise Time	V_{IORISE}		10	—	—	µs
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_{DD}= 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 5.8	V
Interface Supply Voltage	V_{IO}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{IO} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{PK}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4704/05 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should be done only at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, DOUT, GPO1, GPO2, and GPO3.
4. At RF input pin, FMI.

Table 3. DC Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Receiver to Line Output						
V_{DD} Supply Current	I_{FM}	Analog Output Mode	—	19.2	22	mA
V_{DD} Supply Current[1]	I_{FM}	Analog Output Mode Low SNR level	—	19.8	23	mA
V_{DD} RDS Supply Current[2]	I_{FM}	Analog Output Mode	—	19.9	23	mA
V_{DD} Supply Current[2]	I_{FMD}	Digital Output Mode	—	18.0	20.5	mA
Supplies and Interface						
Interface Supply Current	I_{IO}		—	320	600	µA
V_{DD} Powerdown Current	I_{DDPD}		—	10	20	µA
V_{IO} Powerdown Current	I_{IOPD}	SCLK, RCLK inactive	—	1	10	µA
High Level Input Voltage[3]	V_{IH}		0.7 x V_{IO}	—	V_{IO} + 0.3	V
Low Level Input Voltage[3]	V_{IL}		–0.3	—	0.3 x V_{IO}	V
High Level Input Current[3]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
Low Level Input Current[3]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
High Level Output Voltage[4]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
Low Level Output Voltage[4]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V

Notes:

1. LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.
2. Guaranteed by characterization.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, DCLK, DFS, GPO1, GPO2, and GPO3.
4. For output pins SDIO, DOUT, GPO1, GPO2, and GPO3.

Table 4. Reset Timing Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{RST}$ Pulse Width and GPO1, GPO2/$\overline{INT}$ Setup to $\overline{RST}\uparrow$[4]	t_{SRST}	100	—	—	µs
GPO1, GPO2/$\overline{INT}$ Hold from $\overline{RST}\uparrow$	t_{HRST}	30	—	—	ns

Important Notes:

1. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
2. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
3. When selecting 3-wire or SPI modes, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.
4. If GPO1 and GPO2 are actively driven by the user, then minimum t_{SRST} is only 30 ns. If GPO1 or GPO2 is high impedance, then minimum t_{SRST} is 100 µs to provide time for on-chip 1 MΩ devices (active while $\overline{RST}$ is low) to pull GPO1 high and GPO2 low.

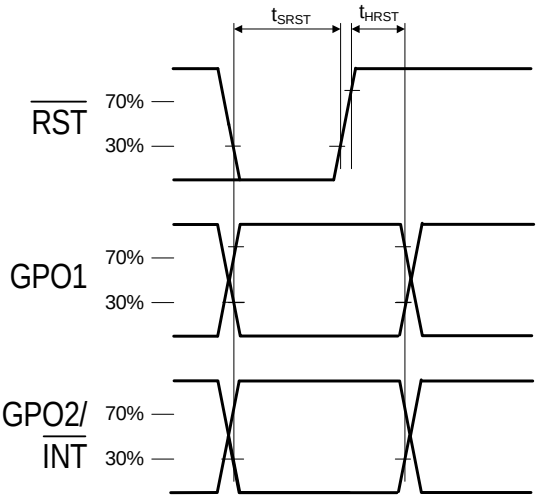


Figure 1. Reset Timing Parameters for Busmode Select

Table 5. 2-Wire Control Interface Characteristics[1,2,3]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold [4, 5]	$t_{HD:DAT}$		0	—	900	ns
SCLK Input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_b}{1pF}$	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		$20 + 0.1\frac{C_b}{1pF}$	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. When V_{IO} = 0 V, SCLK and SDIO are low impedance.
2. When selecting 2-wire mode, the user must ensure that a 2-wire start condition (falling edge of SDIO while SCLK is high) does not occur within 300 ns before the rising edge of $\overline{RST}$.
3. When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of $\overline{RST}$, and stays high until after the first start condition.
4. The Si4704/05 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the minimum $t_{HD:DAT}$ specification.
5. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 KHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

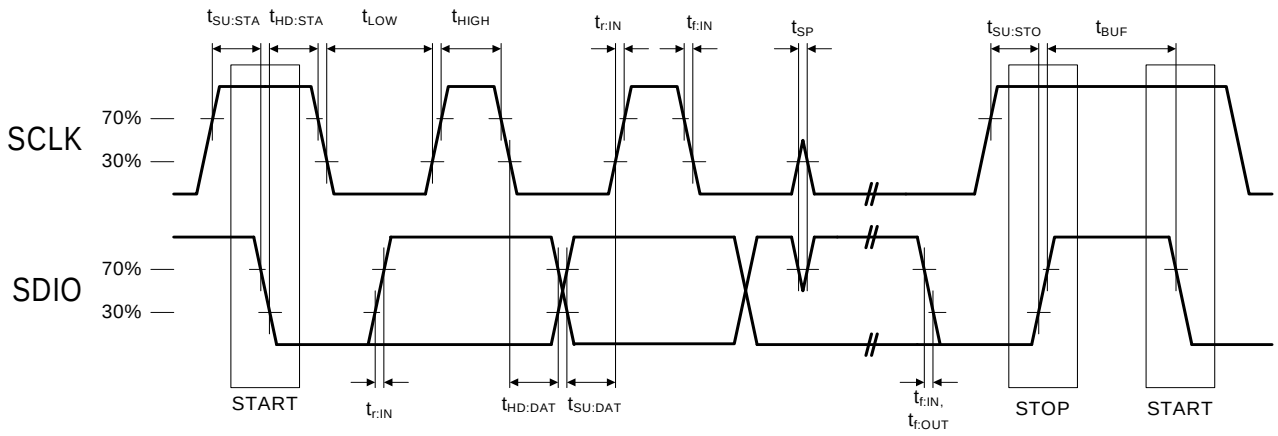


Figure 2. 2-Wire Control Interface Read and Write Timing Parameters

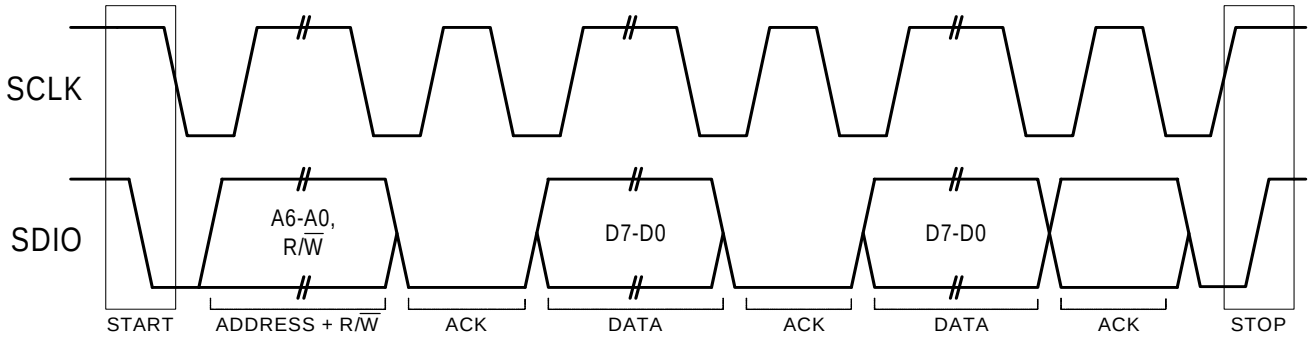


Figure 3. 2-Wire Control Interface Read and Write Timing Diagram

Table 6. 3-Wire Control Interface Characteristics

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK ↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK ↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK ↓ Hold	t_{HSEN}		10	—	—	ns
SCLK ↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK ↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall Time	t_R, t_F		—	—	10	ns

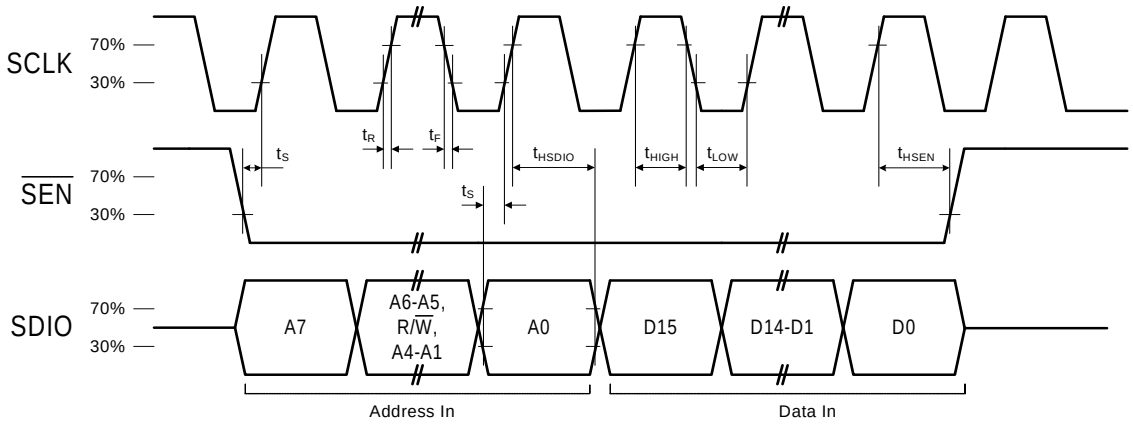


Figure 4. 3-Wire Control Interface Write Timing Parameters

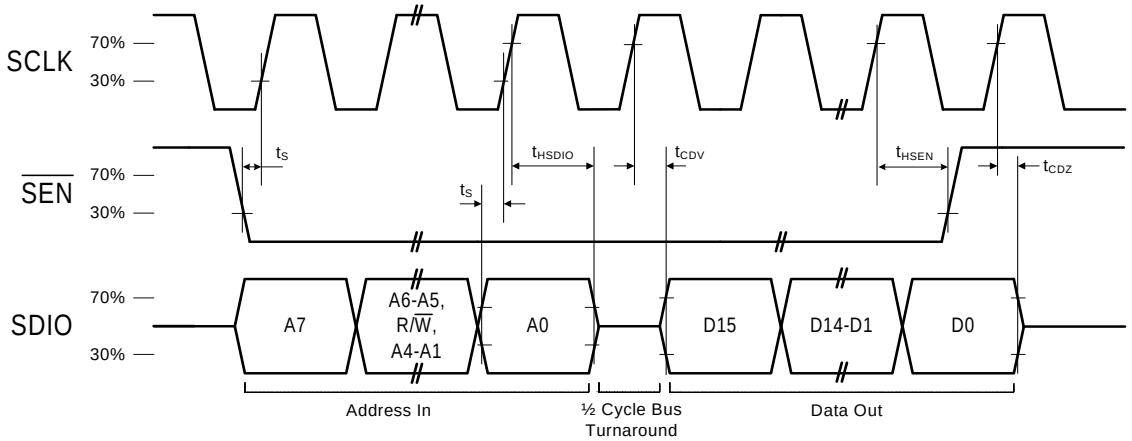


Figure 5. 3-Wire Control Interface Read Timing Parameters

Table 7. SPI Control Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK↑ Setup	t_S		15	—	—	ns
SDIO Input to SCLK↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK↓ Hold	t_{HSEN}		5	—	—	ns
SCLK↓ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK↓ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns
SCLK, $\overline{SEN}$, SDIO, Rise/Fall time	t_R t_F		—	—	10	ns

Note: When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of $\overline{RST}$.

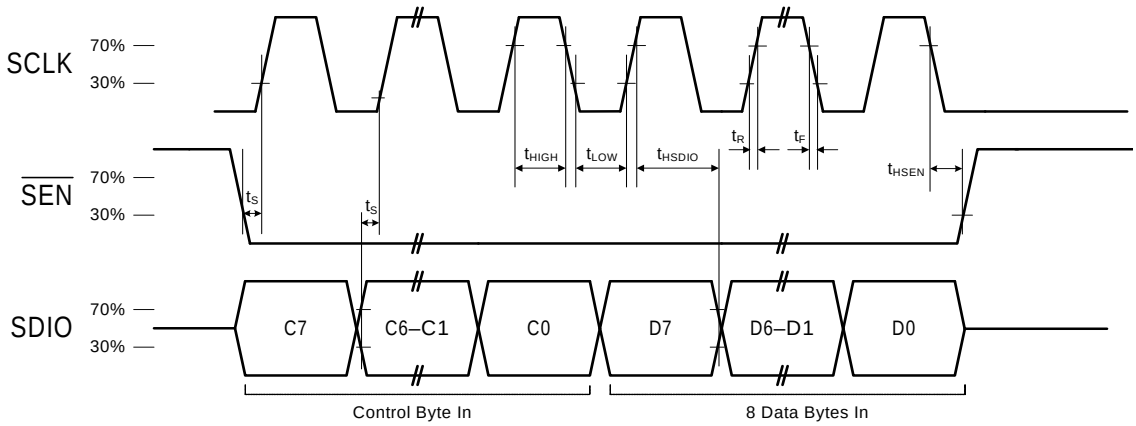


Figure 6. SPI Control Interface Write Timing Parameters

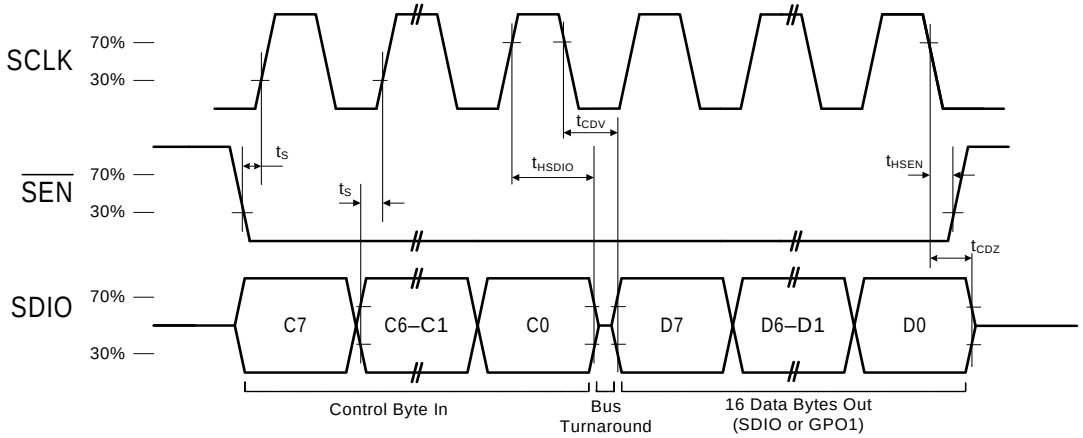


Figure 7. SPI Control Interface Read Timing Parameters

Table 8. Digital Audio Interface Characteristics
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Cycle Time	t_{DCT}		26	—	1000	ns
DCLK Pulse Width High	t_{DCH}		10	—	—	ns
DCLK Pulse Width Low	t_{DCL}		10	—	—	ns
DFS Set-up Time to DCLK Rising Edge	$t_{SU:DFS}$		5	—	—	ns
DFS Hold Time from DCLK Rising Edge	$t_{HD:DFS}$		5	—	—	ns
DOUT Propagation Delay from DCLK Falling Edge	$t_{PD:DOUT}$		0	—	12	ns

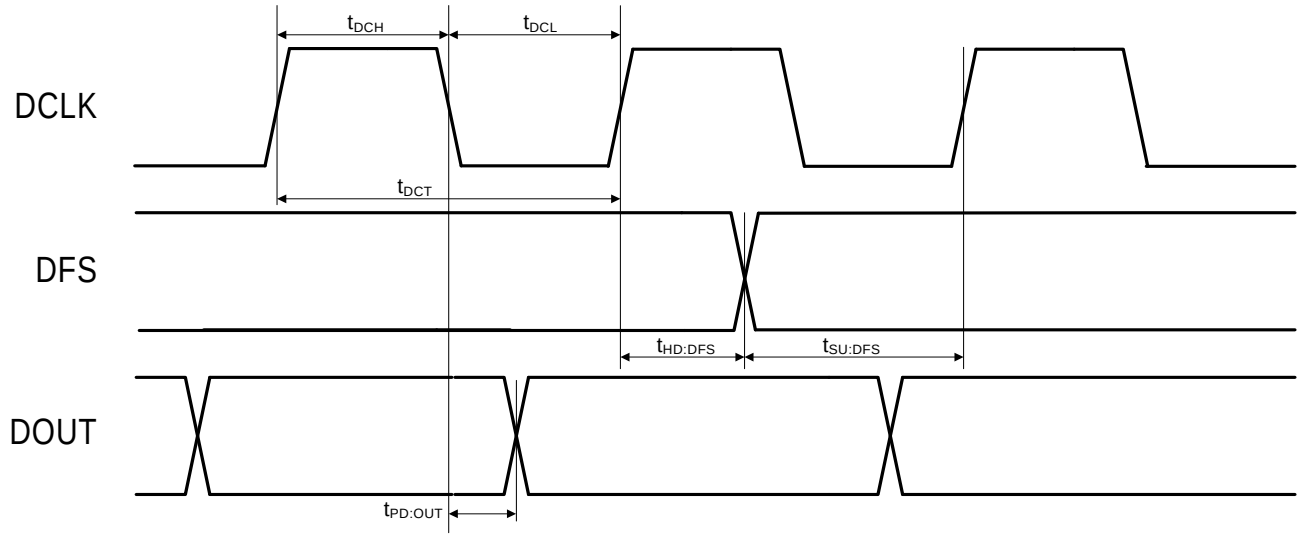


Figure 8. Digital Audio Interface Timing Parameters, I^2S Mode

Table 9. FM Receiver Characteristics[1,2]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency[3]	f_{RF}		76	—	108	MHz
Sensitivity with Headphone Network[4,5,6]		(S+N)/N = 26 dB	—	2.2	3.5	µV EMF
Sensitivity with 50 Ω Network[4,5,6,7]		(S+N)/N = 26 dB	—	1.1	—	µV EMF
RDS Sensitivity[7]		Δf = 2 kHz, RDS BLER < 5%	—	15	—	µV EMF
LPI Sensitivity[7]			—	3.5	—	µV EMF
LNA Input Resistance[7,8]			3	4	5	kΩ
LNA Input Capacitance[7,8]			4	5	6	pF
Input IP3[7,9]			100	105	—	dBµV EMF
AM Suppression[4,5,7,8]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[7]		In-band	35	—	—	dB
Audio Output Voltage[4,5,8]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[4,8,10]			—	—	1	dB
Audio Frequency Response Low[7]		–3 dB	—	—	30	Hz
Audio Frequency Response High[7]		–3 dB	15	—	—	kHz
Audio Stereo Separation[8,10]			25	—	—	dB
Audio Mono S/N[4,5,6,8,11]			55	63	—	dB
Audio Stereo S/N[5,6,8,11,12]			—	58	—	dB
Audio THD[4,8,10]			—	0.1	0.5	%
De-emphasis Time Constant[7]		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs

Notes:

1. Additional testing information is available in application note, “AN388: EVB Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. For frequency range 64–75.9 MHz, refer to Table 10.
4. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
5. Δf = 22.5 kHz.
6. B_{AF} = 300 Hz to 15 kHz, A-weighted.
7. Guaranteed by characterization.
8. V_{EMF} = 1 mV.
9. $|f_2 – f_1| > 2$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4704/05-GM" on page 30.
10. Δf = 75 kHz.
11. At L_{OUT} and R_{OUT} pins.
12. Analog audio output mode.
13. At temperature 25°C.

Table 9. FM Receiver Characteristics[1,2] (Continued)

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio Output Load Resistance[7,11]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[7,11]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[7]		RCLK tolerance = 100 ppm	—	—	80	ms/channel
Powerup Time[7]		From powerdown	—	—	110	ms
RSSI Offset[13]		Input levels of 8 and 60 dBµV at RF Input	–3	—	3	dB

Notes:

1. Additional testing information is available in application note, “AN388: EVB Test Procedure.” Volume = maximum for all tests. Tested at RF = 98.1 MHz.
2. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
3. For frequency range 64–75.9 MHz, refer to Table 10.
4. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
5. Δf = 22.5 kHz.
6. B_{AF} = 300 Hz to 15 kHz, A-weighted.
7. Guaranteed by characterization.
8. V_{EMF} = 1 mV.
9. $|f_2 - f_1| > 2$ MHz, $f_0 = 2 \times f_1 - f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4704/05-GM" on page 30.
10. Δf = 75 kHz.
11. At L_{OUT} and R_{OUT} pins.
12. Analog audio output mode.
13. At temperature 25°C.

Table 10. 64–75.9 MHz Input Frequency FM Receiver Characteristics[1]

(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		64	—	75.9	MHz
Sensitivity with Headphone Network[2,3,4,5]		(S+N)/N = 26 dB	—	4.0	—	µV EMF
LNA Input Resistance[5,6]			3	4	5	kΩ
LNA Input Capacitance[5,6]			4	5	6	pF
Input IP3[5,7]			100	105	—	dBµV EMF
AM Suppression[2,3,5,6]		m = 0.3	40	50	—	dB
Adjacent Channel Selectivity[5]		±200 kHz	—	50	—	dB
Alternate Channel Selectivity[5]		±400 kHz	—	70	—	dB
Audio Output Voltage[2,3,5,6]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[2,6,8]			—	—	1	dB
Audio Frequency Response Low[5]		–3 dB	—	—	30	Hz
Audio Frequency Response High[5]		–3 dB	15	—	—	kHz
Audio Mono S/N[2,3,4,5,6,9]			55	63	—	dB
Audio THD[2,5,6,8]			—	0.1	0.5	%
De-emphasis Time Constant		FM_DEEMPHASIS = 2	70	75	80	µs
		FM_DEEMPHASIS = 1	45	50	54	µs
Audio Common Mode Voltage[9]			0.7	0.8	0.9	V
Audio Output Load Resistance[5,9]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[5,9]	C_L	Single-ended	—	—	50	pF
Seek/Tune Time[5]		RCLK tolerance = 100 ppm	—	—	80	ms/channel
Powerup Time		From powerdown	—	—	110	ms
RSSI Offset		Input levels of 8 and 60 dBµV EMF	–3	—	3	dB

Notes:

1. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers. Tested at RF = 98.1 MHz.
2. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = enabled, and L = R unless noted otherwise.
3. Δf = 22.5 kHz.
4. B_{AF} = 300 Hz to 15 kHz, A-weighted.
5. Guaranteed by characterization.
6. V_{EMF} = 1 mV.
7. $|f_2 – f_1| > 2$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled. Refer to "7. Pin Descriptions: Si4704/05-GM" on page 30.
8. Δf = 75 kHz.
9. At LOUT and ROUT pins.

Table 11. Reference Clock and Crystal Characteristics

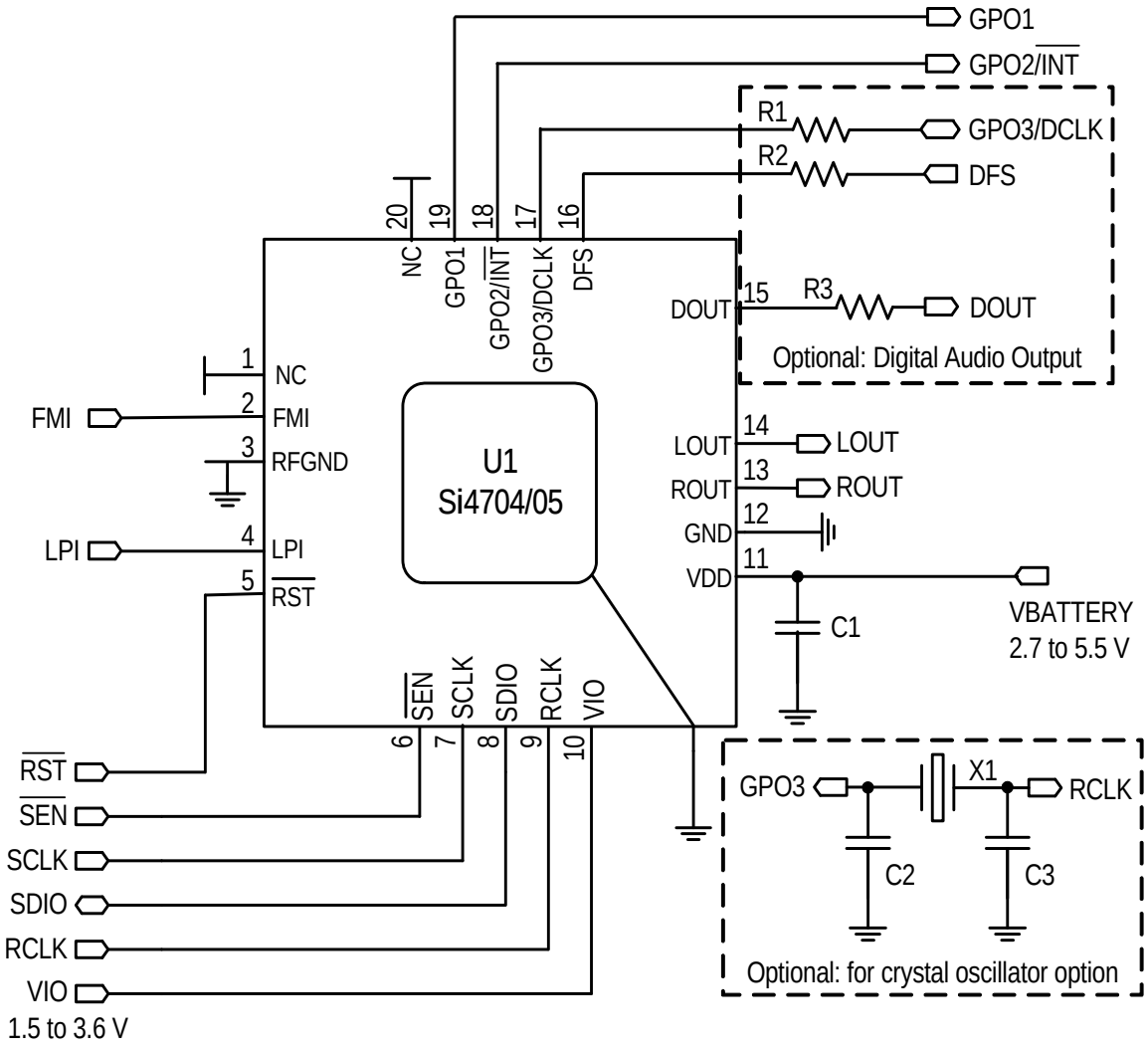
(V_{DD} = 2.7 to 5.5 V, V_{IO} = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock						
RCLK Supported Frequencies[1]			31.130	32.768	40,000	kHz
RCLK Frequency Tolerance[2]			–100	—	100	ppm
REFCLK_PRESCALE			1	—	4095	
REFCLK			31.130	32.768	34.406	kHz
Crystal Oscillator						
Crystal Oscillator Frequency			—	32.768	—	kHz
Crystal Frequency Tolerance[2]			–100	—	100	ppm
Board Capacitance			—	—	3.5	pF

Notes:

1. The Si4704/05 divides the RCLK input by REFCLK_PRESCALE to obtain REFCLK. There are some RCLK frequencies between 31.130 kHz and 40 MHz that are not supported. See “AN332: Universal Programming Guide,” Table 6 for more details.
2. A frequency tolerance of ±50 ppm is required for FM seek/tune using 50 kHz channel spacing.

2. Typical Application Schematic



Notes:

1. Place C1 close to V_{DD} pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 1 and 20 are no connects, leave floating.
4. To ensure proper operation and receiver performance, follow the guidelines in “AN383: Antenna Selection and Universal Layout Guidelines.” Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 or Pin 4 connects to the FM antenna interface. Pin 2 is for a headphone antenna. Pin 4 is for an integrated antenna.
6. RFGND should be locally isolated from GND.
7. Place Si4704/05 as close as possible to antenna jack and keep the FMI and LPI traces as short as possible.

3. Bill of Materials

Component(s)	Value/Description	Supplier
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
U1	Si4704/05 FM Radio Receiver	Silicon Laboratories
Optional Components		
C2, C3	Crystal load capacitors, 22 pF, ±5%, COG (Optional: for crystal oscillator option)	Venkel
X1	32.768 kHz crystal (Optional: for crystal oscillator option)	Epson
R1	Resistor, 2 kΩ (Optional: for digital audio)	Venkel
R2	Resistor, 2 kΩ (Optional: for digital audio)	Venkel
R3	Resistor, 600 Ω (Optional: for digital audio)	Venkel

4. Universal AM/FM RX/FM TX Application Schematic

Figure 9 shows an application schematic that supports the Si47xx family of 3 mm x 3 mm QFN products, including the Si4702/3/4/5 FM receivers, Si471x FM transmitters, Si472x FM transceivers, and Si473x AM/FM receivers.

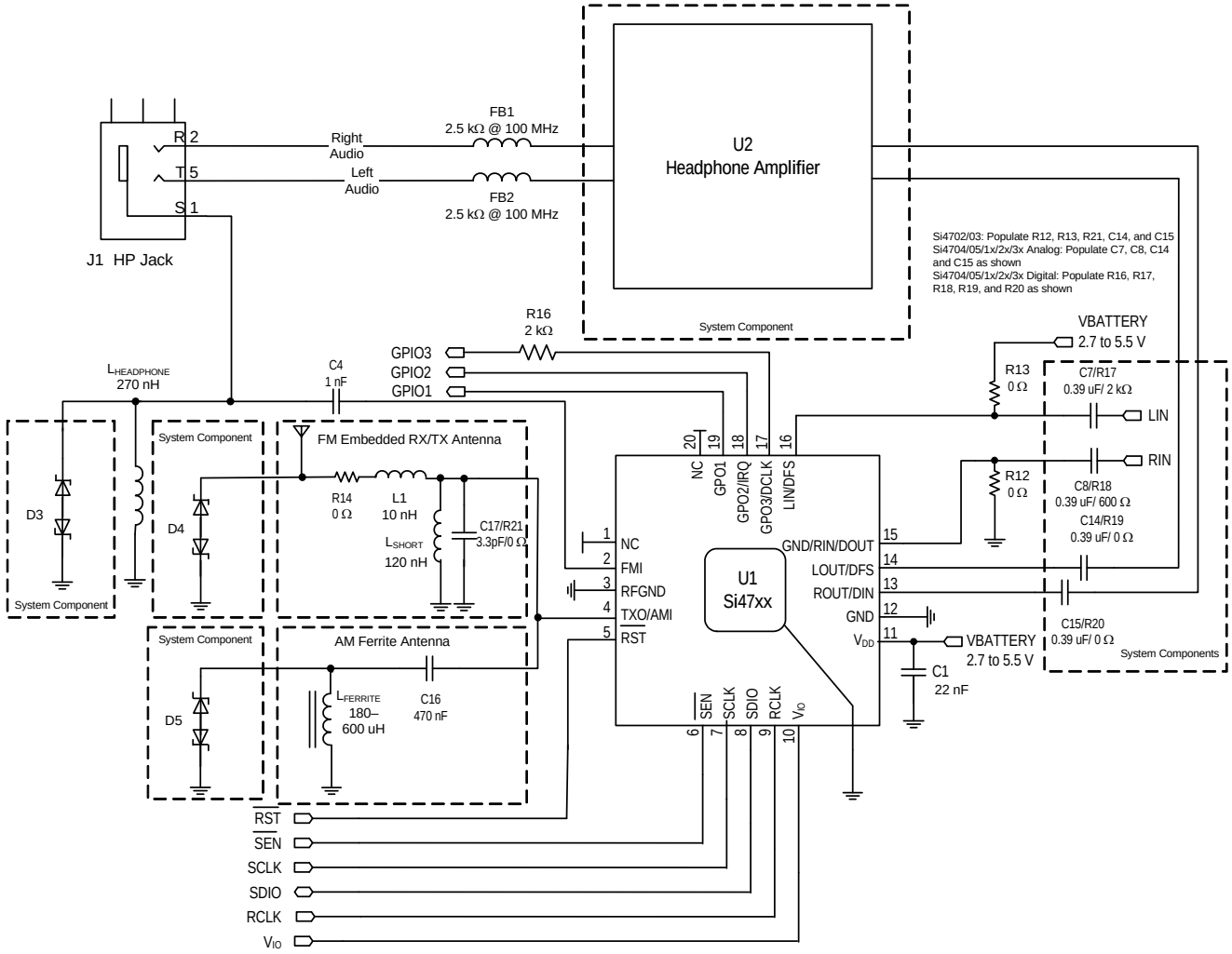


Figure 9. Universal AM/FM RX/FM TX Application Schematic

Following the schematic and layout recommendations detailed in “AN383: Universal Antenna Selection and Layout Guidelines” will result in optimal performance with the minimal application schematic shown in Figure 9, “Universal AM/FM RX/FM TX Application Schematic.” System components are those that are likely to be present for any tuner or transmitter design.

4.1. Universal AM/FM RX/FM TX Bill of Materials

The bill of materials for the expanded application schematic shown in Figure 9 is provided in Table 12. Refer to the individual device layout guides and antenna interface guides for a discussion of the purpose of each component.

Table 12. Universal AM/FM/RX/FM TX Bill of Materials

Designator	Description	Note
C1	Supply bypass capacitor, 22 nF, 10%, Z5U/X7R, 0402	
U1	Silicon Laboratories Si47xx, 3 mm x 3 mm, 20 pin, QFN	
R12, R13, R19, R20, R21	0 Ω jumper, 0402	R12, R13, and R21 for Si4702/03 only
C16	AM antenna ac coupling capacitor, 470 nF, 20%, Z5U/X7R	AM Ferrite Antenna
LFERRITE	AM Ferrite loop stick, 180–600 µH	AM Ferrite Antenna
FB1,FB2	Ferrite bead, 2.5 kΩ @ 100 MHZ, 0603, Murata BLM18BD252SN1D	Headphone Antenna
LHEADPHONE	Headphone antenna matching inductor, 270 nH, 0603, Q>15, Murata LQW18ANR27J00D	Headphone Antenna
LEMBEDDED	Embedded antenna matching inductor, 120 nH, 0603, Q>30, Murata LQW18ANR12J00D	Embedded Antenna
R14	Embedded antenna jumper, 2.2 Ω, 0402	Optional
C2	Supply bypass capacitor, 22 nF, 10%, Z5U/X7R, 0402	Optional
C3	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R, 0402	Optional
C5, C6	Headphone amp output shunt capacitor, 100 pF, 10%, Z5U/X7R, 0402	Optional
R7-R11	Current limiting resistor, 20 Ω–2 kΩ, 0402	Optional
C12, C13	Crystal load capacitor, 22 pF, 5%, COG	Optional
X1	Crystal, Epson FC-135	Optional
C7, C8	Si47xx input ac coupling capacitor, 0.39 µF, X7R/X5R, 0402	System Component
D1-D5	ESD Diode, SOT23-3, California Micro Devices CM1214-01ST	System Component
C11	Supply bypass capacitor, 100 nF, 10%, Z5U/X7R, 0402	Headphone Amplifier
C4	Headphone antenna ac coupling capacitor, 1 nF, 10%, Z5U/X7R, 0402	Headphone Antenna
C9, C10	Headphone amp output ac coupling capacitor, 125 uF, X7R, 0805	Headphone Amplifier
C14, C15	Headphone amp input ac coupling capacitor, 0.39 µF, X7R/X5R, 0402	Headphone Amplifier
R1,R2,R3,R4	Headphone amp feedback/gain resistor, 20 kΩ, 0402	Headphone Amplifier
R5, R6	Headphone amp bleed resistor, 100 kΩ, 0402	Headphone Amplifier
U2	Headphone amplifier, National Semiconductor, LM4910MA	Headphone Amplifier
R16, R17	Current limiting resistor, 2 kΩ, 0402	System Component
R18	Current limiting resistor, 600 Ω, 0402	System Component
L1	VCO filter inductor, 10 nH, 0603, Q>30, Murata, LQW18ANR01J00D	Optional
C17	VCO filter capacitor, 3.3 pF, 0402, COG, Venkel, C0402COG2503R3JN	Optional

5. Functional Description

5.1. Overview

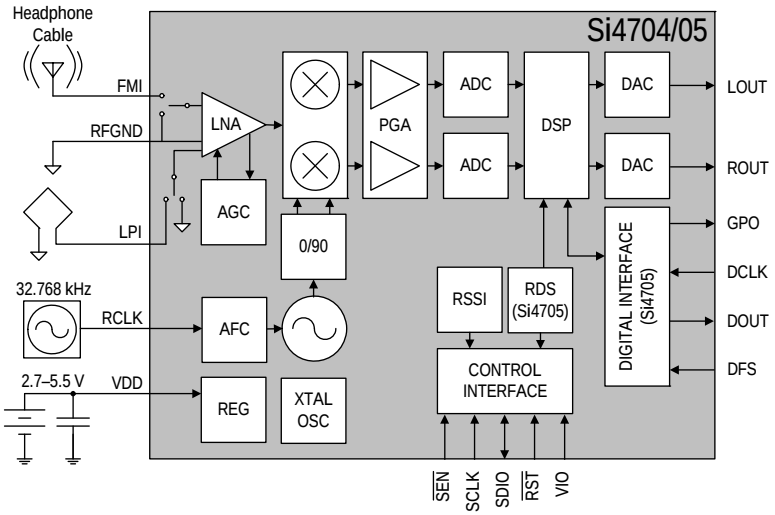


Figure 10. Functional Block Diagram

The Si4704/05 device leverages Silicon Laboratories' highly successful and proven Si4700/01/02/03 FM receiver, and offers unmatched integration and performance allowing FM receiver functionality to be added to any portable device with a single chip. The Si4704/05 offers additional features such as embedded antenna support and a digital audio interface. The Si4704/05 is layout compatible with Silicon Laboratories' Si4710/11 FM Transmitter, Si4720/21 FM Transceiver, and Si4730/31 AM/FM Receiver. The Si4704/05 is the first FM radio receiver integrated circuit to support a short PCB trace or wire antenna, which can be integrated into the enclosure or PCB of a portable device. This feature enables applications that also include Bluetooth functionality to perform FM radio reception without cables. For portable navigation devices, the Si4704/05's embedded antenna feature permits integration of the traffic messaging antenna into the enclosure of the portable device, and eliminates the need for external antenna cables.

The Si4704/05's digital integration reduces the required external components of traditional offerings, resulting in a solution requiring only an external inductor and bypass capacitor, and occupying board space of approximately 15 mm^2. Other advantages of the Si4704/05 include highly reliable device manufacturing, excellent quality, and ease of use to design-in and program.

The Si4704/05 includes line outputs from the on-chip digital-to-analog converters (DAC), digital audio mixers, a programmable reference clock input, and a configurable digital audio interface with the Si4705. The chip supports an I^2C-compliant 2-wire interface, an Si4700/01/02/03 backwards compatible 3-wire control interface, and an SPI control interface.

The Si4704/05 performs much of the FM demodulation digitally to achieve high fidelity, optimal performance versus power consumption, and flexibility of design. The on-board DSP provides unmatched pilot rejection, selectivity, and optimum sound quality. The integrated micro-controller offers both the manufacturer and the end-user unmatched programmability and flexibility in the listening experience.

The Si4705 incorporates on-board processing capability for the European Radio Data System (RDS) and the US Radio Broadcast Data System (RBDS) including all the symbol encoding/decoding, block synchronization, error detection, and error correction functions. RDS allows digital information sent from the broadcaster to be displayed, such as station ID, song name, and music category. In Europe, alternate frequency (AF) information is also provided to automatically change stations in areas where broadcasters use multiple frequencies.

The Si4704/05 has two separate RF inputs. FMI is the input for use with a traditional FM radio headphone antenna. Antennas implemented in the headphone cable should be connected to the FMI input. See “AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines” for detailed information on the implementation of a headphone antenna. The LPI input is for use with a short PCB trace or wire antenna that may be integrated into the system enclosure. There is a clocking mode to choose to clock the Si4704/05 from a reference clock or crystal. On the Si4705, there is an audio output mode to choose between an analog and/or digital audio output. In the analog audio output mode, pin 13 is ROUT, pin 14 is LOUT, and pin 17 is GPO3. In the digital audio mode, pin 15 is DOUT, pin 16 is DFS, and pin 17 is DCLK. Concurrent analog/digital audio output mode requires pins 13, 14, 15, 16, and 17.

The digital audio interface operates in slave mode and supports a variety of MSB-first audio data formats including I^2S and left-justified modes. The interface has three pins: digital data input (DIN), digital frame synchronization input (DFS), and a digital bit synchronization input clock (DCLK). The Si4704/05 supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs and ADCs on the audio baseband processor.

The Si4704/05 is reset by applying a logic low on $\overline{\text{RST}}$ signal. This causes all register values to be reset to their default values. The digital output interface supply (V_{IO}) provides voltage to the $\overline{\text{RST}}$, $\overline{\text{SEN}}$, SDIO, RCLK, DOUT, DFS, and DCLK pins and can be connected to the audio baseband processor's supply voltage to save power and remove the need for voltage level translators. RCLK is not required for register operation.

The Si4704/05 reference clock is programmable, supporting many RCLK inputs as shown in Table 11.

The Si4704/05 integrates support for a tuned loop antenna, which may also be implemented with a PCB trace. This permits mobile devices to receive FM radio signals with a small loop antenna when the headphone cable is not connected. An alterative usage model is to switch between an integrated loop antenna and an external headphone antenna in applications where both are available.

5.2. Application Schematics and Operating Modes

The application schematic for the Si4704/05 is shown in Section "2. Typical Application Schematic" on page 16. The Si4704/05 supports selectable analog, digital, or concurrent analog and digital audio output modes. In the analog output mode, pin 13 is ROUT, pin 14 is LOUT, and pin 17 is GPO3. In the digital output mode, pin 15 is DOUT, pin 16 is DFS, and pin 17 is DCLK. Concurrent analog and digital audio output mode requires pins 13, 14, 15, 16, and 17. In addition to output mode, there is a clocking mode to clock the Si4704/05 from a reference clock or crystal oscillator. The user sets the operating modes with commands as described in Section "6. Commands and Properties" on page 28.

5.3. FM Receiver

The Si4704/05 FM receiver is based on the proven Si4700/01/02/03 FM radio receiver. The part leverages Silicon Laboratories' proven and patented Si4700/01 FM broadcast radio receiver digital architecture, delivering superior RF performance and interference rejection. The proven digital techniques provide excellent sensitivity in weak signal environments while providing superb selectivity and inter-modulation immunity in strong signal environments.

The FM receiver supports the worldwide FM broadcast band (76 to 108 MHz) with channel spacings of 50–200 kHz. The Low-IF architecture utilizes a single converter stage and digitizes the signal using a high-resolution analog-to-digital converter. The resulting digital signals are further processed through an on-chip DSP for digital channel selection, FM demodulation, and ultimately stereo audio output. The audio output can be directed either to an external headphone amplifier via analog in/out or to other system ICs through digital audio interface (I^2S).

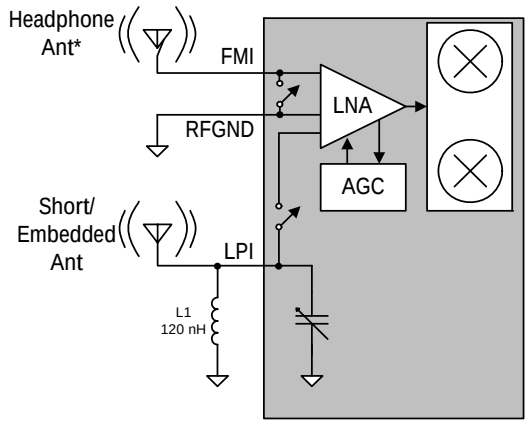
5.4. Integrated Antenna Support

The Si4704/05 is the first FM receiver to support the fast growing trend to integrate the FM receiver antenna into the device enclosure. The chip is designed with this function in mind from the outset, with multiple international patents pending, thus it is superior to many other options in price, board space, and performance.

The Si4704/05 elegantly supports an internal RX antenna allowing for "wire free" listening to FM over Bluetooth. The user can receive FM over the integrated RX antenna and stream it via Bluetooth to a Bluetooth-enabled headset.

Testing indicates that using Silicon Laboratories' patented techniques provides FM performance over an integrated antenna that can be very similar in many key metrics to performance using standard FM receive antennas (e.g., wired headset). Refer to “AN383: Antenna Selection and Universal Layout Guidelines” and “AN306: Si4710/11 Short Monopole Antenna Interface” for additional details on the implementation of support for an integrated antenna.

Figure 11 shows a conceptual block diagram of the Si4704/05 architecture used to support the short antenna. The headphone/dedicated FM receive antenna is therefore optional. Host software can detect the presence of a headphone antenna and switch between the integrated antenna if desired.



*Note: Dedicated RX antenna is optional.

Figure 11. Conceptual Block Diagram of the Si4704/05 Short Antenna Support

5.5. Digital Audio Interface (Si4705 Only)

The digital audio interface operates in slave mode and supports three different audio data formats:

- I^2S
- Left-Justified
- DSP Mode

5.5.1. Audio Data Formats

In I^2S mode, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified mode, by default the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP mode, the DFS becomes a pulse with a width of 1DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP mode: the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency, and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties.

The number of audio bits can be configured for 8, 16, 20, or 24 bits.

5.5.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz. The digital audio interface enables low-power operation by eliminating the need for redundant DACs on the audio baseband processor.

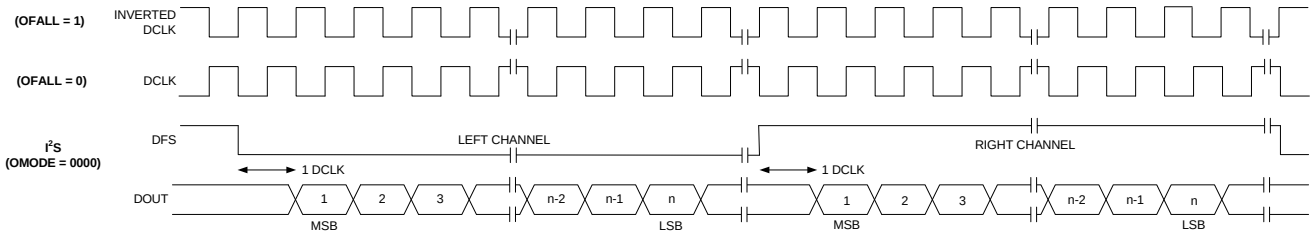


Figure 12. I²S Digital Audio Format

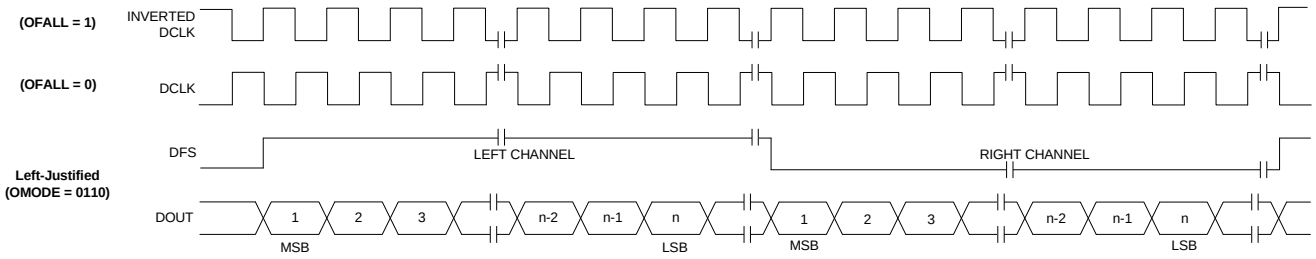


Figure 13. Left-Justified Digital Audio Format

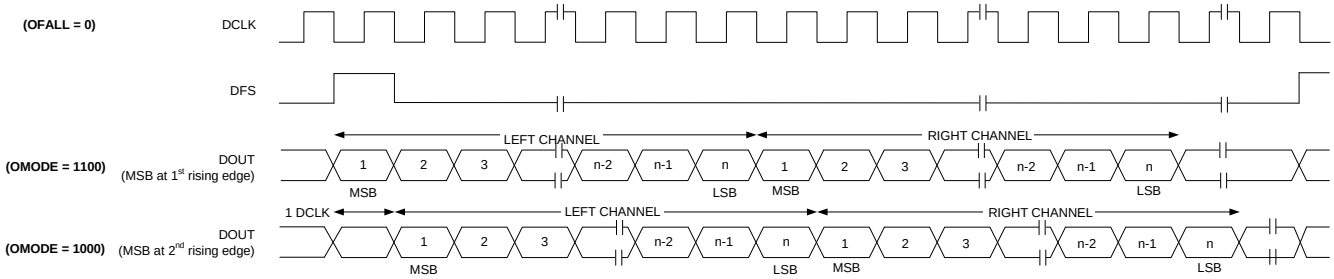


Figure 14. DSP Digital Audio Format

5.6. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 15 below.

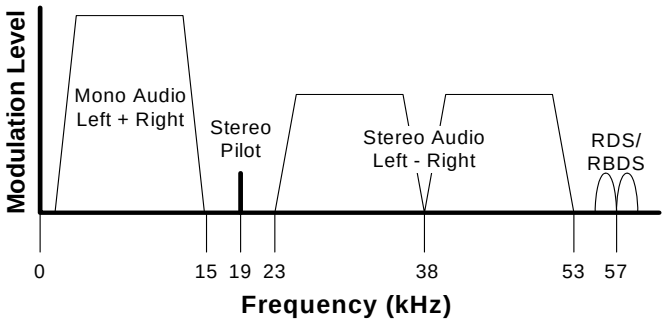


Figure 15. MPX Signal Spectrum

5.6.1. Stereo Decoder

The Si4704/05's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively. The Si4705 uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

5.6.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Stereo/mono status can be monitored with the FM_RSQ_STATUS command. Mono operation can be forced with the FM_BLEND_MONO_THRESHOLD property.

5.7. De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4704/05 incorporates a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs and is set by the FM_DEEMPHASIS property.

5.8. Stereo DAC

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted. Volume is adjusted digitally with the RX_VOLUME property.

5.9. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in very weak signal conditions. The softmute attenuation level is adjustable using the FM_SOFT_MUTE_MAX_ATTENUATION and AM_SOFT_MUTE_MAX_ATTENUATION properties.

5.10. RDS/RBDS Processor (Si4705 Only)

The Si4705 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction.

The Si4705 device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

The Si4705 reports RDS decoder synchronization status and detailed bit errors in the information word for each RDS block with the FM_RDS_STATUS command. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors or that the block checkword contains errors.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

5.11. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology, including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception. The tuning frequency can be directly programmed using the FM_TUNE_FREQ. The Si4704/05 supports channel spacing of 50, 100, or 200 kHz in FM mode.

5.12. Seek

Seek tuning will search up or down for a valid channel. Valid channels are found when the receive signal strength indicator (RSSI) and the signal-to-noise ratio (SNR) values exceed the set threshold. Using the SNR qualifier rather than solely relying on the more traditional RSSI qualifier can reduce false stops and increase the number of valid stations detected. Seek is initiated using the FM_SEEK_START and AM_SEEK_START commands. The RSSI and SNR threshold settings are adjustable using properties (see Table 15).

Two seek options are available. The device will either wrap or stop at the band limits. If the seek operation is unable to find a channel, the device will indicate failure and return to the channel selected before the seek operation began.

5.13. Reference Clock

The Si4704/05 reference clock is programmable, supporting RCLK frequencies in Table 11. Refer to Table 3, "DC Characteristics," on page 5 for switching voltage levels and Table 9, "FM Receiver Characteristics," on page 12 for frequency tolerance information.

An onboard crystal oscillator is available to generate the 32.768 kHz reference when an external crystal and load capacitors are provided. Refer to "2. Typical Application Schematic" on page 16. This mode is enabled using the POWER_UP command. Refer to Table 14, "Si4704/05 Command Summary," on page 28.

The Si4704/05 performance may be affected by data activity on the SDIO bus when using the integrated internal oscillator. SDIO activity results from polling the tuner for status or communicating with other devices that share the SDIO bus. If there is SDIO bus activity while the Si4704/05 is performing the seek/tune function, the crystal oscillator may experience jitter, which may result in mistunes, false stops, and/or lower SNR.

For best seek/tune results, Silicon Laboratories recommends that all SDIO data traffic be suspended during Si4704/05 seek and tune operations. This is achieved by keeping the bus quiet for all other devices on the bus, and delaying tuner polling until the tune or seek operation is complete. The seek/tune complete (STC) interrupt should be used instead of polling to determine when a seek/tune operation is complete.

5.14. Control Interface

A serial port slave interface is provided, which allows an external controller to send commands to the Si4704/05 and receive responses from the device. The serial port can operate in three bus modes: 2-wire mode, 3-wire mode, or SPI mode. The Si4704/05 selects the bus mode by sampling the state of the GPO1 and GPO2 pins on the rising edge of $\overline{RST}$. The GPO1 pin includes an internal pull-up resistor, which is connected while $\overline{RST}$ is low, and the GPO2 pin includes an internal pull-down resistor, which is connected while $\overline{RST}$ is low. Therefore, it is only necessary for the user to actively drive pins which differ from these states. See Table 13.

Table 13. Bus Mode Select on Rising Edge of $\overline{RST}$

Bus Mode	GPO1	GPO2
2-Wire	1	0
SPI	1	1 (must drive)
3-Wire	0 (must drive)	0

After the rising edge of $\overline{RST}$, the pins GPO1 and GPO2 are used as general purpose output (O) pins as described in Section "5.15. GPO Outputs". In any bus mode, commands may only be sent after V_{IO} and V_{DD} supplies are applied.

In any bus mode, before sending a command or reading a response, the user must first read the status byte to ensure that the device is ready (CTS bit is high).

5.14.1. 2-Wire Control Interface Mode

When selecting 2-wire mode, the user must ensure that SCLK is high during the rising edge of RST, and stays high until after the first start condition. Also, a start condition must not occur within 300 ns before the rising edge of RST.

The 2-wire bus mode uses only the SCLK and SDIO pins for signaling. A transaction begins with the START condition, which occurs when SDIO falls while SCLK is high. Next, the user drives an 8-bit control word serially on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 7-bit device address, followed by a read/write bit (read = 1, write = 0). The Si4704/05 acknowledges the control word by driving SDIO low on the next falling edge of SCLK.

Although the Si4704/05 will respond to only a single device address, this address can be changed with the SEN pin (note that the SEN pin is not used for signaling in 2-wire mode). When SEN = 0, the 7-bit device address is 0010001b. When SEN = 1, the address is 1100011b.

For write operations, the user then sends an 8-bit data byte on SDIO, which is captured by the device on rising edges of SCLK. The Si4704/05 acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. The user may write up to 8 data bytes in a single 2-wire transaction. The first byte is a command, and the next seven bytes are arguments.

For read operations, after the Si4704/05 has acknowledged the control byte, it will drive an 8-bit data byte on SDIO, changing the state of SDIO on the falling edge of SCLK. The user acknowledges each data byte by driving SDIO low for one cycle, on the next falling edge of SCLK. If a data byte is not acknowledged, the transaction will end. The user may read up to 16 data bytes in a single 2-wire transaction. These bytes contain the response data from the Si4704/05.

A 2-wire transaction ends with the STOP condition, which occurs when SDIO rises while SCLK is high. For details on timing specifications and diagrams, refer to Table 5, “2-Wire Control Interface Characteristics” on page 7; Figure 2, “2-Wire Control Interface Read and Write Timing Parameters,” on page 8, and Figure 3, “2-Wire Control Interface Read and Write Timing Diagram,” on page 8.

5.14.2. 3-Wire Control Interface Mode

When selecting 3-wire mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

The 3-wire bus mode uses the SCLK, SDIO, and SEN pins. A transaction begins when the user drives SEN low. Next, the user drives a 9-bit control word on SDIO, which is captured by the device on rising edges of SCLK. The control word consists of a 3-bit device address (A7:A5 = 101b), a read/write bit (read = 1, write = 0), and a 5-bit register address (A4:A0).

For write operations, the control word is followed by a 16-bit data word, which is captured by the device on rising edges of SCLK.

For read operations, the control word is followed by a delay of one-half SCLK cycle for bus turn-around. Next, the Si4704/05 will drive the 16-bit read data word serially on SDIO, changing the state of SDIO on each rising edge of SCLK.

A transaction ends when the user sets SEN high, then pulses SCLK high and low one final time. SCLK may either stop or continue to toggle while SEN is high.

In 3-wire mode, commands are sent by first writing each argument to register(s) 0xA1–0xA3, then writing the command word to register 0xA0. A response is retrieved by reading registers 0xA8–0xAF.

For details on timing specifications and diagrams, refer to Table 6, “3-Wire Control Interface Characteristics,” on page 9; Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9, and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.

5.14.3. SPI Control Interface Mode

When selecting SPI mode, the user must ensure that a rising edge of SCLK does not occur within 300 ns before the rising edge of RST.

SPI bus mode uses the SCLK, SDIO, and SEN pins for read/write operations. The system controller can choose to receive read data from the device on either SDIO or GPO1. A transaction begins when the system controller drives SEN = 0. The system controller then pulses SCLK eight times, while driving an 8-bit control byte serially on SDIO. The device captures the data on rising edges of SCLK. The control byte must have one of five values:

- 0x48 = write a command (controller drives 8 additional bytes on SDIO).
- 0x80 = read a response (device drives one additional byte on SDIO).
- 0xC0 = read a response (device drives 16 additional bytes on SDIO).
- 0xA0 = read a response (device drives one additional byte on GPO1).
- 0xE0 = read a response (device drives 16 additional bytes on GPO1).

For write operations, the system controller must drive exactly eight data bytes (a command and seven arguments) on SDIO after the control byte. The data is captured by the device on the rising edge of SCLK.

For read operations, the controller must read exactly 1 byte (STATUS) after the control byte or exactly 16 data bytes (STATUS and RESP1–RESP15) after the control byte. The device changes the state of SDIO (or GPO1, if specified) on the falling edge of SCLK. Data must be captured by the system controller on the rising edge of SCLK.

Keep SEN low until all bytes have transferred. A transaction may be aborted at any time by setting SEN high and toggling SCLK high and then low. Commands will be ignored by the device if the transaction is aborted.

For details on timing specifications and diagrams, refer to Figure 6 and Figure 7 on page 10.

5.15. GPO Outputs

The Si4704/05 provides three general-purpose output pins. The GPO pins can be configured to output a constant low, constant high, or high-Z. The GPO pins are multiplexed with the bus mode pins or DCLK depending on the application schematic of the device. GPO2/INT can be configured to provide interrupts for seek and tune complete, receive signal quality, and RDS.

5.16. Reset, Powerup, and Powerdown

Setting the RST pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RST pin high will bring the device out of reset.

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry while keeping the bus active.

5.17. Programming with Commands

To ease development time and offer maximum customization, the Si4704/05 provides a simple yet powerful software interface to program the receiver. The device is programmed using commands, arguments, properties, and responses.

To perform an action, the user writes a command byte and associated arguments, causing the chip to execute the given command. Commands control an action such as powerup the device, shut down the device, or tune to a station. Arguments are specific to a given command and are used to modify the command. A complete list of commands is available in Table 14, “Si4704/05 Command Summary,” on page 28.

Properties are a special command argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold. A complete list of properties is available in Table 15, “Si4704/05 Property Summary,” on page 28.

Responses provide the user information and are echoed after a command and associated arguments are issued. All commands provide a one-byte status update indicating interrupt and clear-to-send status information. For a detailed description of the commands and properties for the Si4704/05, see “AN332: Universal Programming Guide.”

6. Commands and Properties

Table 14. Si4704/05 Command Summary

Cmd	Name	Description
0x01	POWER_UP	Powerup device and mode selection. Modes include AM or FM receive, analog or digital output, and reference clock or crystal support.
0x10	GET_REV	Returns revision information on the device.
0x11	POWER_DOWN	Powerdown device.
0x12	SET_PROPERTY	Sets the value of a property.
0x13	GET_PROPERTY	Retrieves a property's value.
0x14	GET_INT_STATUS	Read interrupt status bits.
0x15	PATCH_ARGS	Reserved command used for firmware file downloads.
0x16	PATCH_DATA	Reserved command used for firmware file downloads.
0x20	FM_TUNE_FREQ	Selects the FM tuning frequency.
0x21	FM_SEEK_START	Begins searching for a valid frequency.
0x22	FM_TUNE_STATUS	Queries the status of previous FM_TUNE_FREQ or FM_SEEK_START command.
0x23	FM_RSQ_STATUS	Queries the status of the Received Signal Quality (RSQ) of the current channel (Si4705 only).
0x24	FM_RDS_STATUS	Returns RDS information for current channel and reads an entry from the RDS FIFO (Si4705 only).
0x80	GPO_CTL	Configures GPO3 as output or high impedance.
0x81	GPO_SET	Sets GPO3 output level (low or high).

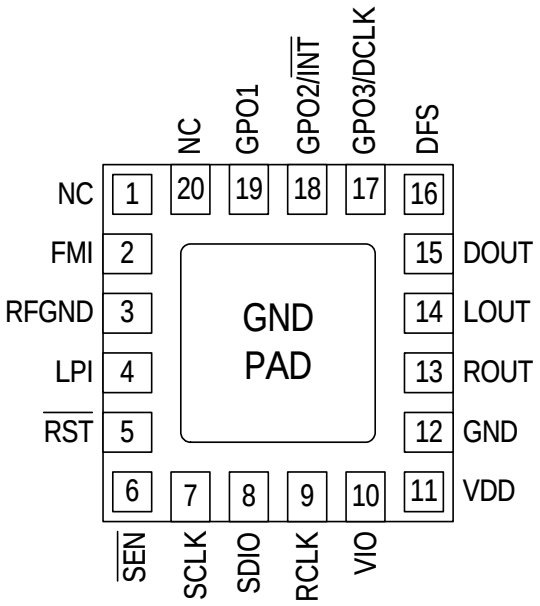
Table 15. Si4704/05 Property Summary

Prop	Name	Description	Default
0x0001	GPO_IEN	Enables interrupt sources.	0x0000
0x0102	DIGITAL_OUTPUT_FORMAT	Configures the digital output format (Si4705 only).	0x0000
0x0104	DIGITAL_OUTPUT_ SAMPLE_RATE	Configures the digital output sample rate in 100 Hz steps. The digital output sample rate is disabled by default (Si4705 only).	0x0000
0x0201	REFCLK_FREQ	Sets frequency of reference clock in Hz. The range is 31130 to 34406 Hz, or 0 to disable the AFC. Default is 32768 Hz.	0x8000
0x0202	REFCLK_PRESCALE	Sets the prescaler value for RCLK input.	0x0001
0x1100	FM_DEEMPHASIS	Sets deemphasis time constant. Default is 75 us.	0x0002
0x1105	FM_BLEND_STEREO_ THRESHOLD	Sets RSSI threshold for stereo blend (Full stereo above threshold, blend below threshold). To force stereo set this to 0. To force mono set this to 127. Default value is 49 dBuV.	0x0031
0x1106	FM_BLEND_MONO_ THRESHOLD	Sets RSSI threshold for mono blend (Full mono below threshold, blend above threshold). To force stereo set this to 0. To force mono set this to 127. Default value is 30 dBuV.	0x001E
0x1108	FM_MAX_TUNE_ ERROR	Sets the maximum freq error allowed before setting the AFC rail (AFCRL) indicator. Default value is 30 kHz.	0x001E
0x1200	FM_RSQ_INT_ SOURCE	Configures interrupt related to Received Signal Quality metrics.	0x0000
0x1201	FM_RSQ_SNR_HI_ THRESHOLD	Sets high threshold for SNR interrupt.	0x007F

Table 15. Si4704/05 Property Summary (Continued)

Prop	Name	Description	Default
0x1202	FM_RSQ_SNR_LO_ THRESHOLD	Sets low threshold for SNR interrupt.	0x0000
0x1203	FM_RSQ_RSSI_HI_ THRESHOLD	Sets high threshold for RSSI interrupt.	0x007F
0x1204	FM_RSQ_RSSI_LO_ THRESHOLD	Sets low threshold for RSSI interrupt.	0x0000
0x1207	FM_RSQ_BLEND_ THRESHOLD	Sets the blend threshold for blend interrupt when boundary is crossed.	0x0081
0x1302	FM_SOFT_MUTE_ MAX_ATTENUATION	Sets maximum attenuation during soft mute (dB). Set to 0 to disable soft mute. Default is 16 dB.	0x0010
0x1303	FM_SOFT_MUTE_ SNR_THRESHOLD	Sets SNR threshold to engage soft mute. Default is 4 dB.	0x0004
0x1400	FM_SEEK_BAND_ BOTTOM	Sets the bottom of the FM band for seek. Default is 8750.	0x222E
0x1401	FM_SEEK_BAND_TOP	Sets the top of the FM band for seek. Default is 10790.	0x2A26
0x1402	FM_SEEK_FREQ_ SPACING	Selects frequency spacing for FM seek.	0x000A
0x1403	FM_SEEK_TUNE_ SNR_THRESHOLD	Sets the SNR threshold for a valid FM Seek/Tune. Default value is 3 dB.	0x0003
0x1404	FM_SEEK_TUNE_ RSSI_TRESHOLD	Sets the RSSI threshold for a valid FM Seek/Tune. Default value is 20 dBuV.	0x0014
0x1500	RDS_INT_SOURCE	Configures RDS interrupt behavior.	0x0000
0x1501	RDS_INT_FIFO_COUNT	Sets the minimum number of RDS groups stored in the receive RDS FIFO required before RDS RECV is set.	0x0000
0x1502	RDS_CONFIG	Configures RDS setting.	0x0000
0x4000	RX_VOLUME	Sets the output volume.	0x003F
0x4001	RX_HARD_MUTE	Mutes the audio output. L and R audio outputs may be muted independently in FM mode.	0x0000

7. Pin Descriptions: Si4704/05-GM



Pin Number(s)	Name	Description
1, 20	NC	No connect. Leave floating.
2	FMI	FM RF input.
3	RFGND	RF ground. Connect to ground plane on PCB.
4	LPI	Loop antenna RF input.
5	RST	Device reset input (active low).
6	SEN	Serial enable input (active low).
7	SCLK	Serial clock input.
8	SDIO	Serial data input/output.
9	RCLK	External reference or crystal oscillator input.
10	V_{IO}	I/O supply voltage.
11	V_{DD}	Supply voltage. May be connected directly to battery.
13	ROUT	Right audio analog line output.
14	LOUT	Left audio analog line output.
15	DOUT	Digital audio output data.
16	DFS	Digital frame synchronization.
17	GPO3/DCLK	General purpose output/digital bit synchronous clock or crystal oscillator input.
18	GPO2/$\overline{\text{INT}}$	General purpose output/interrupt.
19	GPO1	General purpose output.
12, GND PAD	GND	Ground. Connect to ground plane on PCB.

8. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4704-B20-GM	Enhanced Portable Broadcast Radio Tuner • FM Stereo • Firmware Revision 2.0	QFN Pb-free	–20 to 85 °C
Si4705-B20-GM	Enhanced Portable Broadcast Radio Tuner • FM Stereo with RDS • Digital audio output • Firmware Revision 2.0	QFN Pb-free	–20 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

9. Package Markings (Top Marks)

9.1. Si4704 Top Mark

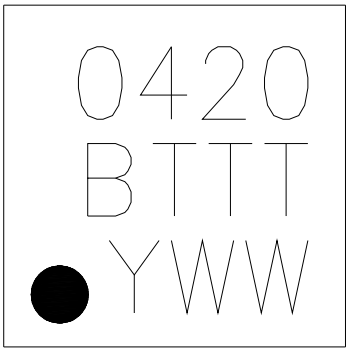


Figure 16. Si4704 Top Mark

9.2. Si4705 Top Mark

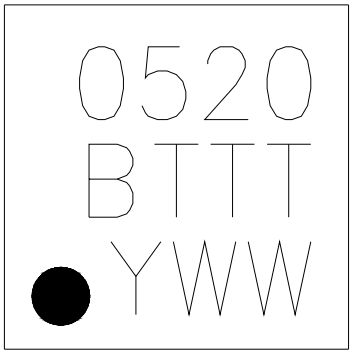


Figure 17. Si4705 Top Mark

9.3. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	04 = Si4704 05 = Si4705
	Firmware Revision	20 = Firmware Revision 20
Line 2 Marking:	R = Die Revision	B = Revision B Die
	TTT = Internal Code	Internal tracking code.
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier.
	Y = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date.

10. Package Outline: Si4704/05-GM

Figure 18 illustrates the package details for the Si4704/05. Table 16 lists the values for the dimensions shown in the illustration.

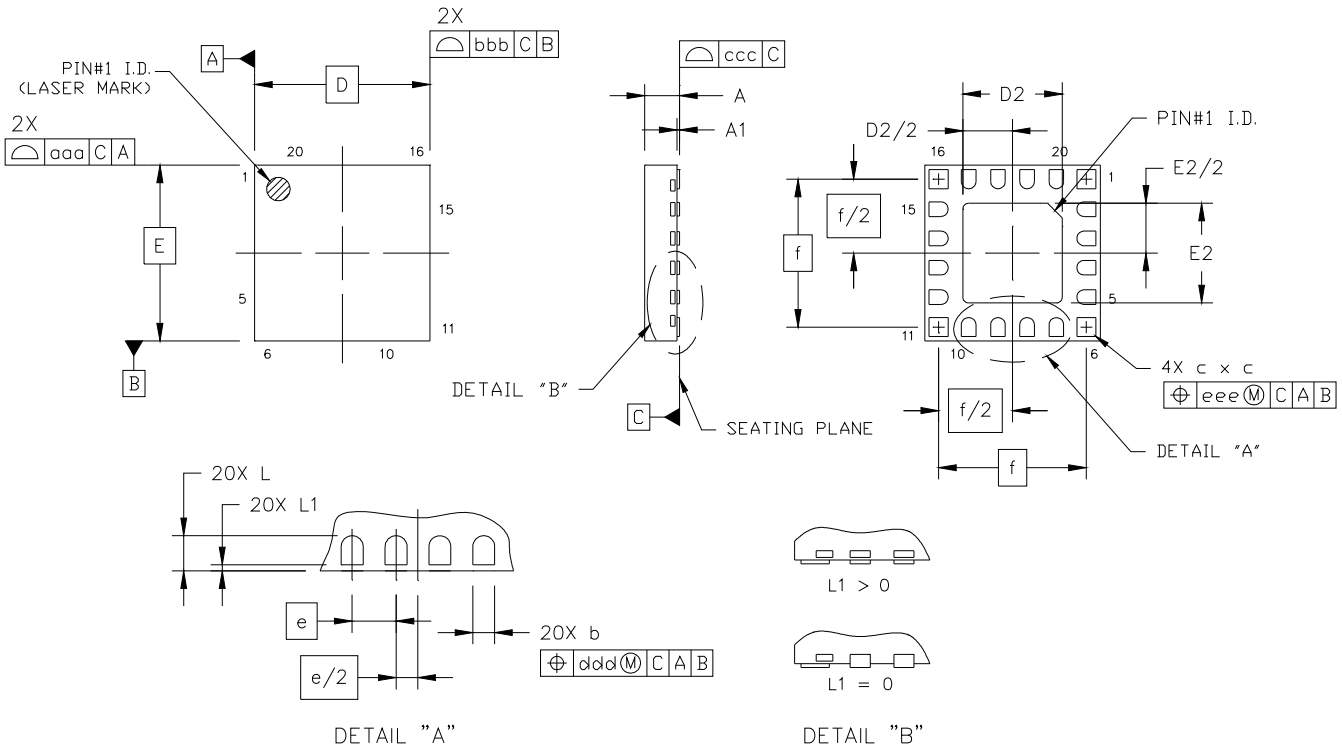


Figure 18. 20-Pin Quad Flat No-Lead (QFN)

Table 16. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.60	1.70	1.80
e		0.50 BSC	
E		3.00 BSC	
E2	1.60	1.70	1.80

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.35	0.40	0.45
L1	0.00	—	0.10
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

11. PCB Land Pattern: Si4704/05-B20-GM

Figure 19 illustrates the PCB land pattern details for the Si4704/05-GM. Table 17 lists the values for the dimensions shown in the illustration.

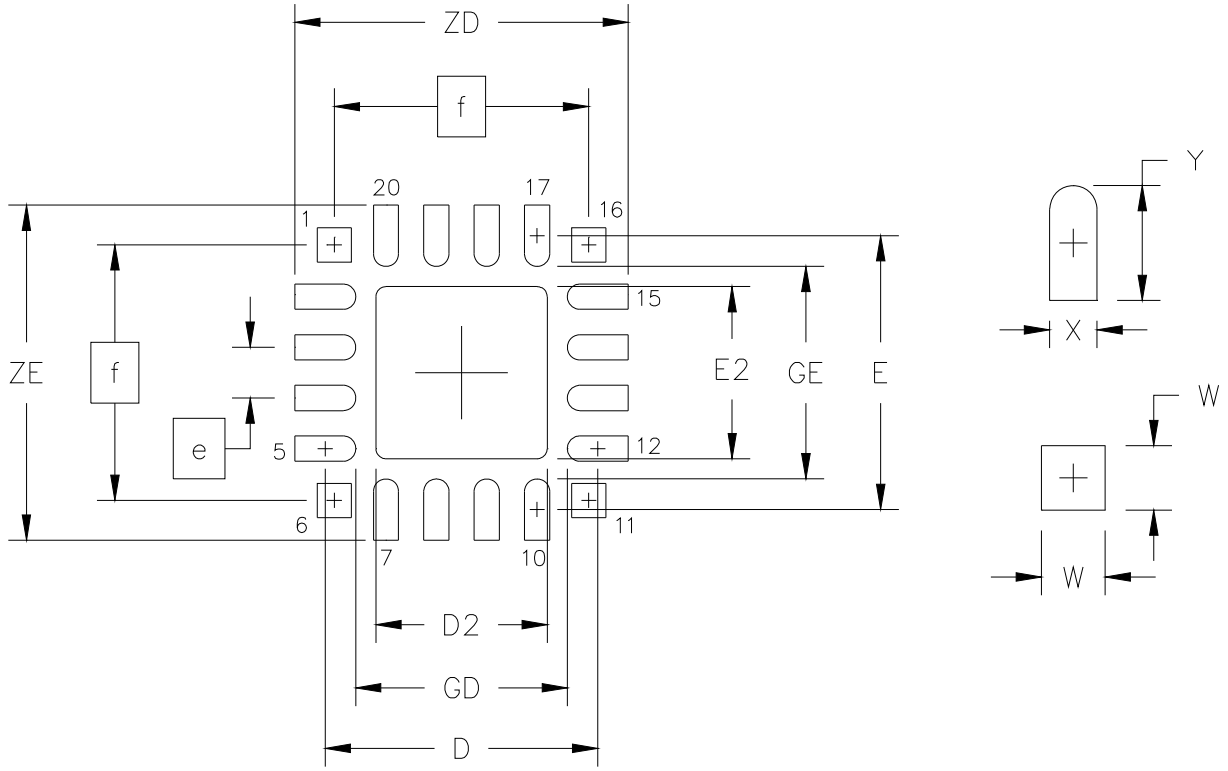


Figure 19. PCB Land Pattern

Table 17. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes: Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 m minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

12. Additional Reference Resources

- AN383: Antenna Selection and Universal Layout Guidelines
- Si47XX Evaluation Board User's Guide
- Si4704/05 Customer Support Site: http://www.mysilabs.com
- AN388: EVB Test Procedure
- AN332: Universal Programming Guide
- AN342: Si4704/05 Evaluation Board Quick Start Guide

This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, send mysilabs user name and request for access to fminfo@silabs.com.

Document Change List

Revision 0.1 to Revision 0.8

- Updated all of page 1.
- Updated Table 3, “DC Characteristics,” on page 5 and Table 4, “Reset Timing Characteristics[1,2,3],” on page 6.
- Updated notes in Table 5, “2-Wire Control Interface Characteristics[1,2,3],” on page 7.
- Updated Table 6, “3-Wire Control Interface Characteristics,” on page 9.
- Updated Figure 4, “3-Wire Control Interface Write Timing Parameters,” on page 9 and Figure 5, “3-Wire Control Interface Read Timing Parameters,” on page 9.
- Updated Table 7, “SPI Control Interface Characteristics,” on page 10 and Table 8, “Digital Audio Interface Characteristics,” on page 11.
- Updated Figure 8, “Digital Audio Interface Timing Parameters, I^{2}S Mode,” on page 11.
- Updated Table 9, “FM Receiver Characteristics[1,2],” on page 12, Table 10, “64–75.9 MHz Input Frequency FM Receiver Characteristics[1],” on page 14, and Table 11, “Reference Clock and Crystal Characteristics,” on page 15.
- Updated Figures 10 through 13.
- Updated “5. Functional Description”.
- Updated Table 14, “Si4704/05 Command Summary,” on page 28 and Table 15, “Si4704/05 Property Summary,” on page 28.
- Updated “7. Pin Descriptions: Si4704/05-GM”, “8. Ordering Guide”, and “9. Package Markings (Top Marks)”.
- Updated “12. Additional Reference Resources”.

Revision 0.8 to Revision 0.9

- Updated Table 3, “DC Characteristics,” on page 5.
- Updated Table 9, “FM Receiver Characteristics[1,2],” on page 12.
- Updated Table 10, “64–75.9 MHz Input Frequency FM Receiver Characteristics[1],” on page 14.
- Updated Table 11, “Reference Clock and Crystal Characteristics,” on page 15.
- Updated Table 14, “Si4704/05 Command Summary,” on page 28 and Table 15, “Si4704/05 Property Summary,” on page 28.
- Updated "8. Ordering Guide" on page 31.

Revision 0.9 to Revision 1.0

- Updated "Table 1. Recommended Operating Conditions" on page 4.
- Updated "Table 3. DC Characteristics" on page 5.
- Updated notes on Table 5, “2-Wire Control Interface Characteristics[1,2,3],” on page 7.
- Updated Table 8, “Digital Audio Interface Characteristics,” on page 11.
- Updated Table 9, “FM Receiver Characteristics[1,2],” on page 12.
- Updated Table 10, “64–75.9 MHz Input Frequency FM Receiver Characteristics[1],” on page 14.
- Updated notes on "2. Typical Application Schematic" on page 16.
- Updated "3. Bill of Materials" on page 17.
- Updated "Figure 11. Conceptual Block Diagram of the Si4704/05 Short Antenna Support" on page 22.
- Updated "7. Pin Descriptions: Si4704/05-GM" on page 30 and "8. Ordering Guide" on page 31.

Revision 1.0 to Revision 1.2

- A reference to “AN231“ on page 21 was corrected to “AN383: Si47xx Antenna, Schematic, Layout and Design Guidelines.”

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: FMinfo@silabs.com
Internet: www.silabs.com